REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	04-10-27	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	A	A	A																	
SHEET	16	17	18																	

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	12	13	14	15	

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ECL, OCTAL ECL/TTL, BI-DIRECTIONAL TRANSLATOR WITH REGISTER, MONOLITHIC SILICON

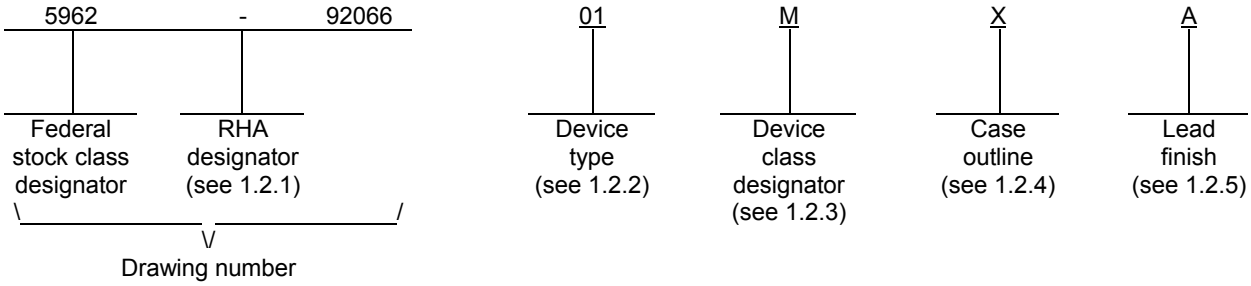
SIZE	CAGE CODE	
A	**67268**	**5962-92066**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	100329	Octal ECL/TTL bi-directional translator with register

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP5-T24 or CDIP6-T24	24	dual-in-line
Y	See figure 1	24	quad-flat

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Negative supply voltage range (V_{EE})	-7.0 V dc to +0.5 V dc
Positive supply voltage range (V_{TTL})	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	805 mW
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	28° C/W

ECL-to-TTL translation

DC input voltage range (V_{IN})	V_{EE} to +0.5 V
Maximum dc output current (I_{OUT})	-50 mA

TTL-to ECL translation

DC input voltage range (V_{IN})	-0.5 V to +6.0 V 2/
DC input current range (I_{IN})	-30 mA to +5.0 mA 2/
Voltage applied to output in high state	-0.5 V to +5.5 V
Maximum current applied to output in low state	48 mA

1.4 Recommended operating conditions.

Negative supply voltage range (V_{EE})	-5.7 V dc minimum to -4.2 V dc maximum
Positive supply voltage range (V_{TTL})	+4.5 V dc minimum to +5.5 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

ECL-to-TTL translation

High level input voltage range (V_{IH})	-1.165 V dc minimum to -0.870 V dc maximum
Low level input voltage range (V_{IL})	-1.830 V dc minimum to -1.475 V dc maximum
Minimum setup time, En to CP (t_s):	
T_C = +25° C	2.0 ns
T_C = +125° C, -55° C	2.5 ns
Minimum hold time, En to CP (t_h):	
T_C = +25° C	2.5 ns
T_C = +125° C, -55° C	3.0 ns
Minimum pulse width, high, CP (t_{PW}):	
T_C = +25° C, -55° C	2.5 ns
T_C = +125° C	5.0 ns
Maximum toggle frequency (f_{MAX}):	
T_C = +25° C, -55° C	200 MHz minimum
T_C = +125° C	100 MHz minimum

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Either voltage limit or current limit is sufficient to protect inputs.

TTL-to-ECL translation

Minimum high level input voltage (V_{IH})	+2.0 V
Maximum low level input voltage (V_{IL})	+0.8 V
Minimum setup time, Tn to CP (t_s):	
T_C = +25° C	2.0 ns
T_C = +125° C, -55° C	2.5 ns
Minimum hold time, Tn to CP (t_h):	
T_C = +25° C	2.0 ns
T_C = +125° C, -55° C	2.5 ns
Minimum pulse width, high, CP (t_{PW}):	
T_C = +25° C	2.0 ns
T_C = +125° C, -55° C	2.5 ns
Maximum toggle frequency (f_{MAX})	250 MHz minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figures 4 and 5.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 32 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $-5.7\ V \le V_{EE} \le -4.2\ V$ $+4.5\ V \le V_{TTL} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
ECL-to-TTL translation								
High level output voltage	V_{OH}	V_{EE} = -4.2 V, -5.7 V, V_{TTL} = 4.5 V, V_{IH} = -1.165 V, V_{IL} = -1.475 V,	I_{OH} = -1.0 mA	1, 2	All	2.5		V
				3		2.4		
			I_{OH} = -3.0 mA	1, 2, 3		2.4		
Low level output voltage	V_{OL}		I_{OL} = 24.0 mA	1, 2, 3	All		0.5	V
High level input current	I_{IH}	V_{EE} = -5.7 V, V_{TTL} = 5.0 V, V_{IN} = -0.87 V		1, 2	All		350	µA
				3			500	
Low level input current	I_{IL}	V_{EE} = -4.2 V, V_{TTL} = 5.0 V, V_{IN} = -1.83 V		1, 2, 3	All	0.5		µA
Output short-circuit current 2/	I_{OS}	V_{EE} = -4.5 V, V_{TTL} = 5.5 V , V_{OUT} = 0.0 V		1, 2, 3	All	-60	-150	mA
High level output disable current	I_{OZH}	V_{EE} = -4.5 V, V_{TTL} = 5.5 V	V_{OUT} = 2.7 V	1, 2, 3	All		70	µA
Low level output disable current	I_{OZL}		V_{OUT} = 0.5	1, 2, 3	All		-1.0	mA
Positive power supply drain current	I_{TTLL}	V_{EE} = -4.5 V, V_{TTL} = 5.5 V		1, 2, 3	All		75	mA
	I_{TTLH}						50	
	I_{TTLZ}						70	
Functional tests		V_{EE} = -5.7 V, -4.2 V, V_{IL} = -1.642 V, V_{IH} = -1.023 V, V_{TTL} = 4.5 V, 5.5 V, see 4.4.1b		7, 8	All			
Propagation delay time, CP to Tn	t_{PLH}, t_{PHL}	See figure 4		9	All	3.1	7.3	ns
				10		3.3	8.0	
				11		3.1	8.0	
Output enable time to high level, OE to Tn	t_{PZH1}			9	All	3.7	9.0	ns
				10		4.0	10.1	
				11		3.4	9.1	
Output enable time to low level, OE to Tn	t_{PZL1}			9	All	4.0	9.3	ns
				10		4.3	10.4	
				11		3.7	9.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $-5.7\ V \le V_{EE} \le -4.2\ V$ $+4.5\ V \le V_{TTL} \le +5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ECL-to-TTL translation - Continued							
Output disable time from high level, OE to Tn	t_{PHZ1}	See figure 4	9	All	3.3	9.0	ns
			10		3.5	9.3	
			11		3.2	10.0	
Output disable time from low level, OE to Tn	t_{PLZ1}		9	All	3.4	8.8	ns
			10		4.1	10.4	
			11		3.0	9.8	
Output disable time from high level, DIR to Tn	t_{PHZ2}		9	All	2.8	8.8	ns
			10		3.0	9.0	
			11		2.6	9.5	
Output disable time from low level, DIR to Tn	t_{PLZ2}		9	All	3.1	8.0	ns
			10		4.0	9.6	
			11		2.7	8.7	
TTL-to ECL translation							
High level output voltage	V_{OH}	V_{EE} = -4.2 V, -5.7 V, V_{TTL} = 4.5 V, 5.5 V, V_{IH} = 3.0 V, V_{IL} = 0.0 V, OE = DIR = -0.87 V	1, 2	All	-1.025	-0.870	V
			3		-1.085	-0.870	
Low level output voltage	V_{OL}		1, 2	All	-1.830	-1.620	V
			3		-1.830	-1.555	
		OE = -1.83 V	1, 2			-1.950	
			3			-1.850	
High level threshold output voltage	V_{OHC}	V_{EE} = -4.2 V, -5.7 V, V_{IH} = 2.0 V, V_{TTL} = 4.5 V, 5.5 V, V_{IL} = 0.8 V	1, 2	All	-1.035		V
			3		-1.085		
Low level threshold output voltage	V_{OLC}	V_{EE} = -4.2 V, -5.7 V, V_{IH} = 2.0 V, V_{TTL} = 4.5 V, 5.5 V, V_{IL} = 0.8 V, OE = DIR = -1.165 V	1, 2	All		-1.610	V
			3			-1.555	
		V_{EE} = -4.2 V, -5.7 V, V_{IH} = 5.0 V, V_{TTL} = 4.5 V, 5.5 V, V_{IL} = 0.0 V, OE = -1.475 V	1, 2			-1.950	
			3			-1.850	
Input clamp diode voltage	V_{CD}	V_{EE} = -4.5 V, V_{TTL} = 4.5 V, I_{IN} = -18 mA	1, 2, 3	All		-1.2	V

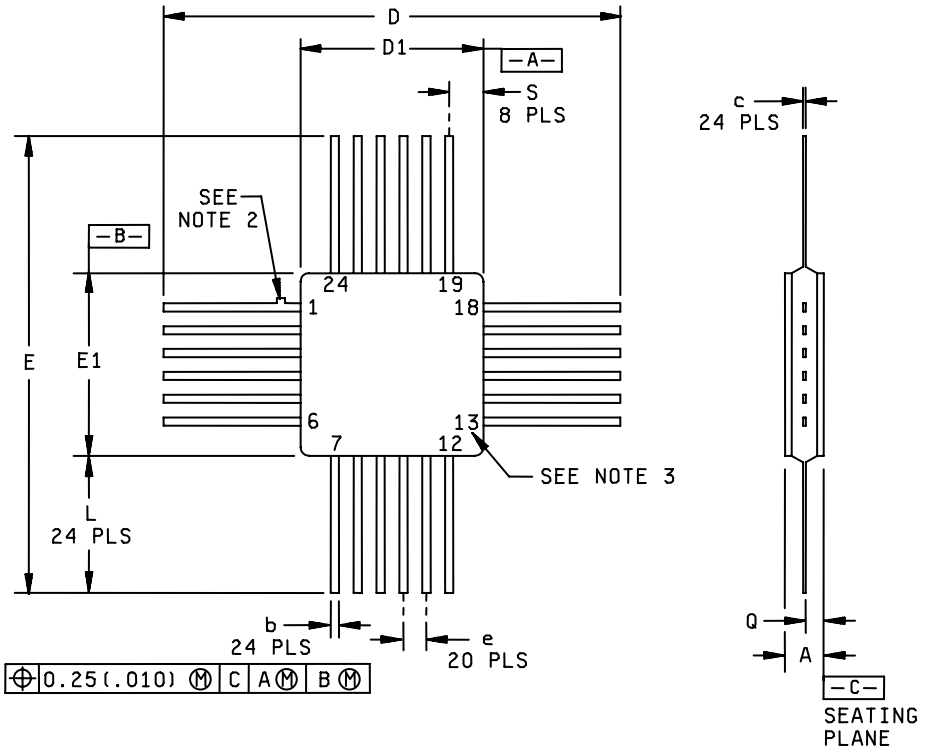
See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $-5.7\ V \le V_{EE} \le -4.2\ V$ $+4.5\ V \le V_{TTL} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
TTL-to-ECL translation - Continued								
High level input current	I_{IH1}	V_{EE} = -4.5 V, V_{TTL} = 5.5 V	V_{IN} = 2.7 V	1, 2, 3	All		70	µA
	I_{IH2}		V_{IN} = 5.5 V	1, 2, 3			1.0	mA
Low level input current	I_{IL}		V_{IN} = 0.5 V	1, 2, 3			-1.0	mA
Negative power supply drain current	I_{EE}	V_{EE} = -4.2 V, -4.8 V, V_{TTL} = 5.0 V		1, 2, 3	All	-210	-70	µA
		V_{EE} = -4.2 V, -5.7 V, V_{TTL} = 5.0 V		1, 2, 3		-220	-70	
Functional tests		V_{EE} = -5.7 V, -4.2 V, V_{IL} = 0.4 V, V_{IH} = 2.4 V, V_{TTL} = 4.5 V, 5.5 V, see 4.4.1b		7, 8	All			
Propagation delay time, CP to En	$t_{PLH'}$ t_{PHL}	See figure 5		9	All	1.6	3.7	ns
				10		1.9	4.3	
				11		1.3	3.8	
Output enable time to high level, OE to En (cutoff to high)	t_{PZH1}			9	All	1.5	4.4	ns
				10		1.7	9.0	
				11		1.0	4.3	
Output disable time from high level, OE to En (high to cutoff)	t_{PHZ1}			9	All	1.6	4.5	ns
				10		1.6	5.0	
				11		1.5	5.0	
Output disable time from high level, DIR to En (high to cutoff)	t_{PHZ2}			9	All	1.6	4.3	ns
				10		1.7	4.7	
				11		1.6	4.7	
Transition time, output 3/	$t_{TLH'}$ t_{THL}			9	All	0.5	2.1	ns
				10		0.4	2.4	
				11		0.4	2.3	

1/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals shall be terminated through 50Ω to -2.0 V. Input terminals not designated shall be high logic level or low logic level.
2/ Not more than one output shall be shorted at a time, and the duration of the short-circuit condition shall not exceed one second.
3/ This parameter is provided as design information only (not tested but guaranteed).

Case Y



Dimension	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A		2.16		.085	
b	0.41	0.46	.016	.018	
c	0.10	0.15	.004	.006	
D	22.10	28.45	.870	1.120	
D1	9.40	10.16	.370	.400	4
E	22.10	28.45	.870	1.120	
E1	9.40	10.16	.370	.400	4
e	1.14	1.40	.045	.055	
L	6.35	9.14	.250	.360	
Q	0.89	1.27	.035	.050	5
S		1.91		.075	

Notes:
1. The preferred unit of measurement is millimeters. However, this item was designed using inch-pound units of measurements. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Lead number 1 is identified by a tab located on the lead.
3. Lead numbers are shown for reference only and do not appear on package.
4. Dimensions D1 and E1 allow for glass meniscus.
5. Dimension Q shall be measured at the point of exit of the lead from the body.

FIGURE 1. Case outline.

Device type	01	
Case outlines	X	Y
Terminal number	Terminal symbol	
1	E4	E1
2	E5	E2
3	E6	E3
4	E7	E4
5	OE	E5
6	V_{CC}	E6
7	V_{CCA}	E7
8	DIR	OE
9	T7	V_{CC}
10	T6	V_{CCA}
11	T5	DIR
12	T4	T7
13	T3	T6
14	T2	T5
15	T1	T4
16	T0	T3
17	V_{TTL}	T2
18	V_{EE}	T1
19	V_{CC}	T0
20	CP	V_{TTL}
21	E0	V_{EE}
22	E1	V_{CC}
23	E2	CP
24	E3	E0

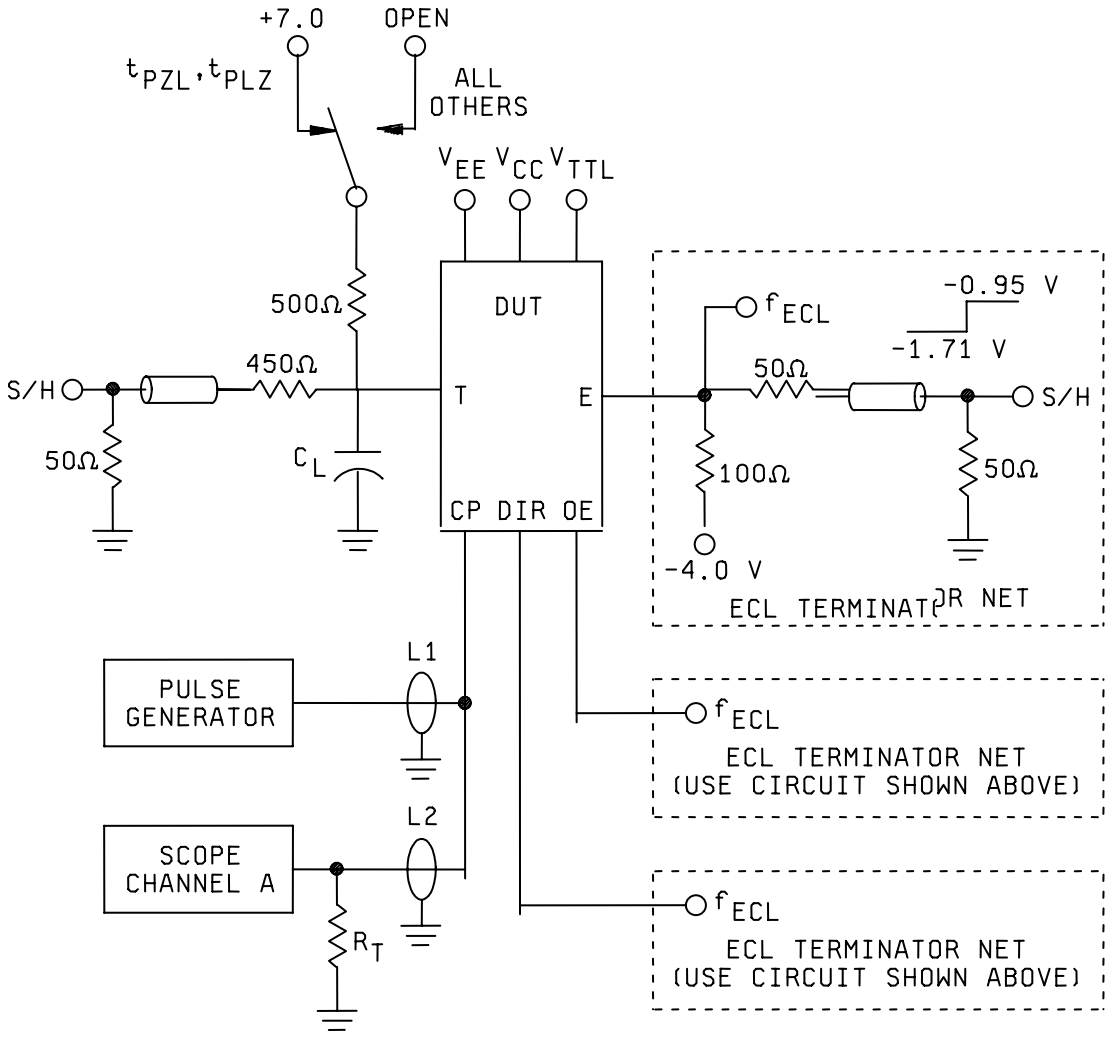
FIGURE 2. Terminal connections.

OE	DIR	CP	ECL Port	TTL Port	Notes
L	L	X	Input	Z	1, 3
L	H	X	Low (cut-off)	Input	2, 3
H	L	↑	L	L	1
H	L	↑	H	H	1
H	L	L	X	NC	1, 3
H	H	↑	L	L	2
H	H	↑	H	H	2
H	H	L	NC	X	2, 3

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance
↑ = Low-to high clock transition
NC = No change

Notes:
1. ECL input to TTL output mode.
2. TTL input to ECL output mode.
3. Retains data present before CP.

FIGURE 3. Truth table.



Notes:

1. $V_{CC} = V_{CCA} = 0.0$ V, $V_{EE} = -4.5$ V, $V_{TTL} = +5.0$ V.
2. L1 and L2 = 50Ω impedance lines.
3. R_T = 50Ω terminator internal to scope.
4. Decoupling 0.1 μF from GND to V_{CC}, V_{EE}, and V_{TTL}.
5. 50Ω to ground termination must be included on ECL I/O pins not monitored by a 50Ω scope to prevent oscillatory feedback.
6. C_L = fixture and stray capacitance = 50 pF
7. All coaxial cable is 50Ω.

FIGURE 4. ECL-to-TTL translation test circuit and switching waveforms.

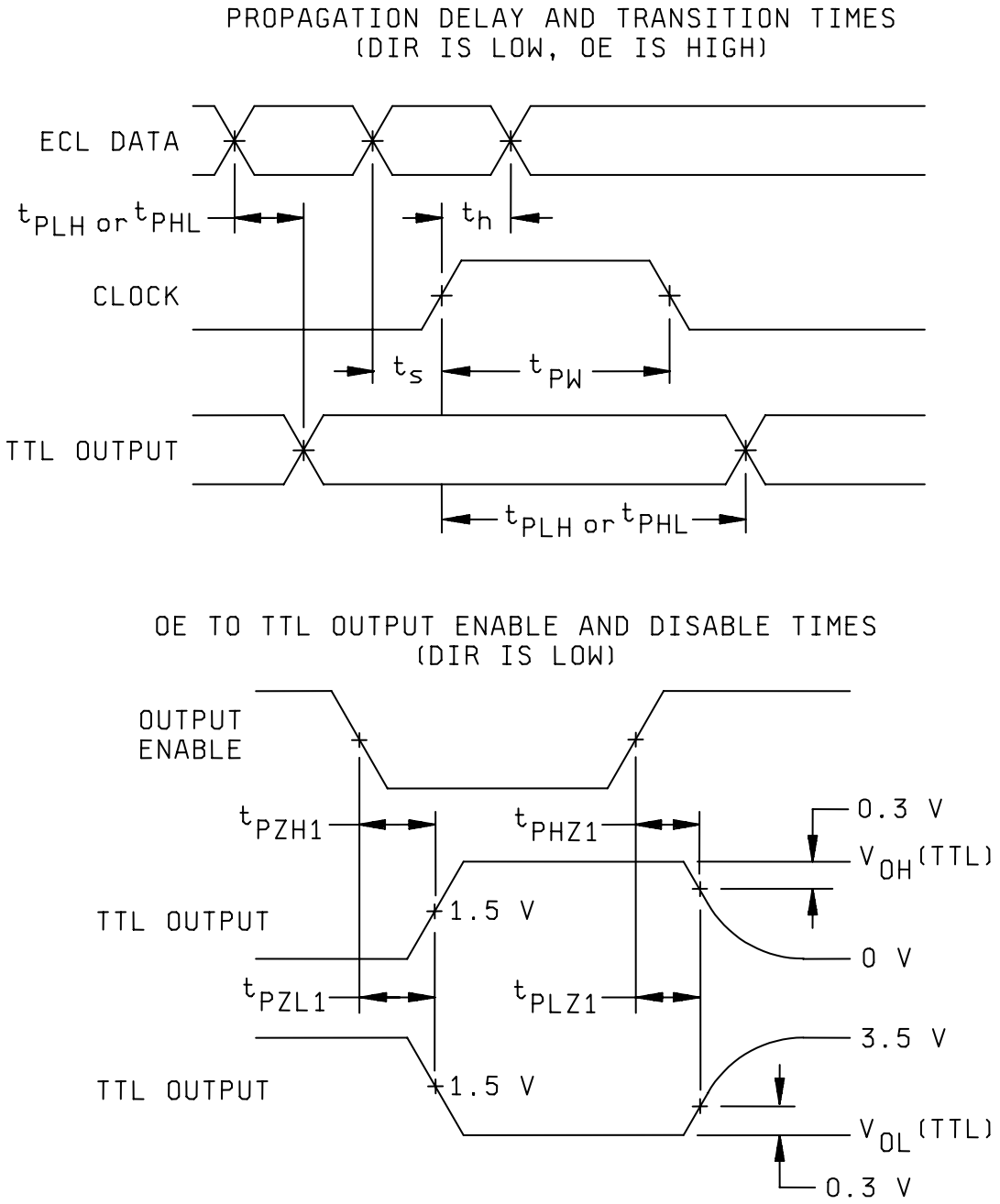


FIGURE 4. ECL-to-TTL translation test circuit and switching waveforms – Continued.

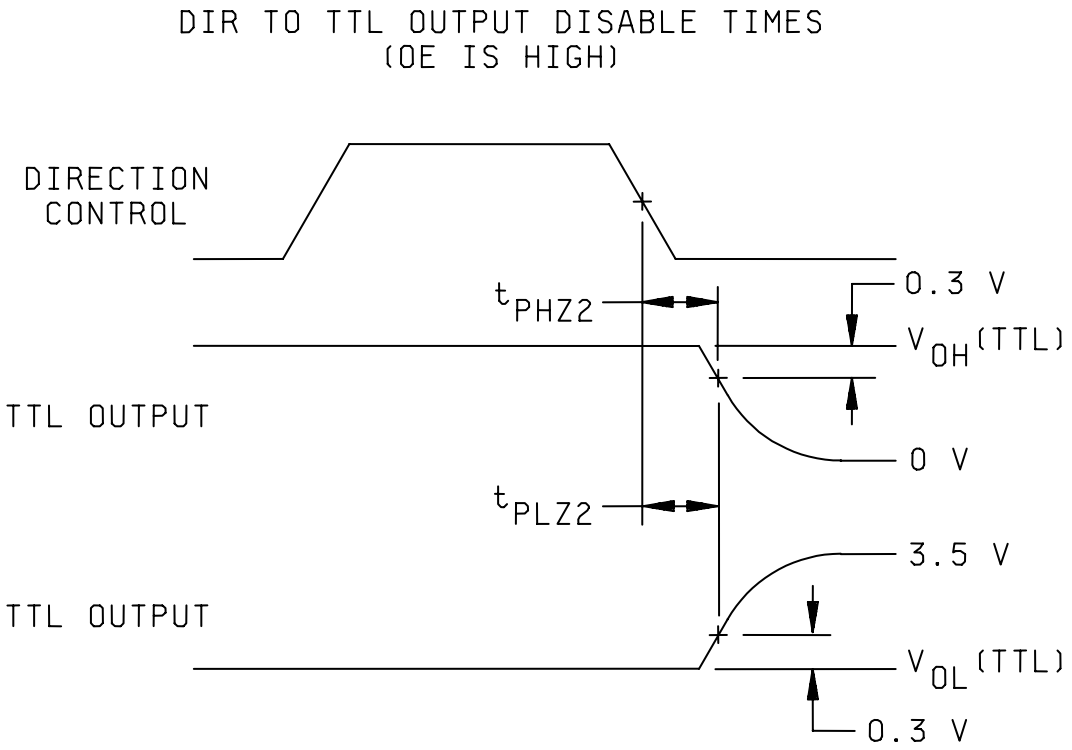
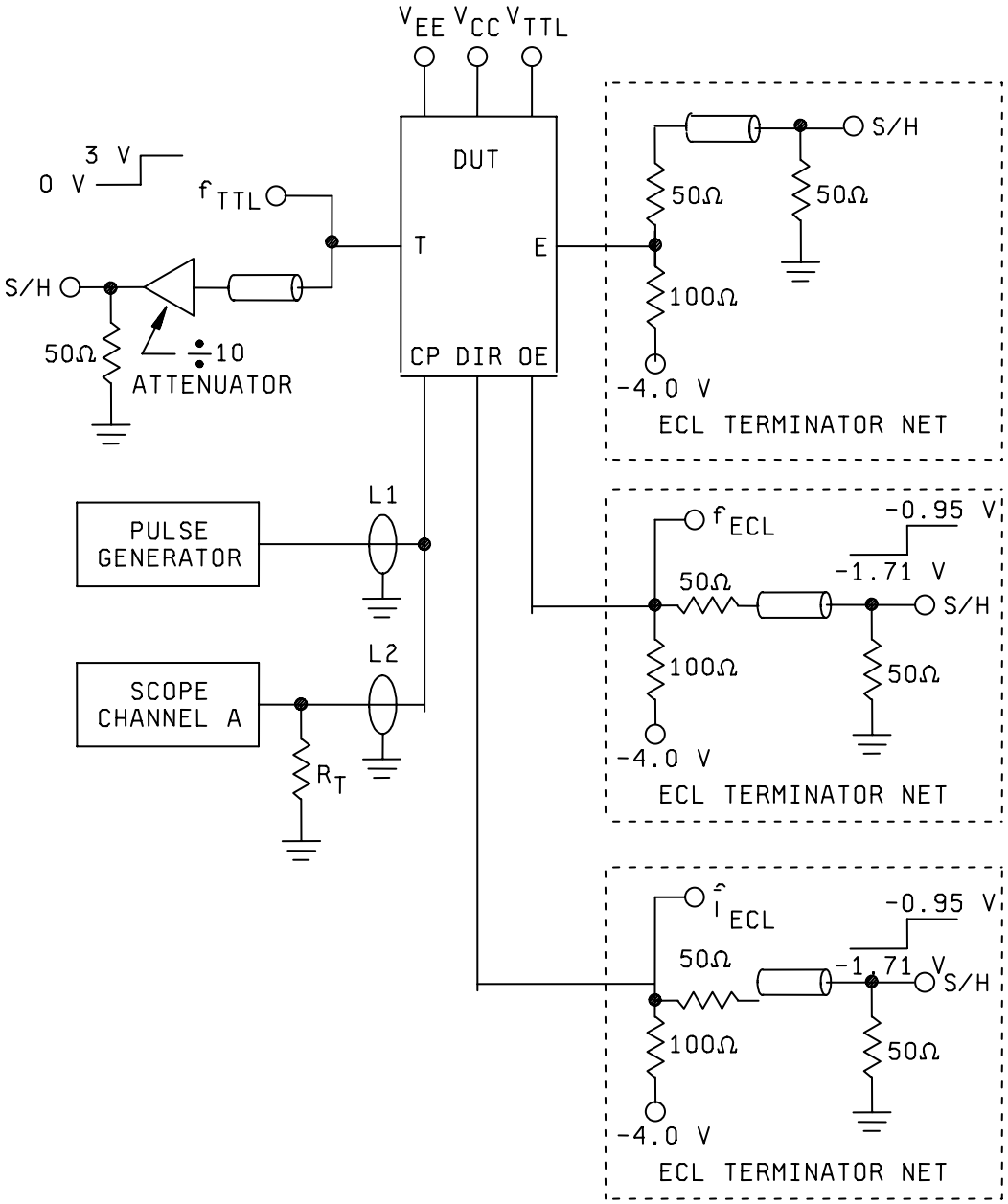


FIGURE 4. ECL-to-TTL translation test circuit and switching waveforms – Continued.

TEST CIRCUIT



Notes:
1. $V_{CC} = V_{CCA} = 0.0$ V, $V_{EE} = -4.5$ V, $V_{TTL} = +5.0$ V, $V_{IH} = +3.0$ V.
2. L1 and L2 = 50Ω impedance lines.
3. $R_T = 50\Omega$ terminator internal to scope.
4. Decoupling 0.1 μF from GND to V_{CC}, V_{EE}, and V_{TTL}.
5. All unused outputs are loaded with 50Ω to GND.
6. All coaxial cable is 50Ω.

FIGURE 5. TTL-to-ECL translation test circuit and switching waveforms.

PROPAGATION DELAY AND TRANSITION TIMES

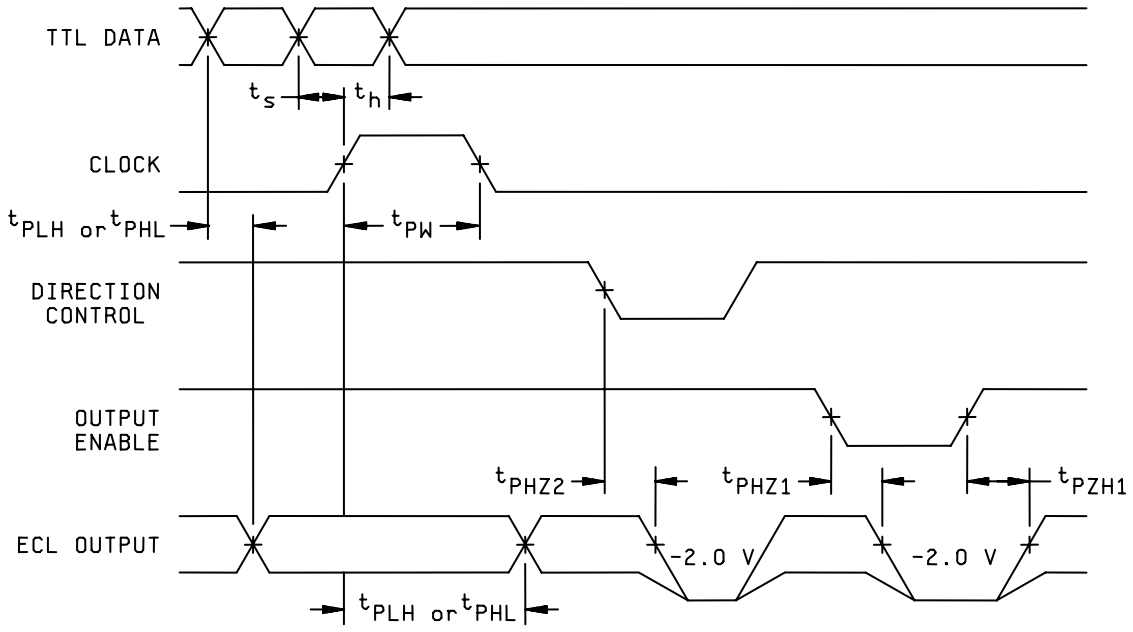


FIGURE 5. TTL-to-ECL translation test circuit and switching waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8	1, 2, 3, 7, 8
Group D end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3, 7, 8	1, 2, 3, 7, 8
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-10-27

Approved sources of supply for SMD 5962-92066 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9206601MXA	27014	100329DMQB
5962-9206601MYA	27014	100329FMQB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090