NL17SG373

Low-Power D-Type Transparent Latch with 3-State Output

The NL17SG373 MiniGate™ is an advanced high−speed CMOS D−Type Transparent Latch with 3−State Output in ultra−small footprint.

The NL17SG373 input structures provide protection when voltages up to 5.5 V are applied, regardless of the supply voltage.

This device is fully specified for partial power−down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Features

- Wide Operating V_{CC} Range: 0.9 V to 3.6 V
- High Speed: t_{PD} = 2.4 ns (Typ) @ V_{CC} = 3.0 V, C_L = 15 pF
- Low Power Dissipation: I_{CC} = 0.5 μA (Max) at T_A = 25°C
- 5.5 V Overvoltage Tolerant (OVT) Input Pins
- Ultra−Small Packages
- These Devices are Pb−Free and are RoHS Compliant

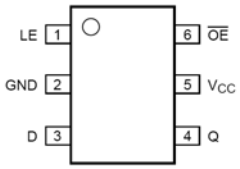

Figure 1. SC88 (Top View)

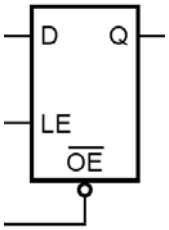

Figure 2. Logic Symbol

ON Semiconductor®

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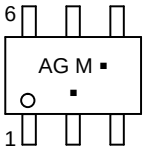
MARKING DIAGRAMS

SC−88
DF SUFFIX
CASE 419B



AG = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

Pin	Function
1	LE
2	GND
3	D
4	Q
5	V_{CC}
6	$\overline{OE}$

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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FUNCTION TABLE

Input			Internal Latch	Output	Operating Mode
$\overline{OE}$	LE	D		Q	
L	H	L	L	L	Enable and Read Register
L	H	H	H	H	(Transparent Mode)
L	L	X	L	L	Latch and Read Register
L	L	X	H	H	
H	X	X	X	Z	Latch Register and Disable Output

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +5.5	V
V_{IN}	DC Input Voltage	−0.5 to +5.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current V_{OUT} < GND, V_{OUT} > V_{CC}	±50	mA
I_O	DC Output Source/Sink Current	±20	mA
I_{CC}	DC Supply Current Per Supply Pin	±50	mA
I_{GND}	DC Ground Current per Ground Pin	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Mode (Note 2) Machine Model (Note 3)	> 3000 > 200	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 4)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22−A114−A.
3. Tested to EIA / JESD22−A115−A.
4. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	0.9	3.6	V
V_{IN}	Digital Input Voltage	0	3.6	V
V_{OUT}	Output Voltage Active Mode	0	V_{CC}	V
T_A	Operating Free−Air Temperature	−55	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Fail Rate V_{CC} = 3.3 V ± 0.3 V	0	10	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = 25°C			T_A = −55°C to +125°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage			0.9	V_{CC}			V_{CC}		V
				1.1 to 1.3	0.7 x V_{CC}			0.7 x V_{CC}		
				1.4 to 1.6	0.65 x V_{CC}			0.65 x V_{CC}		
				1.65 to 1.95	0.65 x V_{CC}			0.65 x V_{CC}		
				2.3 to 2.7	1.7			1.7		
				3.0 to 3.6	2.0			2.0		
V_{IL}	Low−Level Input Voltage			0.9			GND		GND	V
				1.1 to 1.3			0.3 x V_{CC}		0.3 x V_{CC}	
				1.4 to 1.6			0.35 x V_{CC}		0.35 x V_{CC}	
				1.65 to 1.95			0.35 x V_{CC}		0.35 x V_{CC}	
				2.3 to 2.7			0.7		0.7	
				3.0 to 3.6			0.8		0.8	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	0.9	0.75			0.75		V
			I_{OH} = −0.3 mA	1.1 to 1.3	0.75 x V_{CC}			0.75 x V_{CC}		
			I_{OH} = −1.7 mA	1.4 to 1.6	0.75 x V_{CC}			0.75 x V_{CC}		
			I_{OH} = −3.0 mA	1.65 to 1.95	V_{CC} − 0.45			V_{CC} − 0.45		
			I_{OH} = −4.0 mA	2.3 to 2.7	2.0			2.0		
			I_{OH} = −8.0 mA	3.0 to 3.6	2.48			2.48		
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	0.9			0.1		0.1	V
			I_{OL} = 0.3 mA	1.1 to 1.3			0.25 x V_{CC}		0.25 x V_{CC}	
			I_{OL} = 1.7 mA	1.4 to 1.6			0.25 x V_{CC}		0.25 x V_{CC}	
			I_{OL} = 3.0 mA	1.65 to 1.95			0.45		0.45	
			I_{OL} = 4.0 mA	2.3 to 2.7			0.4		0.4	
			I_{OL} = 8.0 mA	3.0 to 3.6			0.4		0.4	
I_{IN}	Input Leakage Current	0 ≤ V_{IN} ≤ 3.6 V		0 to 3.6			±0.1		±0.5	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND		3.6			0.5		10	μA
I_{OZ}	3−State Output Leakage Current	V_{IN} = V_{IH} or V_{IL}; V_{OUT} = 0 to 3.6 V		0.9 to 3.6			0.1		1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25 °C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, D to Q	C_L = 10 pF, R_L = 1 MΩ	0.9	–	15.3	–	–	–	ns
			1.1 to 1.3	–	6.3	12.3	1.0	14.4	
			1.4 to 1.6	–	4.4	8.1	1.0	9.4	
			1.65 to 1.95	–	3.6	6.2	0.5	6.7	
			2.3 to 2.7	–	2.6	3.9	0.5	4.4	
			3.0 to 3.6	–	2.1	3.1	0.5	3.7	
		C_L = 15 pF, R_L = 1 MΩ	0.9	–	17.7	–	–	–	ns
			1.1 to 1.3	–	7.1	13.6	1.0	15.6	
			1.4 to 1.6	–	5.0	9.2	1.0	10.4	
			1.65 to 1.95	–	4.1	6.9	1.0	7.1	
			2.3 to 2.7	–	2.9	4.4	0.5	5.0	
			3.0 to 3.6	–	2.4	3.4	0.5	3.9	
		C_L = 30 pF, R_L = 1 MΩ	0.9	–	29	–	–	–	ns
			1.1 to 1.3	–	9.3	17.3	1.0	21.2	
			1.4 to 1.6	–	6.4	11.6	1.0	12.6	
			1.65 to 1.95	–	5.3	9.1	1.0	9.6	
			2.3 to 2.7	–	4	5.7	1.0	6.1	
			3.0 to 3.6	–	3.3	4.4	1.0	4.8	
t_{PLH}, t_{PHL}	Propagation Delay, LE to Q	C_L = 10 pF, R_L = 1 MΩ	0.9	–	15.3	–	–	–	ns
			1.1 to 1.3	–	6.3	12.3	1.0	14.4	
			1.4 to 1.6	–	4.4	8.1	1.0	9.4	
			1.65 to 1.95	–	3.6	6.2	0.5	6.7	
			2.3 to 2.7	–	2.6	3.9	0.5	4.4	
			3.0 to 3.6	–	2.1	3.1	0.5	3.7	
		C_L = 15 pF, R_L = 1 MΩ	0.9	–	17.7	–	–	–	ns
			1.1 to 1.3	–	7.1	13.6	1.0	15.6	
			1.4 to 1.6	–	5.0	9.2	1.0	10.4	
			1.65 to 1.95	–	4.1	6.9	1.0	7.1	
			2.3 to 2.7	–	2.9	4.4	0.5	5.0	
			3.0 to 3.6	–	2.4	3.4	0.5	3.9	
		C_L = 30 pF, R_L = 1 MΩ	0.9	–	29	–	–	–	ns
			1.1 to 1.3	–	9.3	17.3	1.0	21.2	
			1.4 to 1.6	–	6.4	11.6	1.0	12.6	
			1.65 to 1.95	–	5.3	9.1	1.0	9.6	
			2.3 to 2.7	–	4	5.7	1.0	6.1	
			3.0 to 3.6	–	3.3	4.4	1.0	4.8	

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25 °C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PZH}, t_{PZL}	Output Enable Time, $\overline{OE}$ to Q	C_L = 10 pF, R_L = 5 kΩ	0.9	–	18.9	–	–	–	ns
			1.1 to 1.3	–	6.0	10.2	1	10.6	
			1.4 to 1.6	–	4.5	6.5	1	7.0	
			1.65 to 1.95	–	3.9	5.4	1	5.8	
			2.3 to 2.7	–	2.5	3.5	1	3.8	
			3.0 to 3.6	–	2.1	2.7	1	3	
		C_L = 15 pF, R_L = 5 kΩ	0.9	–	22	–	–	–	ns
			1.1 to 1.3	–	6.8	11.6	1	12.1	
			1.4 to 1.6	–	5.1	7.2	1	7.9	
			1.65 to 1.95	–	4.4	6.1	1	6.5	
			2.3 to 2.7	–	2.9	3.9	1	4.2	
			3.0 to 3.6	–	2.3	3	1	3.3	
		C_L = 30 pF, R_L = 5 kΩ	0.9	–	31.8	–	–	–	ns
			1.1 to 1.3	–	9.1	15.7	1	16.2	
			1.4 to 1.6	–	6.7	9.5	1	10.5	
			1.65 to 1.95	–	5.7	7.9	1	8.6	
			2.3 to 2.7	–	3.8	5	1	5.5	
			3.0 to 3.6	–	2.9	3.8	1	4.2	
t_{PHZ}, t_{PLZ}	Output Disable Time, $\overline{OE}$ to Q	C_L = 10 pF, R_L = 5 kΩ	0.9	–	11.3	–	–	–	ns
			1.1 to 1.3	–	5.3	8.3	1	8.4	
			1.4 to 1.6	–	4.1	5.8	1	6.1	
			1.65 to 1.95	–	4.2	5.7	1	5.9	
			2.3 to 2.7	–	3.0	4	1	4.2	
			3.0 to 3.6	–	3.4	4.7	1	5	
		C_L = 15 pF, R_L = 5 kΩ	0.9	–	11	–	–	–	ns
			1.1 to 1.3	–	5.8	8.2	1	11	
			1.4 to 1.6	–	3.9	5.9	1	8	
			1.65 to 1.95	–	4.5	6.6	1	7.4	
			2.3 to 2.7	–	3.2	4.3	1	5.1	
			3.0 to 3.6	–	4.8	6.2	1	6.7	
		C_L = 30 pF, R_L = 5 kΩ	0.9	–	17.7	–	–	–	ns
			1.1 to 1.3	–	9.9	15.7	1	16	
			1.4 to 1.6	–	7.7	10.8	1	11.6	
			1.65 to 1.95	–	6	12.9	1	12.9	
			2.3 to 2.7	–	5	9.1	1	9.5	
			3.0 to 3.6	–	4	12.5	1	13	

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25 °C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		0 to 3.6		1.5	–	–	–	pF
C_O	Output Capacitance	V_O = GND	0		3	–	–	–	pF
C_{PD}	Power dissipation Capacitance (Note 5)	f =10 MHz; V_I = GND to V_{CC}	0.9	–	1.6	–		–	pF
			1.1 to 1.3	–	1.7	–		–	
			1.4 to 1.6	–	1.8	–		–	
			1.65 to 1.95	–	1.9	–		–	
			2.3 to 2.7	–	2.2	–		–	
			3.0 to 3.6	–	2.7	–		–	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ ns; C_L = 5 pF, 10 pF, 15 pF and 20 pF)

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = 25 °C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
t_W	Pulse Width, LE	High	0.9	–	4.0	–	–	–	ns
			1.1 to 1.3	–	0.7	–	2.1	–	
			1.4 to 1.6	–	0.5	–	1.3	–	
			1.65 to 1.95	–	0.4	–	1.0	–	
			2.3 to 2.7	–	0.3	–	0.8	–	
			3.0 to 3.6	–	0.2	–	0.8	–	
t_{SU}	Set−Up Time, D to LE	High or Low	0.9	–	2.1	–	–	–	ns
			1.1 to 1.3	–	0.5	–	2.7	–	
			1.4 to 1.6	–	0.3	–	1.5	–	
			1.65 to 1.95	–	0.3	–	1.2	–	
			2.3 to 2.7	–	0.2	–	0.9	–	
			3.0 to 3.6	–	0.2	–	0.7	–	
t_H	Hold Time D to LE	High or Low	0.9	–	−2.8	–	–	–	ns
			1.1 to 1.3	–	−0.7	–	−0.1	–	
			1.4 to 1.6	–	−0.4	–	−0.1	–	
			1.65 to 1.95	–	−0.4	–	0	–	
			2.3 to 2.7	–	−0.3	–	0.2	–	
			3.0 to 3.6	–	−0.4	–	0.3	–	

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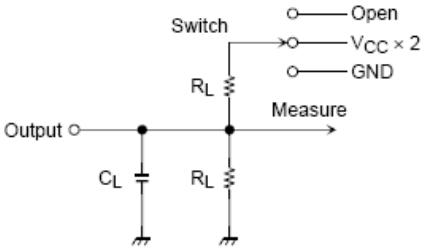
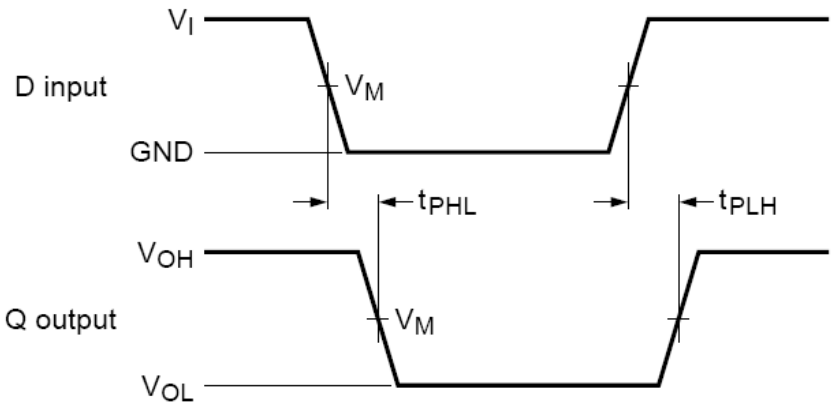


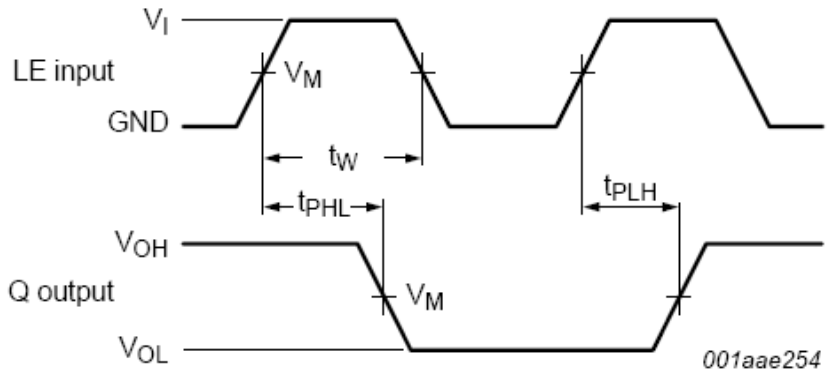
Characteristics	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	V_{CC} × 2
t_{pHZ}, t_{pZH}	GND

Figure 3. Test Circuit



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. t_{PLH}, t_{PHL} Waveforms (D to Q)



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 5. t_{PLH}, t_{PHL}, t_W Waveforms (LE to Q)

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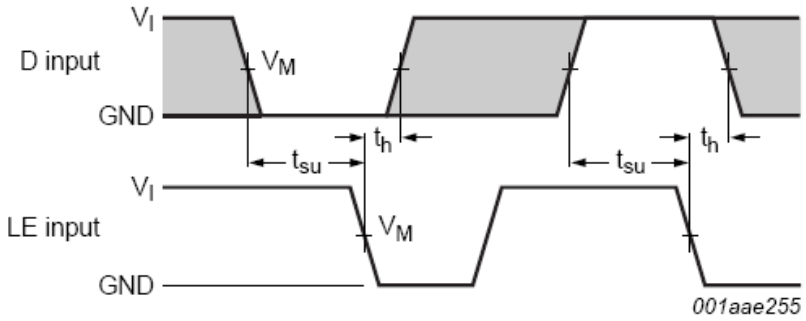
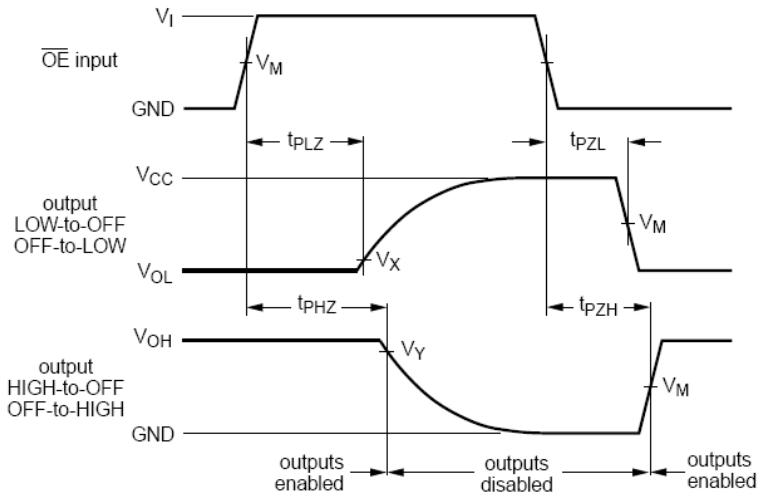


Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. t_{SU}, t_H Waveforms (D to LE)

MEASUREMENT POINTS FOR FIGURES 4, 5 AND 6

Supply Voltage	Input			Output
V_{CC}	V_M	V_I	$t_r = t_f$	V_M
0.9 V to 3.6 V	0.5 x V_{CC}	V_{CC}	≤ 3.0 ns	0.5 x V_{CC}



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL} Waveforms ($\overline{OE}$ to Q)

MEASUREMENT POINTS FOR FIGURE 7

Supply Voltage	Input			Output		
V_{CC}	V_M	V_I	$t_r = t_f$	V_M	V_X	V_Y
0.9 V	0.5 x V_{CC}	V_{CC}	≤ 3.0 ns	0.5 x V_{CC}	V_{OL} + 0.1 V	V_{OH} − 0.1 V
1.1 V to 1.3 V	0.5 x V_{CC}	V_{CC}	≤ 3.0 ns	0.5 x V_{CC}	V_{OL} + 0.1 V	V_{OH} − 0.1 V
1.4 V to 1.6 V	0.5 x V_{CC}	V_{CC}	≤ 3.0 ns	0.5 x V_{CC}	V_{OL} + 0.1 V	V_{OH} − 0.1 V
1.65 V to 1.95 V	0.5 x V_{CC}	V_{CC}	≤ 3.0 ns	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	0.5 x V_{CC}	V_{CC}	≤ 3.0 ns	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} − 0.15 V
3.0 V to 3.6 V	0.5 x V_{CC}	V_{CC}	≤ 3.0 ns	0.5 x V_{CC}	V_{OL} + 0.3 V	V_{OH} − 0.3 V

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ORDERING INFORMATION

Device	Package	Shipping†
NL17SG373DFT2G	SC−88 / SOT−363 / SC−70−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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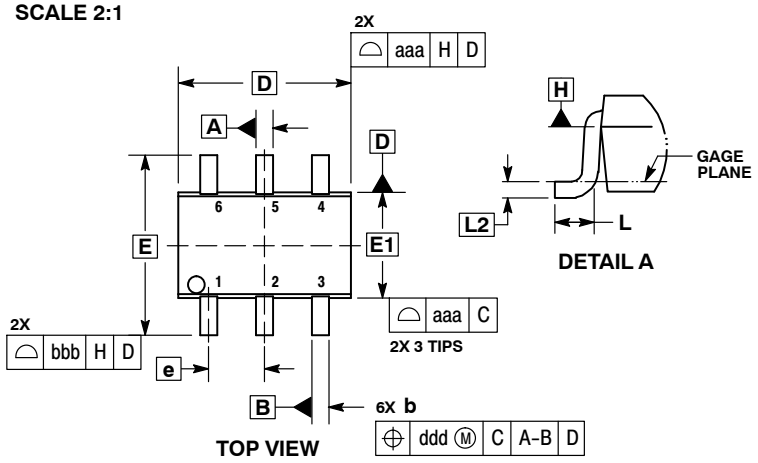
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

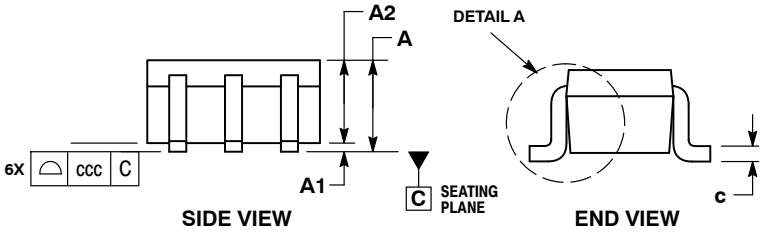
ON Semiconductor®

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

1
SCALE 2:1

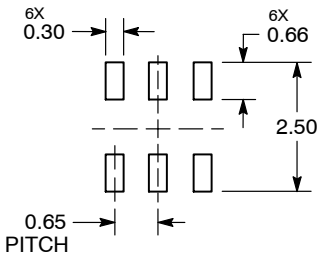




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−−	−−−	1.10	−−−	−−−	0.043
A1	0.00	−−−	0.10	0.000	−−−	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

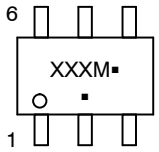
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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