2.5-V/3.3-V OSCILLATOR GAIN STAGE/BUFFERS

FEATURES

- **Low-Voltage PECL Input and Low-Voltage PECL or LVDS Outputs**
- **Clock Rates to 1 GHz**
  - **250-ps Output Transition Times**
  - **0.12 ps Typical Intrinsic Phase Jitter**
  - **Less than 630 ps Propagation Delay Times**
- **2.5-V or 3.3-V Supply Operation**
- **2-mm x 2-mm Small-Outline No-Lead Package**

APPLICATIONS

- **PECL-to-LVDS Translation**
- **Clock Signal Amplification**

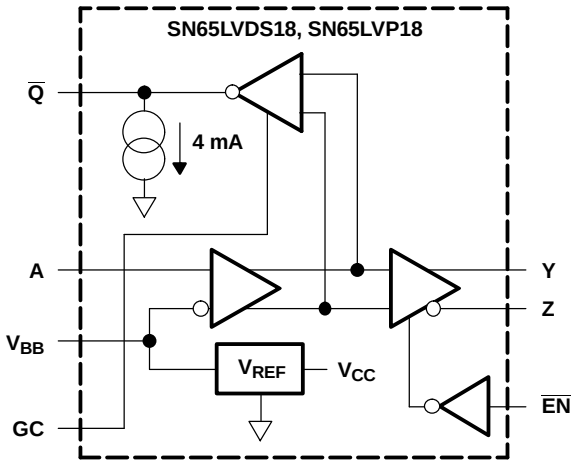
DESCRIPTION

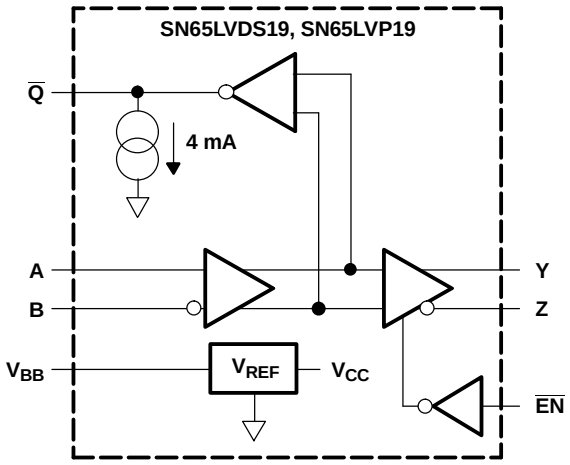
These four devices are high frequency oscillator gain stages supporting both LVPECL or LVDS on the high gain outputs in 3.3-V or 2.5-V systems. Additionally, provides the option of both single-ended input (PECL levels on the SN65LVx18) and fully differential inputs on the SN65LVx19.

The SN65LVx18 provides the user a Gain Control (GC) for controlling the $\overline{Q}$ output from 300 mV to 860 mV either by leaving it open (NC), grounded, or tied to V_{CC}. (When left open, the $\overline{Q}$ output defaults to 575 mV.) The $\overline{Q}$ on the SN65LVx19 defaults to 575 mV as well.

Both devices provide a voltage reference (V_{BB}) of typically 1.35 V below V_{CC} for use in receiving single-ended PECL input signals. When not used, V_{BB} should be unconnected or open.

All devices are characterized for operation from –40°C to 85°C.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS(1)

INPUT	OUTPUT	GAIN CONTROL	BASE PART NUMBER	PART MARKING
Single-ended	LVDS	Yes	SN65LVDS18	ER
Single-ended	LVPECL	Yes	SN65LVP18	EP
Differential	LVDS	No	SN65LVDS19	ET
Differential	LVPECL	No	SN65LVP19	ES

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{CC}	Supply voltage (2)	–0.5 V to 4 V
V_I	Input voltage	–0.5 V to V_{CC} + 0.5 V
V_O	Output voltage	–0.5 V to V_{CC} + 0.5 V
I_O	V_{BB} output current	±0.5 mA
	HBM electrostatic discharge (3)	±3 kV
	CDM electrostatic discharge (4)	±1500 V
	Continuous power dissipation	See Power Dissipation Ratings Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground (see Figure 1).
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A-7
(4) Tested in accordance with JEDEC Standard 22, Test Method C101

DISSIPATION RATINGS

PACKAGE	T_A < 25°C POWER RATING	OPERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
DRF	403 mW	4.0 mW/°C	161 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage		2.375	2.5 or 3.3	3.6	V
V_{IC}	Common-mode input voltage (V_{IA} + V_{IB})/2	SN65LVDS19 or SN65LVP19	1.2		V_{CC} – (V_{ID}/2)	V
$\|V_{ID}\|$	Differential input voltage magnitude $\|V_{IA}$ - $V_{IB}\|$	SN65LVDS19 or SN65LVP19	0.8		1	V
V_{IH}	High-level input voltage	$\overline{EN}$	2		V_{CC}	V
		SN65LVDS18 or SN65LVP18	V_{CC}– 1.17		V_{CC}– 0.44	
V_{IL}	Low-level input voltage	$\overline{EN}$	0		0.8	V
		SN65LVDS18 or SN65LVP18	V_{CC}– 2.25		V_{CC}– 1.52	
I_O	Output current to V_{BB}		–400 (1)		400	µA
R_L	Differential load resistance		90		132	Ω
T_A	Operating free-air temperature		-40		85	°C

(1) The algebraic convention, where the least positive (more negative) value is designated minimum, is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	R_L = 100 Ω, $\overline{EN}$ at 0 V, Other inputs open		30	36	mA
		Outputs unloaded, $\overline{EN}$ at 0 V, Other inputs open		17	22	
V_{BB}	Reference voltage(2)	I_{BB} = –400 µA	V_{CC}– 1.44	V_{CC}– 1.35	V_{CC}– 1.25	V
I_{IH}	High-level input current, $\overline{EN}$	V_I = 2 V	–20		20	µA
I_{IAH} or I_{IBH}	High-level input current, A or B	V_I = V_{CC}	–20		20	
I_{IL}	Low-level input current, $\overline{EN}$	V_I = 0.8 V	–20		20	
I_{IAL} or I_{IBL}	Low-level input current, A or B	V_I = GND	–20		20	
SN65LVDS18/19 Y AND Z OUTPUT CHARACTERISTICS						
$\|V_{OD}\|$	Differential output voltage magnitude, $\|V_{OY}– V_{OZ}\|$	See Figure 1 and Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states				50	
$V_{OC(SS)}$	Steady-state common- mode output voltage (see Figure 3)		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3	–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	100	
I_{OYZ} or I_{OZZ}	High-impedance output current	$\overline{EN}$ at V_{CC}, V_O = 0 V or V_{CC}	–1		1	µA
I_{OYS} or I_{OZS}	Short-circuit output current	$\overline{EN}$ at 0 V, V_{OY} or V_{OZ} = 0 V	–50		50	mA
$I_{OS(D)}$	Differential short-circuit output current, $\|I_{OY}– I_{OZ}\|$	$\overline{EN}$ at 0 V, V_{OY} = V_{OZ}	–12		12	
SN65LVP18/19 Y AND Z OUTPUT CHARACTERISTICS						
V_{OYH} or V_{OZH}	High-level output voltage	3.3 V; 50 Ω from Y and Z to V_{CC} - 2 V	V_{CC}– 1.13		V_{CC}– 0.85	V
V_{OYL} or V_{OZL}	Low-level output voltage		V_{CC}– 1.87		V_{CC}– 1.61	
V_{OYL} or V_{OZL}	Low-level output voltage	2.5 V; 50 Ω from Y and Z to V_{CC}– 2 V	V_{CC}– 1.92		V_{CC}– 1.61	
$\|V_{OD}\|$	Differential output voltage magnitude, $\|V_{OH}– V_{OL}\|$		0.6	0.8	1	
I_{OYZ} or I_{OZZ}	High-impedance output current	$\overline{EN}$ at V_{CC}, V_O = 0 V or V_{CC}	–1		1	µA
$\overline{Q}$ OUTPUT CHARACTERISTICS (see Figure 1)						
V_{OH}	High-level output voltage	No load		V_{CC}– 0.94		V
V_{OL}	Low-level output voltage	GC Tied to GND, No load		V_{CC}– 1.22		V
		GC Open, No load		V_{CC}– 1.52		
		GC Tied to V_{CC}, No load		V_{CC}– 1.82		
$V_{O(pp)}$	Peak-to-peak output voltage	GC Tied to GND		300		mV
		GC Open		575		
		CGT Tied to V_{CC}		860		

(1) Typical values are at room temperature and with a V_{CC} of 3.3 V.
(2) Single-ended input operation is limited to V_{CC}≥ 3.0 V.

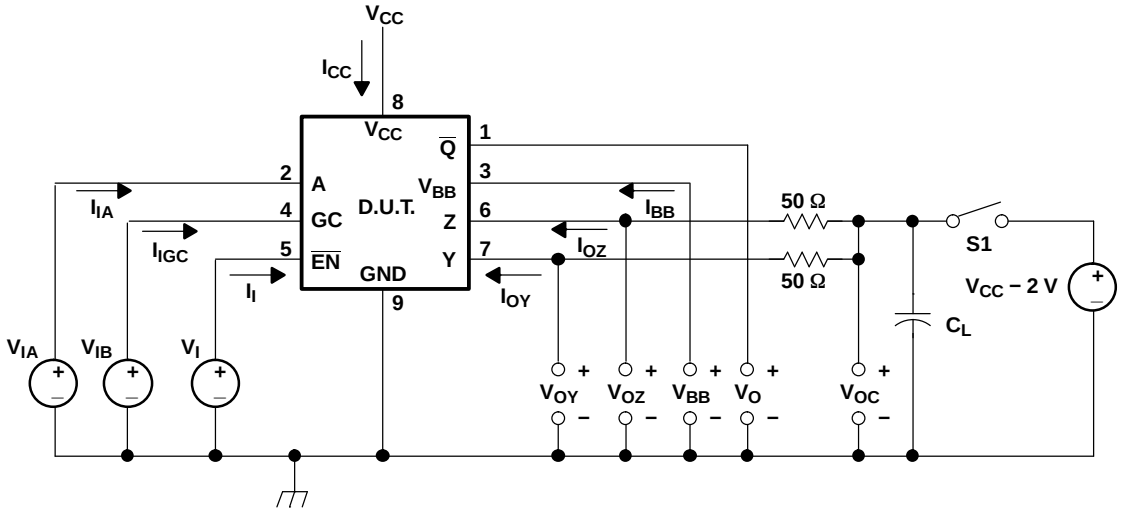
SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PD}	Propagation delay time, t_{PLH} or t_{PHL}	A to $\overline{Q}$	See Figure 4		340	460	ps
		D to Y or Z			460	630	
$t_{SK(P)}$	Pulse skew, $\lvert t_{PLH} - t_{PHL} \rvert$					20	
$t_{SK(PP)}$	Part-to-part skew (2)		V_{CC} = 3.3 V			80	ps
			V_{CC} = 2.5 V			130	
t_r	20%-to-80% differential signal rise time		LVDS, See Figure 4		140	250	ps
			LVPECL, See Figure 4		190	300	
t_f	20%-to-80% differential signal fall time		LVDS, See Figure 4		140	250	ps
			LVPECL, See Figure 4		210	300	
$t_{jit(per)}$	RMS period jitter(3)		2-GHz 50%-duty-cycle square-wave input, See Figure 5		2	4	ps
$t_{jit(cc)}$	Peak cycle-to-cycle jitter (4)				17	24	
$t_{jit(ph)}$	Intrinsic phase jitter		1 GHz		0.12		ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output		See Figure 6			30	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output					30	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output					30	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output					30	

(1) Typical values are at room temperature and with a V_{CC} of 3.3 V.
(2) Part-to-part skew is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle pairs.

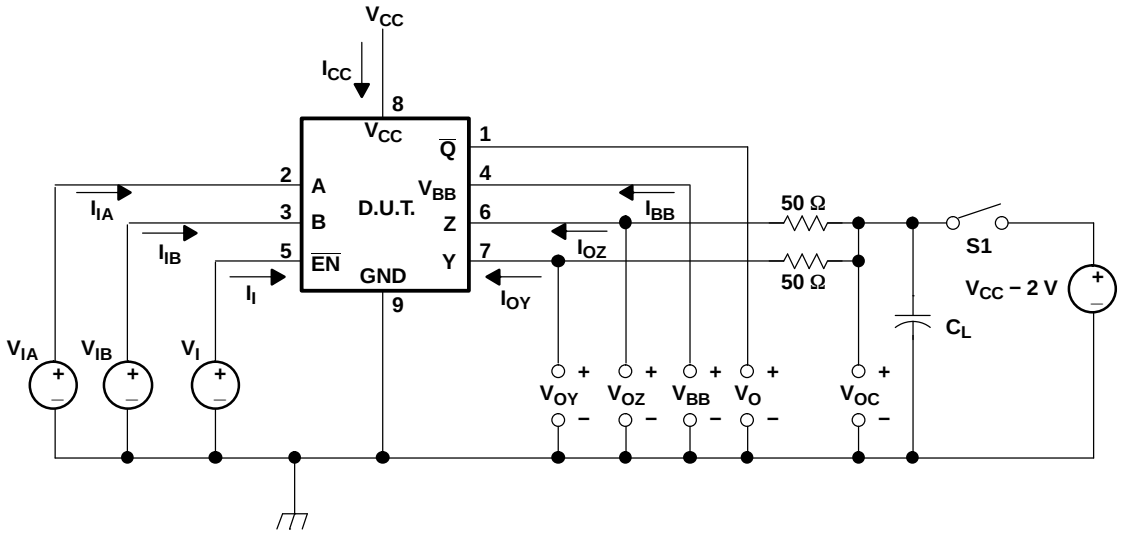
PARAMETER MEASUREMENT INFORMATION



(1) C_L is the instrumentation and test fixture capacitance.
(2) S1 is open for the SN65LVDS18 and closed for the SN65LVP18.

Figure 1. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP18

PARAMETER MEASUREMENT INFORMATION (continued)



(1) C_L is the instrumentation and test fixture capacitance.

(2) S1 is open for the SN65LVDS19 and closed for the SN65LVP19.

Figure 2. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP19

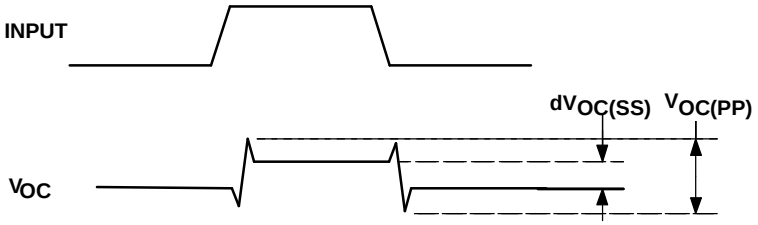


Figure 3. V_{OC} Definitions

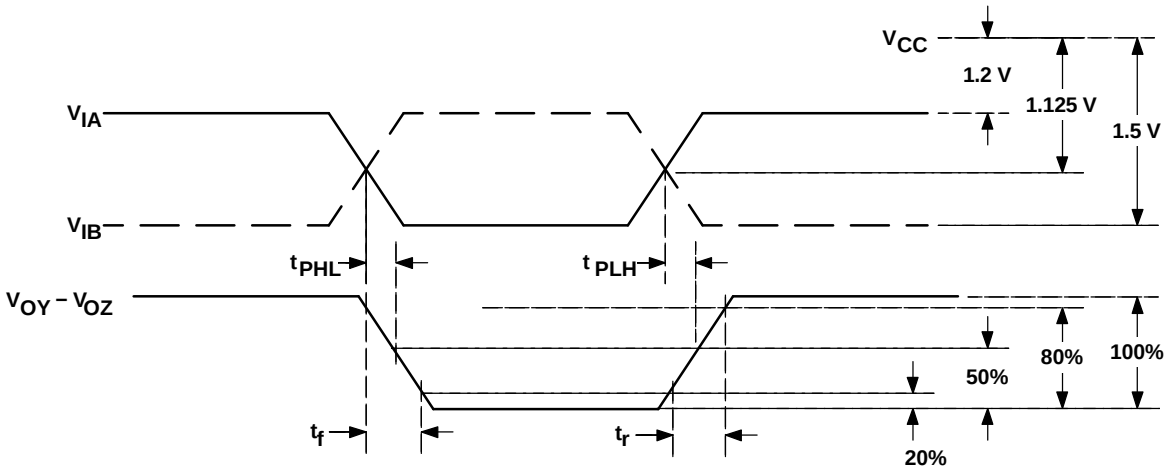


Figure 4. Propagation Delay and Transition Time Test Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

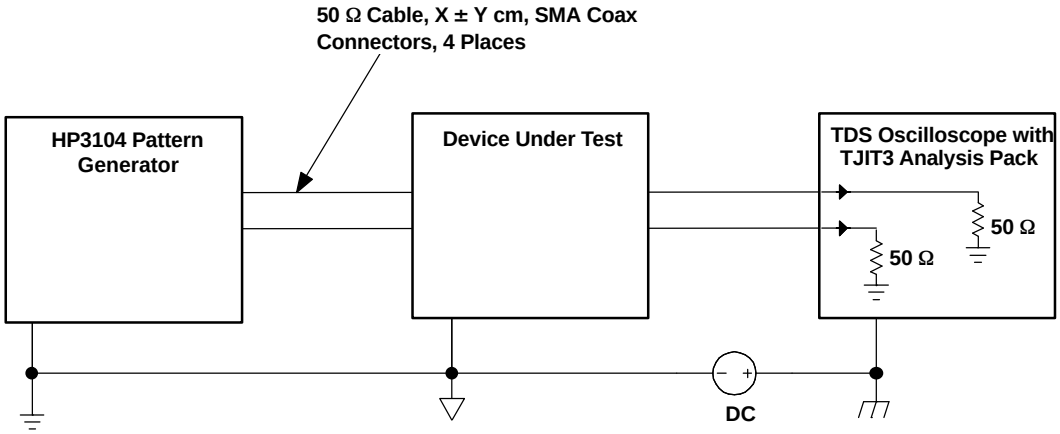


Figure 5. Jitter Measurement Setup

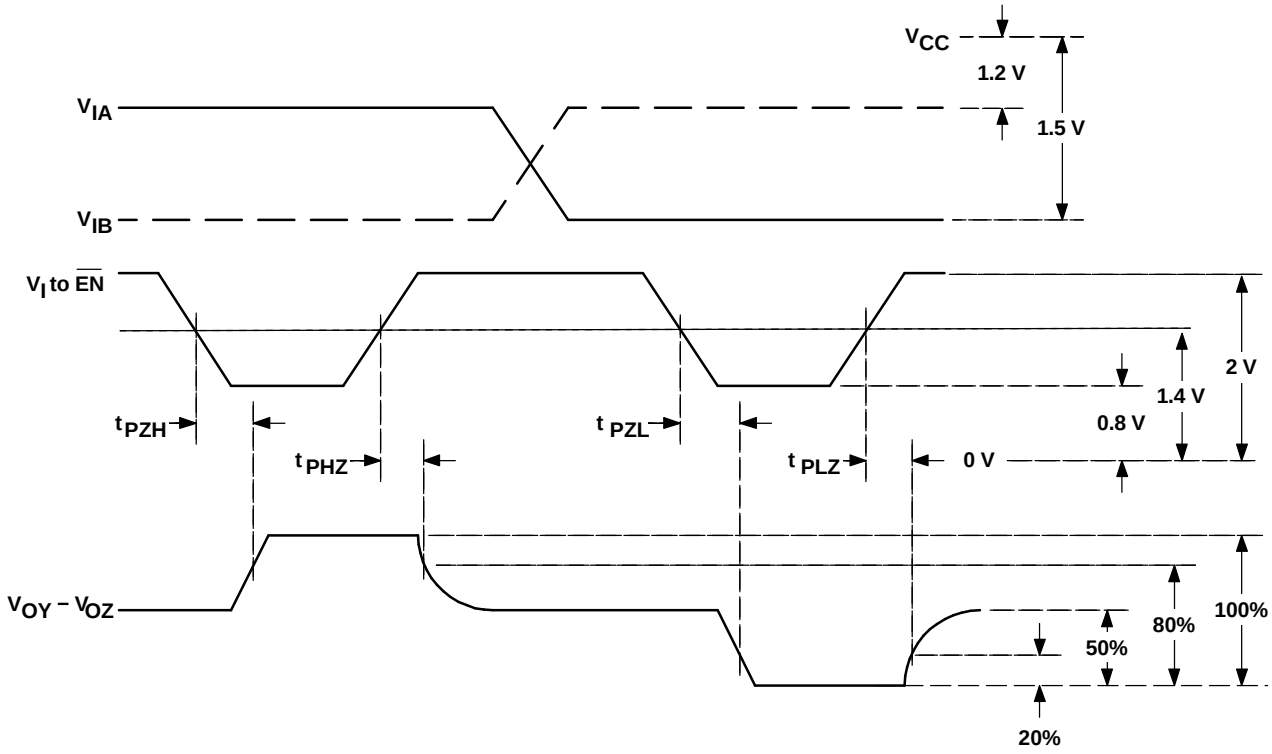


Figure 6. Enable and Disable Time Test Waveforms

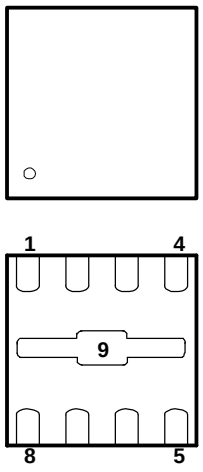
DEVICE INFORMATION

FUNCTION TABLE (1)

SN65LVDS18, SN65LVP18					SN65LVDS19, SN65LVP19					
A	$\overline{EN}$	$\overline{Q}$	Y	Z	A	B	$\overline{EN}$	$\overline{Q}$	Y	Z
H	L	L	H	L	H	H	L	?	?	?
L	L	H	L	H	L	H	L	H	L	H
X	H	?	Z	Z	H	L	L	L	H	L
Open	L	?	?	?	L	L	L	?	?	?
X	Open	?	?	?	X	X	H	?	Z	Z
					Open	Open	L	?	?	?
					X	X	Open	?	?	?

(1) H = high, L = low, Z = high impedance, ? = indeterminate

DRF PACKAGE
TOP VIEW



BOTTOM VIEW

Package Pin Assignments – Numerical Listing

SN65LVDS18, SN65LVP18		SN65LVDS19, SN65LVP19	
PIN	SIGNAL	PIN	SIGNAL
1	$\overline{Q}$	1	$\overline{Q}$
2	A	2	A
3	V_{BB}	3	B
4	GC	4	V_{BB}
5	$\overline{EN}$	5	$\overline{EN}$
6	Z	6	Z
7	Y	7	Y
8	V_{CC}	8	V_{CC}
9	GND	9	GND

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

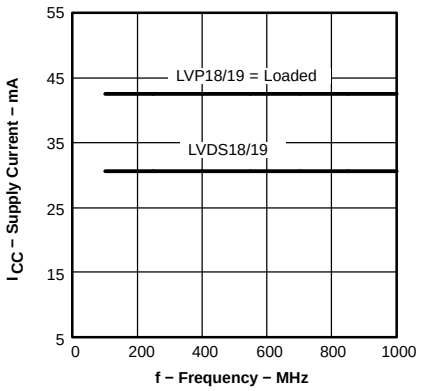


Figure 7.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

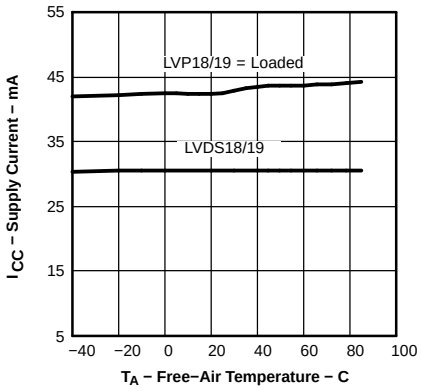


Figure 8.

LVDS18/19 RISE/FALL TIME vs FREE-AIR TEMPERATURE

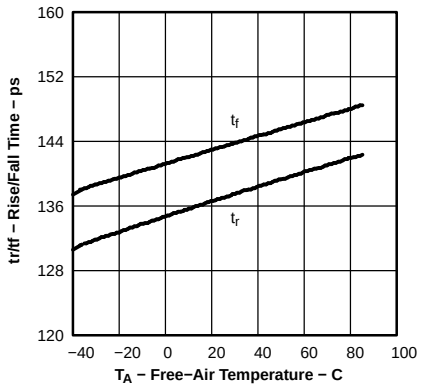


Figure 9.

LVP18/19 RISE/FALL TIME vs FREE-AIR TEMPERATURE

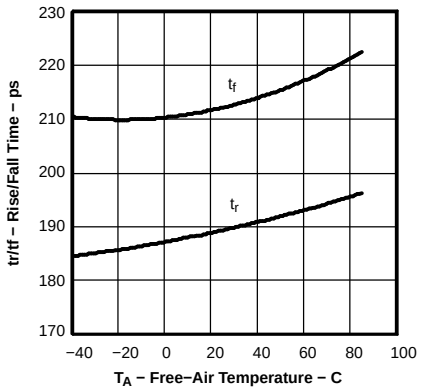


Figure 10.

LVDS18/19 PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

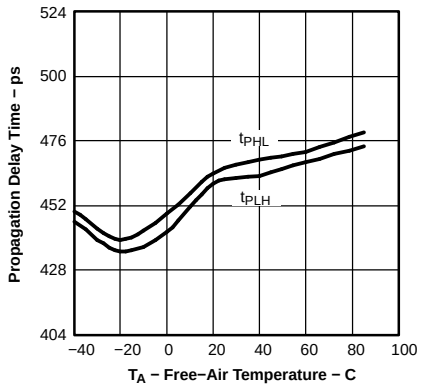


Figure 11.

PERIOD JITTER vs FREQUENCY

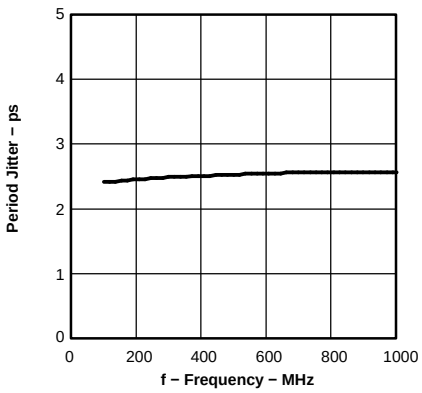


Figure 12.

CYCLE-TO-CYCLE JITTER vs FREQUENCY

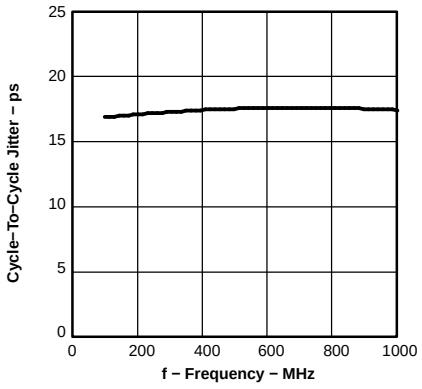
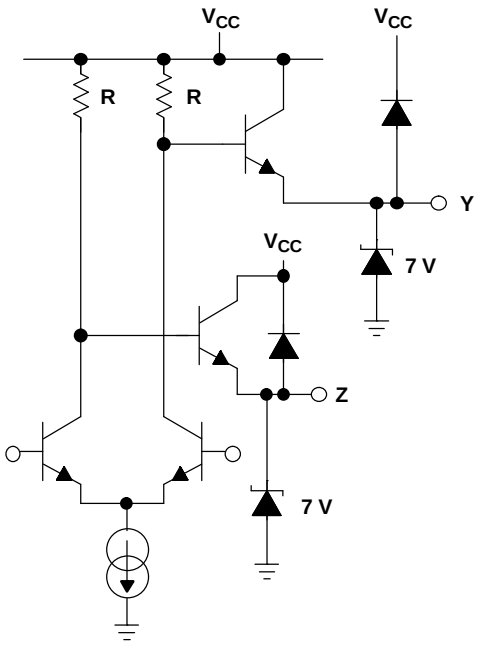


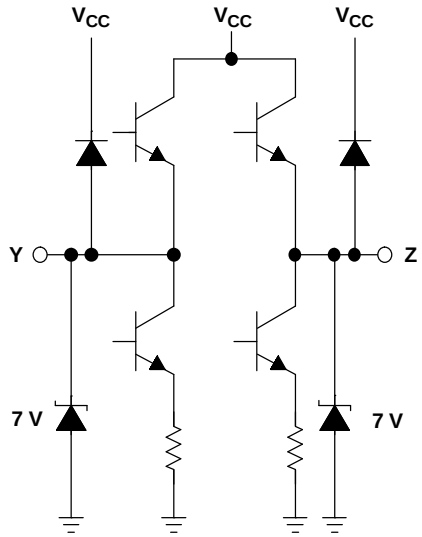
Figure 13.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

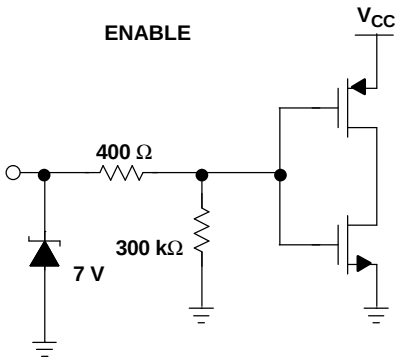
OUTPUT LVP18/19



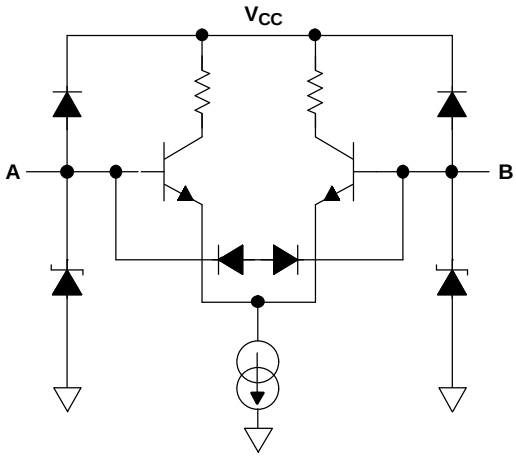
OUTPUT LVDS18/19



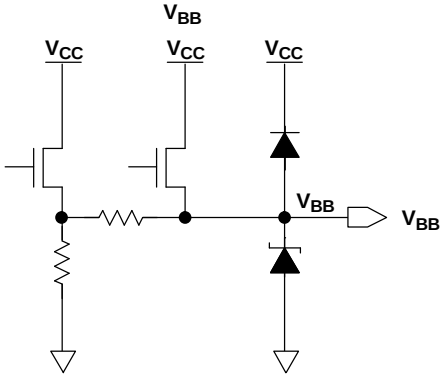
ENABLE



INPUT



OUTPUT



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS18DRFT	Active	Production	WSON (DRF) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ER
SN65LVDS19DRFT	Active	Production	WSON (DRF) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ET
SN65LVP18DRFT	Active	Production	WSON (DRF) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	EP
SN65LVP19DRFT	Active	Production	WSON (DRF) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ES

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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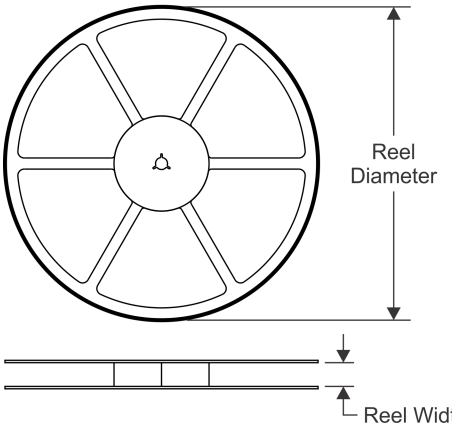
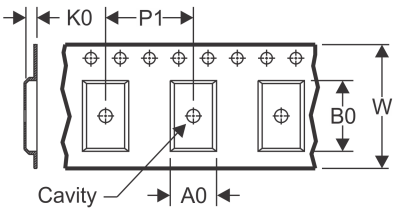
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

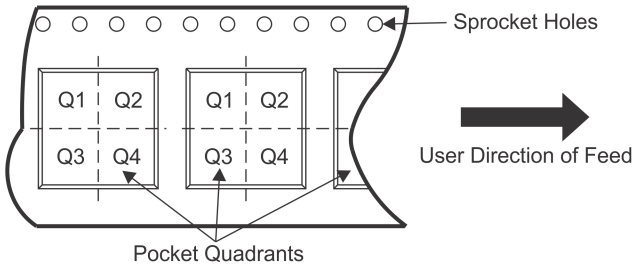


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

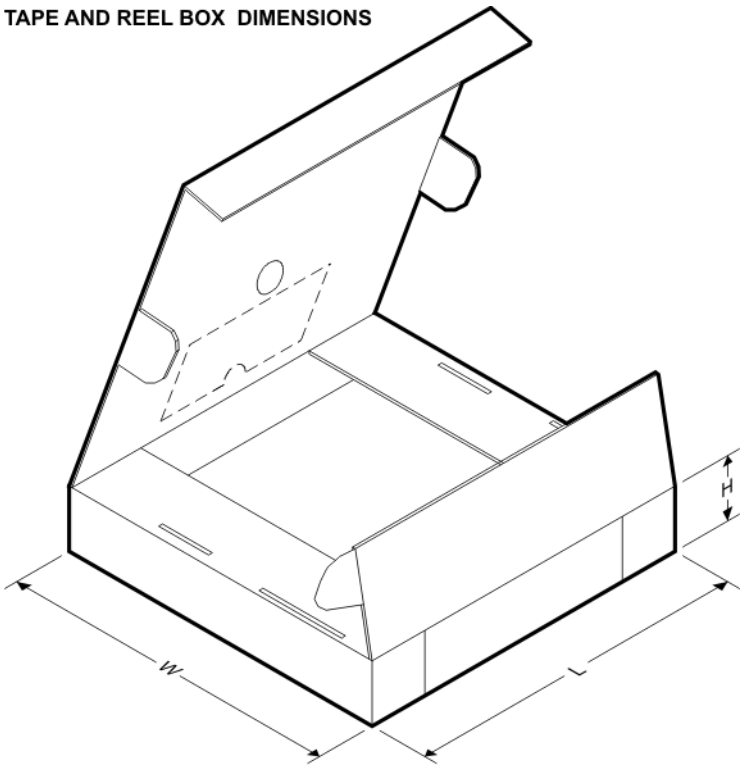
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS18DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVDS19DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP18DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP19DRFT	WSON	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2

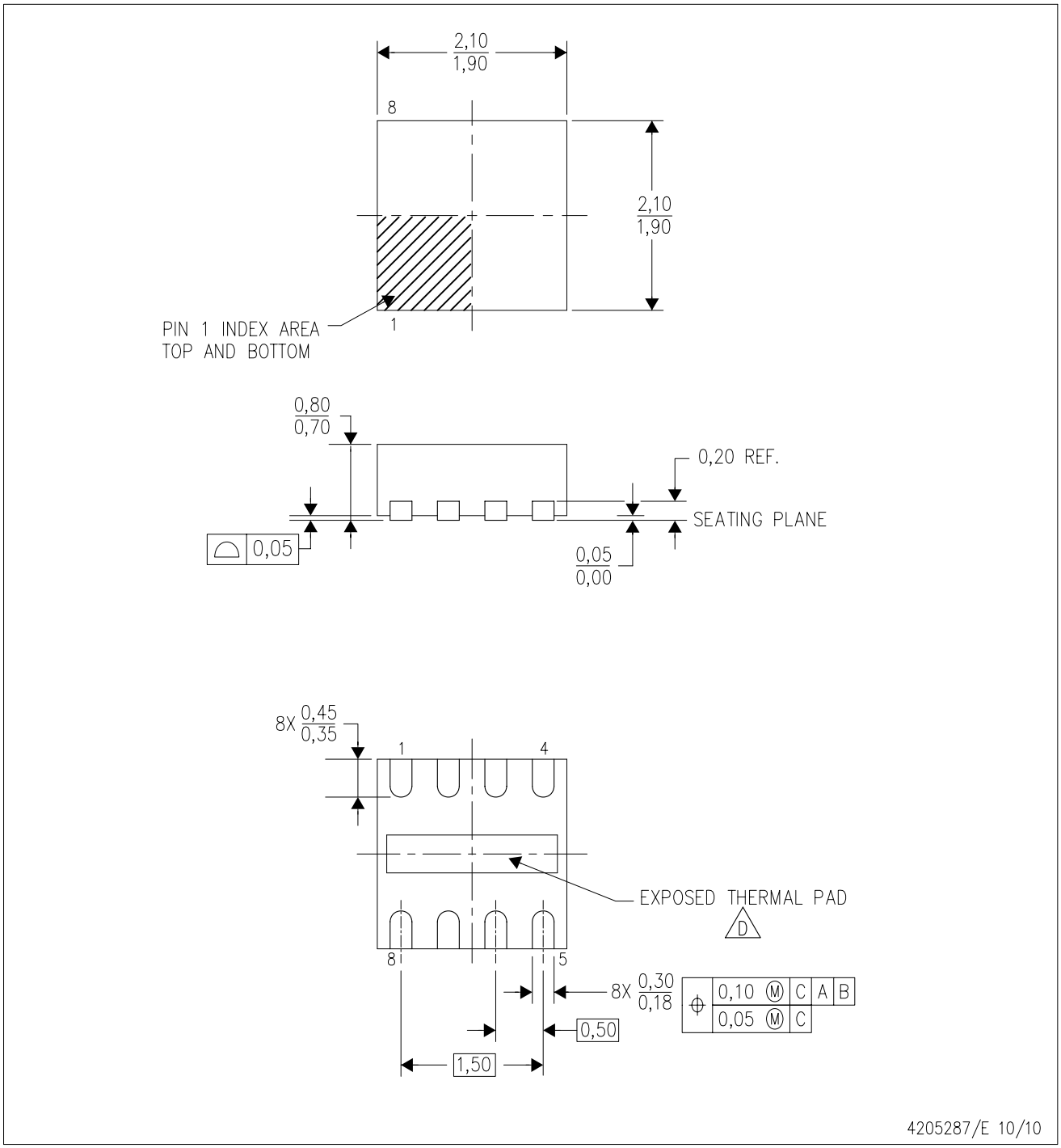
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS18DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVDS19DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVP18DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVP19DRFT	WSON	DRF	8	250	337.0	343.0	29.0

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

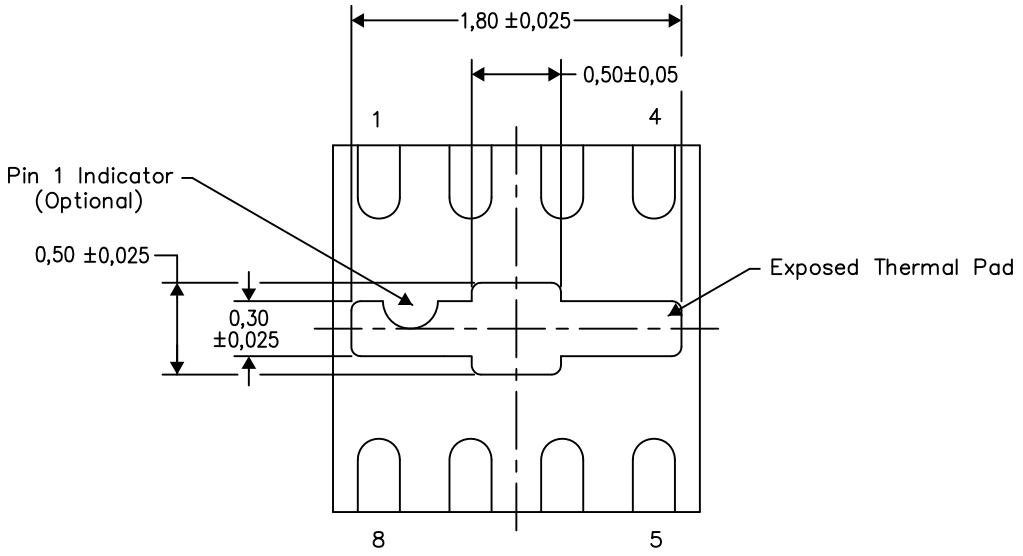
DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



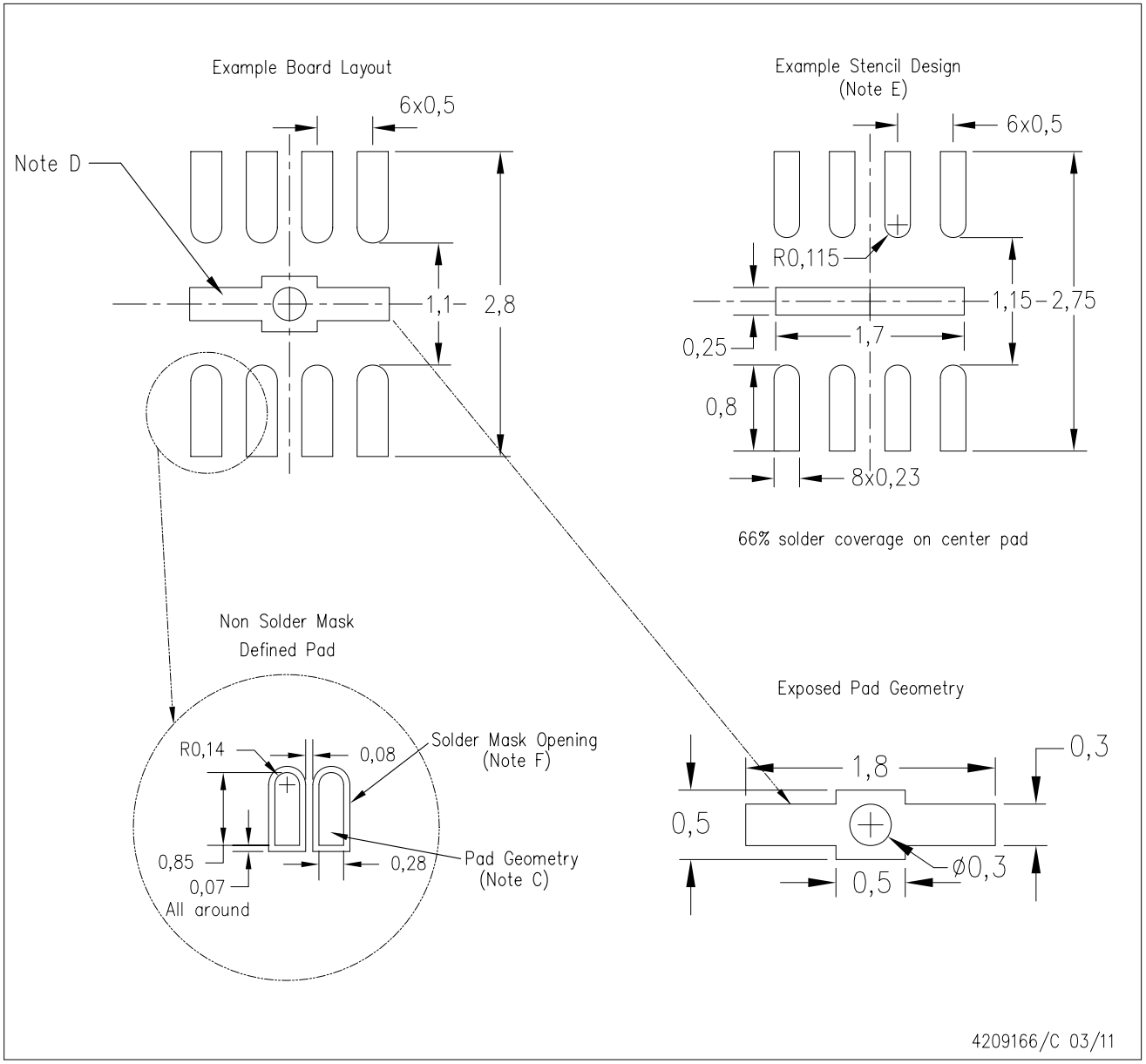
Bottom View

Exposed Thermal Pad Dimensions

4206840/H 12/14

NOTE: A. All linear dimensions are in millimeters

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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