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FQP4N80

N-Channel QFET® MOSFET 800 V, 3.9 A, 3.6 Ω

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 3.9 A, 800 V, $R_{DS(on)} = 3.6 \Omega$ (Max.) @ $V_{GS} = 10$ V, $I_D = 1.95$ A
- Low Gate Charge (Typ. 19 nC)
- Low $Crss$ (Typ. 8.6 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP4N80	Unit
V_{DSS}	Drain-Source Voltage	800	V
I_{DM}	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	3.9	A
	- Continuous ($T_C = 100^\circ\text{C}$)	2.47	A
I_{DM}	Drain Current - Pulsed	(Note 1)	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	130	W
	- Derate above 25°C	1.04	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQP4N80	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.96	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP4N80	FQP4N80	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	800	--	--	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	--	0.95	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 800 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$	--	--	0	μA
		$V_{\text{DS}} = 640 \text{ V}$, $T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{\text{GS}} = 30 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{\text{GS}} = -30 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	--	--	0	nA

On Characteristics

$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250 \mu\text{A}$	--	5.0	--	V
$R_{\text{DS}(\text{on})}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 3.9 \text{ A}$	--	2.8	3.6	Ω
g_{FS}	Forward Transconductance	$V_{\text{DS}} = 10 \text{ V}$, $I_D = 3.9 \text{ A}$	--	3.8	--	mS

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{\text{DS}} = 250 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, 1.0 MHz	--	680	880	pF
C_{oss}	Output Capacitance	--	--	75	100	pF
C_{rss}	Reverse Transfer Capacitance	--	--	8.6	12	pF

Switching Characteristics

$t_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}} = 100 \text{ V}$, $I_D = 3.9 \text{ A}$, $R_G = 25 \Omega$	--	16	40	ns
t_r	Turn-On Rise Time	--	--	45	100	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	--	--	35	80	ns
t_f	Turn-Off Fall Time	--	--	35	80	ns
t_{tr}	Total Gate Charge	$V_{\text{DS}} = 640 \text{ V}$, $I_D = 3.9 \text{ A}$, $V_{\text{GS}} = 10 \text{ V}$	--	19	25	nC
Q_{gs}	Gate-Source Charge	--	--	4.2	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	9.1	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	3.9	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	15.6	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 3.9 \text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 3.9 \text{ A}$, $dI_F / dt = 100 \text{ A}/\mu\text{s}$	--	575	--	ns
Q_{rr}	Reverse Recovery Charge	--	--	3.65	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $L = 57 \text{ mH}$, $I_{\text{AS}} = 3.9 \text{ A}$, $V_{\text{DD}} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{\text{SD}} \leq 3.9 \text{ A}$, $dI/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{\text{DD}} \leq \text{BV}_{\text{DSS}}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Characteristics

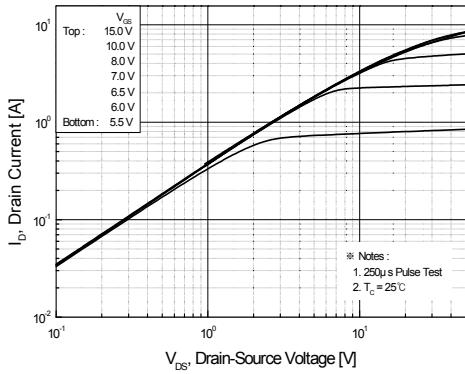


Figure 1. On-Region Characteristics

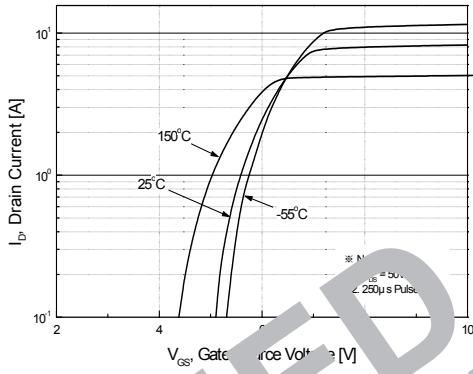


Figure 2. Transfer Characteristics

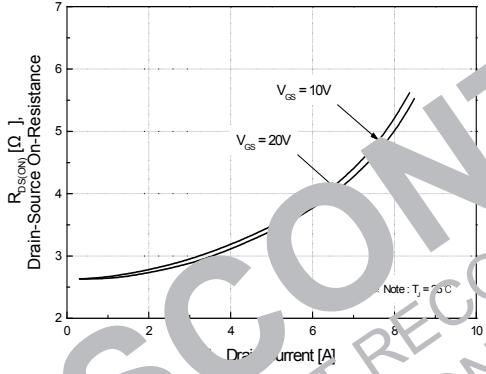


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

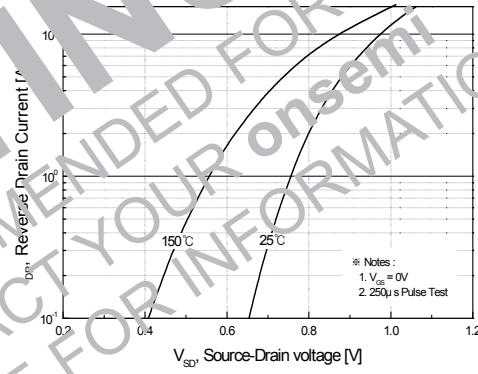


Figure 4. Body Diode Forward Voltage
Variation vs. Source Current
and Temperature

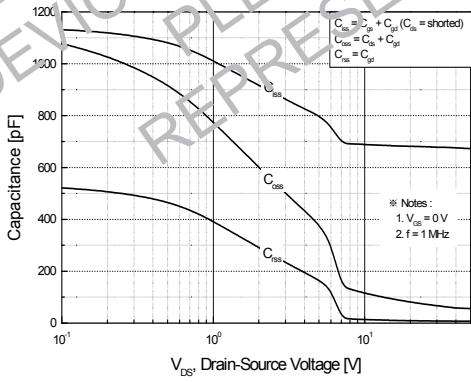


Figure 5. Capacitance Characteristics

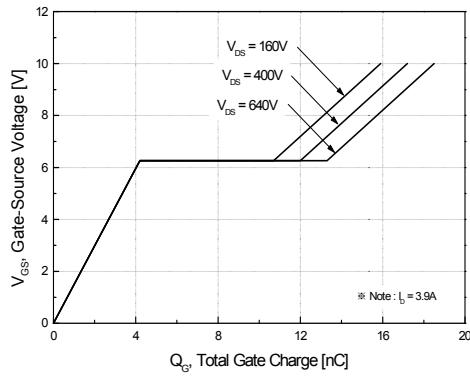


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

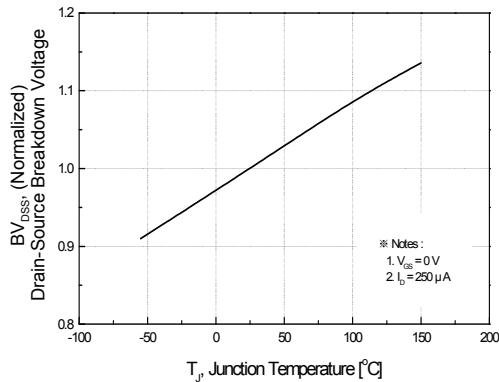


Figure 7. Breakdown Voltage Variation vs. Temperature

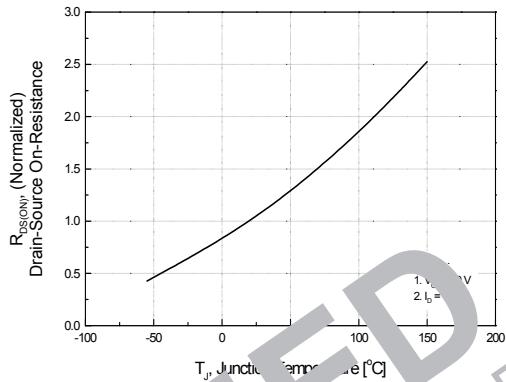


Figure 8. On-Resistance Variation vs. Temperature

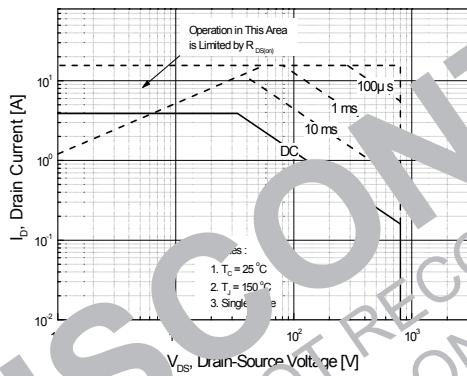


Figure 9. Maximum Safe Operating Area

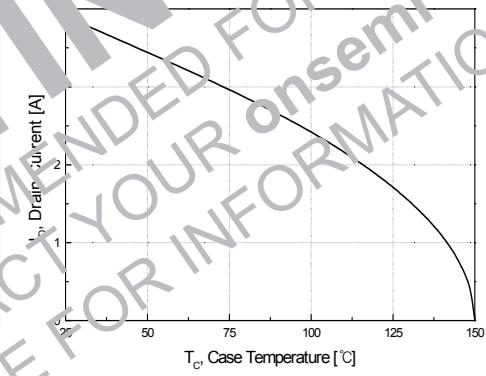


Figure 10. Maximum Drain Current vs. Case Temperature

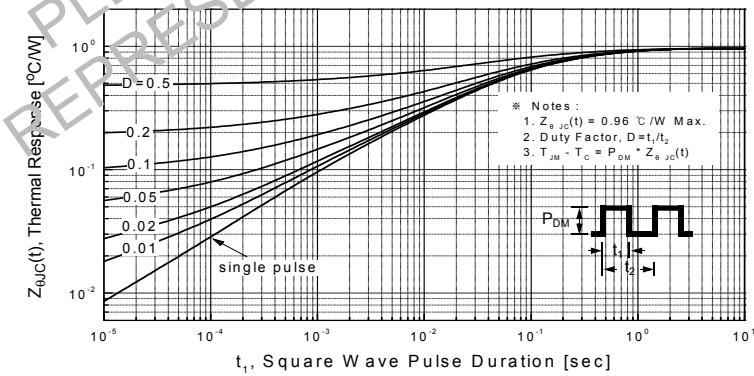


Figure 11. Transient Thermal Response Curve

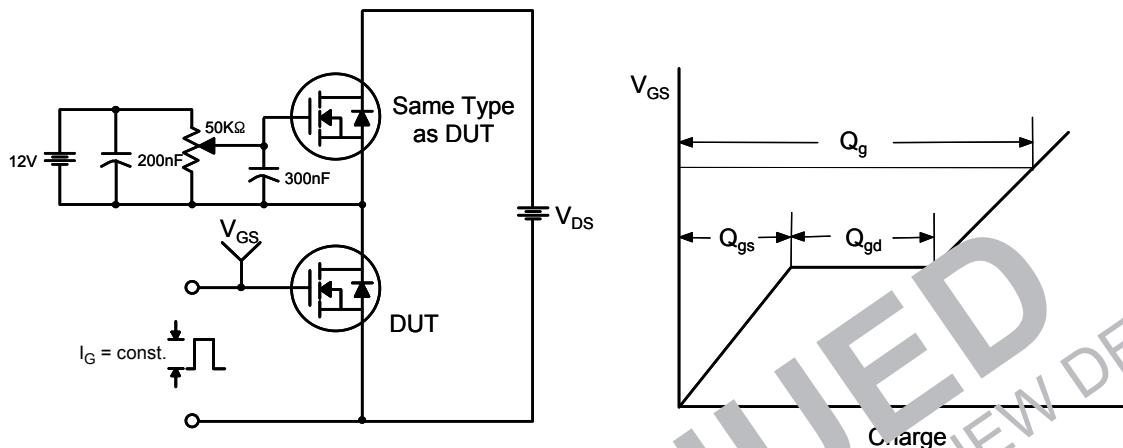


Figure 12. Gate Charge Test Circuit & Waveforms



Figure 13. Resistive Switching Test Circuit & Waveforms

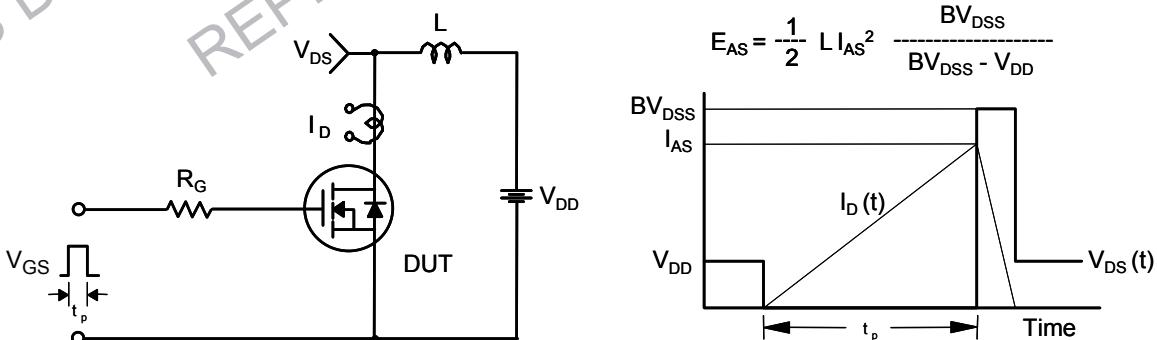
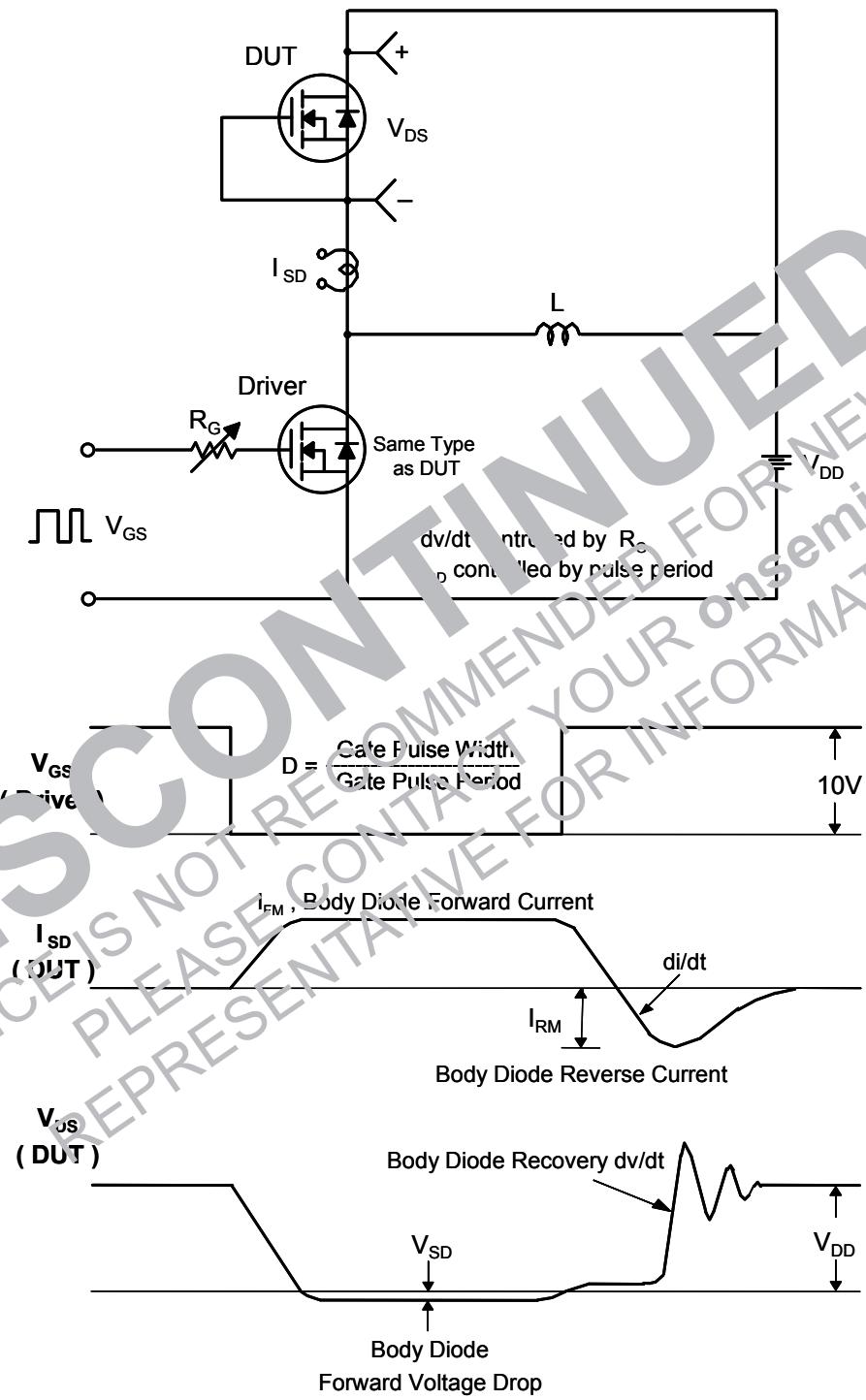


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

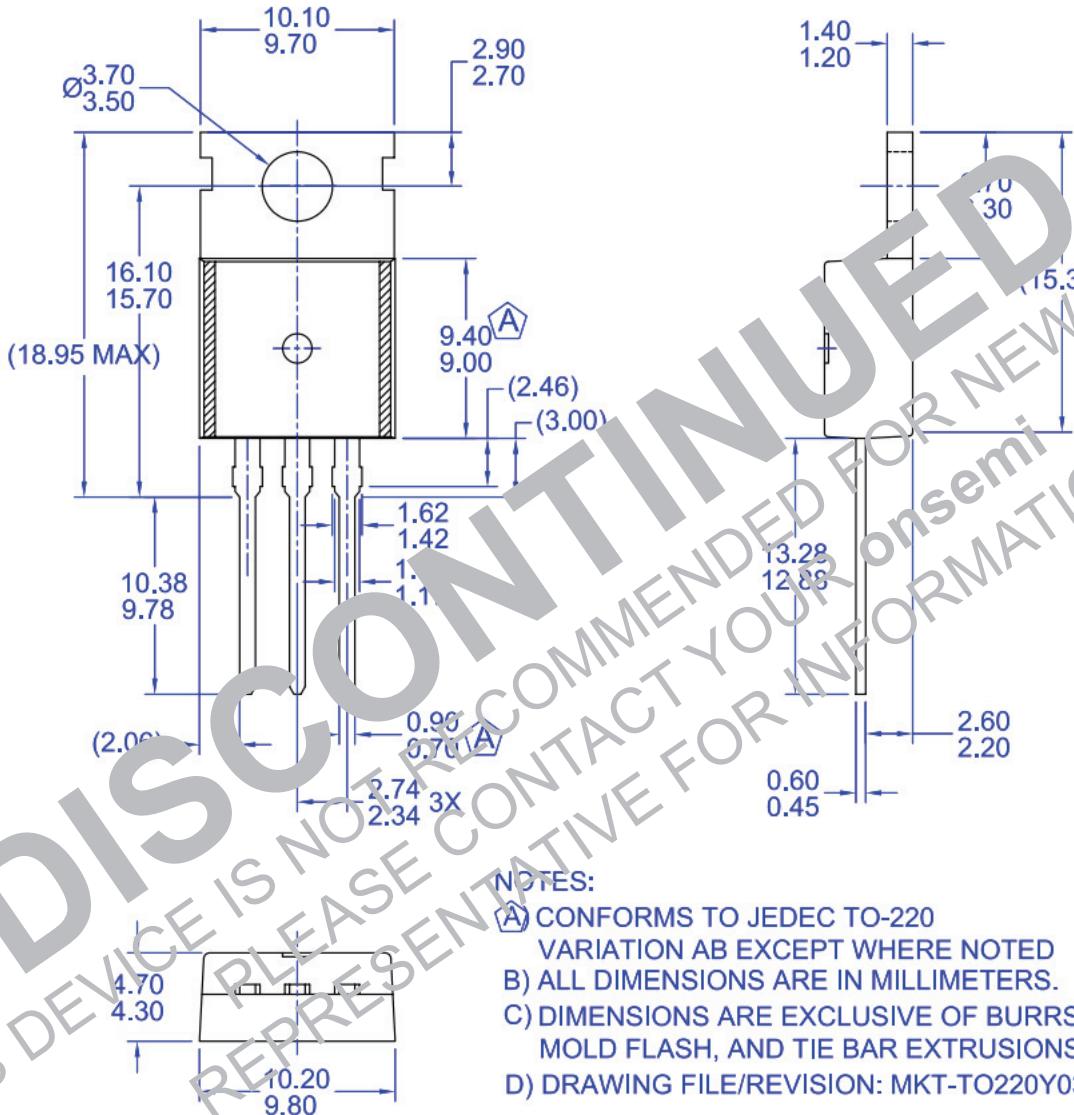


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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