

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSII)

## SSM3J14T

### Power Management Switch

### DC-DC Converters

- Suitable for high-density mounting due to compact package
- Low on Resistance:  $R_{on} = 145 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.5 \text{ V}$ )  
:  $R_{on} = 85 \text{ m}\Omega$  (max) (@ $V_{GS} = -10 \text{ V}$ )
- High-speed switching

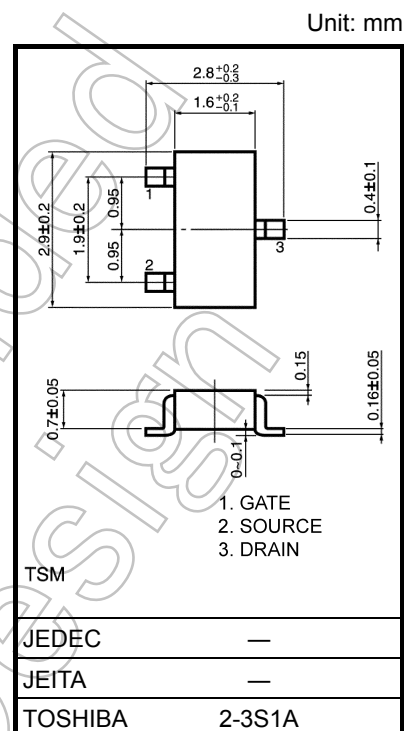
### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		$V_{DS}$	-30	V
Gate-Source voltage		$V_{GSS}$	$\pm 20$	V
Drain current	DC	$I_D$	-2.7	A
	Pulse	$I_{DP}$ (Note 2)	-5.4	
Drain power dissipation		$P_D$ $t = 10 \text{ s}$ (Note 1)	1.25	W
			0.7	
Channel temperature		$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range		$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

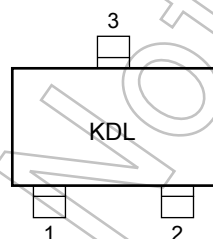
Note 1: Mounted on FR4 board  
(25.4 mm  $\times$  25.4 mm  $\times$  1.6 t, Cu pad: 645 mm<sup>2</sup>)

Note 2: The pulse width limited by maximum channel temperature.

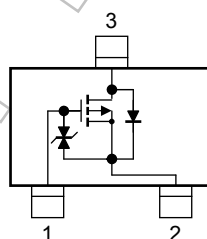


Weight: 10 mg (typ.)

### Marking



### Equivalent Circuit



### Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

The Channel-to-Ambient thermal resistance  $R_{th(ch-a)}$  and the drain power dissipation  $P_D$  vary according to the board material, board area, board thickness and pad area, and are also affected by the environment in which the product is used. When using this device, please take heat dissipation fully into account

Start of commercial production  
2001-07

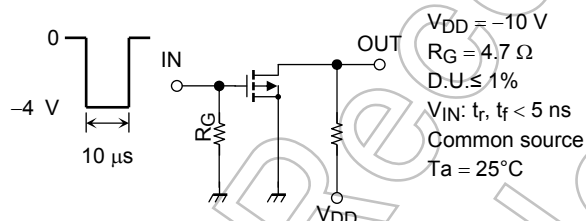
## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$	—	—	$\pm 1$	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR) DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0$	-30	—	—	V
	$V_{(BR) DSX}$	$I_D = -1 \text{ mA}, V_{GS} = 20 \text{ V}$	-15	—	—	V
Drain cut-off current	$I_{DSS}$	$V_{DS} = -30 \text{ V}, V_{GS} = 0$	—	—	-1	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = -5 \text{ V}, I_D = -0.1 \text{ mA}$	-0.8	—	-2.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -5 \text{ V}, I_D = -1.35 \text{ A}$ (Note 3)	2.0	—	—	S
Drain-source on resistance	$R_{DS(ON)}$	$I_D = -1.35 \text{ A}, V_{GS} = -10 \text{ V}$ (Note 3)	—	63	85	$\text{m}\Omega$
		$I_D = -1.35 \text{ A}, V_{GS} = -4.5 \text{ V}$ (Note 3)	—	106	145	
		$I_D = -1.35 \text{ A}, V_{GS} = -4.0 \text{ V}$ (Note 3)	—	120	170	
Input capacitance	$C_{iss}$	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	413	—	pF
Reverse transfer capacitance	$C_{rss}$	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	77	—	pF
Output capacitance	$C_{oss}$	$V_{DS} = -15 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	113	—	pF
Switching time	Turn-on time	$t_{on}$	—	29	—	ns
	Turn-off time	$t_{off}$	—	29	—	

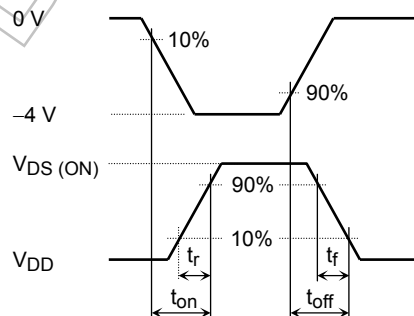
Note 3: Pulse test

## Switching Time Test Circuit

(a) Test circuit



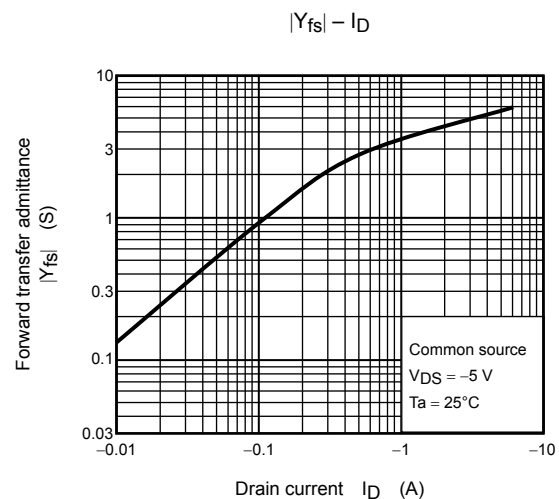
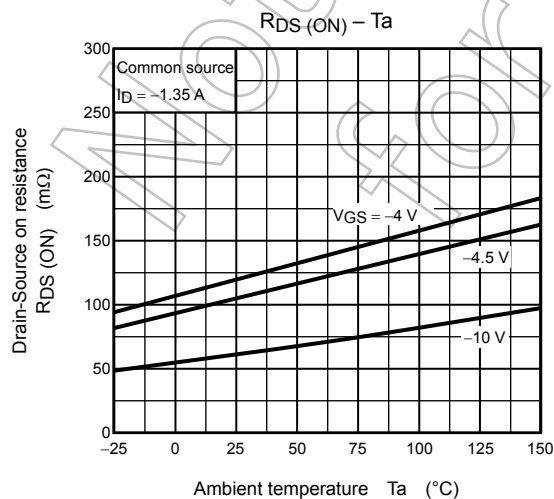
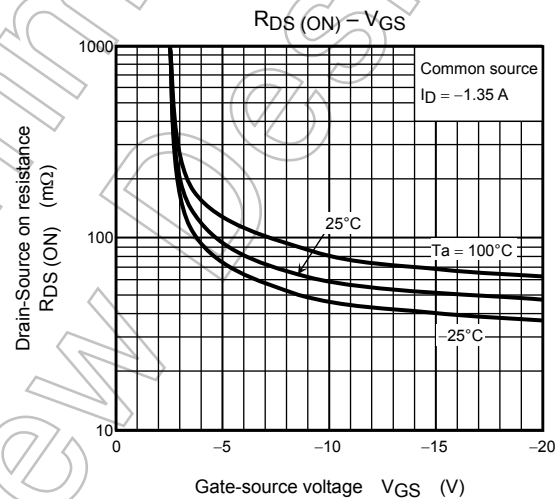
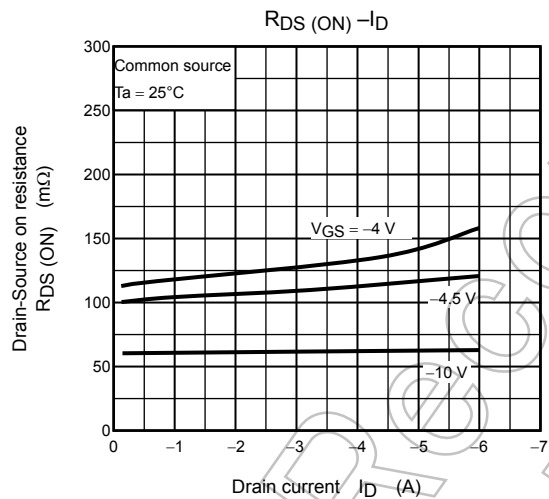
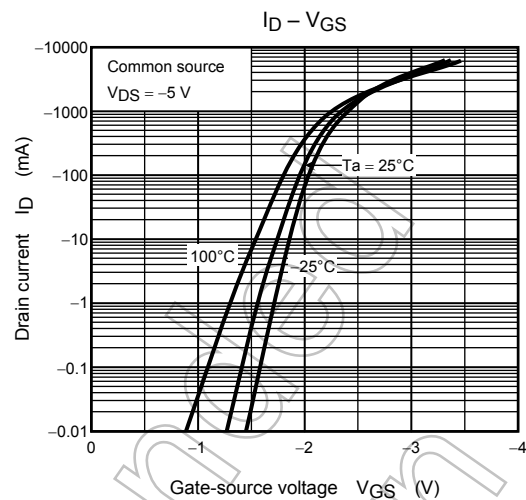
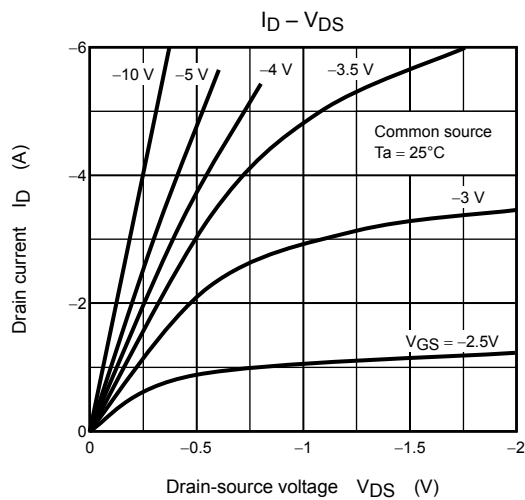
(b)  $V_{IN}$

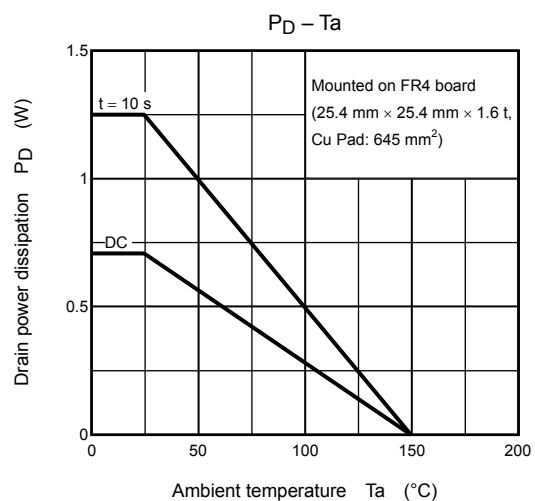
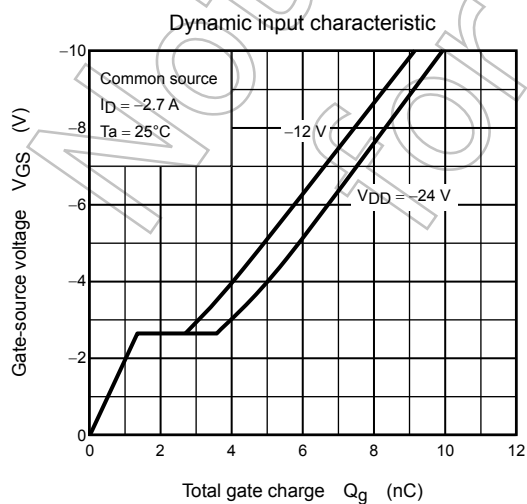
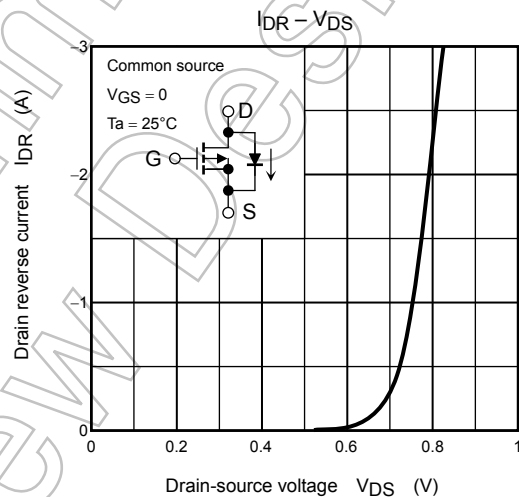
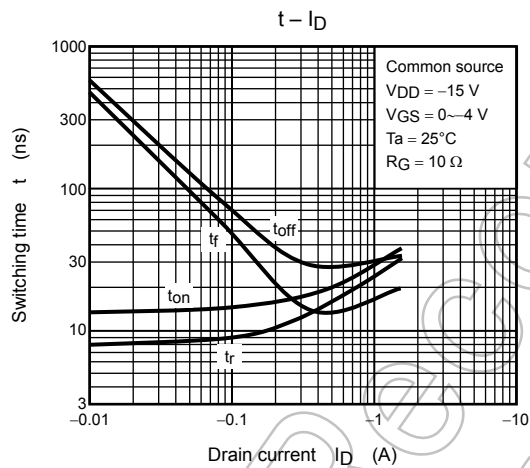
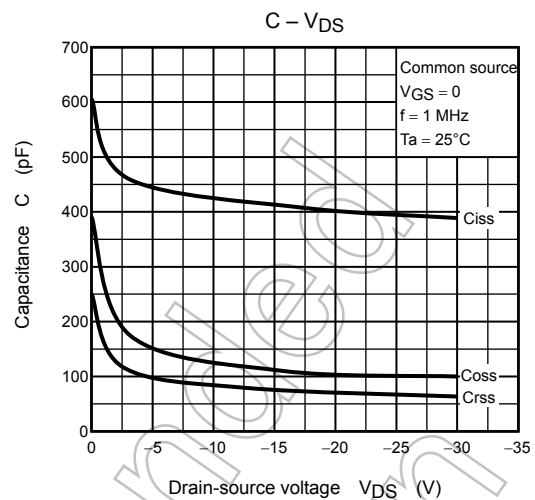
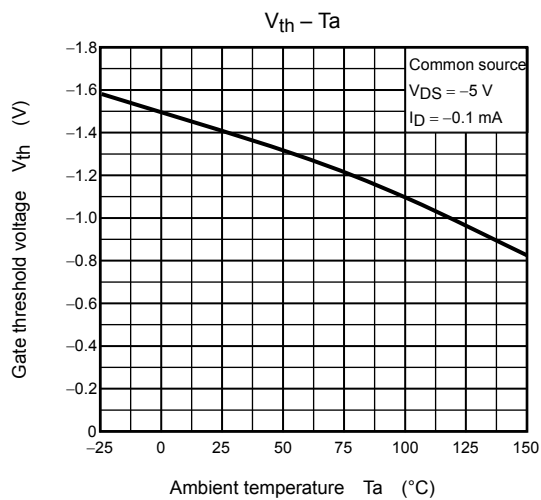


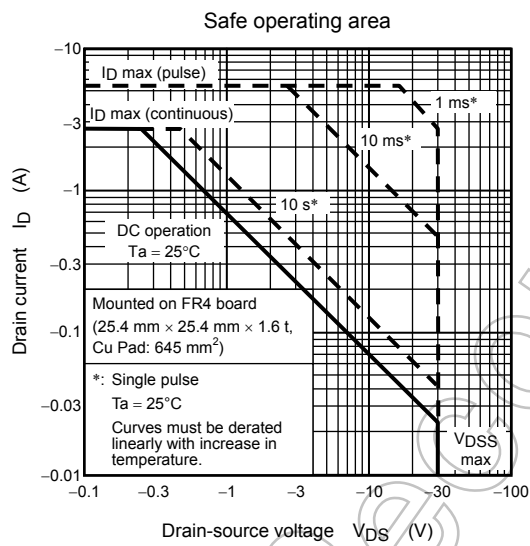
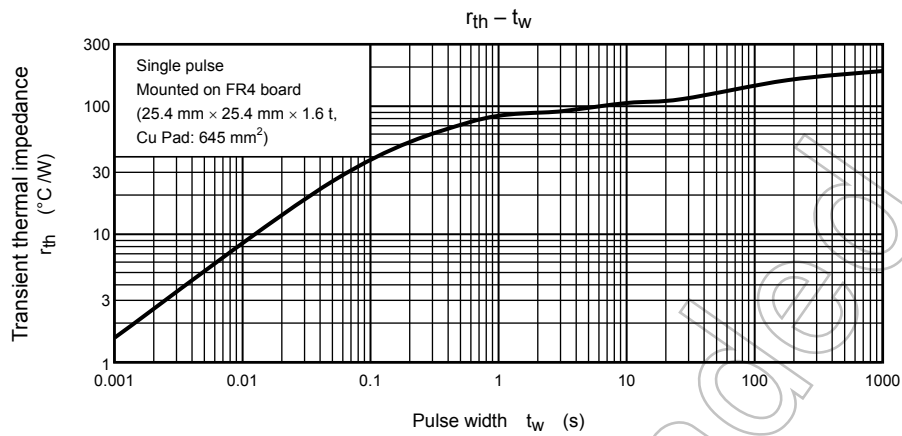
(c)  $V_{OUT}$

## Precaution

$V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D = -100 \mu\text{A}$  for this product. For normal switching operation,  $V_{GS(ON)}$  requires higher voltage than  $V_{th}$  and  $V_{GS(OFF)}$  requires lower voltage than  $V_{th}$ . (relationship can be established as follows:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ ) Please take this into consideration for using the device.







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