MADR-009443

Quad Driver for GaAs FET or PIN Diode Switches and Attenuators

Rev. V5

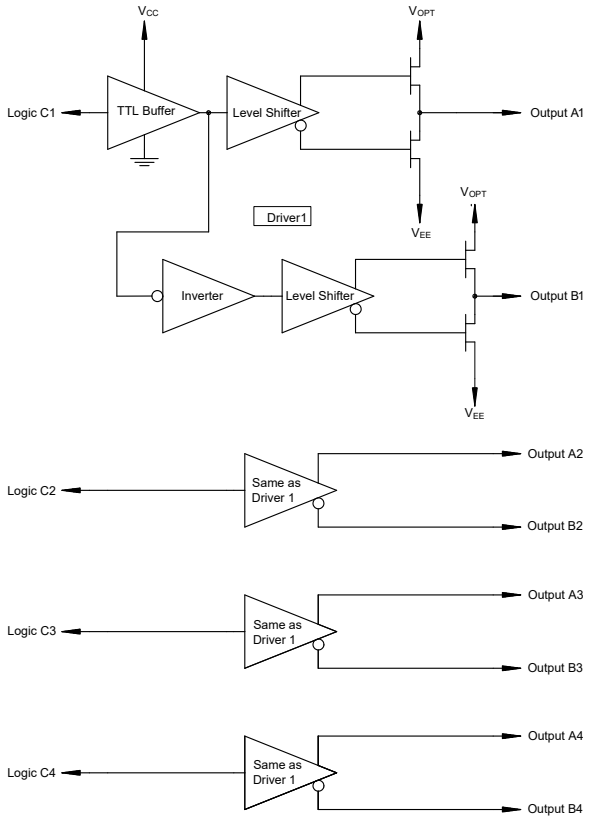
Features

- High Voltage CMOS Technology
- Four Channel
- Positive Voltage Control
- CMOS device using TTL input levels
- Low Power Dissipation
- Low Cost 4 mm, 20-lead PQFN Package
- 100% Matte Tin Plating over Copper
- Halogen-Free “Green” Mold Compound
- RoHS* Compliant

Description

The MADR-009443 is a four channel driver used to translate TTL control inputs into gate control voltages for GaAs FET microwave switches and attenuators. High speed analog CMOS technology is utilized to achieve low power dissipation at moderate to high speeds, encompassing most microwave switching applications. The output HIGH level is optionally 0 to 2 V (relative to GND) to optimize the intermodulation products of FET control devices at low frequencies. For driving PIN diode circuits, the outputs are nominally switched between +5 V & -5 V. The actual driver output voltages will be lower when driving large currents due to the resistance of the output devices.

Functional Schematic



Ordering Information[1]

Part Number	Package
MADR-009443-000100	Bulk Packaging
MADR-009190-000DIE	100 piece waffle pack
MADR-009443-0001TR	1000 piece reel

1. Reference Application Note M513 for reel size information.

Pin Configuration[2]

Pin #	Function	Pin #	Function
1	Ground	11	Output A4
2	N/C	12	Output B4
3	N/C	13	V_{EE}
4	Output A1	14	N/C
5	Output B1	15	V_{CC}
6	Output A2	16	C4
7	Output B2	17	C3
8	NC	18	C2
9	Output A3	19	C1
10	Output B3	20	V_{OPT}

2. The bottom of the die should be isolated or connected to ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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DC Characteristics over Guaranteed Operating Range

Symbol	Parameter	Test Conditions	Units	Min.	Typ.	Max.
V_{IH}	Input High Voltage	Guaranteed High Input Voltage	V	2.0	—	—
V_{IL}	Input Low Voltage	Guaranteed Low Input Voltage	V	—	—	0.8
V_{OH}	Output High Voltage	I_{OH} = -0.5 mA	V	V_{OPT} - 0.1	—	—
V_{OL}	Output Low Voltage	I_{OL} = +0.5 mA	V	—	—	V_{EE} + 0.1
I_{IN}	Input Leakage Current (per input)	V_{IN} = V_{CC} or GND, V_{EE} = min, V_{CC} = max, V_{OPT} = min or max	nA	-250	—	250
I_{OH}	DC Output Current - High (per output)	V_{CC} = +5.0 V, V_{EE} = -5.0 V, V_{OPT} = +5.0 V	mA	-35	—	—
I_{OL}	DC Output Current - Low (per output)	V_{CC} = +5.0 V, V_{EE} = -5.0 V, V_{OPT} = +5.0 V	mA	—	—	35
I_{OH_SPIKE}	Peak Spike Output Current (Rising Edge) (per output)	V_{CC} = +5.0 V, V_{EE} = -5.0 V, V_{OPT} = +5.0 V, C_L = 25 pF	mA	—	35	—
I_{OL_SPIKE}	Peak Spike Output Current (Falling Edge) (per output)	V_{CC} = +5.0 V, V_{EE} = -5.0 V, V_{OPT} = +5.0 V, C_L = 25 pF	mA	—	50	—
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5 V, V_{CC} = +5.5 V, V_{OPT} = +5.5 V, No Output Load	µA	—	—	20
ΔI_{CC}	Additional Supply Current (per TTL input pin)	V_{CC} = max, V_{IN} = V_{CC} -2.1 V	mA	—	—	1.0
I_{EE}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5 V, V_{CC} = +5.5 V, V_{OPT} = +5.5 V, No Output Load	µA	—	—	20
I_{OPT}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5 V, V_{CC} = +5.5 V, V_{OPT} = +5.5 V, No Output Load	µA	—	—	20
R_{NFET}	Output Resistance NFET On (to V_{EE})	V_{CC} = +5.0 V, V_{EE} = -5.0 V, V_{OPT} = +5.0 V, V_{OUT} = -4.9 V +25°C, Note 3	Ω	—	40	—
R_{PFET}	Output Resistance PFET On (to V_{OPT})	V_{CC} = +5.0 V, V_{EE} = -5.0 V, V_{OPT} = +5.0 V, V_{OUT} = +4.9 V +25°C, Note 3	Ω	—	45	—

3. See plot of R_{NFET} and R_{PFET} for variations over temperature for driving 4.99k and 82 Ω resistive load. (Note that this corresponds to 1 mA and 33 mA currents at +25°C). V_{OUT} is approximate for 1 mA load.

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AC Characteristics Over Guaranteed Operating Range[4]

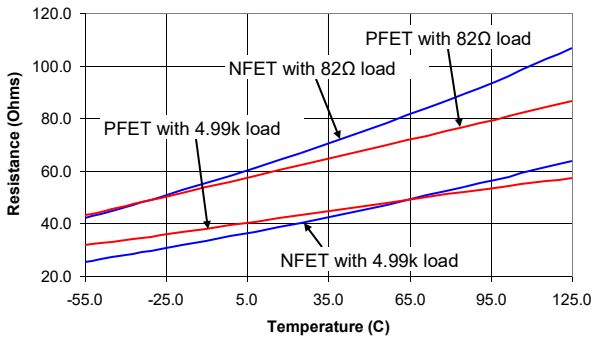
Symbol	Parameter	Unit	Typical performance		
			-40°C	+25°C	+85°C
T_{PLH}	Propagation Delay	ns	20	22	25
T_{PHL}	Propagation Delay	ns	20	22	25
T_{TLH}	Output Transition Time (Rising Edge)	ns	5	6	8
T_{THL}	Output Transition Time (Falling Edge)	ns	5	6	8
T_{skew}	Delay Skew	ns	2	2	2
PRF (max.)	50% Duty Cycle	MHz	DC	—	10
C_{IN}	Input Capacitance	pF	5	5	5
C_{PDC}	Power Dissipation Capacitance[5]	pF	50	50	50
C_{PDE}	Power Dissipation Capacitance[5]	pF	100	100	100

4. VCC = 4.5 V, VOPT = 0 V, VEE = min or max, CL = 25 pF, input LOGIC1 = 3 V, LOGIC0 = 0 V, TRISE, TFALL = 6 ns.
5. Total Power Dissipation is calculated by the following formula: PD = VCC2fC PDC + VEE2fCPDE

Truth Table

Input	Outputs	
Cn	An	Bn
Logic “0”	V_{EE}	V_{OPT}
Logic “1”	V_{OPT}	V_{EE}

Output Resistance vs. Temperature[6]



6. Output resistance were measured under the condition of V_{CC} = +5.0 V, V_{OPT} = +5.0 V, and V_{EE} = -5.0 V, with load resistors from outputs to ground.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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Guaranteed Operating Ranges (for driving FET or PIN devices)[7,8,9]

Symbol	Parameter	Unit	Min.	Typ.	Max.
V_{CC}	Positive DC Supply Voltage	V	4.5	5.0	5.5
V_{EE}	Negative DC Supply Voltage	V	-10.5	-5.0	-4.5
V_{OPT}[10,11]	Optional DC Output Supply Voltage	V	0	—	V_{CC}
V_{OPT} - V_{EE}	Negative Supply Voltage Range	V	4.5	Note 10,11	16.0
V_{CC} - V_{EE}	Positive to negative Supply Range	V	9.0	10.0	16.0
T_{OPER}	Operating Temperature	°C	-40	+25	+85
I_{OH}	DC Output Current - High	mA	-35	—	—
I_{OL}	DC Output Current - Low	mA	—	—	35
T_{RISE}, T_{FALL}	Maximum Input Rise or Fall Time	ns	—	—	500

7. Unused logic inputs must be tied to either GND or V_{CC}.
8. MACOM recommends that V_{CC} be powered on before V_{EE}, and powered off after V_{EE}.
9. 0.01 µF decoupling capacitors are required on the power supply lines.
10. V_{OPT} is grounded in most cases when FETs are driven. To improve the intermodulation performance and the 1 dB compression point of GaAs control devices at low frequencies, V_{OPT} can be increased to between 1 and 2 V. The nonlinear characteristics of the GaAs control devices will approximate performance at 500 MHz. It should be noted that the control current that is on the GaAs MMICs will increase when positive controls are applied.
11. When this driver is used to drive PIN diodes, V_{OPT} is often set to +5 V, with V_{EE} set to -5 V.

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Absolute Maximum Ratings[12]

Symbol	Parameter	Unit	Min.	Max.
V_{CC}	Positive DC Supply Voltage	V	-0.5	7.0
I_{CC}	Positive DC Supply Current ($-0.5\ V \le V_{IN} \le 0.8\ V$; $2.0\ V \le V_{IN} \le V_{CC} + 0.5\ V$; $V_{CC} - V_{IN} \le 7.0\ V$)	mA	—	20
V_{EE}	Negative DC Supply Voltage	V	-11.0	0.5
I_{EE}	Negative DC Supply Current (per Output)[13]	mA	-50	—
V_{OPT}	Optional DC Output Supply Voltage	V	-0.5	V_{CC} +0.5
I_{OPT}	Optional DC Output Supply Current (per Output)[13]	V	—	50
$V_{OPT} - V_{EE}$	Output to Negative Supply Voltage Range	V	-0.5	18.0
$V_{CC} - V_{EE}$	Positive to Negative Supply Voltage Range	V	-0.5	18.0
V_{IN}	DC Input Voltage	V	-0.5 Note 14	V_{CC} +0.5
V_O	DC Output Voltage	V	V_{EE} – 0.5	V_{OPT} + 0.5
P_D[15]	Power Dissipation in Still Air	W	—	1
T_{OPER}	Operating Temperature	°C	-55	125
T_{STG}	Storage Temperature	°C	-65	150
ESD	ESD Sensitivity	kV	2.0	—

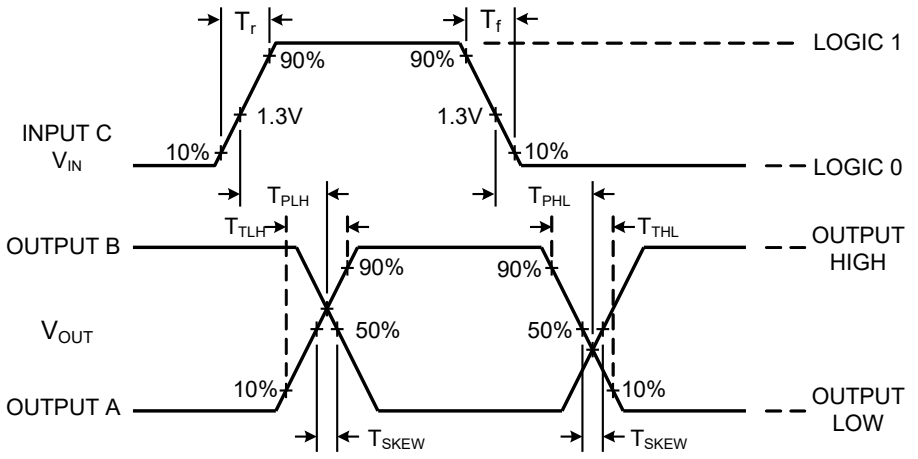
12. All voltages are referenced to GND. All inputs and outputs incorporate latch-up protection structures.
13. The maximum I_{EE} and I_{OPT} are specified under the condition of V_{CC} = +5.5 V, V_{EE} = -5.5 V, V_{OPT} = +5.5 V, and the total power dissipation is within 1 W in still air.
14. If $V_{CC} \ge 6.5$ V, then the minimum for V_{IN} is V_{CC} - 7.0 V.
15. Derate -7 mW/°C from 65°C to 85°C.

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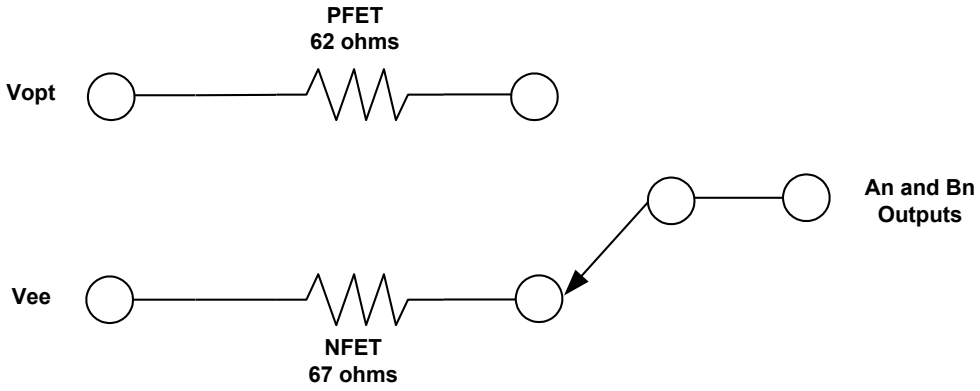
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Switching Waveforms



Equivalent Output Circuit for An and Bn Outputs (33 mA load at 25°C)

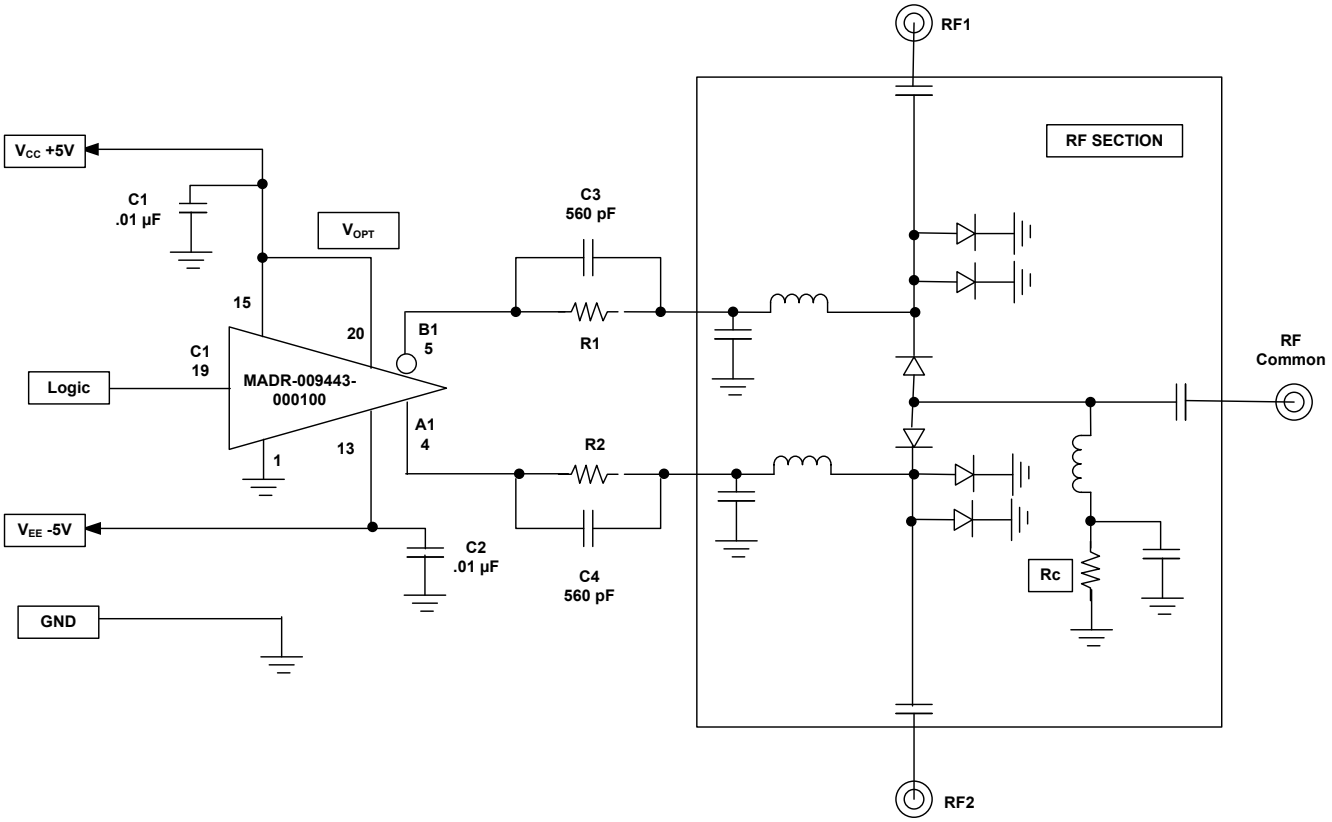


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Typical Application for a SPDT Switch[16]



16. Only one section of MADR-009443 is shown. The other three sections will have equivalent performance.

Description of Circuit

The MADR-009443 provides four pairs of complementary outputs that are each capable of driving a maximum of ±35 mA into a load. In addition, with proper capacitor selection (C3 & C4) used in parallel with the current setting resistor (R1 & R2), additional spiking current can be achieved.

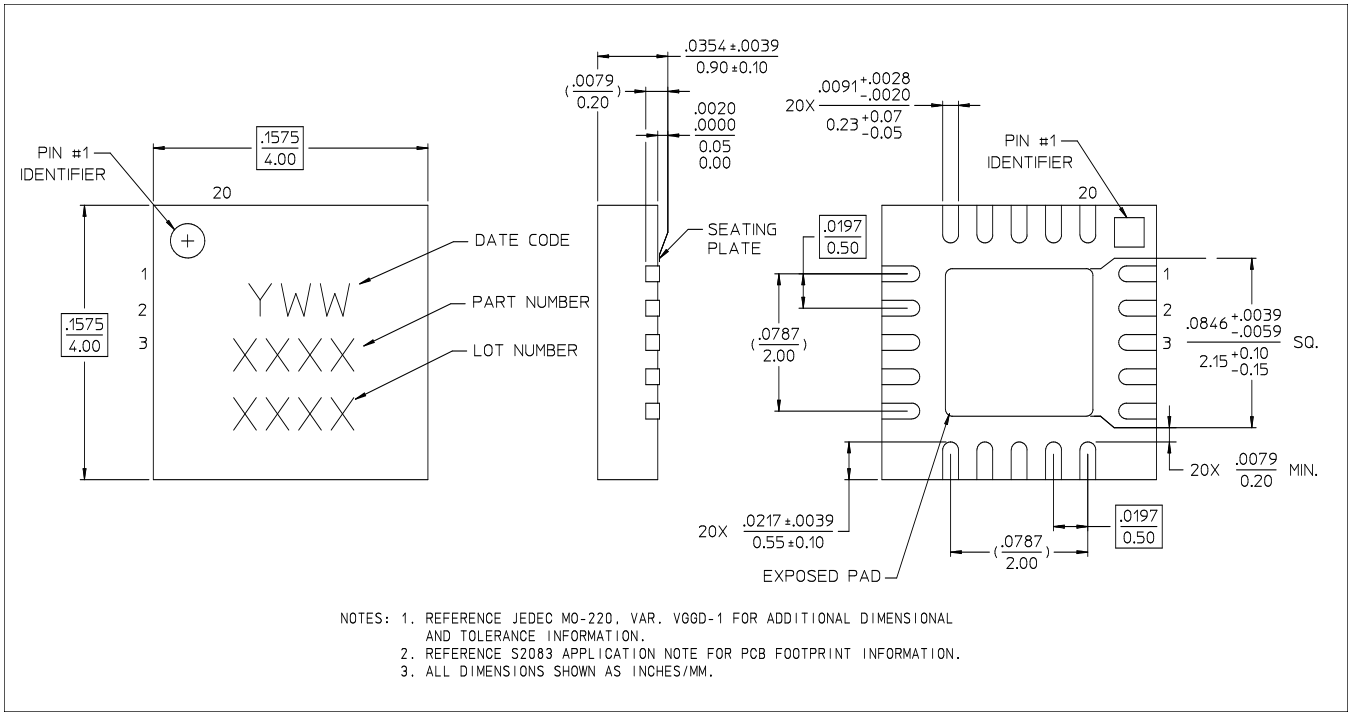
To achieve the Non-Inverting and Inverting complementary voltages, each output is switched between two internal FETs. The FETs are connected to V_{OPT} for the positive output and V_{EE} for the negative output. V_{OPT} and V_{EE} are adjustable for various configurations and have the following limitations: V_{EE} can be no more negative than -10.5 volts; V_{OPT} can be no more positive than +5.5 volts and V_{OPT} must always be less than or equal to V_{CC}. Increasing V_{OPT} beyond V_{CC} will prevent the device from switching states when commanded to by the logic input. The most common configuration is to drive V_{EE} at -5.0 volts with V_{CC} and V_{OPT} tied together at +5.0 volts.

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Lead-Free, 4 mm, 20-lead PQFN†



NOTES: 1. REFERENCE JEDEC MO-220, VAR. VGGD-1 FOR ADDITIONAL DIMENSIONAL AND TOLERANCE INFORMATION.
2. REFERENCE S2083 APPLICATION NOTE FOR PCB FOOTPRINT INFORMATION.
3. ALL DIMENSIONS SHOWN AS INCHES/MM.

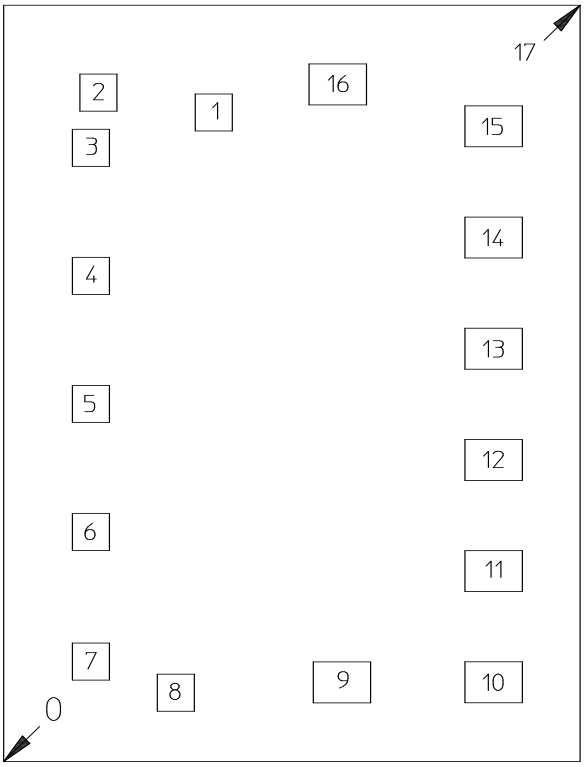
† Reference Application Note M538 for lead-free solder reflow recommendations.
Plating is 100% matte tin over copper.

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Die Outline (*MADR-009190-000DIE*)



Pad Configuration[17,18]

Die Size: 1325 x 1735 µm (nominal)

Pad No.	X (µm) nominal	Y (µm) nominal	Pad Size (µm) X x Y	Pad Function
0	0	0	Lower left edge of die	N/A
1	482.95	1489	85 x 85	Vee
2	217.85	1534.6	85 x 85	Vcc
3	200.45	1407.9	85 x 85	C4
4	200.45	1114.2	85 x 85	C3
5	200.45	820.45	85 x 85	C2
6	200.45	526.8	85 x 85	C1
7	200.45	229.35	85 x 85	Vopt
8	395.6	157.95	85 x 85	GND
9	777.55	181.5	132 x 94	A1
10	1126.35	181.75	132 x 94	B1
11	1126.35	436.85	132 x 94	A2
12	1126.35	691.95	132 x 94	B2
13	1126.35	947.05	132 x 94	A3
14	1126.35	1202.15	132 x 94	B3
15	1126.35	1457.3	132 x 94	A4
16	767.9	1553.5	132 x 94	B4
17	1325	1735	Upper right edge of die	N/A

17. All X,Y dimensions are at bond pad center.
18. Die thickness is 8.0 mils.

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