

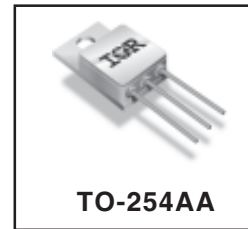
**POWER MOSFET
THRU-HOLE (TO-254AA)**

IRFMG50
1000V, N-CHANNEL
HEXFET[®] MOSFET TECHNOLOGY

Product Summary

| Part Number | R _{DS(on)} | I _D |
|-------------|---------------------|----------------|
| IRFMG50 | 2.0Ω | 5.6A |

HEXFET[®] MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.



TO-254AA

Features:

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets

Absolute Maximum Ratings

| | Parameter | | Units |
|--|---------------------------------|--|-------|
| I _D @ V _{GS} = 10V, T _C = 25°C | Continuous Drain Current | 5.6 | A |
| I _D @ V _{GS} = 10V, T _C = 100°C | Continuous Drain Current | 3.5 | |
| I _{DM} | Pulsed Drain Current ① | 22.4 | |
| P _D @ T _C = 25°C | Max. Power Dissipation | 150 | W |
| | Linear Derating Factor | 1.2 | W/°C |
| V _{GS} | Gate-to-Source Voltage | ±20 | V |
| E _{AS} | Single Pulse Avalanche Energy ② | 860 | mJ |
| I _{AR} | Avalanche Current ① | 5.6 | A |
| E _{AR} | Repetitive Avalanche Energy ① | 15 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 1.0 | V/ns |
| T _J | Operating Junction | -55 to 150 | °C |
| T _{STG} | Storage Temperature Range | | |
| | Lead Temperature | 300(0.063in./1.6mm from case for 10 sec) | |
| | Weight | 9.3 (Typical) | g |

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-------------------------------------|--|------|------|------|-------|---|
| BV _{DSS} | Drain-to-Source Breakdown Voltage | 1000 | — | — | V | V _{GS} = 0V, I _D = 1.0mA |
| ΔBV _{DSS} /ΔT _J | Temperature Coefficient of Breakdown Voltage | — | 1.4 | — | V/°C | Reference to 25°C, I _D = 1.0mA |
| R _{DS(on)} | Static Drain-to-Source On-State Resistance | — | — | 2.0 | Ω | V _{GS} = 10V, I _D = 3.5A ④ |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | — | 4.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| g _{fs} | Forward Transconductance | 5.2 | — | — | S | V _{DS} > 15V, I _{DS} = 3.5A ④ |
| I _{DSS} | Zero Gate Voltage Drain Current | — | — | 25 | μA | V _{DS} = 800V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 800V, V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Leakage Forward | — | — | 100 | nA | V _{GS} = 20V |
| I _{GSS} | Gate-to-Source Leakage Reverse | — | — | -100 | | V _{GS} = -20V |
| Q _g | Total Gate Charge | — | — | 200 | nC | V _{GS} = 10V, I _D = 5.6A V _{DS} = 400V |
| Q _{gs} | Gate-to-Source Charge | — | — | 20 | | |
| Q _{gd} | Gate-to-Drain ('Miller') Charge | — | — | 110 | | |
| t _{d(on)} | Turn-On Delay Time | — | — | 30 | ns | V _{DD} = 400V, I _D = 5.6A, V _{GS} = 10V, R _G = 2.35Ω |
| t _r | Rise Time | — | — | 44 | | |
| t _{d(off)} | Turn-Off Delay Time | — | — | 210 | | |
| t _f | Fall Time | — | — | 60 | | |
| L _S + L _D | Total Inductance | — | 6.8 | — | nH | Measured from Drain lead (6mm/ 0.25in.) to Source lead (6mm /0.25in.) from package |
| C _{iss} | Input Capacitance | — | 2400 | — | pF | V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz |
| C _{oss} | Output Capacitance | — | 240 | — | | |
| C _{rss} | Reverse Transfer Capacitance | — | 80 | — | | |

Source-Drain Diode Ratings and Characteristics

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-----------------|--|--|-----|------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 5.6 | A | T _J = 25°C, I _S = 5.6A, V _{GS} = 0V ④ T _J = 25°C, I _F = 5.6A, di/dt ≤ 100A/μs V _{DD} ≤ 50V ④ |
| I _{SM} | Pulse Source Current (Body Diode) ① | — | — | 22.4 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.8 | V | |
| t _{rr} | Reverse Recovery Time | — | — | 1200 | ns | |
| Q _{RR} | Reverse Recovery Charge | — | — | 8.4 | μC | |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D . | | | | |

Thermal Resistance

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-------------------|---------------------|-----|------|------|-------|----------------------|
| R _{thJC} | Junction-to-Case | — | — | 0.83 | °C/W | |
| R _{thCS} | Case-to-sink | — | 0.21 | — | | |
| R _{thJA} | Junction-to-Ambient | — | — | 48 | | Typical socket mount |

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

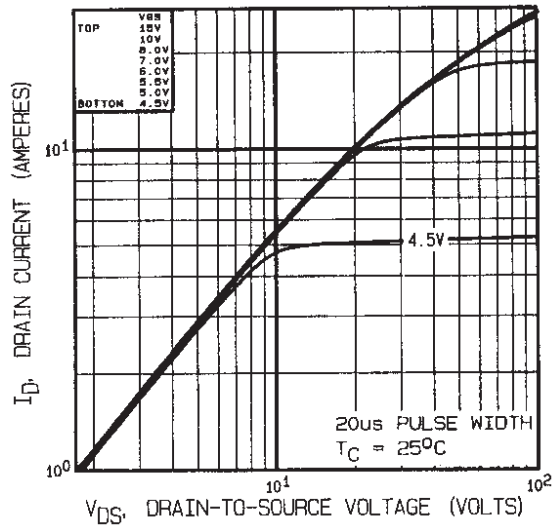


Fig 1. Typical Output Characteristics

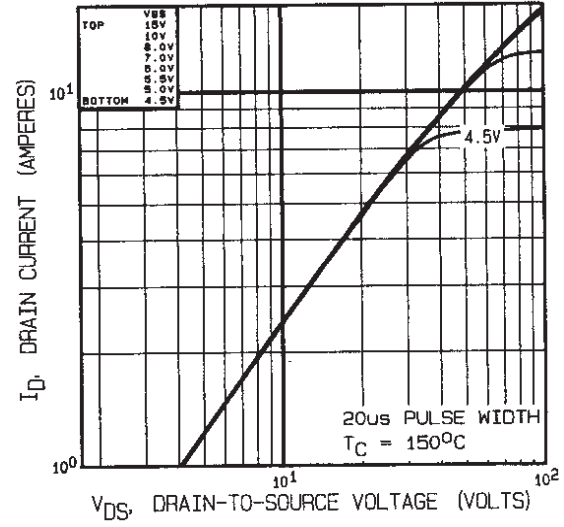


Fig 2. Typical Output Characteristics

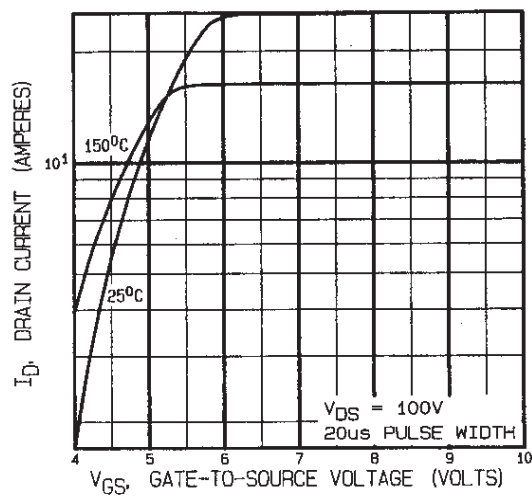


Fig 3. Typical Transfer Characteristics

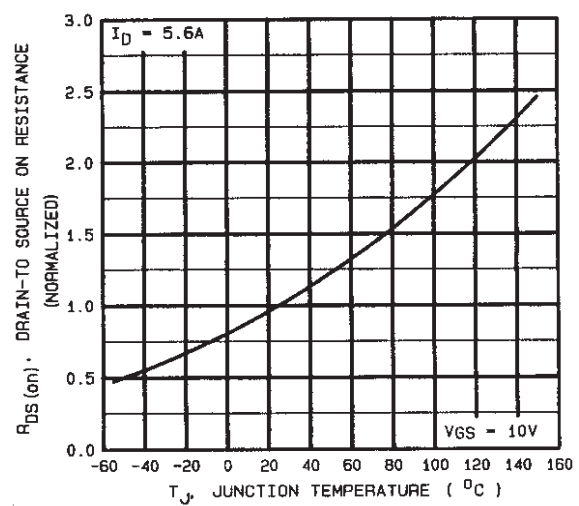


Fig 4. Normalized On-Resistance
Vs. Temperature

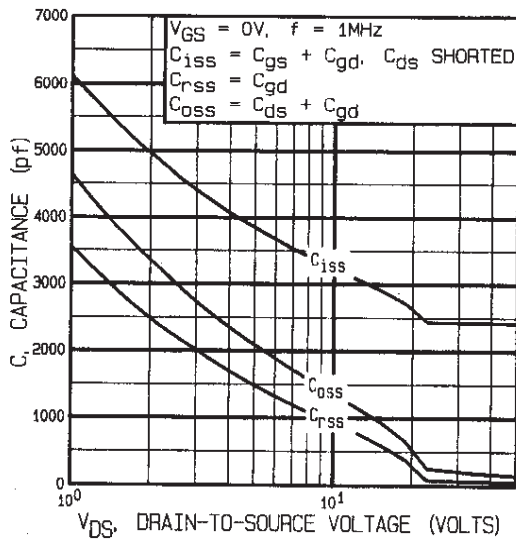


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

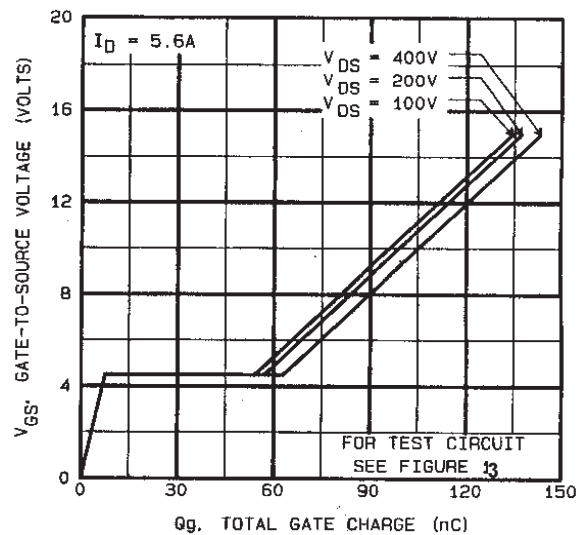


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

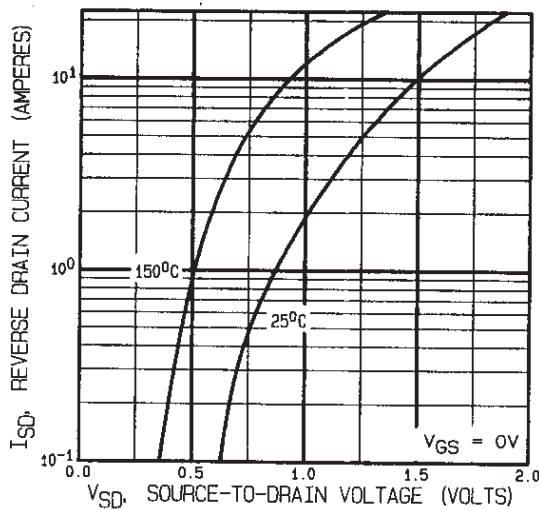


Fig 7. Typical Source-Drain Diode Forward Voltage

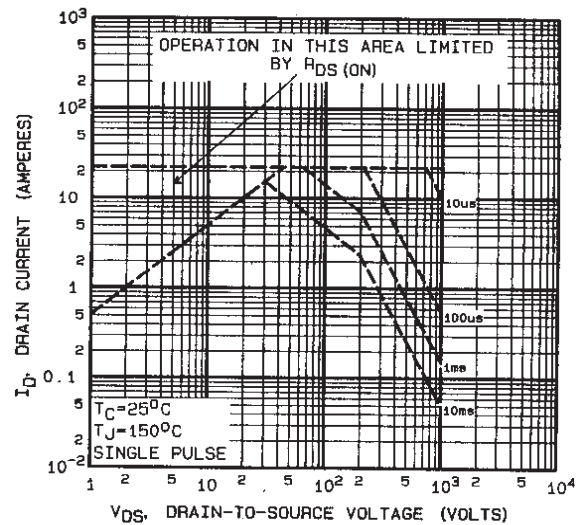


Fig 8. Maximum Safe Operating Area

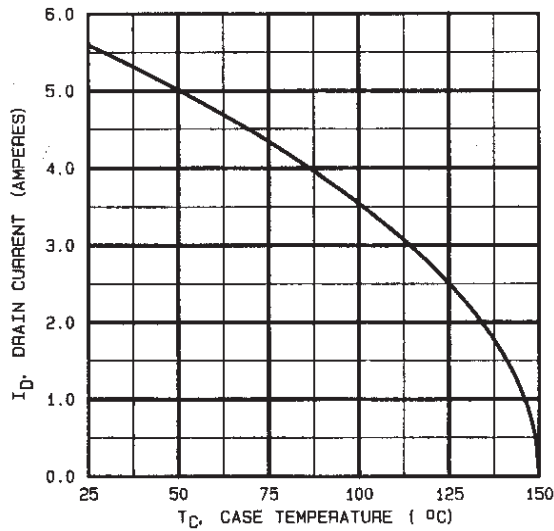


Fig 9. Maximum Drain Current Vs. Case Temperature

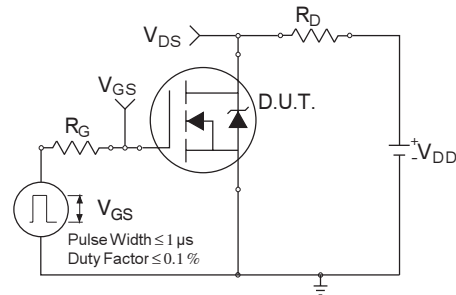


Fig 10a. Switching Time Test Circuit

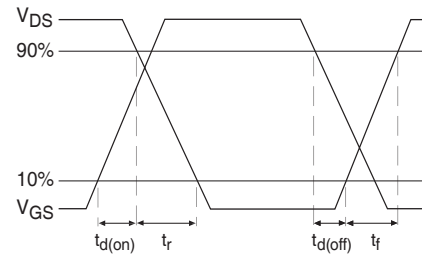


Fig 10b. Switching Time Waveforms

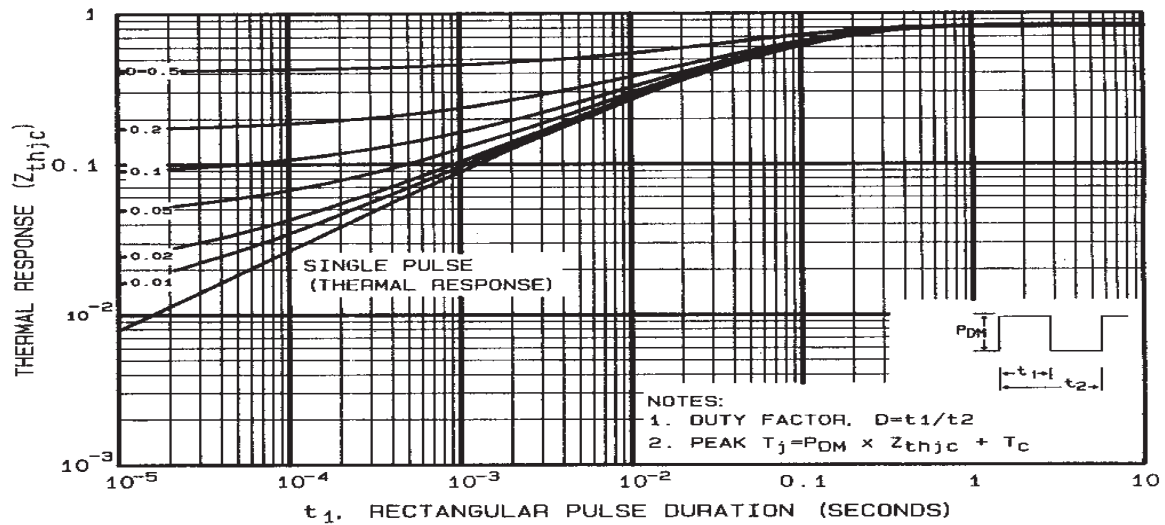


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

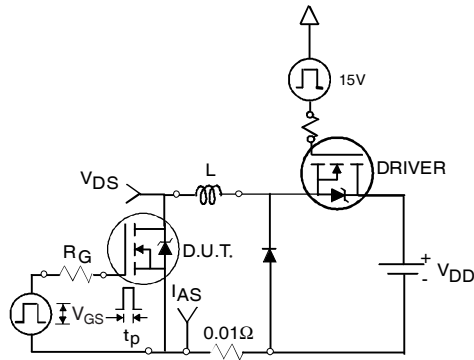


Fig 12a. Unclamped Inductive Test Circuit

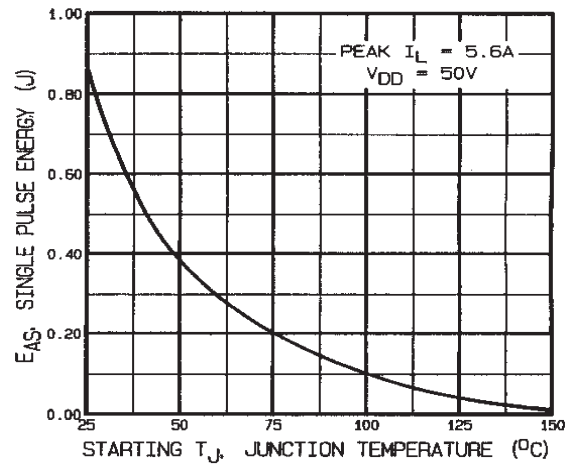
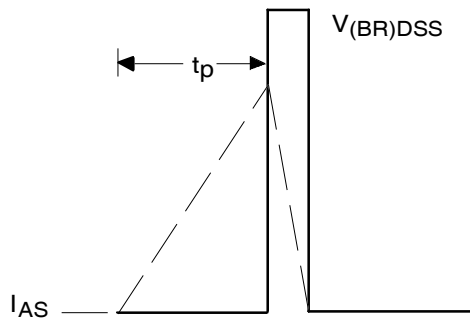
Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

Fig 12b. Unclamped Inductive Waveforms

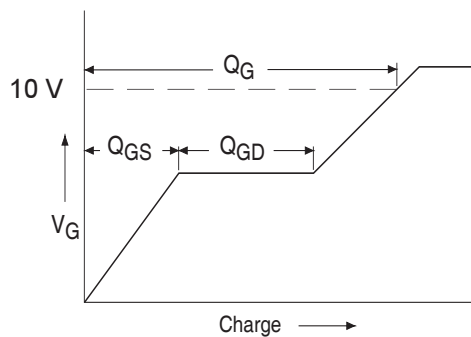


Fig 13a. Basic Gate Charge Waveform

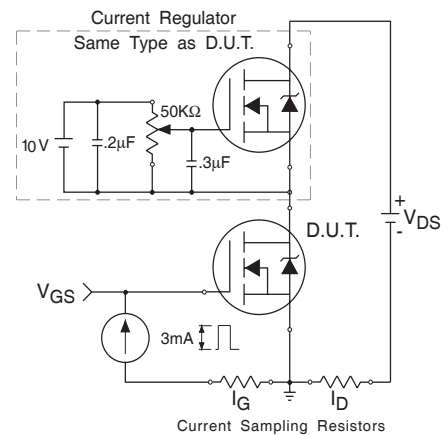
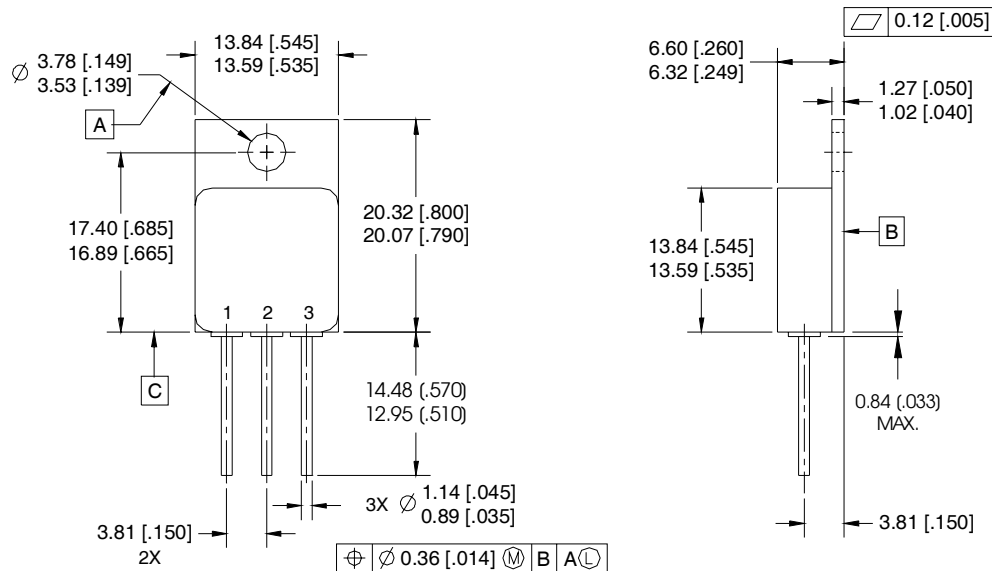


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 54mH$
Peak $I_L = 5.6A$, $V_{GS} = 10V$
- ③ $I_{SD} \leq 5.6A$, $di/dt \leq 120A/\mu s$,
 $V_{DD} \leq 1000V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions —Low-Ohmic TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

CAUTION

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

IR LEOMINSTER : 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776

TAC Fax: (310) 252-7903

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Data and specifications subject to change without notice. 06/2008