Quad Output µModule Regulator with Digital Power System Management

FEATURES

- **Quad Outputs, Dual 12A and Dual 5A, Step-Down µModule® Regulator with Digital Interface**
- **Wide Input Voltage Range: 4.5V to 15V**
- **Dual 12A DC Output from 0.6V to 3.3V**
- **Dual 5A DC Output from 0.6V to 5.5V**
- **±0.5% Total Output Voltage Regulation with Servo**
- **±5% Current Readback Accuracy in 12A Channels**
- 400kHz PMBus-Compliant I^2C Serial Interface
- Integrated 16-Bit ΔΣ ADC
- Accurate Monitoring Input and Four Output Voltages, Currents, and Temperatures
- Digital Programmable Output Voltage Trim, Sequencing and Margining for Each Channel
- Manage Faults and Warnings
- Onboard EEPROM Fault Log Record
- Dual True Differential Sensing Amplifier
- Parallelable Output for Higher Output Current
- Drop-In Pin Compatible with Quad Output LTM4671 Non-PSM µModule Regulator
- 16mm × 16mm × 4.72mm BGA Package

APPLICATIONS

- Telecom, Networking and Industrial Equipment
- Multi-Rail Point of Load Regulation
- FPGAs, DSPs and ASICs Application

DESCRIPTION

The LTM®4673 is a quad output, dual 12A and dual 5A, switching mode DC/DC step-down µModule (powermodule) regulator integrated with 4-channel power system manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry, and create fault logs. Operating over an input voltage range of 4.5V to 15V, the LTM4673 supports an output voltage range of 0.6V to 3.3V for 12A channels and 0.6V to 5.5V for 5A channels. Only bulk input and output capacitors are needed.

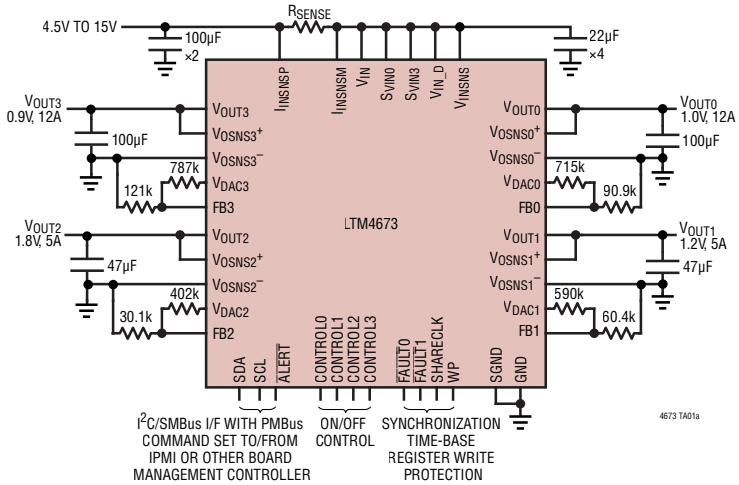
The LTM4673's 2-wire serial interface allows outputs to be precisely margined, tuned and programmable sequenced up and down. An internal 16-bit ADC monitors and supervises input and all four output voltages, currents and temperatures. Faults can be programmed for overcurrent and undercurrent, voltage and temperature threshold limits for four output channels as well as over and undervoltage for the input.

The LTM4673 is offered in a 16mm × 16mm × 4.72mm BGA package with RoHS compliant terminal finish.

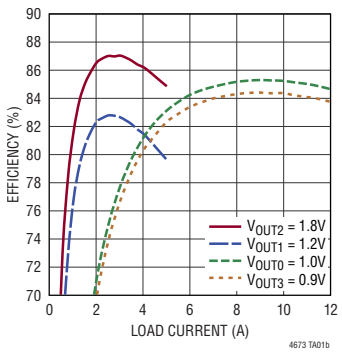
Configurable Output Array

TYPICAL APPLICATION

Dual 12A, Dual 5A Output DC/DC µModule Regulator with Digital Power System Management



Efficiency vs Load Current, 12V Input



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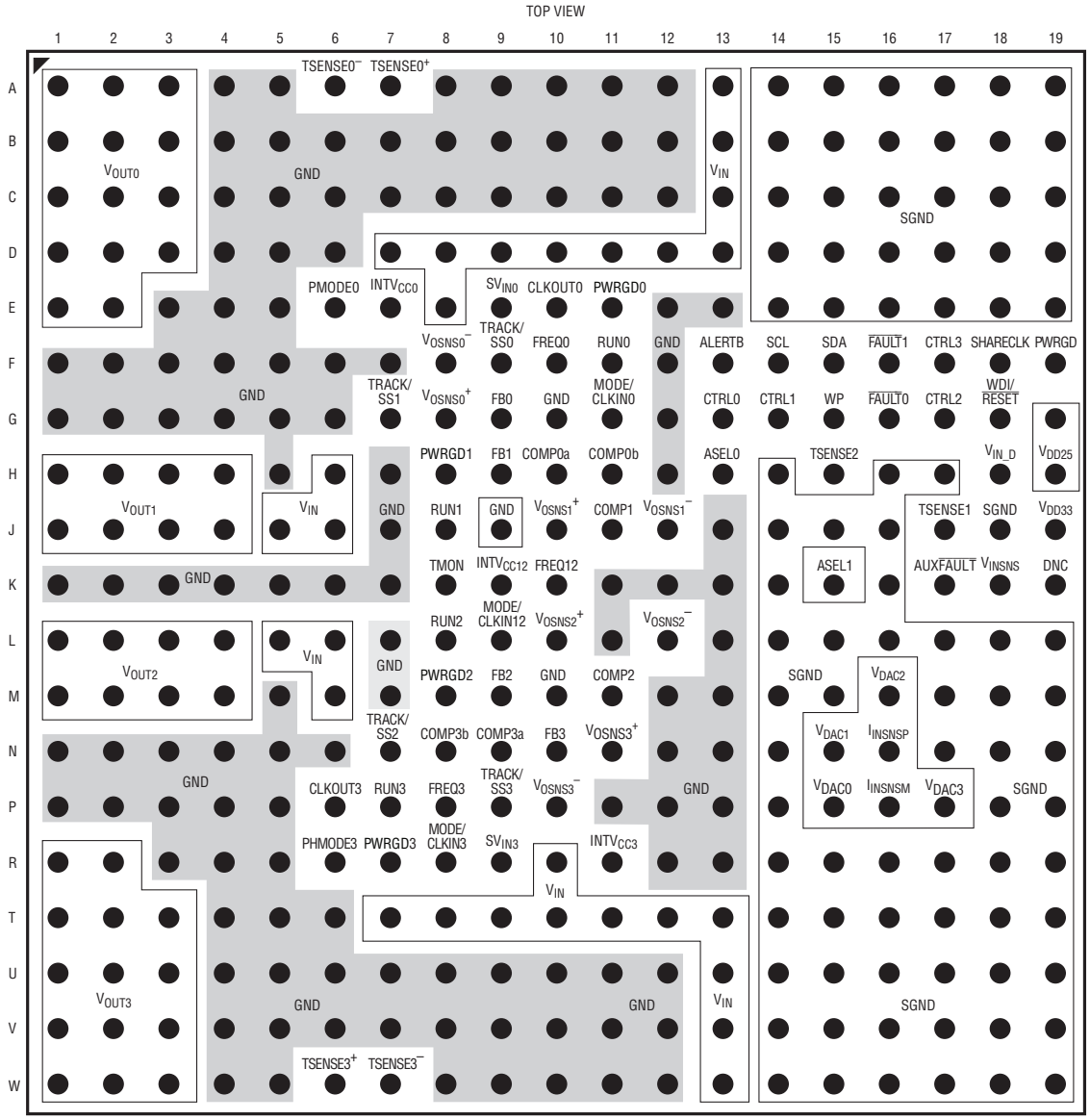
PIN CONFIGURATION



BGA PACKAGE
361-PIN (16mm × 16mm × 4.72mm)
θ_{JCTOP} = 12.3 °C/W, $\theta_{JCBOTTOM}$ =2.2 °C/W, θ_{JA} = 8.2 °C/W (NOTE 18)
WEIGHT = 3.0g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4673EY#PBF	SAC305 (RoHS)	LTM4673Y	e1	BGA	4	–40°C to 125°C
LTM4673IY#PBF	SAC305 (RoHS)	LTM4673Y	e1	BGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. Pad or ball finish code is per IPC/JEDEC J-STD-609.
- This product is not recommended for second side reflow.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), SV_{IN} = V_{IN} = 12V, unless otherwise noted. Per the typical application in Figure 53.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: (12A Channels)							
V_{IN}	Input DC Voltage		●	4.5		15	V
$V_{OUT(RANGE)}$	Output Voltage Range		●	0.6		3.3	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF, CCM, SV_{IN} = V_{IN} = 4.5V to 15V, I_{OUT} = 0A to 12A, V_{OUT} = 1.5V (DAC Disconnect) V_{OUT} = 0.6V to 3.3V, (DAC Soft Connect), (Note 12)	 ●			 1.5 0.5	 % %
$I_{Q(VIN)}$	Input Supply Bias Current	MODE/CLKIN = 3.3V, FCM, V_{OUT} = 1.5V, I_{OUT} = 0A MODE/CLKIN = 0V, DCM, V_{OUT} = 1.5V, I_{OUT} = 0A RUN0-3 = 0V, Shutdown			75 3 250		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{OUT} = 1.5V, I_{OUT} = 12A			1.7		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{OUT} = 1.5V (Note 14)				12	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 4.5V to 15V, I_{OUT} = 0A	●		0.01	0.05	%/V
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 12A (DAC Disconnect)	●		0.2	0.5	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF ×3 Ceramic, V_{OUT} = 1.5V			18		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF ×3 Ceramic, V_{OUT} = 1.5V (Note 12)			5		mV
t_{START}	Turn-On Time	TRACK/SS = 0.1µF, SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V, C_{OUT} = 100µF ×3 Ceramic			1		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 25% to 0% of Full Load, V_{OUT} = 1.5V, C_{OUT} = 100µF ×3 Ceramic (Note 12)			±50		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 25% to 0% of Full Load, V_{OUT} = 1.5V, C_{OUT} = 100µF ×3 Ceramic (Note 12)			30		µs
I_{OUTPK}	Output Current Limit	V_{OUT} = 1.5V		12.5			A
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.594	0.6	0.606	V
I_{FB}	Current at V_{FB} Pin	(Note 16)				±50	nA
$R_{FB(TOP)}$	Resistor Between V_{OUT} and V_{FB} Pins			60.05	60.40	60.75	kΩ
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising Hysteresis		1.10	1.20 150	1.35	V mV
UVLO	Undervoltage Lockout	PWRGD Falling Hysteresis		2.45	2.6 0.4	2.75	V V
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			6		µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 13)			25		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 16)			80		ns
V_{PWRGD}	PWRGD Trip Level	V_{FB} with Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		 –10.5 5	 –8 8	 –5 10.5	 % %
R_{PWRGD}	PWRGD Pull-Down Resistance	1mA Load			8	15	Ω
$INTV_{CC}$	Internal V_{CC} Voltage			3.0	3.3	3.6	V
FREQ	Default Switching Frequency				600		kHz
CLKIN0, CLKIN3	CLKIN Input High Threshold CLKIN Input Low Threshold			1		 0.3	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), SV_{IN} = V_{IN} = 12V, unless otherwise noted. Per the typical application in Figure 53.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: (5A Channels)							
V_{IN}	Input DC Voltage		●	4.5		15	V
$V_{OUT(RANGE)}$	Output Voltage Range		●	0.6		5.5	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF, CCM, SV_{IN} = V_{IN} = 4.5V to 15V, I_{OUT} = 0A to 5A, V_{OUT} = 1.5V (DAC Disconnect) V_{OUT} = 0.6V to 5.5V, (DAC Soft Connect), (Note 12)	 ●			 1.5 0.5	 % %
$I_{Q(VIN)}$	Input Supply Bias Current	MODE/CLKIN = GND, FCM, VOUT = 1.5V, IOUT = 0A MODE/CLKIN = 3.3V, Burst Mode, V_{OUT} = 1.5V, I_{OUT} = 0A			20 4		mA mA
$I_{S(VIN)}$	Input Supply Current	V_{OUT} = 1.5V, I_{OUT} = 5A			0.75		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{OUT} = 1.5V (Note 14)				5	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 4.5V to 15V, I_{OUT} = 0A	●		0.01	0.1	%/V
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 5A (DAC Disconnect)	●		0.2	0.5	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{OUT} = 1.5V			4		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{OUT} = 1.5V (Note 12)			22		mV
t_{START}	Turn-On Time	TRACK/SS = 0.01µF, V_{OUT} = 1.5V, C_{OUT} = 100µF Ceramic			6		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 25% to 0% of Full Load, V_{OUT} = 1.5V, C_{OUT} = 100µF Ceramic (Note 12)			35		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 25% to 0% of Full Load, V_{OUT} = 1.5V, C_{OUT} = 100µF Ceramic (Note 12)			60		µs
I_{OUTPK}	Output Current Limit	V_{OUT} = 1.5V		6			A
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.592	0.6	0.608	V
I_{FB}	Current at V_{FB} Pin	(Note 16)				±30	nA
$R_{FB(TOP)}$	Resistor Between V_{OUT} and V_{FB} Pins			60.05	60.40	60.75	kΩ
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising Hysteresis		1.15	1.25 250	1.35	V mV
UVLO	Undervoltage Lockout	PWRGD Falling Hysteresis		2.25	2.5 0.5	2.7	V V
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			1.5		µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 13)			20		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 16)			45		ns
V_{PWRGD}	PWRGD Trip Level	V_{FB} with Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		 –10.5 5	 –8 8	 –5 10.5	 % %
R_{PWRGD}	PWRGD Pull-Down Resistance	10mA Load			25		Ω
$INTV_{CC}$	Internal V_{CC} Voltage			3.0	3.3	3.6	V
FREQ	Default Switching Frequency				1		MHz
MODE/CLKIN12	MODE/CLKIN12 High Threshold MODE/CLKIN12 Low Threshold			1		 0.3	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN_D} = V_{INSNS} = 12V, V_{DD33}, V_{DD25} pins floating, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Power Supply Characteristics							
V_{IN_D}	V_{IN_D} Supply Input Operating Range	V_{DD33} Floating (Note 17)	●	4.5		15	V
I_{IN_D}	V_{IN_D} Supply Current	V_{DD33} Floating (Note 17)	●		10	13	mA
I_{VDD33}	V_{DD33} Supply Current	3.13V ≤ V_{DD33} ≤ 3.47V, V_{IN_D} = V_{DD33} (Note 17)	●		10	13	mA
V_{UVLO_VDD33}	V_{DD33} Undervoltage Lockout	V_{DD33} Ramping Up, V_{IN_D} = V_{DD33} (Note 17)	●	2.25	2.55	2.8	V
	V_{DD33} Undervoltage Lockout Hysteresis				120		mV
V_{DD33}	Supply Input Operating Range	V_{IN_D} = V_{DD33}	●	3.13		3.47	V
	Regulator Output Voltage	V_{IN_D}= 4.5V	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	V_{IN_D} = 4.5V, V_{DD33} = 0V	●	50	90	140	mA
V_{DD25}	Regulator Output Voltage	V_{IN_D} = 3.47V	●	2.35	2.5	2.65	V
	Regulator Output Short-Circuit Current	V_{IN_D} = 3.47V, V_{DD25} = 0V	●	30	55	80	mA
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts (Note 17)			30		ms
DAC Output Characteristics (Note 17)							
N_V_{DAC}	Resolution				10		Bits
V_{FS_VDAC}	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF, DAC Polarity = 1	Buffer Gain Setting_0 Buffer Gain Setting_1		1.38 2.65		V V
INL_V_{DAC}	Integral Nonlinearity	(Note 5)				±2	LSB
DNL_V_{DAC}	Differential Nonlinearity	(Note 5)				±2.4	LSB
V_{OS_VDAC}	Offset Voltage	(Note 5)				±15	mV
V_{DAC}	Load Regulation	V_{DACn} = 2.65V, I_{VDACn} Sourcing = 2mA			100		ppm/mA
		V_{DACn} = 0.1V, I_{VDACn} Sinking = 2mA			100		ppm/mA
	PSRR	DC: 3.13V ≤ V_{DD33} ≤ 3.47V, V_{IN_D} = V_{DD33}			60		dB
	Leakage Current	V_{DACn} Hi-Z, 0V ≤ V_{DACn} ≤ 6V				±100	nA
	Short-Circuit Current Low	V_{DACn} Shorted to GND			–6		mA
	Short-Circuit Current High	V_{DACn} Shorted to V_{DD33}			6		mA
C_{OUT}	Output Capacitance	V_{DACn} Hi-Z			10		pF
t_{S_VDAC}	DAC Output Update Rate	Fast Servo Mode			250		µs
Voltage Supervisor Characteristics (Note 17)							
V_{VS}	Voltage Range (Programmable)	Low Resolution Mode High Resolution Mode		0 0		6 3.8	V V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode			4		mV/LSB
		0V to 6V Range: Low Resolution Mode			8		mV/LSB
TUE_VS	Total Unadjusted Error	2V ≤ V_{VS} ≤ 6V, Low Resolution Mode				±1.25	% of Reading
		1.5V < V_{VS} ≤ 3.8V, High Resolution Mode				±1.0	% of Reading
		0.8V ≤ V_{VS} ≤ 1.5V, High Resolution Mode				±1.5	% of Reading
t_{S_VS}	Update Period				12.21		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN_D} = V_{INSNS} = 12V, V_{DD33}, V_{DD25} pins floating, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Supervisor Characteristics (Note 17)							
V_{IN_CS}	Current Sense Range (Note 17)	Differential Voltage		–170		170	mV
N_CS	Current Sense Resolution (Note 3)	IOUT_OC_FAULT_LIMIT • IOUT_CAL_GAIN, IOUT_UC_FAULT_LIMIT • IOUT_CAL_GAIN			400		µV/LSB
TUE_CS	Total Unadjusted Error	50mV ≤ |V_{CS}| ≤ 170mV				±3	% of Reading
		|V_{CS}| < 50mV				±1.5	mV
V_{OS_CS}	Offset Error	V_{CS} = 0				±600	µV
t_{S_CS}	Update Period				12.21		µs
$I_{O\text{-}RB\text{-}ACC}$	Output Current, Readback Accuracy	READ_IOUT*n*, Channels 0 and 3, V_{IN} = 12V, V_{OUTn} = 1.0V, 0 ≤ I_{OUTn} ≤ 12A (Note 15)	●		±0.36A of Reading		A
		READ_IOUT*n*, Channels 1 and 2, V_{IN} = 12V, V_{OUTn} = 1.0V, 0 ≤ I_{OUTn} ≤ 3A (Note 15)			±0.5A of Reading		A
V_{INSNS} Input Characteristics (Note 17)							
V_{INSNS}	V_{INSNS} Input Voltage Range	(Note 10)		0		15	V
I_{VINSNS}	V_{INSNS} Input Current	V_{VINSNS} = 4.5V			140		µA
		V_{VINSNS} = 12V			250		µA
		V_{VINSNS} = 15V			300		µA
TUE_{VINSNS_T}	VIN_ON, VIN_OFF Threshold Total Unadjusted Error	4.5V ≤ V_{VINSNS} ≤ 8V				±2.0	% of Reading
		V_{VINSNS} > 8V				±1.0	% of Reading
TUE_VIN	READ_VIN Total Unadjusted Error	4.5V ≤ V_{VINSNS} ≤ 15V				±0.5	% of Reading
DAC Soft-Connect Comparator Characteristics (Note 17)							
V_{OS_CMP}	Offset Voltage	V_{DACn} = 0.2V			±1	±18	mV
		V_{DACn} = 1.3V			±2	±26	mV
		V_{DACn} = 2.65V			±3	±52	mV
Input Current Sense Characteristics (Note 17)							
V_{IIN}	Common Mode Input Range	$V_{IINSNSP}$ = $V_{IINSNSM}$ (Note 10)		4.5		15	V
I_{IIN}	$I_{IINSNSP}$, $I_{IINSNSM}$ Input Current	$V_{IINSNSP}$ = $V_{IINSNSM}$ = V_{IINSNS}			0.5	2	µA
FS_IIN	Full-Scale Input Current Sense Voltage Range	Referred to ($V_{IINSNSP}$ – $V_{IINSNSM}$) High Range Medium Range Low Range		–100 –50 –20		100 50 20	mV mV mV
TUE_IIN	Total Unadjusted Error	|$V_{IINSNSP}$ – $V_{IINSNSM}$| = 100mV, High Range |$V_{IINSNSP}$ – $V_{IINSNSM}$| = 50mV, Medium Range |$V_{IINSNSP}$ – $V_{IINSNSM}$| = 20mV, Low Range				±0.6 ±0.65 ±0.75	% of Reading % of Reading % of Reading
		|$V_{IINSNSP}$ – $V_{IINSNSM}$| = 20mV, High Range |$V_{IINSNSP}$ – $V_{IINSNSM}$| = 15mV, Medium Range |$V_{IINSNSP}$ – $V_{IINSNSM}$| = 10mV, Low Range				±1 ±1 ±1	% of Reading % of Reading % of Reading
		|$V_{IINSNSP}$ – $V_{IINSNSM}$| = 0mV, High Range |$V_{IINSNSP}$ – $V_{IINSNSM}$| = 0mV, Medium Range |$V_{IINSNSP}$ – $V_{IINSNSM}$| = 0mV, Low Range				±100 ±75 ±50	µV µV µV
CMRR_IIN	DC CMRR	4.5V ≤ $V_{IINSNSP}$ = V_{IINSNS} ≤ 15V, |$V_{IINSNSP}$ – $V_{IINSNSM}$| = 100mV, High Range		85			dB
	AC CMRR	$V_{IINSNSP}$ = V_{IINSNS}= 12V ± 100mV, f = 62.5kHz			85		dB
t_{CONV_IIN}	Conversion Time (Note 4)				25		ms
t_{UPDATE}	Update Rate (Note 4)				5.4		Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN_D} = 12V, V_{DD33}, V_{DD25} pins floating, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Stage Temperature Sensor Characteristics (READ_TEMPERATURE_1) (Note 17)							
t_{CONV_TSENSE}	Conversion Time	For One Channel, (Total Latency for All Channels Is 4 • 66ms)			66		ms
I_{TSENSE_HI}	T_{SENSE} High Level Current				–64		µA
I_{TSENSE_LOW}	T_{SENSE} Low Level Current				–4		µA
TUE_TS	Total Unadjusted Error (Note 15)	Ideal Diode Assumed (12A Channels)			±3		°C
		Ideal Diode Assume (5A Channels); –40°C to 0°C			±14		°C
		Ideal Diode Assume (5A Channels); 0°C to 125°C			±5		°C
N_TS	Maximum Ideality Factor	READ_TEMPERATURE_1 = 175°C MFR_TEMP_1_GAIN = 1/N_TS				1.10	°C
IC Temperature Sensor Characteristics (READ_TEMPERATURE_2) (Note 17)							
TUE_TS2	Total Unadjusted Error				±1		°C
General Purpose Output (AUX$\overline{FAULT}$) Characteristics (Note 17)							
$V_{AUX\overline{FAULT}}$	Output High Voltage	$I_{AUX\overline{FAULT}}$ = –5µA, V_{DD33} = 3.13V			13		V
$I_{AUX\overline{FAULT}}$	Output Sourcing Current	AUX$\overline{FAULT}$ Pull-Up Enabled, $V_{AUX\overline{FAULT}}$ = 1V			–7		µA
	Output Sinking Current	Strong Pull-Down Enabled, $V_{AUX\overline{FAULT}}$ = 0.4V			5		mA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ $V_{AUX\overline{FAULT}}$ ≤ 15V				±1	µA
Energy Meter Characteristics (Note 17)							
TUE_ETB	Energy Meter Time-Base Error					±1.5	% of Reading
TUE_PIN	READ_PIN Total Unadjusted Error	$V_{IINSNSP}$ – $V_{IINSNSM}$ = 50mV, Medium Range				±1	% of Reading
TUE_EIN	Energy Meter Total Unadjusted Error	$V_{IINSNSP}$ – $V_{IINSNSM}$ = 50mV, Medium Range				±2.5	% of Reading
EEPROM Characteristics							
Endurance	(Notes 6, 9)	0°C < T_J < 85°C During EEPROM Write Operations		10,000			Cycles
Retention	(Notes 6, 9)	T_J < 125°C		10			Years
t_{MASS_WRITE}	Mass Write Operation Time (Note 7)	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operations			440	4100	ms
Digital Inputs SCL, SDA, CONTROL0, CONTROL1, CONTROL2, CONTROL3, WDI/$\overline{RESET}$, $\overline{FAULT0}$, $\overline{FAULT1}$, WP (Note 17)							
V_{IH}	High Level Input Voltage	$\overline{FAULT0}$, $\overline{FAULT1}$, SDA, SCL, WDI/$\overline{RESET}$, WP		2.1			V
		CONTROL*n* Only		1.85			V
V_{IL}	Low Level Input Voltage	$\overline{FAULT0}$, $\overline{FAULT1}$, SDA, SCL, WDI/$\overline{RESET}$, WP				1.5	V
		CONTROL*n* Only				1.6	V
V_{HYST}	Input Hysteresis				20		mV
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V				±2	µA
t_{SP}	Pulse Width of Spike Suppressed	$\overline{FAULT0}$, $\overline{FAULT1}$, CONTROL*n*			10		µs
		SDA, SCL			98		ns
t_{FAULT_MIN}	Minimum Low Pulse Width for Externally Generated Faults			180			ms
$t_{\overline{RESET}}$	Pulse Width to Assert Reset	$V_{WDI/\overline{RESET}}$ ≤ 1.5V		300			µs
t_{WDI}	Pulse Width to Reset Watchdog Timer	$V_{WDI/\overline{RESET}}$ ≤ 1.5V		0.3		200	µs
f_{WDI}	Watchdog Timer Interrupt Input Frequency					1	MHz
C_{IN}	Input Capacitance				10		pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN_D} = 12V, V_{DD33}, V_{DD25} pins floating, unless otherwise indicated.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input SHARECLK (Note 17)						
V_{IH}	High Level Input Voltage		1.6			V
V_{IL}	Low Level Input Voltage				0.8	V
$f_{SHARECLK\_IN}$	Input Frequency Operating Range		90		110	kHz
t_{LOW}	Assertion Low Time	$V_{SHARECLK}$ < 0.8V	0.825		1.11	µs
t_{RISE}	Rise Time	$V_{SHARECLK}$ < 0.8V to $V_{SHARECLK}$ > 1.6V			450	ns
I_{LEAK}	Input Leakage Current	0V ≤ $V_{SHARECLK}$ ≤ V_{DD33} + 0.3V			±1	µA
C_{IN}	Input Capacitance			10		pF
Digital Outputs SDA, $\overline{ALERT}$, SHARECLK, $\overline{FAULT0}$, $\overline{FAULT1}$, PWRGD (Note 17)						
V_{OL}	Digital Output Low Voltage	I_{SINK} = 3mA			0.4	V
$f_{SHARECLK\_OUT}$	Output Frequency Operating Range	5.49k Pull-Up to V_{DD33}	90	100	110	kHz
Digital Inputs ASEL0,ASEL1 (Note 17)						
V_{IH}	Input High Threshold Voltage		V_{DD33} – 0.5			V
V_{IL}	Input Low Threshold Voltage				0.5	V
$I_{IH,IL}$	High, Low Input Current	ASEL[1:0] = 0, V_{DD33}			±95	µA
I_{HIZ}	Hi-Z Input Current				±24	µA
C_{IN}	Input Capacitance			10		pF
Serial Bus Timing Characteristics (Note 17)						
f_{SCL}	Serial Clock Frequency (Note 8)		10		400	kHz
t_{LOW}	Serial Clock Low Period (Note 8)		1.3			µs
t_{HIGH}	Serial Clock High Period (Note 8)		0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start (Note 8)		1.3			µs
$t_{HD,STA}$	Start Condition Hold Time (Note 8)		600			ns
$t_{SU,STA}$	Start Condition Setup Time (Note 8)		600			ns
$t_{SU,STO}$	Stop Condition Setup Time (Note 8)		600			ns
$t_{HD,DAT}$	Data Hold Time (LTM4673 Receiving Data) (Note 8)		0			ns
	Data Hold Time (LTM4673 Transmitting Data) (Note 8)		300		900	ns
$t_{SU,DAT}$	Data Setup Time (Note 8)		100			ns
t_{SP}	Pulse Width of Spike Suppressed (Note 8)			98		ns
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Mfr_config_all_longer_pmbus_timeout = 0 Mfr_config_all_longer_pmbus_timeout = 1		25 200	35 280	ms ms
Additional Digital Timing Characteristics						
t_{OFF_MIN}	Minimum Off-Time for Any Channel	(Note 17)		100		ms

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4673 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4673E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4673I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The current sense resolution is determined by the L11 format and the mV units of the returned value. For example, a full-scale value of 170mV returns a L11 value of 0xF2A8 = 680 • 2^{-2} = 170. This is the lowest range that can represent this value without overflowing the L11 mantissa and the resolution for 1LSB in this range is 2^{-2}mA = 250µA. Each successively lower range improves resolution by cutting the LSB size in half.

Note 4: The nominal time between successive ADC conversions (latency of the ADC) for any given channel is t_{UPDATE_ADC}.

Note 5: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

Note 6: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 7: The LTM4673 will not acknowledge any PMBus commands, except for MFR_COMMON, when a STORE_USER_ALL command is being executed. See also OPERATION section.

Note 8: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are: (20 + 0.1 • C_B) (ns) < t_r < 300ns and (20 + 0.1 • C_B) (ns) < t_f < 300ns. C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is 3.13V < V_{IO} < 3.6V.

Note 9: EEPROM endurance and retention will be degraded when T_J > 125°C.

Note 10: While READ_VIN operates with 0V ≤ V_{INSNS} ≤ 15V, the valid READ_IIN, READ_PIN, and MFR_EIN operating range is 4.5V ≤ V_{INSNS} ≤ 15V.

Note 11: V_{SENSE} and I_{SENSE} input currents are characterized by input current and input differential current. Input current is defined as current into a single device pin (see Note 2). Input differential current is defined as ($I^+ – I^–$) where I^+ is the current into the positive device pin and $I^–$ is the current into the negative device pin.

Note 12: Tested on bench at nominal conditions.

Note 13: The minimum on-time is tested at wafer sort.

Note 14: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

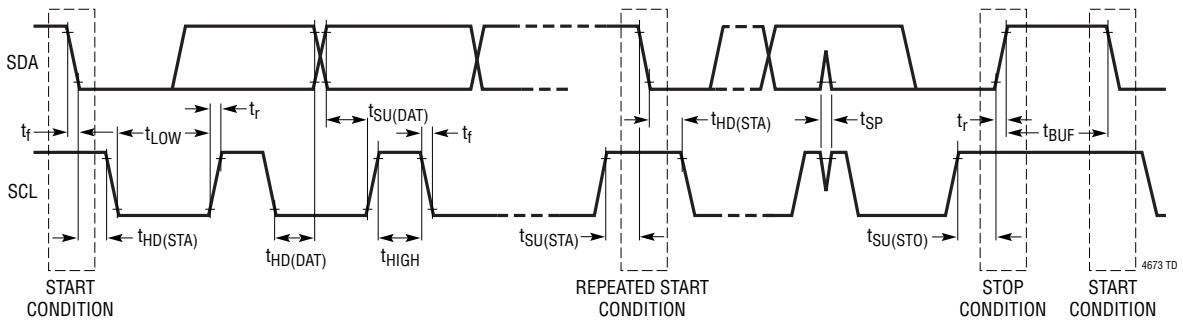
Note 15: Guaranteed by design.

Note 16: 100% tested at wafer level.

Note 17: Tested at IC level-ATE.

Note 18: θ values are determined by simulation per JESD51 conditions. θ_{JA} value is obtained with demo board.

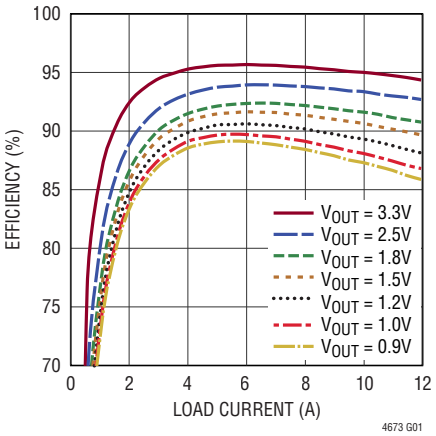
PMBus TIMING DIAGRAM



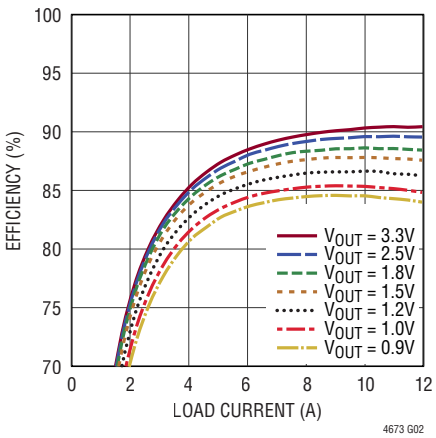
TYPICAL PERFORMANCE CHARACTERISTICS

Dual 12A Channels

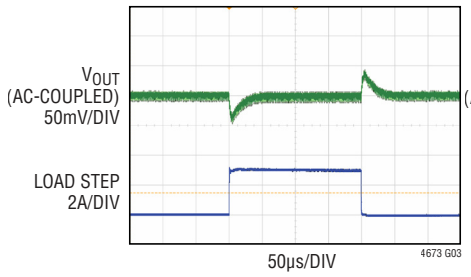
Efficiency vs Load Current from $5V_{IN}$



Efficiency vs Load Current from $12V_{IN}$

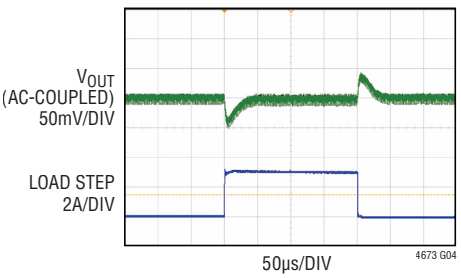


1.0V Output Transient Response



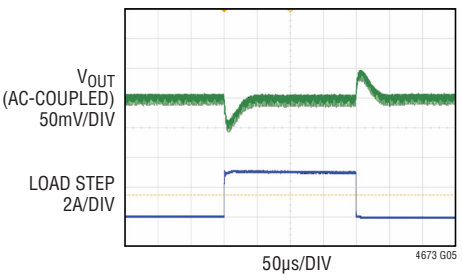
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 600kHz
C_{OUT} = 100µF ×3 CERAMIC CAPACITORS
EXT COMP: R_{TH} = 5k, C_{TH} = 2200pF, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

1.2V Output Transient Response



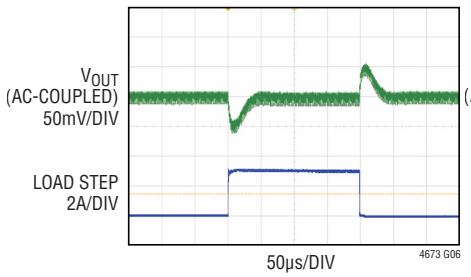
V_{IN} = 12V
V_{OUT} = 1.2V
FREQUENCY = 600kHz
C_{OUT} = 100µF ×3 CERAMIC CAPACITORS
EXT COMP: R_{TH} = 5k, C_{TH} = 2200pF, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

1.5V Output Transient Response



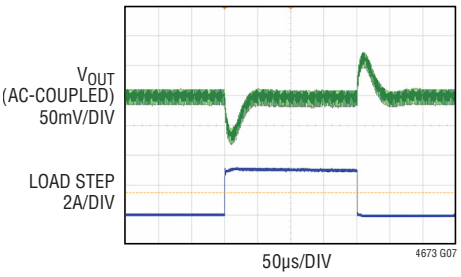
V_{IN} = 12V
V_{OUT} = 1.5V
FREQUENCY = 600kHz
C_{OUT} = 100µF ×3 CERAMIC CAPACITORS
EXT COMP: R_{TH} = 5k, C_{TH} = 2200pF, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

1.8V Output Transient Response



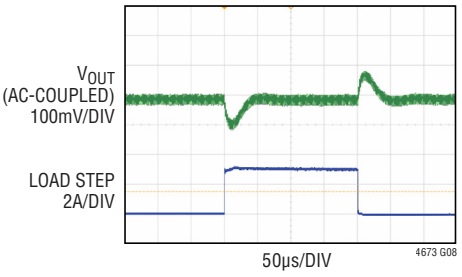
V_{IN} = 12V
V_{OUT} = 1.8V
FREQUENCY = 600kHz
C_{OUT} = 100µF ×3 CERAMIC CAPACITORS
EXT COMP: R_{TH} = 5k, C_{TH} = 2200pF, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

2.5V Output Transient Response



V_{IN} = 12V
V_{OUT} = 2.5V
FREQUENCY = 600kHz
C_{OUT} = 100µF ×3 CERAMIC CAPACITORS
EXT COMP: R_{TH} = 5k, C_{TH} = 2200pF, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

3.3V Output Transient Response

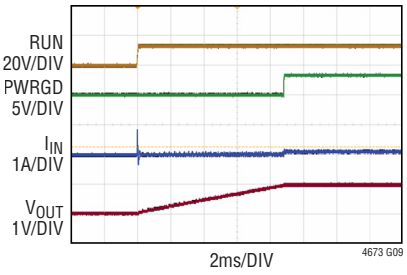


V_{IN} = 12V
V_{OUT} = 3.3V
FREQUENCY = 600kHz
C_{OUT} = 100µF ×3 CERAMIC CAPACITORS
EXT COMP: R_{TH} = 5k, C_{TH} = 2200pF, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

TYPICAL PERFORMANCE CHARACTERISTICS

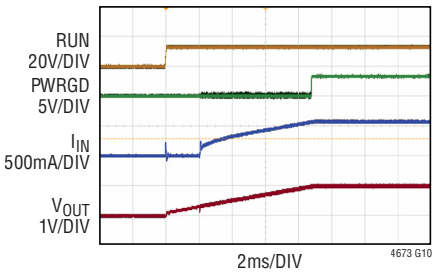
Dual 12A Channels

Start-Up Waveform with No Load Current Applied



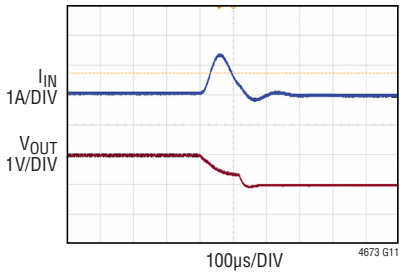
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 600kHz
C_{OUT} = 330µF ×1 POSCAP
100µF ×2 CERAMIC CAPACITORS
C_{SS} = 0.1µF

Start-Up Waveform with 12A Load Current Applied



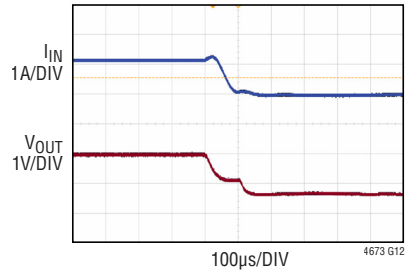
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 600kHz
C_{OUT} = 330µF ×1 POSCAP
100µF ×2 CERAMIC CAPACITORS
C_{SS} = 0.1µF

Short-Circuit Waveform with No Load Current Exist, V_{OUT} Undervoltage Fault Response



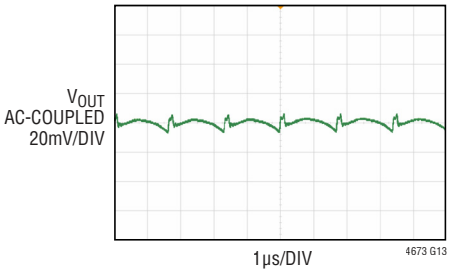
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 600kHz
C_{OUT} = 330µF ×1 POSCAP,
100µF ×2 CERAMIC CAPACITORS

Short-Circuit Waveform with 12A Load Current, V_{OUT} Undervoltage Fault Response



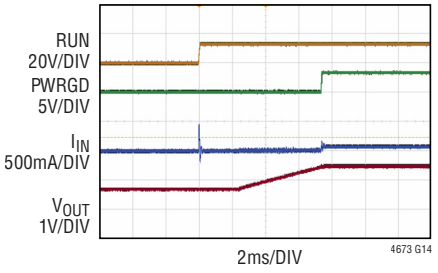
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 600kHz
C_{OUT} = 330µF ×1 POSCAP,
100µF ×2 CERAMIC CAPACITORS

Output Voltage Ripple



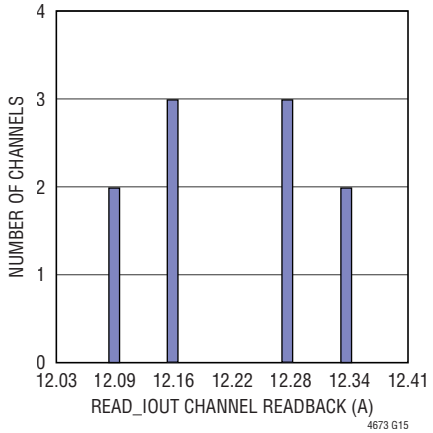
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 600kHz
C_{OUT} = 100µF ×3 CERAMIC CAPACITORS

Start into Prebiased Output



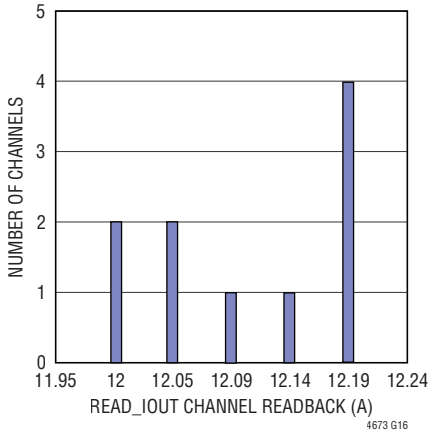
V_{IN} = 12V
V_{OUT} = 1.5V
V_{OUT} PREBIASED TO 0.9V
FREQUENCY = 600kHz
C_{OUT} = 330µF ×1 POSCAP
100µF ×2 CERAMIC CAPACITORS

READ_IOUT of 10 LTM4673 Channels (DC2810A)



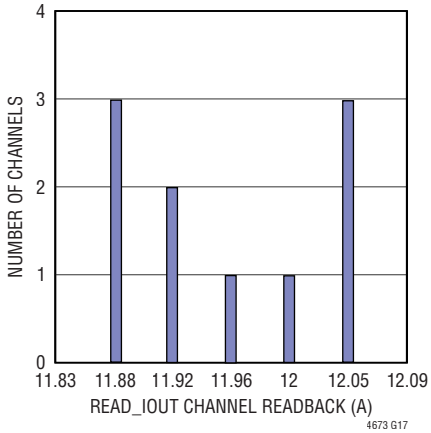
$12V_{IN}$, $1V_{OUT}$, T_J = –40°C, I_{OUTn} = 12A,
SYSTEM HAVING REACHED THERMALLY
STEADY-STATE CONDITION, NO AIRFLOW

READ_IOUT of 10 LTM4673 Channels (DC2810A)



$12V_{IN}$, $1V_{OUT}$, T_J = 25°C, I_{OUTn} = 12A,
SYSTEM HAVING REACHED THERMALLY
STEADY-STATE CONDITION, NO AIRFLOW

READ_IOUT of 10 LTM4673 Channels (DC2810A)

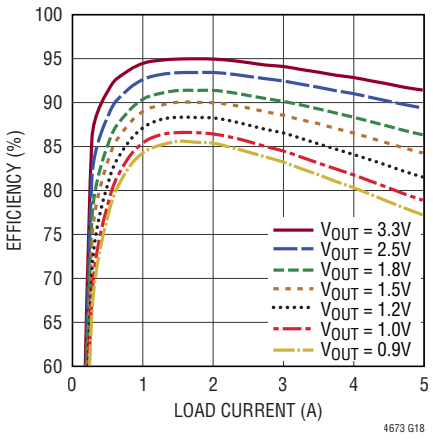


$12V_{IN}$, $1V_{OUT}$, T_J = 125°C, I_{OUTn} = 12A,
SYSTEM HAVING REACHED THERMALLY
STEADY-STATE CONDITION, NO AIRFLOW

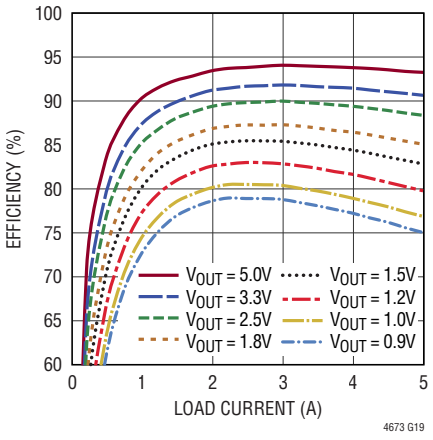
TYPICAL PERFORMANCE CHARACTERISTICS

Dual 5A Channels

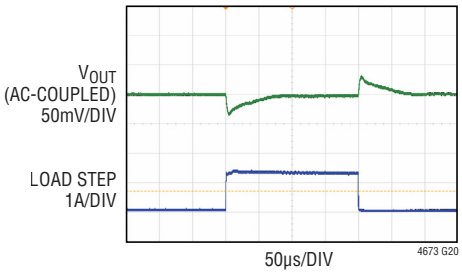
Efficiency vs Load Current from $5V_{IN}$



Efficiency vs Load Current from $12V_{IN}$

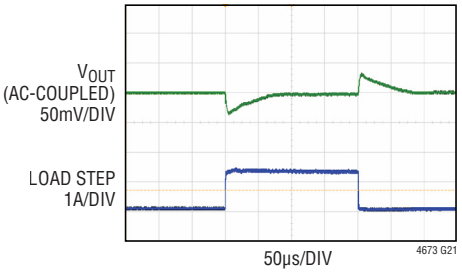


1.0V Output Transient Response



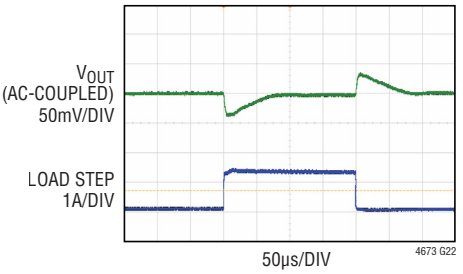
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1, 47µF ×2 CERAMIC CAPACITORS
INTERNALLY COMPENSATED
C_{FF} = 33pF
1.25A (25%) LOAD STEP, 1A/µs

1.2V Output Transient Response



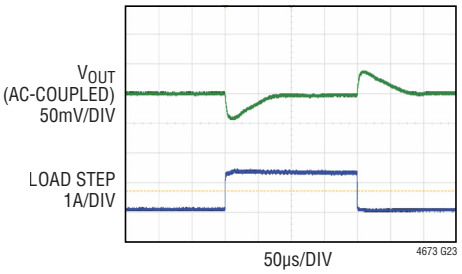
V_{IN} = 12V
V_{OUT} = 1.2V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1, 47µF ×2 CERAMIC CAPACITORS
INTERNALLY COMPENSATED
C_{FF} = 33pF
1.25A (25%) LOAD STEP, 1A/µs

1.5V Output Transient Response



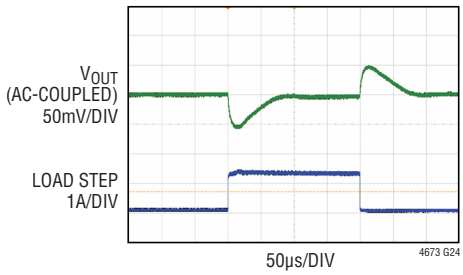
V_{IN} = 12V
V_{OUT} = 1.5V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1, 47µF ×2 CERAMIC CAPACITORS
INTERNALLY COMPENSATED
C_{FF} = 33pF
1.25A (25%) LOAD STEP, 1A/µs

1.8V Output Transient Response



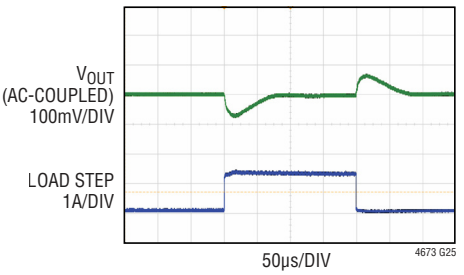
V_{IN} = 12V
V_{OUT} = 1.8V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1, 47µF ×2 CERAMIC CAPACITORS
INTERNALLY COMPENSATED
C_{FF} = 33pF
1.25A (25%) LOAD STEP, 1A/µs

2.5V Output Transient Response



V_{IN} = 12V
V_{OUT} = 2.5V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1, 47µF ×2 CERAMIC CAPACITORS
INTERNALLY COMPENSATED
C_{FF} = 33pF
1.25A (25%) LOAD STEP, 1A/µs

3.3V Output Transient Response

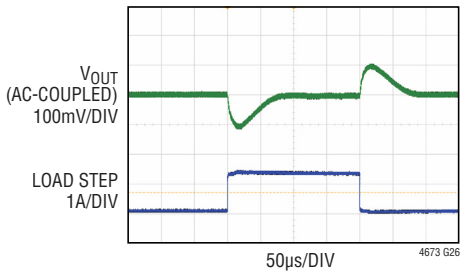


V_{IN} = 12V
V_{OUT} = 3.3V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1, 47µF ×2 CERAMIC CAPACITORS
INTERNALLY COMPENSATED
C_{FF} = 33pF
1.25A (25%) LOAD STEP, 1A/µs

TYPICAL PERFORMANCE CHARACTERISTICS

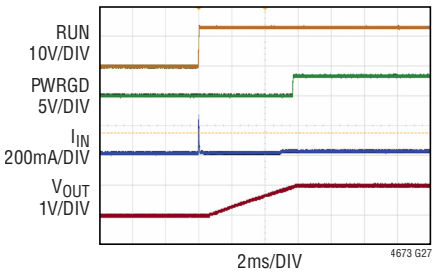
Dual 5A Channels

5V Output Transient Response



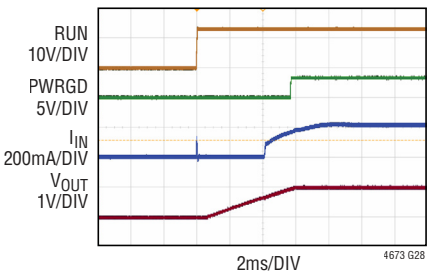
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1, 47µF ×2 CERAMIC CAPACITORS
INTERNALLY COMPENSATED
C_{FF} = 33pF
1.25A (25%) LOAD STEP, 1A/µs

Start-Up Waveform with No Load Current Applied



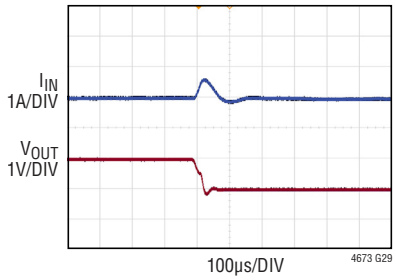
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1 POSCAP
47µF ×2 CERAMIC CAPACITORS
C_{FF} = 100pF, C_{SS} = 0.1µF

Start-Up Waveform with 5A Load Current Applied



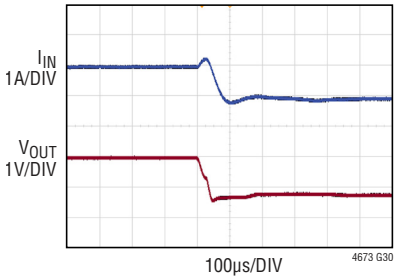
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1 POSCAP
47µF ×2 CERAMIC CAPACITORS
C_{FF} = 100pF, C_{SS} = 0.1µF

Short-Circuit Waveform with No Load Current, V_{OUT} Undervoltage Fault Response



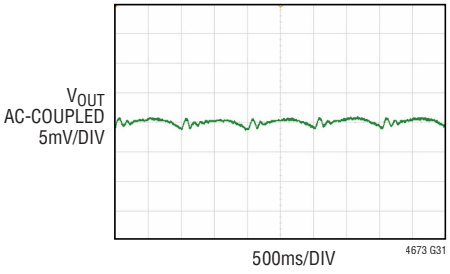
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 1MHz
C_{OUT} = 100µF ×1, 47µF ×2 CERAMIC CAPACITORS
C_{FF} = 100pF

Short-Circuit Waveform with 5A Load Current, V_{OUT} Undervoltage Fault Response



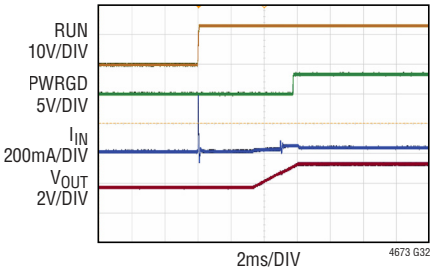
V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1, 47µF ×2 CERAMIC CAPACITORS
C_{FF} = 100pF

Output Ripple with No Load Current Applied



V_{IN} = 12V
V_{OUT} = 1V
FREQUENCY = 1MHz
C_{OUT} = 1× 10µF, 47µF ×2 CERAMIC CAPACITORS
C_{FF} = 100pF

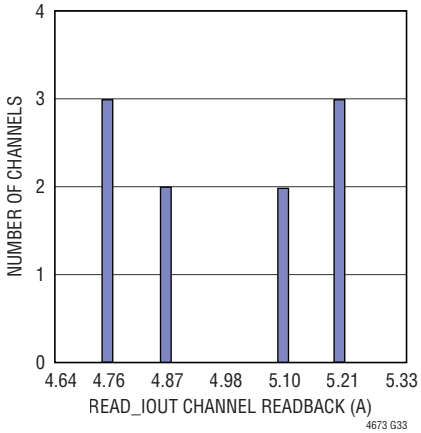
Start Into Prebiased Output



V_{IN} = 12V
V_{OUT} = 3.3V
V_{OUT} PREBIASED TO 1.8V
FREQUENCY = 1MHz
C_{OUT} = 10µF ×1 POSCAP
47µF ×2 CERAMIC CAPACITORS
C_{FF} = 100pF, C_{SS} = 0.1µF

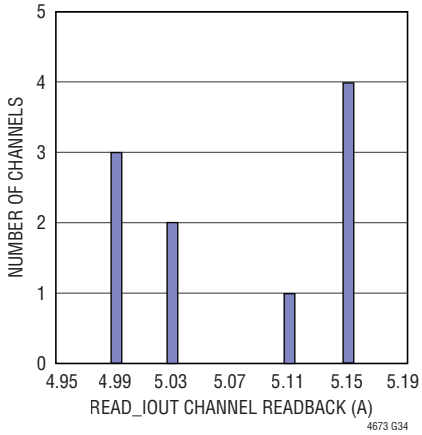
TYPICAL PERFORMANCE CHARACTERISTICS

READ_IOUT of 10 LTM4673 Channels (DC2810A)



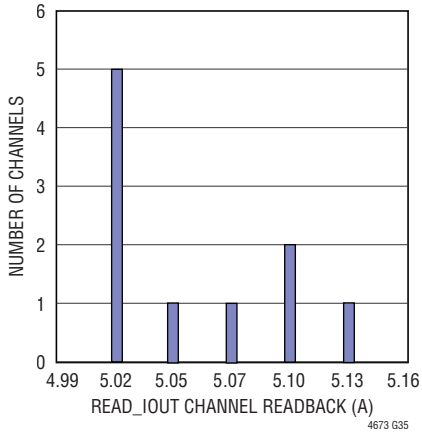
$12V_{IN}$, $2.5V_{OUT}$, T_J = –40°C, I_{OUTn} = 5A, SYSTEM HAVING REACHED THERMALLY STEADY-STATE CONDITION, NO AIRFLOW

READ_IOUT of 10 LTM4673 Channels (DC2810A)



$12V_{IN}$, $2.5V_{OUT}$, T_J = 25°C, I_{OUTn} = 5A, SYSTEM HAVING REACHED THERMALLY STEADY-STATE CONDITION, NO AIRFLOW

READ_IOUT of 10 LTM4673 Channels (DC2810A)



$12V_{IN}$, $2.5V_{OUT}$, T_J = 125°C, I_{OUTn} = 5A, SYSTEM HAVING REACHED THERMALLY STEADY-STATE CONDITION, NO AIRFLOW

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (Pins A4-A5, A8-A12, B4-B12, C4-C12, D4-D6, E3-E5, E12-E13, F1-F7, F12, G1-G6, G10, G12, H5, H7, H12, J7, J9, J13, K1-K7, K11-K13, L7, L11, L13, M5, M7, M10, M12-M13, N1-N6, N12-N13, P1-P5, P11-P13, R3-R5, R12-R13,T4-T6, U4-U12, V4-V12, W4-W5, W8-W12): Power Ground Pins for Both Input and Output Returns. Use large PCB copper areas to connect all GND together.

V_{IN} (Pins A13, B13, C13, D7-D13, E8, H6, J5-J6, L5-L6, M6, R10, T7-T13, U13, V13, W13): Power Input. Pins connect to the drain of the internal top MOSFET and Signal V_{IN} to the internal 3.3V regulator for the control circuitry for each switching mode regulator channel. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of V_{IN} pins and GND pins.

Pins For Dual 12A Channels

V_{OUT0} (Pins A1-A3, B1-B3, C1-C3, D1-D3, E1-E2), V_{OUT3} (Pins R1-R2, T1-T3, U1-U3, V1-V3, W1-W3): Power Output Pins of Each 12A Switching Mode Regulator Channel. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See the Applications Information section for paralleling outputs.

$TSENSE0^-$ (Pin A6), $TSENSE3^-$ (Pin W7): Low Side of the Internal Temperature Monitor.

$TSENSE0^+$ (Pin A7), $TSENSE3^+$ (Pin W6): Temperature Monitor of Each 12A Switching Mode Regulator Channel. An internal diode connected NPN transistor is placed between $TSENSE^+$ and $TSENSE^-$ pins. See the Applications Information section.

PHMODE0 (Pin E6), PHMODE3 (Pin R6): Control Input to the Phase Selector of Each 12A Switching Mode Regulator Channel. Determines the phase relationship between internal oscillator and CLKOUT. Tie it to $INTV_{CC}$ for 2-phase operation, tie it to SGND for 3-phase operation, and floating for 4-phase operation. See Applications Information section for details.

PIN FUNCTIONS

$INTV_{CC0}$ (Pin E7), $INTV_{CC3}$ (Pin R11): Internal 3.3V Regulator Output of Each 12A Switching Mode Regulator Channel. The internal power drivers and control circuits are powered from this voltage. Decouple each pin to GND with a minimum of 2.2µF local low ESR ceramic capacitor.

SV_{IN0} (Pin E9), SV_{IN3} (Pin R9): Signal V_{IN}. Filtered input voltage to the on-chip 3.3V regulator. Tie this pin to the V_{IN} pin in most applications or connect SV_{IN} to an external voltage supply of at least 4V which must also be greater than V_{OUT}.

CLKOUT0 (Pin E10), CLKOUT3 (Pin P6): Output Clock Signal for PolyPhase Operation of Each 12A Switching Mode Regulator Channel. The phase of CLKOUT with respect to CLKIN is determined by the state of the respective PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. See Applications Information section for details.

PWRGD0 (Pin E11), PWRGD3 (Pin R7): Output Power Good with Open-Drain Logic of Each 12A Switching Mode Regulator Channel. PWRGD is pulled to ground when the voltage on the FB pin is not within ±8% of the internal 0.6V reference.

V_{OSNS0}^- (Pin F8), V_{OSNS3}^- (Pin P10): Negative Voltage Sense Pin for Digital V_{OUT} Measurement and Negative Input to the Differential Remote Sense Amplifier of Each 12A Switching Mode Regulator Channel. Connect an external resistor between FB and V_{OSNS}^- pins to set the output voltage of the specific channel. See the Applications Information section for details.

TRACK/SS0 (Pin F9), TRACK/SS3 (Pin P9): Output Tracking and Soft-Start Pin of Each 12A Switching Mode Regulator Channel. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 6µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function. See the Applications Information section for details.

FREQ0 (Pin F10), FREQ3 (Pin P8): Switching Frequency Program Pin of Each 12A Switching Mode Regulator Channel. Frequency is set internally to 600kHz. An external resistor can be placed from this pin to GND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

RUN0 (Pin F11), RUN3 (Pin P7): Run Control Input of Each 12A Switching Mode Regulator Channel. Internally connected to its corresponding CONTROL*n* output. Leave this pin floating.

V_{OSNS0}^+ (Pin G8), V_{OSNS3}^+ (Pin N11): Positive Voltage Sense Pin for Digital V_{OUT} Measurement and Positive Input to the Differential Remote Sense Amplifier of Each 12A Switching Mode Regulator Channel. Internally, these pins are connected to V_{FB} with a 60.4k 0.5% precision resistor. It is very important to connect these pins to the V_{OUT}, and cannot be left open. See the Applications Information section for details.

FB0 (Pin G9), FB3 (Pin N10): The Negative Input of the Error Amplifier for Each 12A Switching Mode Regulator Channel. This pin is internally connected to V_{OSNS0}^+ or V_{OSNS3}^+, respectively, with a 60.4kΩ precision resistor. Output voltages can be programmed with an additional resistor between FB and V_{OSNS}^- pins. In PolyPhase® operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

MODE/CLKIN0 (Pin G11), MODE/CLKIN3 (Pin R8): Discontinuous Mode Select Pin and External Synchronization Input to Phase Detector of Each 12A Switching Mode Regulator Channel. Tie MODE/CLKIN to GND for discontinuous mode of operation. Floating MODE/CLKIN or tying it to a voltage above 1V will select forced continuous mode. Furthermore, connecting MODE/CLKIN to an external clock will synchronize the system clock to the external clock and puts the part in forced continuous mode. See Applications Information section for details.

COMP0a (Pin H10), COMP3a (Pin N9): Current Control Threshold and Error Amplifier Compensation Point of Each 12A Switching Mode Regulator Channel. The internal current comparator threshold is linearly proportional to this voltage. Tie the COMPa pins from different channels together for parallel operation. The device is internal compensated. Connect to COMP0b or COMP3b, respectively, to use the internal compensation. Or connect to a Type-II C-R-C network to use customized compensation.

PIN FUNCTIONS

COMP0b (Pin H11), COMP3b (Pin N8): Internal Loop Compensation Network for Each 12A Switching Mode Regulator Channel. Connect to COMP0a or COMP3a, respectively, to use the internal compensation in majority of applications.

Pins for Dual 5A Channels

TRACK/SS1 (Pin G7), TRACK/SS2 (Pin N7): Output Tracking and Soft-Start Pin of Each 5A Switching Mode Regulator Channel. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 1.4µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function. See the Applications Information section for details.

V_{OUT1} (Pins H1-H4, J1-J4), V_{OUT2} (Pins L1-L4, M1-M4): Power Output Pins of Each 5A Switching Mode Regulator Channel. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See the Applications Information section for paralleling outputs.

PWRGD1 (Pin H8), PWRGD2 (Pin M8): Output Power Good with Open-Drain Logic of Each 5A Switching Mode Regulator Channel. PWRGD is pulled to ground when the voltage on the FB pin is not within ±8% of the internal 0.6V reference.

FB1 (Pin H9), FB2 (Pin M9): The Negative Input of the Error Amplifier for Each 5A Switching Mode Regulator Channel. This pin is internally connected to V_{OSNS1} or V_{OSNS2}, respectively, with a 60.4kΩ precision resistor. Output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

RUN1 (Pin J8), RUN2 (Pin L8): Run Control Input of Each 5A Switching Mode Regulator Channel. Internally connected to its corresponding CONTROL*n* output. Leave this pin floating.

V_{OSNS1}^+ (Pin J10), V_{OSNS2}^+ (Pin L10): Positive Voltage Sense Pin for Digital V_{OUT} Measurement and Sense Pin of Each 5A Switching Mode Regulator Channel. Internally, these pins are connected to V_{FB} with a 60.4k 0.5% precision resistor. It is very important to connect these pins to the V_{OUT}, and cannot be left open. See the Applications Information section for details.

V_{OSNS1}^- (Pin J12), V_{OSNS2}^- (Pin L12): Negative Voltage Sense Pin for Digital V_{OUT} Measurement and Negative Output Voltage Sense Pin of Each 5A Switching Mode Regulator Channel.

COMP1 (Pin J11), COMP2 (Pin M11): Current Control Threshold and Error Amplifier Compensation Point of Each 5A Switching Mode Regulator Channel. The internal current comparator threshold is linearly proportional to this voltage. Tie the COMP pins from different channels together for parallel operation. These channels are internal compensated.

TMON (Pin K8): Temperature Monitor for 5A Output Channels. A voltage proportional to the measured on-die temperature will appear at this pin. The voltage-to-temperature scaling factor is 200°K/V. See the Applications Information section for detailed information on the TMON function. Tie this pin to $INTV_{CC12}$ to disable the temperature monitor circuit.

$INTV_{CC12}$ (Pin K9): Internal 3.3V Regulator Output for Both 5A Switching Mode Regulator Channels. The internal power drivers and control circuits are powered from this voltage. Decouple each pin to GND with a minimum of 2.2µF local low ESR ceramic capacitor.

FREQ12 (Pin K10): Switching Frequency Program Pin for Both 5A Switching Mode Regulator Channels. Frequency is set internally to 1MHz. An external resistor can be placed from this pin to GND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

MODE/CLKIN12 (Pin L9): Mode Select and External Synchronization Input Pin for Both 5A Switching Mode Regulator Channels. Tie this pin to GND to forced continuous current operation. Floating this pin or tying it to $INTV_{CC12}$ enables high efficiency Burst Mode operation at

PIN FUNCTIONS

light loads. When drive this pin with an external clock, the phase-locked loop will force the channel 1 turn on signal to be synchronized with the rising edge of the CLKIN12 signal. Channel 2 will also be synchronized with the rising edge of the CLKIN12 signal with a 180° phase shift. See Applications Information section for details.

Pins for Digital Power System Management

SGND (Pins A14-A19, B14-B19, C14-C19, D14-D19, E14-E19,H14,H16-H17, J14-J16, J18, K14, K16, L14-L19, M14-M15, M17-M19, N14, N17-N19, P14, P18-P19, R14-R19, T14-T19, U14-U19, V14-V19, W14-W19): Signal Ground Return Path of the LTM4673. SGND is not internally connected to GND. Connect SGND to GND local to the LTM4673.

$\overline{\text{ALERT}}$ (Pin F13): Open-Drain Output. Generates an interrupt request in a fault/warning situation.

SCL (Pin F14): PMBus Serial Clock Input Pin (400kHz Maximum).

SDA (Pin F15): PMBus Bidirectional Serial Data Pin.

SHARECLK (Pin F18): Bidirectional Clock Sharing Pin. Connect a 5.49k pull-up resistor to V_{DD33}. Connect to all other SHARECLK pins in the system.

PWRGD (Pin F19): Power-Good Open Drain Output. Indicates when selected outputs are power good. Can be used as system power-on reset.

CONTROL0 (Pin G13), CONTROL1 (Pin G14), CONTROL2 (Pin G17), CONTROL3 (Pin F17): Control Input Pins for Channel 0, 1, 2, 3, Respectively. Pull this pin above its rising threshold to enable the corresponding channel after a TON_DELAY. Do not leave CONTROL pins floating.

WP (Pin G15): Digital Input. Write-protect input pin, active high.Do not leave floating.

$\overline{\text{FAULT}}$0 (Pin G16), $\overline{\text{FAULT}}$1 (Pin F16): Open-Drain Output and Digital Input. Active low bidirectional fault indicator-0 and indicator-1, respectively. Connect a 10k pull-up resistor to V_{DD33}.

WDI/$\overline{\text{RESET}}$ (Pin G18): Watchdog Timer Interrupt and Chip Reset Input. Connect a 10k pull-up resistor to V_{DD33}. Rising edge resets watchdog counter. Holding this pin low for more than $t_{\overline{\text{RESET}}}$ resets the internal digital IC.

V_{DD25} (Pins G19, H19): 2.5V Internally Regulated Voltage Output. Do not connect to V_{DD25} pins of any other devices. No external decoupling is required.

ASEL0 (Pin H13), ASEL1 (Pin K15): Ternary Address Select Pin 0 and Pin 1 Input. Connect to V_{DD33}, GND or float to encode 1 of 3 logic states.

V_{IN_D} (Pin H18): Power Supply Input to the Internal Digital IC (4.5 to 15V). If a 4.5V to 15V supply voltage is unavailable, short V_{IN_D} to V_{DD33} and power directly from a 3.3V supply.

TSENSE1 (Pin J17), TSENSE2 (Pin H15): Temperature Monitor of Each 5A Switching Mode Regulator Channel. An internal diode connected NPN transistor is placed between TSENSE and SGND pins. See the Applications Information section.

V_{DD33} (Pin J19): If shorted to V_{IN_D}, it serves as 3.13V to 3.47V supply input pin. Otherwise it is a 3.3V internally regulated voltage output. If using the internal regulator to provide V_{DD33}, do not connect to V_{DD33} pins of any other devices. No external decoupling is required.

AUX$\overline{\text{FAULT}}$ (Pin K17): Auxiliary Fault Output Pin. Output high voltage optionally pulled-up to 12V by 5µA. Can be configured to pull low when OV/OC/UC detected.

V_{INSNS} (Pin K18): V_{IN} SENSE Input. This voltage is compared against the V_{IN} On and Off voltage thresholds in order to determine when to enable and disable the four outputs.

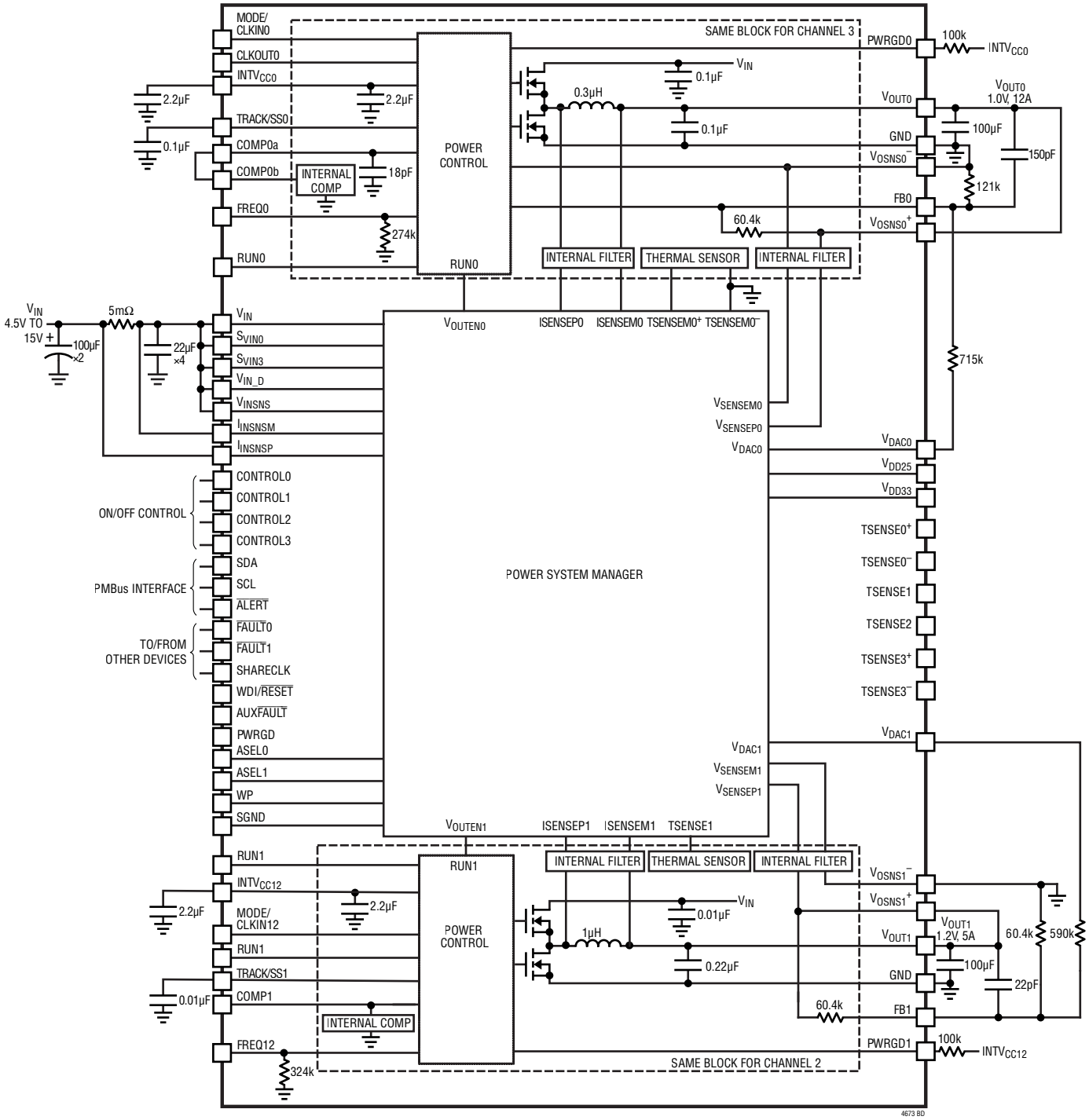
DNC (Pin K19): Do not connect this pin to external circuitry. Float this pin. Solder this pin to mounting pads on the PC board for mechanical integrity.

I_{INSNSP} (Pin N16): Differential (+) Input Current Sensing Pin. If unused, connect to V_{INSNS}.

I_{INSNSM} (Pin P16): Differential (–) Input Current Sensing Pin. If unused, connect to VINSNS.

V_{DAC0} (Pin P15), V_{DAC1} (Pin N15), V_{DAC2} (Pin M16), V_{DAC3} (Pin P17) : DAC Outputs for Channel 0, 1, 2, 3, Respectively.

BLOCK DIAGRAM



DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 15V, V_{OUT} = 1.5V)		44	66		µF
C_{OUT0}, C_{OUT3}	External Output Capacitor Requirement (V_{IN} = 4.5V to 15V, V_{OUT} = 1.5V)	I_{OUT} = 12A	100	200		µF
C_{OUT1}, C_{OUT2}	External Output Capacitor Requirement (V_{IN} = 4.5V to 15V, V_{OUT} = 1.5V)	I_{OUT} = 5A	22	47		µF

OPERATION

The LTM4673 is a quad output standalone nonisolated switch mode DC/DC power supply integrated with power system manager LTC®2975. The input voltage range is from 4.5V to 15V. It has built-in four separate regulator channels which can deliver 12A, 12A, 5A, 5A continuous output current with few external input and output capacitors. Two 12A regulators provide precisely regulated output voltage programmable from 0.6V to 3.3V while the other two 5A regulator channels can support output voltage from 0.6V to 5.5V, each via a single external resistor. Dual true differential remote sensing amplifiers are included in the high current channels to get accurate regulation at load point. The typical application schematic is shown in Figure 53.

The LTM4673 has integrated four separate constant on-time valley current mode regulators, power MOSFETs, inductors, and other supporting discrete components. For switching noise-sensitive applications, the switching frequency can be adjusted by external resistors and the µModule can be externally synchronized to a clock. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4673 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors. For Dual 12A output rails, an optional Type II C-R-C external compensation network is allowed to customize the stability and transient performance.

Current mode control provides the flexibility of paralleling any of the separate regulator channels with accurate current sharing. With a build in clock interleaving between each two regulator channels, the LTM4673 could easily employ a 2+1+1 or 2+2 channels parallel operation which is more than flexible in a multi-rail POL application like FPGA.

Furthermore, the LTM4673 has CLKIN and CLKOUT pins for frequency synchronization or PolyPhase multiple devices which allow up to 8 phases of 12A or 5A channels can be cascaded to run simultaneously.

Current mode control also provides cycle-by-cycle fast current monitoring. An internal overvoltage and undervoltage comparators pull the open-drain PWRGD output low if the output feedback voltage exits a ±8% window around the regulation point. Furthermore, in an overvoltage condition, internal top MOSFET is turned off and bottom MOSFET is turned on and held on until the overvoltage condition clears.

Pulling the RUN pin below 0.6V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, Burst Mode operation can be enabled to achieve higher efficiency compared to continuous mode for the dual 5A channels by setting MODE/PLLIN pin floating or tying to $INTV_{CC}$. The TRACK/SS pin is used for power supply tracking and soft-start programming. See the Applications Information section.

Five different temperature sensing pins are included inside the module to monitor the temperature of the module for different channels. See the Applications Information section for details.

OPERATION

The LTM4673 has integrated power system manager LTC2975 inside the module. Features of the LTM4673 that enable power system management, rail sequening and fault monitering and reporting are as follows:

- Accept PMBus compatible programming commands.
- Read input current, input voltage, input power, and accumulated input energy.
- Trim all four channels' output voltages (typically in 0.02% steps), in closed-loop servo operating mode, autonomously or through PMBus programming.
- Margin all four channels' output voltages to PMBus programmed limits.
- Monitor input voltage, four output voltages, four output currents, four inductor temperatures and internal power system management controller temperature.
- Sequence the startup of DC/DC converters via PMBus programming and the CONTROL input pins. The LTM4673 supports time-based sequencing and tracking sequencing. Cascade sequence on with time based sequence off is also supported.
- Report the four output voltages status through the power good outputs.
- Generate interrupt requests by asserting the $\overline{\text{ALERT}}$ pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the LTM4673 $\overline{\text{FAULT}}$0 and $\overline{\text{FAULT}}$1 pins.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARECLK pin.
- Store command register contents with CRC to EEPROM through PMBus programming.
- Restore EEPROM contents through PMBus programming or when V_{DD33} is applied on power-up.
- Log telemetry and status data to EEPROM in response to a faulted-off condition.
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Respond to a fault condition by continuing operation indefinitely, latching-off after a programmable deglitch period, latching-off immediately or sequencing off after TOFF_DELAY. Use retry mode to automatically recover from a latched-off condition. With retry enabled, MFR_RETRY_COUNT programs the number of retries (0 to 6 or infinite) for all pages.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output OV, UV, OC and UC faults.
- Record minimum and maximum input voltage, input current, input power, output voltages, output currents and output temperatures.
- Access user EEPROM data directly, without altering RAM space (Mfr_ee_unlock, Mfr_ee_erase, and Mfr_ee_data). Facilitates in-house bulk programming.
- Optionally stop trimming the DC/DC converter output voltage after it reaches the initial margin or nominal target. Optionally allow trimming to restart if target drifts outside of V_{OUT} warning limits.
- Accurately handle inductor self-heating transients using a proprietary algorithm. These self-heating effects are combined with external temperature sensor readings to improve accuracy of current supervisors and ADC current measurement.
- Prevent a DC/DC converter from re-entering the on state after a power cycle until a programmable interval (MFR_RESTART_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR_VOUT_DISCHARGE_THRESHOLD).
- Accommodate multiple hosts with Command Plus.

OPERATION

EEPROM

The LTM4673 contains internal EEPROM (Nonvolatile Memory) to store configuration settings and fault log information. EEPROM endurance, retention and mass write operation time are specified over the operating temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Operating the EEPROM above 125°C may result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 85°C, a slight degradation in the data retention characteristics of the fault log may occur.

It is recommended that the EEPROM not be written using STORE_USER_ALL or bulk programming when $T_J > 125°C$.

The degradation in EEPROM retention for temperatures >125°C can be approximated by calculating the dimensionless acceleration factor using Equation 1.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]} \quad (1)$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

$k = 8.617 \bullet 10^{-5}$ eV/°K

T_{USE} = 125°C specified junction temperature

T_{STRESS} = actual junction temperature °C

Example: Calculate the effect on retention when operating at a junction temperature of 145°C for 10 hours.

T_{STRESS} = 145°C

T_{USE} = 125°C

AF = 8.65

Equivalent operating time at 125°C = 86.5 hours.

So the overall retention of the EEPROM was degraded by 86.5 hours as a result of operation at a junction temperature of 145°C for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 175,200 hours at a junction temperature of 125°C.

AUX$\overline{\text{FAULT}}$

The AUX$\overline{\text{FAULT}}$ pin can be configured to indicate when some fault conditions have been detected, using a third output level. See Figure 1 for a conceptual view of this multiplexing.

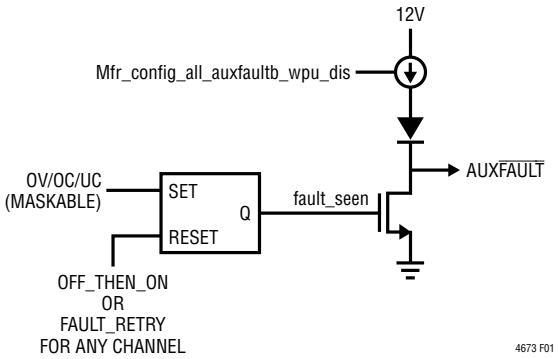


Figure 1. AUX$\overline{\text{FAULT}}$ MUX

The MFR_CONFIG2_LTM4673 and MFR_CONFIG3_LTM4673 commands can be used on a per channel basis to select which, if any, fault conditions will cause the AUX$\overline{\text{FAULT}}$ pin to be driven to its third output level (fast pull-down to GND). The only fault types which can be propagated to the AUX$\overline{\text{FAULT}}$ pin are overvoltage faults and overcurrent/undercurrent faults.

MFR_CONFIG_ALL_AUXFAULTB_WPU selects whether the AUX$\overline{\text{FAULT}}$ pin is in the hi-Z state, or weakly pulled-up to approximately 12V, using a 5µA current. As shown in Figure 1, the pull-down to GND overrides if any enabled faults are detected.

OPERATION

$\overline{\text{RESET}}$

Holding the WDI/$\overline{\text{RESET}}$ pin low for more than $t_{\overline{\text{RESET}}}$ will cause the LTM4673 to enter the power-on reset state. While in the power-on reset state, the device will not communicate on the I^{2}C bus. Following the subsequent rising-edge of the WDI/$\overline{\text{RESET}}$ pin, the LTM4673 will execute its power-on sequence per the user configuration stored in EEPROM. Connect WDI/$\overline{\text{RESET}}$ to V_{DD33} with a 10k resistor. WDI/$\overline{\text{RESET}}$ includes an internal 256µs deglitch filter so additional filter capacitance on this pin is not recommended.

PMBus SERIAL DIGITAL INTERFACE

The LTM4673 communicates with a host (main) using the standard PMBus serial bus interface. The PMBus PMBus Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTM4673 is a subordinate device. The main can communicate with the LTM4673 using the following formats:

- Main transmitter, subordinate receiver
- Main receiver, subordinate transmitter

The following SMBus commands are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figure 2 to Figure 14 illustrate the aforementioned SMBus protocols. All transactions support PEC (packet error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the SMBus timeout may be extended using the Mfr_config_all_longer_pmbus_timeout setting.

PMBus

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language.

The PMBus two wire interface is an incremental extension of the SMBus. SMBus is built upon I^{2}C with some minor differences in timing, DC parameters and protocol. The SMBus protocols are more robust than simple I^{2}C byte commands because they provide timeouts to prevent bus hangs and optional Packet Error Checking (PEC) to ensure data integrity. In general, a main device that can be configured for I^{2}C communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: Section 5: Transport. This can be found at www.pmbus.org.

For a description of the differences between SMBus and I^{2}C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B – Differences between SMBus and I^{2}C. This can be found at www.smbus.org.

When using an I^{2}C controller to communicate with a PMBus part it is important that the controller be able to write a byte of data without generating a stop. This will allow the controller to properly form the repeated start of a PMBus read command by concatenating a start command byte write with an I^{2}C read.

Device Address

The I^{2}C/SMBus address of the LTM4673 equals the base address + N where N is a number from 0 to 8. N can be configured by setting the ASEL0 and ASEL1 pins to V_{DD33}, GND or FLOAT. See Table 1. Using one base address and the nine values of N, nine LTM4673s can be connected together to control thirty six outputs. The base address is stored in the MFR_I2C_BASE_ADDRESS register. The base address can be written to any value, but generally should not be changed unless the desired range of addresses overlap existing addresses. Watch that the address range does not overlap with other I^{2}C/SMBus device or global addresses, including I^{2}C/SMBus multiplexers and bus buffers. This will bring you great happiness.

The LTM4673 always responds to its global address and the SMBus Alert Response address regardless of the state of its ASEL pins and the MFR_I2C_BASE_ADDRESS register.

OPERATION

Processing Commands

The LTM4673 uses a dedicated processing block to ensure quick response to all of its commands. There are a few exceptions where the part will NACK a subsequent command because it is still processing the previous command. These are summarized in the following tables. MFR_COMMON is a special command that may always be read even when the part is busy. This provides an alternate method for a host to determine if the LTM4673 is busy.

EEPROM Related Commands

COMMAND	TYPICAL DELAY*	COMMENT
STORE_USER_ALL	t_{MASS_WRITE}	See Electrical Characterization table. The LTM4673 will not accept any commands while it is transferring register contents to the EEPROM. The command byte will be NACKed. MFR_COMMON may always be read.
RESTORE_USER_ALL	30ms	The LTM4673 will not accept any commands while it is transferring EEPROM data to command registers. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_CLEAR	175ms	The LTM4673 will not accept any commands while it is initializing the fault log EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_STORE	20ms	The LTM4673 will not accept any commands while it is transferring fault log RAM buffer to EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
Internal Fault log	20ms	An internal fault log event is a one time event that uploads the contents of the fault log to EEPROM in response to a fault. Internal fault logging may be disabled. Commands received during this EEPROM write are NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_ RESTORE	2ms	The LTM4673 will not accept any commands while it is transferring EEPROM data to the fault log RAM buffer. The command byte will be NACKed. MFR_COMMON may always be read.

*The typical delay is measured from the command's stop to the next command's start.

Other Commands

COMMAND	TYPICAL DELAY*	COMMENT
MFR_CONFIG	<50µs	The LTM4673 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.
IOUT_CAL_GAIN	<500µs	The LTM4673 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.

*The delay is measured from the command's stop to the next command's start.

Other PMBus Timing Notes

COMMAND	COMMENT
CLEAR_FAULTS	The LTM4673 will accept commands while it is completing this command but the affected status flags will not be cleared for up to 500µs.

OPERATION

Table 1. LTM4673 Address Look-Up Table with MFR_I2C_BASE_ADDRESS Set to 7-Bit 0x5C

ADDRESS PINS			HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS							
ASEL1	ASEL0	DESCRIPTION	7-Bit	8-Bit	6	5	4	3	2	1	0	R/W
X	X	Alert Response	0C	19	0	0	0	1	1	0	0	1
X	X	Global	5B	B6	1	0	1	1	0	1	1	0
L	L	N = 0	5C*	B8	1	0	1	1	1	0	0	0
L	NC	N = 1	5D	BA	1	0	1	1	1	0	1	0
L	H	N = 2	5E	BC	1	0	1	1	1	1	0	0
NC	L	N = 3	5F	BE	1	0	1	1	1	1	1	0
NC	NC	N = 4	60	C0	1	1	0	0	0	0	0	0
NC	H	N = 5	61	C2	1	1	0	0	0	0	1	0
H	L	N = 6	62	C4	1	1	0	0	0	1	0	0
H	NC	N = 7	63	C6	1	1	0	0	0	1	1	0
H	H	N = 8	64	C8	1	1	0	0	1	0	0	0

H = Tie to V_{DD33}, NC = No Connect = Open or Float, L = Tie to GND, X = Don't Care
*MFR_I2C_BASE_ADDRESS = 7-Bit 0x5C (Factory Default)

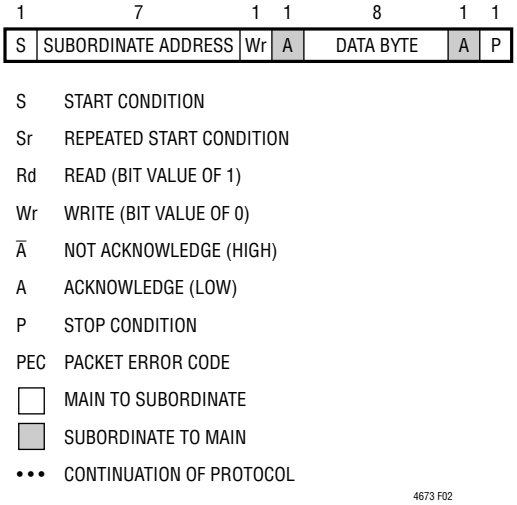


Figure 2. PMBus Packet Protocol Diagram Element Key

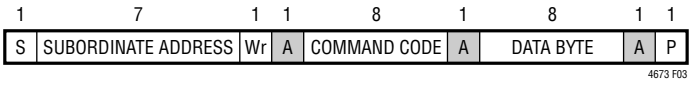


Figure 3. Write Byte Protocol

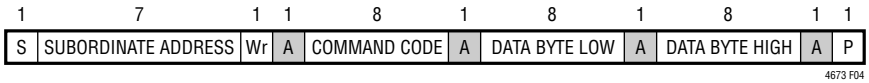


Figure 4. Write Word Protocol

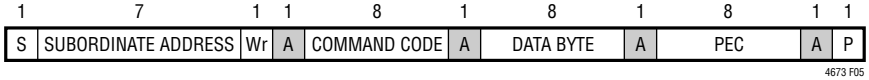


Figure 5. Write Byte Protocol with PEC

OPERATION

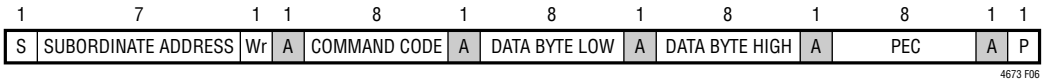


Figure 6. Write Word Protocol with PEC

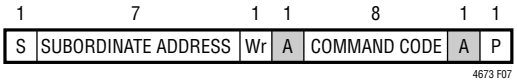


Figure 7. Send Byte Protocol

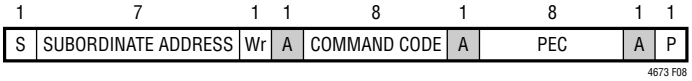


Figure 8. Send Byte Protocol with PEC

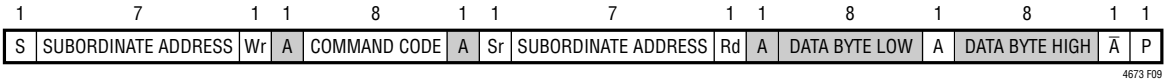


Figure 9. Read Word Protocol

Figure 10. Read Word Protocol with PEC

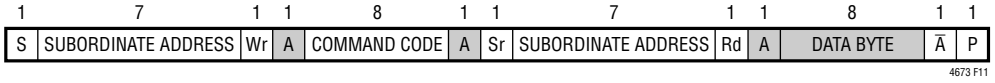


Figure 11. Read Byte Protocol

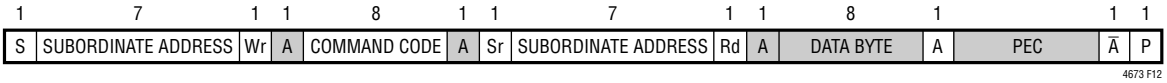


Figure 12. Read Byte Protocol with PEC

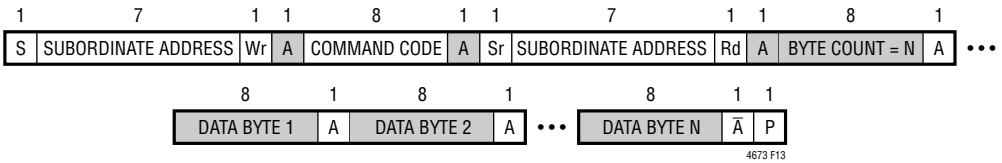


Figure 13. Block Read

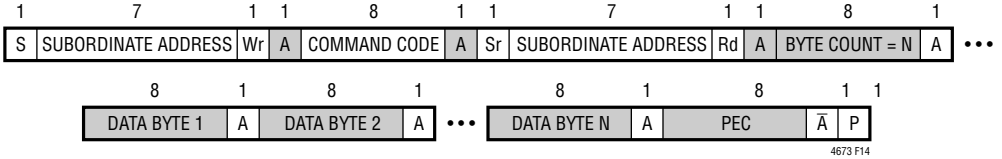


Figure 14. Block Read with PEC

PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	67
OPERATION	0x01	Operating mode control. ON/OFF, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x80	72
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus ON/OFF command setting.	R/W Byte	Y	Reg		Y	0x1E	73
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	99
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	68
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	79
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	79
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	118
VOUT_MODE	0x20	Output voltage data format and mantissa exponent (2^{-13}).	R Byte	Y	Reg			0x13	86
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	Pg00: 1.0 0x2000 Pg01: 1.2 0x2666 Pg02: 1.8 0x399A Pg03: 0.9 0x1CCD	86
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	Pg00: 4.0 0x8000 Pg01: 6.0 0xC000 Pg02: 6.0 0xC000 Pg03: 4.0 0x8000	86
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	Pg00: 1.05 0x219A Pg01: 1.26 0x2852 Pg02: 1.89 0x3C7B Pg03: 0.945 0x1E3E	86
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	Pg00: 0.95 0x1E66 Pg01: 1.14 0x247A Pg02: 1.71 0x36B9 Pg03: 0.855 0x1B5C	86
VIN_ON	0x35	Input voltage above which power conversion can be enabled.	R/W Word	N	L11	V	Y	4.5 0xCA40	81
VIN_OFF	0x36	Input voltage below which power conversion is disabled. All RUN pins go off immediately or sequence off after TOFF_DELAY (See Mfr_track_en_chan*n*).	R/W Word	N	L11	V	Y	4.4 0xCA33	81
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R Word	Y	L11	mΩ	Y	Trimmed at ATE, read-only, paged, stored in factory-only NVM.	87
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	Pg00: 1.10 0x2333 Pg01: 1.32 0x2A3D Pg02: 1.98 0x3F5D Pg03: 0.99 0x1FAE	86

NOTE: The data format abbreviations are detailed in the Data Formats table.

PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	94
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	Pg00: 1.07 0x2266 Pg01: 1.29 0x2947 Pg02: 1.94 0x3DEC Pg03: 0.97 0x1EF6	86
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	Pg00: 0.93 0x1D9A Pg01: 1.11 0x2385 Pg02: 1.67 0x3548 Pg03: 0.83 0x1AA4	86
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for Ton_max_fault and power good de-assertion.	R/W Word	Y	L16	V	Y	Pg00: 0.90 0x1CCD Pg01: 1.08 0x228F Pg02: 1.62 0x33D7 Pg03: 0.81 0x19EC	86
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	94
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	Pg00: 17 0xDA20 Pg01: 8 0xD200 Pg02: 8 0xD200 Pg03: 17 0xDA20	95
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	95
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	Pg00: 13 0xD340 Pg01: 6 0xCB00 Pg02: 6 0xCB00 Pg03: 13 0xD340	88
IOUT_UC_FAULT_LIMIT	0x4B	Output undercurrent fault limit. Used to detect a reverse current and must be a negative value.	R/W Word	Y	L11	A	Y	Pg00: –3 0xC500 Pg01: –1.5 0xBD00 Pg02: –1.5 0xBD00 Pg03: –3 0xC500	88
IOUT_UC_FAULT_RESPONSE	0x4C	Action to be taken by the device when an output undercurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	95
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	128 0xF200	89
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	96
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	125 0xEBE8	89
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	–20.0 0xDD80	89
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	–45.0 0xE530	89
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	96
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at VINSNS pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	81
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	96

PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at VINSNS pin.	R/W Word	N	L11	V	Y	14.0 0xD380	81
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at VINSNS pin.	R/W Word	N	L11	V	Y	0 0x8000	81
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at VINSNS pin.	R/W Word	N	L11	V	Y	0 0x8000	81
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	96
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	Pg00: 0.96 0x1EB8 Pg01: 1.15 0x24DD Pg02: 1.73 0x374C Pg03: 0.86 0x1BA6	86
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted when Mfr_config_all_pwrgd_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	Pg00: 0.94 0x1E14 Pg01: 1.13 0x2418 Pg02: 1.69 0x3625 Pg03: 0.85 0x1B13	86
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to RUN pin = ON.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	91
TON_RISE	0x61	Time from when the RUN pin goes high until the LTM4673 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	ms	Y	10.0 0xD280	91
TON_MAX_FAULT_LIMIT	0x62	Maximum time from RUN pin on assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	ms	Y	15.0 0xD3C0	91
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	97
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to RUN pin = OFF.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	91
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	100
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R Word	Y	Reg			NA	100
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	101
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	101
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	101
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	102
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	102
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	103
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	105
READ_IIN	0x89	DC/DC converter input current.	R Word	Y	L11	A		NA	105
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	105
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	106

PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
READ_TEMPERATURE_1	0x8D	Power stage temperature sensor. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	106
READ_TEMPERATURE_2	0x8E	Control IC die temperature.	R Word	N	L11	°C		NA	106
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	106
READ_PIN	0x97	DC/DC converter input power.	R Word	Y	L11	W		NA	105
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	118
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	NA	119
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	119
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	NA	119
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	119
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	119
MFR_LTC_RESERVED_1	0xB5	Manufacturer reserved.	R/W Word	Y	Reg		Y	NA	119
MFR_T_SELF_HEAT	0xB8	Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor.	R Word	Y	L11	°C		NA	89
MFR_IOUT_CAL_GAIN_TAU_INV	0xB9	Inverse of time constant for Mfr_t_self_heat changes scaled by 4 • t_{CONV_SENSE}.	R/W Word	Y	L11		Y	0.0 0x8000	89
MFR_IOUT_CAL_GAIN_THETA	0xBA	Thermal resistance from inductor core to point measured by external temperature sensor.	R/W Word	Y	L11	°C/W	Y	0.0 0x8000	89
MFR_READ_IOUT	0xBB	Alternate data format for READ_IOUT. One LSB = 2.5mA.	R Word	Y	CF	2.5mA		NA	107
MFR_LTC_RESERVED_2	0xBC	Manufacturer reserved.	R/W Word	Y	Reg			NA	119
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	79
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	80
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	80
MFR_EIN	0xC0	Input Energy data bytes.	R Block	N	Reg			NA	83
MFR_EIN_CONFIG	0xC1	Configuration register for energy and input current.	R/W Byte	N	Reg		Y	0x00	83
MFR_SPECIAL_LOT	0xC2	Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value.	R Byte	Y	Reg		Y	NA	119
MFR_IIN_CAL_GAIN_TC	0xC3	Temperature coefficient applied to IIN_CAL_ GAIN.	R/W Word	N	CF	ppm	Y	0x0000	84
MFR_IIN_PEAK	0xC4	Maximum measured value of READ_IIN	R Word	Y	L11	A		NA	106
MFR_IIN_MIN	0xC5	Minimum measured value of READ_IIN.	R Word	Y	L11	A		NA	106
MFR_PIN_PEAK	0xC6	Maximum measured value of READ_PIN.	R Word	Y	L11	W		NA	106
MFR_PIN_MIN	0xC7	Minimum measured value of READ_PIN.	R Word	Y	L11	W		NA	106

PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
MFR_COMMAND_PLUS	0xC8	Alternate access to block read and other data. Commands for all additional hosts.	R/W Word	N	Reg				69
MFR_DATA_PLUS0	0xC9	Alternate access to block read and other data. Data for additional host 0.	R/W Word	N	Reg				69
MFR_DATA_PLUS1	0xCA	Alternate access to block read and other data. Data for additional host 1.	R/W Word	N	Reg				69
MFR_CONFIG_LTM4673	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	Pg00: 0x0088 Pg01: 0x1088 Pg02: 0x2088 Pg03: 0x3088	74
MFR_CONFIG_ALL_LTM4673	0xD1	Configuration bits that are common to all pages.	R/W Word	N	Reg		Y	0x0F7B	77
MFR_FAULTB0_PROPAGATE	0xD2	Configuration that determines if a channel's faulted off state is propagated to the $\overline{\text{FAULT}}$0 pin.	R/W Byte	Y	Reg		Y	0x00	98
MFR_FAULTB1_PROPAGATE	0xD3	Configuration that determines if a channel's faulted off state is propagated to the $\overline{\text{FAULT}}$1 pin.	R/W Byte	Y	Reg		Y	0x00	98
MFR_PWRGD_EN	0xD4	Configuration that maps WDI/$\overline{\text{RESET}}$ status and individual channel power good to the PWRGD pin.	R/W Word	N	Reg		Y	0x0000	92
MFR_FAULTB0_RESPONSE	0xD5	Action to be taken by the device when the $\overline{\text{FAULT}}$0 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	98
MFR_FAULTB1_RESPONSE	0xD6	Action to be taken by the device when the $\overline{\text{FAULT}}$1 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	98
MFR_IOUT_PEAK	0xD7	Maximum measured value of READ_IOUT.	R Word	Y	L11	A		NA	108
MFR_IOUT_MIN	0xD8	Minimum measured value of READ_IOUT.	R Word	Y	L11	A		NA	108
MFR_CONFIG2_LTM4673	0xD9	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	75
MFR_CONFIG3_LTM4673	0xDA	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	76
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	N	L11	ms	Y	200 0xF320	97
MFR_RESTART_DELAY	0xDC	Delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W Word	N	L11	ms	Y	400 0xFB20	92
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT.	R Word	Y	L16	V		NA	108
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN.	R Word	N	L11	V		NA	108
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	108
MFR_DAC	0xE0	Manufacturer register that contains the code of the 10-bit DAC.	R/W Word	Y	Reg			0x01FF	86
MFR_POWERGOOD_ ASSERTION_DELAY	0xE1	Power-good output assertion delay.	R/W Word	N	L11	ms	Y	100 0xEB20	93
MFR_WATCHDOG_T_FIRST	0xE2	First watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	93
MFR_WATCHDOG_T	0xE3	Watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	93

PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
MFR_PAGE_FF_MASK	0xE4	Configuration defining which channels respond to global page commands (PAGE=0xFF).	R/W Byte	N	Reg		Y	0x0F	68
MFR_PADS	0xE5	Current state of selected digital I/O pads.	R/W Word	N	Reg			NA	103
MFR_I2C_BASE_ADDRESS	0xE6	Base value of the I^2C/SMBus address byte.	R/W Byte	N	Reg		Y	0x5C	69
MFR_SPECIAL_ID	0xE7	Manufacturer code for identifying the LTM4673.	R Word	N	Reg		Y	0x448X	119
MFR_IIN_CAL_GAIN	0xE8	The nominal resistance of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	5.0 0xCA80	84
MFR_VOUT_DISCHARGE_THRESHOLD	0xE9	Coefficient used to multiply VOUT_COMMAND in order to determine V_{OUT} off threshold voltage.	R/W Word	Y	L11		Y	2.0 0xC200	86
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	109
MFR_FAULT_LOG_RESTORE	0xEB	Command a transfer of the fault log previously stored in EEPROM back to RAM.	Send Byte	N				NA	109
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	110
MFR_FAULT_LOG_STATUS	0xED	Fault logging status.	R Byte	N	Reg		Y	NA	110
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	110
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	104
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient applied to IOUT_CAL_GAIN.	R Word	Y	CF	ppm	Y	3900 0x0F3C	88
MFR_RETRY_COUNT	0xF7	Retry count for all faulted off conditions that enable retry.	R/W Byte	N	Reg		Y	0x07	97
MFR_TEMP_1_GAIN	0xF8	Inverse of external diode temperature non ideality factor. One LSB = 2^{-14}.	R/W Word	Y	CF		Y	1 0x4000	89
MFR_TEMP_1_OFFSET	0xF9	Offset value for the external temperature.	R/W Word	Y	L11	°C	Y	0 0x8000	89
MFR_IOUT_SENSE_VOLTAGE	0xFA	Absolute value of $V_{ISENSEP} - V_{ISENSEM}$. One LSB = 3.05µV.	R Word	Y	CF	3.05µV		NA	108
MFR_VOUT_MIN	0xFB	Minimum measured value of READ_VOUT.	R Word	Y	L16	V		NA	108
MFR_VIN_MIN	0xFC	Minimum measured value of READ_VIN.	R Word	N	L11	V		NA	108
MFR_TEMPERATURE_1_MIN	0xFD	Minimum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	109

PMBus COMMAND SUMMARY

Data Formats

L11	Linear_5s_11s	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Example: READ_VIN = 10V For b[15:0] = 0xD280 = 1101_0010_1000_0000b Value = $640 \cdot 2^{-6} = 10$ See PMBus Spec Part II: Paragraph 7.1
L16	Linear_16u	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where Y = b[15:0] is an unsigned integer and N = Vout_mode_parameter is a 5-bit two's complement exponent that is hardwired to –13 decimal. Example: VOUT_COMMAND = 4.75V For b[15:0] = 0x9800 = 1001_1000_0000_0000b Value = $38912 \cdot 2^{-13} = 4.75$ See PMBus Spec Part II: Paragraph 8.3.1
Reg	Register	PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in detailed PMBus Command Register Description.
CF	Custom Format	PMBus data field b[15:0] Value is defined in detailed PMBus Command Register Description. This is often an unsigned or two's complement integer scaled by an MFR specific constant.

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OVERVIEW

The typical LTM4673 application circuit is shown in Figure 53. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 6 for specific external capacitor requirements for a particular application.

The LTM4673 is a 4-channel Power System Management module that is capable of sequencing, margining, trimming, supervising output voltage for OV/UV conditions, supervising output current for OC/UC conditions, fault management, voltage/current/temperature readback for four DC/DC converter channels, and readback of high side input current, input voltage, input power, input energy, and junction temperature. Multiple ADI power system managers can coordinate operation using the SHARECLK, $\overline{\text{FAULT}}$, and CONTROL pins. The LTM4673 utilizes a PMBus compliant interface and command set.

POWERING LTM4673

The LTM4673 can be powered two ways. The first method requires that a voltage between 4.5V and 15V be applied to the V_{IN_D} pin. See Figure 15. An internal linear regulator converts V_{IN_D} down to $INTV_{CC}$ which is used to drive all of the internal circuitry of the LTM4673.

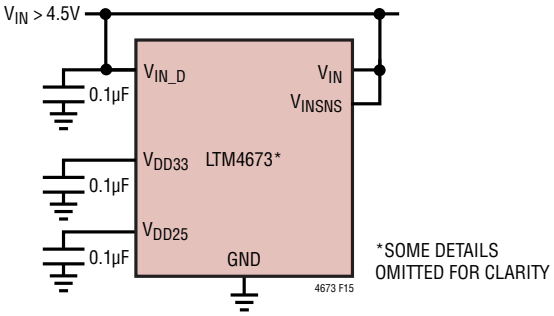

Figure 15. Powering LTM4673 Directly from an Intermediate Bus

Alternatively, power from an external 3.3V supply may be applied directly to the V_{DD33} using a voltage between 3.2V and 3.6V. See Figure 16. Tie V_{IN_D} to the V_{DD33} pins. All functionality is available when using this alternate power method. The higher voltages needed for the RUN pins and bias for the V_{SENSE} pins are charge pumped from V_{DD33}.

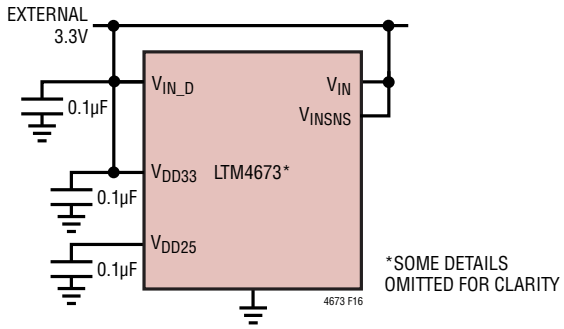

Figure 16. Powering LTM4673 from External 3.3V Supply

V_{IN} TO V_{OUT} STEP-DOWN RATIOS

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of each regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated with Equation 2.

$$D_{(MAX)} = 1 - t_{OFF(MIN)} \bullet f_{SW} \quad (2)$$

where $t_{OFF(MIN)}$ is the minimum off-time, 80ns typical for LTM4673, and f_{SW} is the switching frequency. Conversely, the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated with Equation 3.

$$D_{(MIN)} = t_{ON(MIN)} \bullet f_{SW} \quad (3)$$

where $T_{ON(MIN)}$ is the minimum on-time, 25ns typical for LTM4673. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. These constraints are shown in the Typical Performance Characteristic curve labeled V_{IN} to V_{OUT} Step-Down Ratio. Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

INPUT DECOUPLING CAPACITORS

The LTM4673 module should be connected to a low AC-impedance DC source. For each 12A regulator channel, one piece 22µF input ceramic capacitor is required, for each 5A regulator channel, one piece 10µF input ceramic capacitor is required for RMS ripple current decoupling. Bulk input capacitor is only needed when the

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input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated with Equation 4.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)} \quad (4)$$

where $\eta\%$ is the estimated efficiency of the power module.

OUTPUT VOLTAGE PROGRAMMING AND TRIMMING

The PWM controller has an internal 0.6V reference voltage.

For the 12A channels (CH0, CH3), a 60.4k 0.5% internal feedback resistor connects each regulator channel V_{OSNS}^+ and FB pin together. Adding a resistor R_{FB} from FB pin to V_{OSNS}^- programs the output voltage.

For the 5A channels (CH1, CH2), a 60.4k 0.5% internal feedback resistor connects each regulator channel V_{OSNS}^+ and FB pin together. Adding a resistor R_{FB} from FB pin to GND programs the output voltage (Equation 5)

$$R_{FB(BOT)} = \frac{60.4k}{\frac{V_{OUT}}{0.6} - 1} \quad (5)$$

LTM4673 is capable of trimming/margining the output voltage with a resistor connecting between V_{DAC} and V_{FB}. A correction voltage is developed on the V_{DAC} pin by the closed-loop servo algorithm. See Figure 53 as an example. Please refer to the design example in the Applications Information section to determine the resistance.

For parallel operation of N-channels, Use Equation 6 to solve for R_{FB}.

$$R_{FB(BOT)} = \frac{\left(\frac{60.4k}{N}\right)}{\left(\frac{V_{OUT}}{0.6} - 1\right)} \quad (6)$$

Table 2. V_{FB} Resistor Table vs Various Output Voltages for Single Channel Operation

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB} (k)	OPEN	90.9	60.4	40.2	30.1	19.1	13.3	8.25

OUTPUT DECOUPLING CAPACITORS

With an optimized high frequency, high bandwidth design, only single piece of low ESR output ceramic capacitor is required for each regulator channel to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 6 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 25% load step transient. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The Analog Devices LTpowerCAD® Design Tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

FORCED CONTINUOUS CURRENT MODE (CCM)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse.

For the 12A channels (CH0, CH3), CCM can be enabled by tying the MODE/CLKIN0 or MODE/CLKIN3 pin to the respective $INTV_{CC}$ or simply floating it.

For the 5A channels (CH1, CH2), CCM can be enabled by tying the MODE/CLKIN12 pin to GND.

During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4673's output voltage is in regulation.

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DISCONTINUOUS MODE/BURST MODE OPERATION

In applications where high efficiency at intermediate current is desired, discontinuous mode or Burst Mode operation can be achieved.

For the 12A channels (CH0, CH3), discontinuous mode (DCM) can be achieved by tying the MODE/CLKIN0 or MODE/CLKIN3 pin to GND. In discontinuous mode, the reverse current comparator will sense the inductor current and turn off bottom MOSFET when the inductor current drops to zero and becomes negative. Both power MOSFETs will remain off with the output capacitor supplying the load current until the COMP voltage rises above its zero current threshold to initiate the next switching cycle.

For the 5A channels (CH1, CH2), Burst Mode operation can be achieved by tying MODE/CLKIN12 pin to $INTV_{CC12}$ or simply floating. In Burst Mode operation, a current reversal comparator (I_{REV}) detects the negative inductor current and shuts off the bottom power MOSFET, resulting in discontinuous operation and increased efficiency. Both power MOSFETs will remain off until the COMP voltage rises above the zero current level to initiate another cycle. During this time, the output capacitor supplies the load current and the part is placed into a low current sleep mode.

OPERATING FREQUENCY

The operating frequency of the LTM4673 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 600kHz for 12A channels and 1MHz for 5A channels. In most applications, no additional frequency adjusting is required.

For the 12A channels (CH0, CH3), if an operating frequency other than 600kHz is required by the application, the operating frequency can be increased by adding a resistor, R_{FSET}, between the FREQ0 or FREQ3 pins and SGND. The operating frequency can be calculated by Equation 7.

$$f(Hz) = \frac{1.67e^{11}}{274k \,||\, R_{FSET}(\Omega)} \quad (7)$$

The frequency can be decreased below 600kHz by adding a resistor R_{FSET} between FREQ0 or FREQ3 pins to $INTV_{CC0}$ or $INTV_{CC3}$ and calculated by Equation 8.

$$R_{FSET}(M\Omega) = \frac{2.04}{4.6 - (7.5 \bullet 10^{-6} \bullet FREQ(Hz))} \quad (8)$$

The programmable operating frequency range for channels 0 and 3 is from 400kHz to 3MHz.

For the 5A channels (CH1, CH2), If an operating frequency other than 1MHz is required by the application, the operating frequency can be increased by adding a resistor, R_{FSET}, between the FREQ12 pin and SGND. The operating frequency can be calculated by Equation 9.

$$f(Hz) = \frac{3.2e^{11}}{324k \,||\, R_{FSET}(\Omega)} \quad (9)$$

The frequency can be decreased below 1MHz by adding a resistor R_{FSET} between FREQ12 pin and $INTV_{CC12}$ and calculated by Equation 10.

$$R_{FSET}(M\Omega) = \frac{2.1}{3.77 - (3.54 \bullet 10^{-6} \bullet FREQ(Hz))} \quad (10)$$

The programmable operating frequency range for channels 1 and 2 is from 500kHz to 3MHz. Also, the µModule can be externally synchronized to a clock at ±30% around set operating frequency.

FREQUENCY SYNCHRONIZATION AND CLOCK-IN

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows all internal top MOSFET turn-on to be locked to the rising edge of the same external clock. The external clock frequency range must be within ±30% around the set frequency.

A pulse detection circuit is used to detect a clock on the MODE/CLKIN0 pin for CH0 (12A) channel, MODE/CLKIN3 pin for CH3 (12A) channel and MODE/CLKIN12 pin for both CH1 and CH2 5A channels to turn on the phase-locked loop.

The pulse width of the clock has to be at least 400ns. The clock high level must be above 1V and clock low level below 0.3V. During the start-up of the regulator, the

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phase-locked loop function is disabled. When the module is driven with an external clock, forced continuous mode (CCM) is automatically enabled.

SOFT-START

The TRACK/SS pin provides a means to either soft-start of each regulator channel or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal soft-start current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated with Equation 11.

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{I_{SS}} \quad (11)$$

where C_{SS} is the capacitance on the TRACK/SS pin and the I_{SS} is the soft-start current which equals 6µA for the 12A output channels (CH0, CH3) and 1.4µA for the 5A output channels (CH1, CH2).

POWER GOOD

Four PWRGD pins of power channels are open-drain pins that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PWRGD glitches during transients or dynamic V_{OUT} changes, the LTM4673's PWRGD falling edge includes a blanking delay of approximately 52 switching cycles.

The power good pins of the power system manager inside the module is open drain output. It indicates when selected outputs are power good. This pin can be used as system power-on reset. Please refer to register MFR_PWRGD_EN and its description in PMBus Command Description section.

STABILITY COMPENSATION

The LTM4673 module internal compensation loop of each regulator channel is designed and optimized for low ESR ceramic output capacitors only application (COMPb tied to COMPa for 12A channels). Table 6 is provided for most application requirements using the optimized internal compensation. In cases which require all ceramic output capacitors for output ripple or dynamic transient spike reduction, an additional 10pF to 15pF phase boost cap (C_{FF}) is required between V_{OUT} and FB pins.

For specific optimized requirement for the dual 12A channels, disconnect COMPb from COMPa and apply a Type II C_{TH}-R_{TH}-C_{THP} compensation network from COMPa to SGND to achieve external compensation.

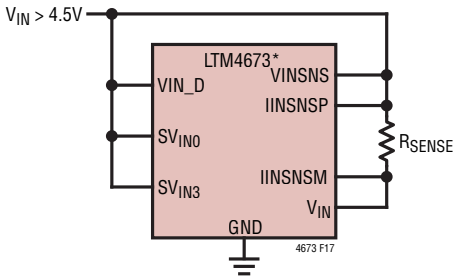
The LTpowerCAD design tool is available to download online to perform specific control loop optimization and analyze the control stability and load transient performance.

SETTING COMMAND REGISTER VALUES

The command register settings described herein are intended as a reference and for the purpose of understanding the registers in a software development environment. In actual practice, the LTM4673 can be completely configured for stand-alone operation with the DC1613 USB to I^2C/SMBus/ PMBus controller and software GUI using intuitive menu driven objects.

MEASURING INPUT CURRENT

The LTM4673 is capable of measuring the current of the input power source. The device also measures the input supply voltage, enabling it to calculate input power. The LTM4673 has an accurate internal time base allowing the chip to calculate input energy since energy is the product of power and time. The units for each of the measured parameters are amps, volts, watts, and millijoules.



*SOME DETAILS OMITTED FOR CLARITY

Figure 17. Input Current Sense Circuit for LTM4673

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Input current is measured by placing a sense resistor, R_{SENSE}, in series with the desired current load path as shown in Figure 17. If R_{SENSE} has low thermal drift characteristics, the MFR_IIN_CAL_GAIN_TC register value may be set to zero. Otherwise, choose a setting for the MFR_IIN_CAL_GAIN_TC value in units of ppm/°C to correct for R_{SENSE} thermal drift.

For best results, it is recommended to locate R_{SENSE} close to and isothermal with the LTM4673.

The input current sense path includes an internal, anti-aliasing low pass filter with typical 32dB rejection at 62.5kHz.

The Mfr_ein_config_iin_range bits select one of three input current sense amplifier ranges: high, medium and low. The R_{SENSE} value should be chosen to satisfy the input range. The maximum allowable input ranges are as follows: ±100mV range for high range, ±50mV for medium range and ±20mV for low range. For best accuracy, use the lowest range setting encompassing the maximum input signal.

To help choose the R_{SENSE} value and Mfr_ein_config_iin_range setting for your application, use the Electrical Characteristics table for TUE_IIN, along with Figure 18 and Figure 19. Figure 18 and Figure 19 serve as extrapolated guides while the Electrical Characteristics table shows tested TUE_IIN conditions. After selecting R_{SENSE}, write its value in mΩ to the MFR_IIN_CAL_GAIN register, and READ_IIN will return the sensed current in amps. Figure 18 and Figure 19 show absolute value of the expected worst case READ_IIN Total Unadjusted

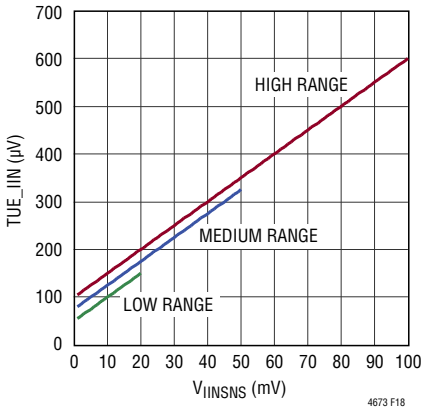


Figure 18. TUE_IIN vs READ_IIN Input Voltage in µV

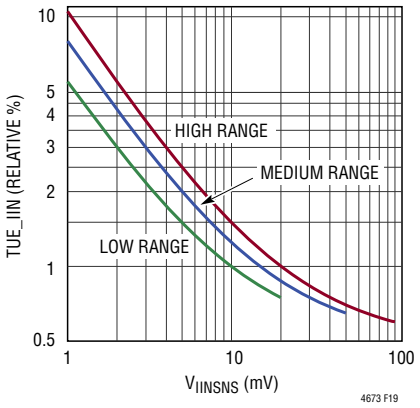
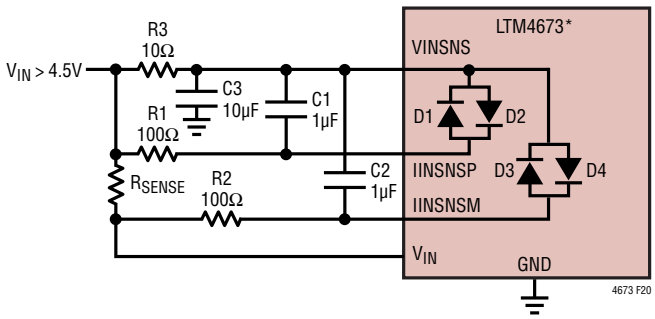


Figure 19. TUE_IIN vs READ_IIN Input Voltage in Percentage

Error, TUE_IIN, in µV and in relative % of current sense input voltage reading, V_{IINSNS}, as a function of V_{IINSNS} ($V_{IINSNSP} – V_{IINSNSP}$) for high range, medium range and low range settings.

MEASURING INPUT VOLTAGE

READ_VIN returns input voltage on the VINSNS pin. TUE_VIN reflects READ_VIN measurement error. Large ripple on the VINSNS pin may affect READ_VIN, READ_PIN, and MFR_EIN accuracy. To reduce ripple induced measurement errors, consider adding the optional anti-aliasing filter components shown in Figure 20. R3 and C3 filter VINSNS with 30dB attenuation at 62.5kHz. R1, R2, C1, C2 add additional filtering for I_{INSNS} inputs and prevent the internal diodes, D1 to D4, from turning on.



*SOME DETAILS OMITTED FOR CLARITY

Figure 20. Optional V_{INSNS} Filtering

MEASURING INPUT POWER

READ_PIN returns input power in watts calculated from the product of the most recent V_{VINSNS} and I_{INSNS}

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measurements. Although the Electrical Characteristics table only specifies READ_PIN Total Unadjusted Error (TUE_PIN) under typical conditions, TUE_PIN is actually bounded by the sum of TUE_IIN and TUE_VIN.

$$TUE\_PIN \leq TUE\_IIN + TUE\_VIN$$

For example, if $15mV < |V_{IINSNS}| < 50mV$ with the current sense amplifier set for medium range, TUE_IIN ≤ 1% and TUE_PIN is less than 1% (TUE_IIN) + 0.5% (TUE_VIN) = 1.5%.

Since current sense ranges include positive and negative inputs, READ_PIN returns signed values indicating power transfer magnitude and direction.

MEASURING INPUT ENERGY

The 12-byte data block, MFR_EIN, contains a 48-bit accumulated energy measurement in mJ, Energy_value[47:0], and a 48-bit elapsed time in milliseconds since energy began accumulating, Energy_time[47:0]. Refer to INPUT CURRENT AND ENERGY and MFR_COMMAND_PLUS sections of the PMBUS COMMAND DESCRIPTION for accumulated energy and elapsed time data access details. Energy_value can accumulate up to $(2^{48} – 1)$ mJ of energy before wrapping. Energy can accumulate for $(2^{48} – 1)$ ms, or about 8925 years, before Energy_time wraps. Accumulation of negative power measurements decreases Energy_value, and the energy meter saturates when it reaches 0 millijoules.

The energy meter time base error (TUE_ETB) specifies error in the internal energy time base accuracy: Energy_time is accurate with maximum error of TUE_ETB. Accumulated energy includes errors from current sense measurements, voltage sense measurements, and the internal time base. Energy_value error (TUE_EIN) is bounded by the summation of TUE_IIN, TUE_VIN, and TUE_ETB.

$$TUE\_EIN \leq TUE\_IIN + TUE\_VIN + TUE\_ETB$$

For example, if V_{IINSNS} = 20mV with high current sense amplifier range, TUE_IIN is less than 1% error, TUE_VIN is less than 0.5% error, and TUE_ETB is less than 1.5% error. Therefore the energy measurement error (TUE_EIN) is less than 3%.

SEQUENCE, SERVO, MARGIN AND RESTART OPERATIONS

Command Units On/Off

Three control parameters determine how a particular channel is turned on and off: The CONTROL pins, the OPERATION command and the value of the input voltage measured at the V_{INSNS} pin (V_{IN}). In all cases, V_{IN} must exceed VIN_ON in order to enable the device to respond to the CONTROL pins or OPERATION commands. When V_{IN} drops below VIN_OFF an immediate OFF or sequence off after TOFF_DELAY of all channels will result (See Mfr_track_en_chan*n*). Refer to the OPERATION section in the data sheet for a detailed description of the ON_OFF_CONFIG command.

Some examples of typical ON/OFF configurations are:

1. A DC/DC converter may be configured to turn on any time V_{IN} exceeds VIN_ON.
2. A DC/DC converter may be configured to turn on only when it receives an OPERATION command.
3. A DC/DC converter may be configured to turn on only via the CONTROL pin.
4. A DC/DC converter may be configured to turn on only when it receives an OPERATION command and the CONTROL pin is asserted.

ON Sequencing

The TON_DELAY command sets the amount of time that a channel will wait following the start of an ON sequence before its RUN pin will enable a DC/DC converter. Once the DC/DC converter has been enabled, the TON_RISE value determines the time at which the device soft-connects the DAC and servos the DC/DC converter output to the VOUT_COMMAND value. The TON_MAX_FAULT_LIMIT value determines the time at which the device checks for an undervoltage condition. If a TON_MAX_FAULT occurs, the channel can be configured to disable the DC/DC converter and propagate the fault to other channels using the bidirectional $\overline{FAULT}$ pins. Figure 21 shows a typical on-sequence using the CONTROL pin. Note that overvoltage faults are checked against the VOUT_OV_FAULT_LIMIT

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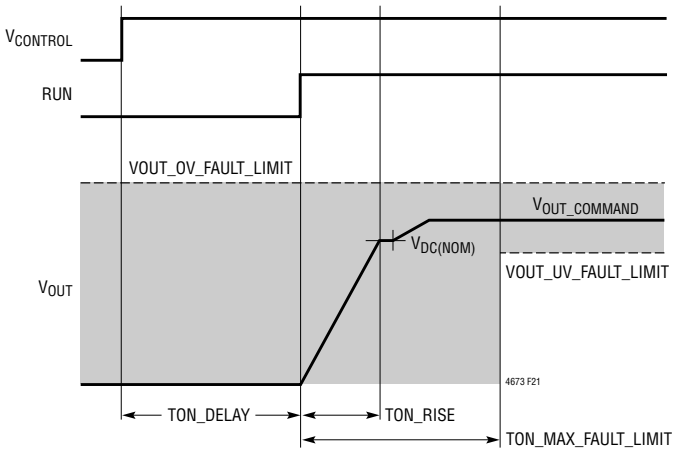

Figure 21. Typical ON Sequence Using Control Pin

value at all times the device is powered up and not in a reset state nor margining while ignoring OVs.

On State Operation

Once a channel has reached the ON state, the OPERATION command can be used to command the DC/DC converter's output to margin high, margin low, or return to a nominal output voltage indicated by VOUT_COMMAND. The user also has the option of configuring a channel to continuously trim the output of the DC/DC converter to the VOUT_COMMAND voltage, or the channel's V_{DACn} output can be placed in a high impedance state thus allowing the DC/DC converter output voltage to go to its nominal value, $V_{DCn(NOM)}$. Refer to the MFR_CONFIG_LTM4673 command for details on how to configure the output voltage servo.

Servo Modes

The ADC, DAC and internal processor comprise a digital servo loop that can be configured to operate in several useful modes. The servo target refers to the desired output voltage.

Continuous/non-continuous trim mode: MFR_CONFIG_LTM4673 b[7]. In continuous trim mode, the servo will update the DAC in a closed loop fashion each time it takes a V_{OUT} reading. The update rate is determined by the time it takes to step through the ADC MUX which is no more than t_{UPDATE_ADC}. See Electrical Characteristics table Note 5. In non-continuous trim mode, the servo will drive the DAC until the ADC measures the output voltage desired and then stop updating the DAC.

As part of continuous/noncontinuous trim mode, fast servo mode can be used to speed up large output transitions, such as margin commands, or ON events. To use, set Mfr_config_fast_servo_off = 0. When enabled, fast servo is started by a change to the target voltage or a new soft connect. The DAC is ramped one LSB every t_{S_VDAC} period until it is near the new target voltage, at which point slow servo mode is entered to avoid overshoot.

Non-continuous servo on warn mode: MFR_CONFIG_LTM4673 b[7] = 0, b[6] = 1. When in non-continuous mode, the LTM4673 will re-trim (re-servo) the output if the output drifts beyond the OV or UV warn limits.

DAC Modes

The DACs that drive the V_{DACn} pins can operate in several useful modes. See MFR_CONFIG_LTM4673.

- Soft-connect. Using the ADI patented soft-connect feature, the DAC output is driven to within 1 LSB of the voltage at the DC/DC's feedback node before connecting, to avoid introducing transients on the output. This mode is used when servoing the output voltage. During startup, the LTM4673 waits until TON_RISE has expired before connecting the DAC. This is the most common operating mode.
- Disconnected. DAC output is high Z.
- DAC manual with soft-connect. Non servo mode. The DAC soft connects to the feedback node. Soft-connect drives the DAC code to match the voltage at the feedback node. After connection, the DAC is moved by writing DAC codes to the MFR_DAC.
- DAC manual with hard connect. Non servo mode. The DAC hard connects to the feedback node using the current value in MFR_DAC. After connection, the DAC is moved by writing DAC codes to the MFR_DAC.

Margining

The LTM4673 margins and trims the output of a DC/DC converter by forcing a voltage across an external resistor connected between the DAC output and the feedback node or the trim pin. Preset limits for margining are stored in the VOUT_MARGIN_HIGH/LOW registers.

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Margining is actuated by writing the appropriate bits to the OPERATION register.

Margining requires the DAC to be connected. Margin requests that occur when the DAC is disconnected will be ignored.

OFF Sequencing

An off sequence is initiated using the CONTROL pin or the OPERATION command. The TOFF_DELAY value determines the amount of time that elapses from the beginning of the off sequence until each channel's V_{OUT_EN} pin is pulled low, thus disabling its DC/DC converter.

V_{OUT} OFF Threshold Voltage

The MFR_VOUT_DISCHARGE_THRESHOLD command register allows the user to specify the OFF threshold that the output voltage must decay below before the channel can enter/re-enter the ON state. The OFF threshold voltage is specified by multiplying MFR_VOUT_DISCHARGE_THRESHOLD and VOUT_COMMAND. In the event that an output voltage has not decayed below its OFF threshold before attempting to enter the ON state, the channel will continue to be held off, the appropriate bit is set in the STATUS_MFR_SPECIFIC register, and the $\overline{\text{ALERT}}$ pin will be asserted low. When the output voltage has decayed below its OFF threshold, the channel can enter the ON state.

Automatic Restart via MFR_RESTART_DELAY and CONTROL Pin

An automatic restart sequence can be initiated by driving the CONTROL pin to the off state for >10µs and then releasing it. The automatic restart brings all RUN pins low for a time period = MFR_RESTART_DELAY and then brings each RUN pin high according to their respective TON_DELAY. (see Figure 22). RUN pins can be mapped to any of the CONTROL pins by the MFR_CONFIG_LTM4673 command. This feature allows a host to restart the power in a controlled manner.

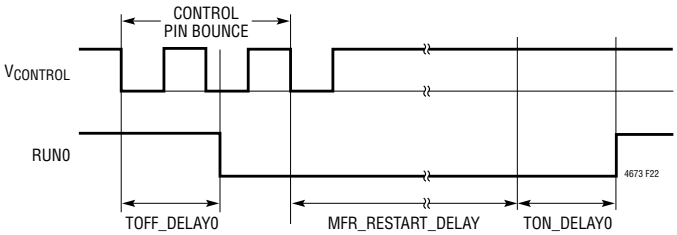

Figure 22. Off Sequence with Automatic Restart

FAULT MANAGEMENT

Output Overvoltage, Undervoltage, Overcurrent and Undercurrent Faults

The high-speed voltage supervisor OV and UV fault thresholds are configured using the VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT commands, respectively. The VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE commands determine the responses to OV/UV faults. In addition, the high-speed current supervisor OC and UC fault thresholds are configured using the IOUT_OC_FAULT_LIMIT and IOUT_UC_FAULT_LIMIT commands, respectively. The IOUT_OC_FAULT_RESPONSE and IOUT_UC_FAULT_RESPONSE commands determine the responses to OC/UC faults. Fault responses can range from disabling the DC/DC converter immediately, waiting to see if the fault condition persists for some interval before disabling the DC/DC converter, or allowing the DC/DC converter to continue operating in spite of the fault. If a DC/DC converter is disabled, the LTM4673 can be configured to retry one to six times, retry continuously without limitation, or latch-off. The retry interval is specified using the MFR_RETRY_DELAY command. Latched faults are reset by toggling the CONTROL pin, using the OPERATION command, or removing and reapplying the bias voltage to the V_{INSNS} pin. All fault and warning conditions result in the $\overline{\text{ALERT}}$ pin being asserted low and the corresponding bits being set in the status registers. The CLEAR_FAULTS command resets the contents of the status registers and de-asserts the $\overline{\text{ALERT}}$ output.

Output Overvoltage, Undervoltage, and Overcurrent Warnings

OV, UV, and OC warning thresholds are processed by the LTM4673's ADC. These thresholds are set by the VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, and

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IOUT_OC_WARN_LIMIT commands, respectively. Note that there is no I_{OUT} UC warning threshold. If a warning occurs, the corresponding bits are set in the status registers and the $\overline{ALERT}$ output is asserted low. Note that a warning will never cause a V_{OUT_EN} output pin to disable a DC/DC converter.

Configuring the AUX$\overline{FAULT}$ Output

The AUX$\overline{FAULT}$ output may be used to indicate an output OV, OC, or UC fault. Use the MFR_CONFIG2_LTM4673 and MFR_CONFIG3_LTM4673 registers to configure the AUX$\overline{FAULT}$ pin to assert low in response to VOUT_OV, IOUT_OC or IOUT_UC fault conditions. The AUX$\overline{FAULT}$ output will stop pulling low when the LTM4673 is commanded to re-enter the ON state following a faulted-off condition.

A charge-pumped 5µA pull-up to 12V is also available on the AUX$\overline{FAULT}$ output. Refer to the MFR_CONFIG_ALL_LTM4673 register description in the PMBUS COMMAND DESCRIPTION section for more information.

MULTICHANNEL PARALLEL OPERATION

For the application that demand more than 12A of output current, the LTM4673 multiple regulator channels can be easily paralleled to run out of phase to provide more output current without increasing input and output voltage ripples.

For the 12A channels (CH0, CH3), each channel has its own MODE/CLKIN and CLKOUT pin. The CLKOUT signal can be connected to the CLKIN pin of the following stage to line up both frequency and the phase of the entire system. Tying the PHMODE pin to $INTV_{CC}$, SGND or floating the pin generates a phase difference between the clock applied on the MODE/CLKIN pin and CLKOUT of 180° degrees, 120° degrees, or 90° degrees respectively, which corresponds to 2-phase, 3-phase, or 4-phase operation.

For the 5A channels (CH1, CH2), a preset built-in 180° phase difference between channel 1 and channel 2. MODE/CLKIN12 allows both channels to be synchronized to an external clock or the CLKOUT signal from any of the 12A channels.

Figure 23 shows a 2 + 2 channel parallel concept schematic for clock phasing.

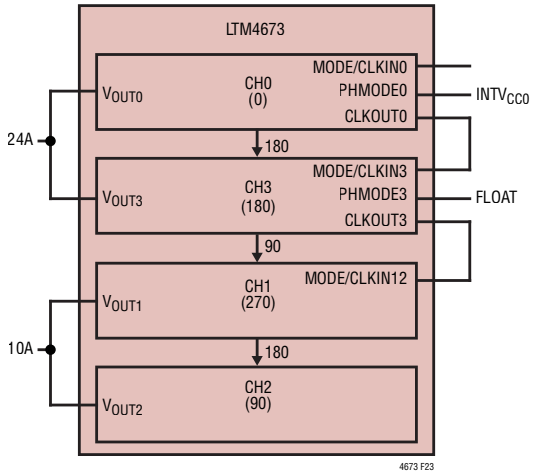

Figure 23. 2 + 2 Channel Parallel Concept Schematic

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when each pair of channels are paralleled to achieve two dual-phase designs.

The LTM4673 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie V_{OSNS}^+, V_{OSNS}^-, TRACK/SS, FB and COMP pins of each paralleling channel together. A single CONTROL*n* pin can be used to enable paralleled channels. See MFR_CONFIG_LTM4673 for more details. Figure 54 shows an example of parallel operation and pin connection.

INPUT RMS RIPPLE CURRENT CANCELLATION

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 24 shows this graph.

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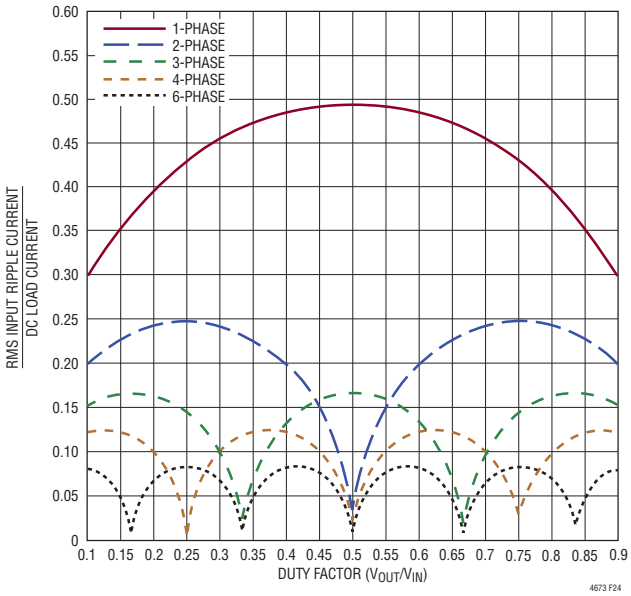

Figure 24. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

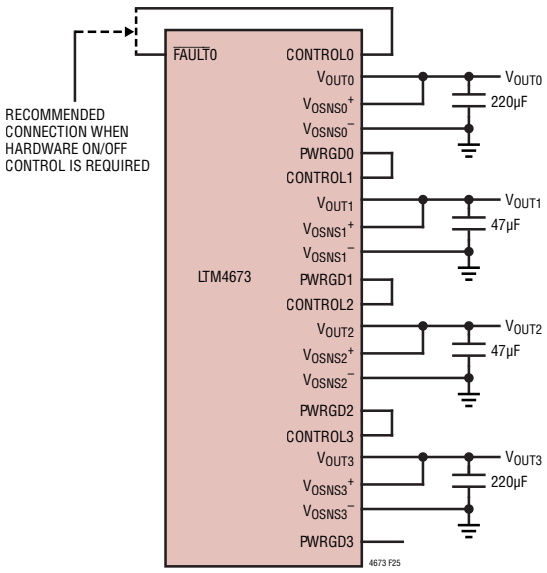

Figure 25. LTM4673 Configured to Cascade Sequence ON and Time-Base Sequence OFF

Cascade Sequence ON with Time-Based Sequence OFF

Cascade sequence ON allows a main channel to sequence on a series of subordinate channels by connecting each channel's power good output to the control pin of the next channel in the chain. Please note that the power good signal is that of the power supply and not derived from the LTM4673's internal power good processing. Power good based cascade sequence OFF is not supported, OFF sequencing must be managed using immediate or time based sequence OFF. See also Tracking Based Sequencing section.

Cascade sequence ON is illustrated in Figure 25. For each subordinate channel Mfr_config_cascade_on is asserted high and the associated control input is connected to the power good output of the previous power supply. In this configuration each subordinate channel's startup is delayed until the previous channel has powered up.

Cascade sequence OFF is not directly supported. Options for reversing the sequence when turning the channels off include:

- Using the OPERATION command to turn off all the channels with an appropriate off delay.
- Using the FAULT pin to bring all the channels down immediately or in sequence with an appropriate off delay.

When asserted, Mfr_config_cascade_on enables a subordinate channel to honor fault retries even when its control pin is low. Additionally, if the system has faulted off after zero or a finite number of retries, an OPERATION command may be used to turn all cascade channels off then on to clear the faulted off state when the subordinate's control pin is low. For this reason we refer to the control pin as being redefined as a sequence pin.

The waveform of Figure 26 illustrates cascade sequence ON and time based sequence OFF using the configuration illustrated in Figure 25. In this example the $\overline{\text{FAULT0}}$ pin is used as a broadcast off signal. Turning the system off with the $\overline{\text{FAULT0}}$ requires all subordinate channels to be configured with Mfr_faultb0_response_chan*n* asserted high. After the system is turned off, the LTM4673 will assert $\overline{\text{ALERT}}$ with all subordinate channels indicating a Status_mfr_fault0_in event.

Output Voltage Tracking

Output voltage tracking of LTM4673 can be programmed externally using the TRACK/SS pin of each regulator channel with appropriate sequence of control signals. See

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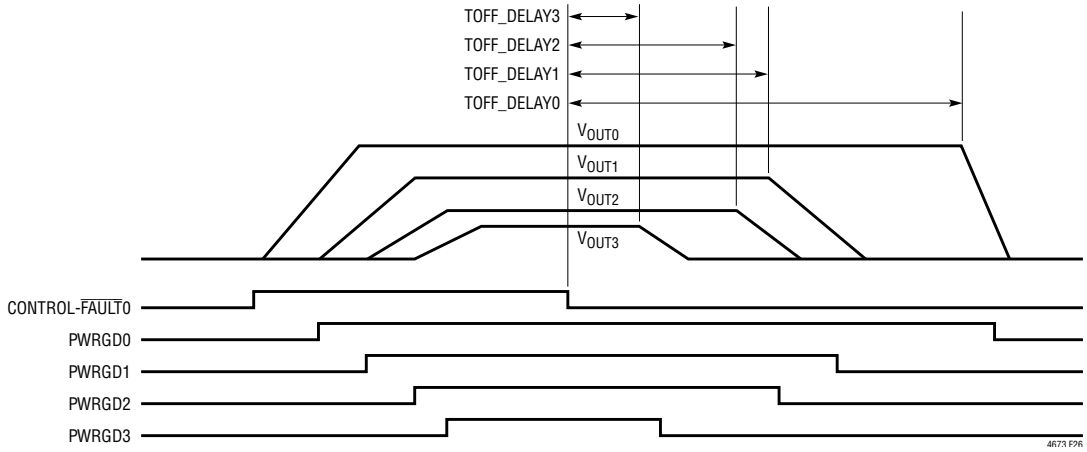

Figure 26. Cascade Sequence ON with Time Based Sequence Down on $\overline{FAULT0}$

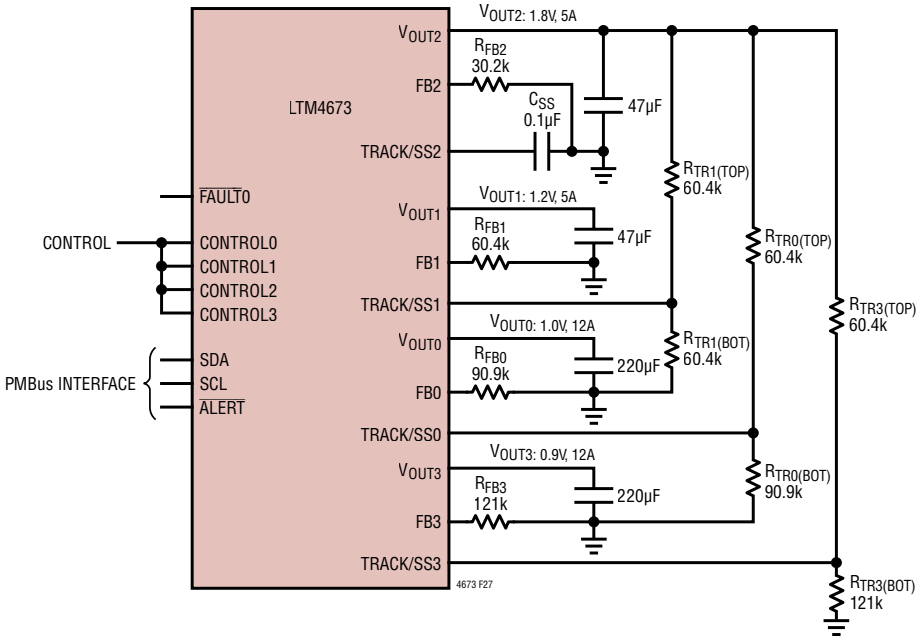

Figure 27. LTM4673 Configured to Control, Supervise and Monitor All Four Channels with Output Voltage Tracking

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Figure 27. Channels that track a main channel must be enabled before the main channel comes up and disabled after the main channel comes down. Enabling the subordinate channels when the main is down requires supervisors monitoring the subordinates to disable UV detection. Subordinate UC detection must also be disabled when the subordinates are tracking the main down to prevent false UC events. All channels configured for tracking must track off together in response to a fault on any channel or any other condition that can bring one or more of the channels down. Prematurely disabling a subordinate channel via its CONTROL pin may cause that channel to shut down out of sequence (see Figure 30).

An important feature of the LTM4673 is the ability to control, monitor and supervise all subordinate channels that are configured to track a main channel on and off.

The LTM4673 supports the following tracking features:

- Track channels on and off without issuing false UV/UC events when the subordinate channels are tracking up or down.
- Track all channels down in response to a fault from a subordinate or main.
- Track all channels down when V_{INSNS} drops below VIN_OFF, share clock is held low or RESTORE_USER_ALL is issued.
- Ability to reconfigure selected channels that are part of a tracking group to sequence up after the group has tracked up or sequence down before the group has tracked down.

The LTM4673 supports tracking through the coordinated programing of Ton_delay, Ton_rise,Toff_delay and Mfr_track_en_chan*n*. The main channel must be configured to turn on after all the subordinate channels have turned on and to turn off before all the subordinate channels turn off. Subordinates that are enabled before the main will remain off until the tracking pin allows them to turn on. Subordinates will be turned off via the tracking pin even though their run pin is still asserted. Ton_rise must be extended on the subordinates so that it ends relative to the rise of the TRACK pin.

When Mfr_track_en_chan*n* is enabled the channel is reconfigured to:

- Sequence down on fault, VIN_OFF, SHARECLK low or RESTORE_USER_ALL.
- Ignore UV and UC during TOFF_DELAY. Note that ignoring UV and UC during TON_RISE and TON_MAX_FAULT always happens regardless of how this bit is set.

The following example illustrates configuring an LTM4673 with one main channel and three subordinates.

Main Channel 2

TON_DELAY = Ton_delay_main

TON_RISE = Ton_rise_main

TOFF_DELAY = Toff_delay_main

MFR_TRACK_EN_CHAN 2 = 0

Subordinate Channel 0, 1, 3

TON_DELAY = Ton_delay_subordinate

TON_RISE = Ton_rise_main + Ton_rise_subordinate

TOFF_DELAY = Toff_delay_main + T_off_delay_subordinate

MFR_TRACK_EN_CHAN 0, 1, 3 = 1

Where:

Ton_delay_main > Ton_delay_subordinate

Toff_delay_subordinate > time for main channel to fall.

The system response to a control pin toggle is illustrated in Figure 28.

The system response to a UV fault on a subordinate channel is illustrated in Figure 29.

Since the subordinate regulator's TRACK/SS is connected to the main's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the subordinate output voltage when TRACK/SS voltage is below 0.6V, the subordinate output voltage and the main output voltage should satisfy Equation 12 during the start-up.

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}} \quad (12)$$

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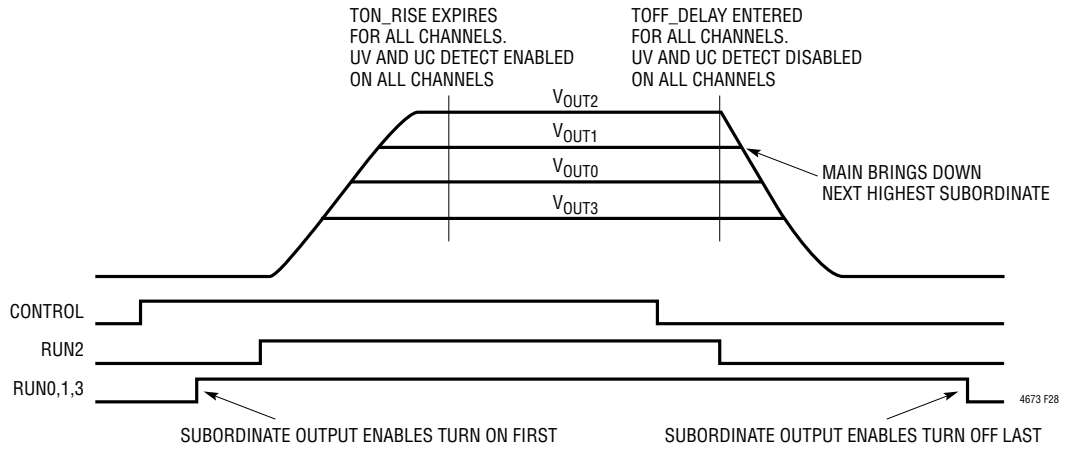

Figure 28. Control Pin Tracking All Supplies Up And Down

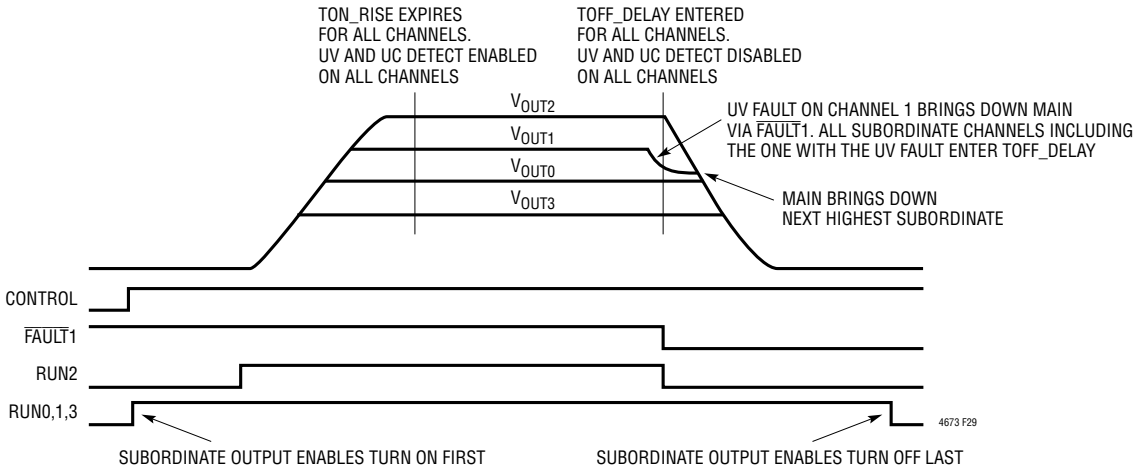

Figure 29. Fault on Channel 1 Tracking All Supplies Down

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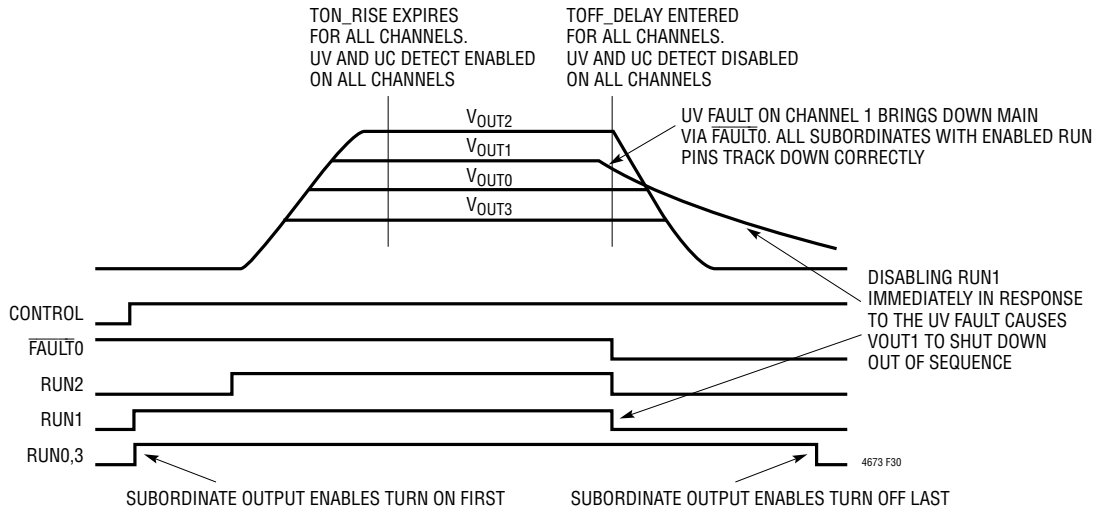

Figure 30. Improperly Configured Fault Response on Faulting Channel Disrupts Tracking

The $R_{FB(SL)}$ is the feedback resistor and the $RTR_{(TOP)}$/$RTR_{(BOT)}$ is the resistor divider on the TRACK/SS pin of the subordinate regulator, as shown in Figure 27.

Following Equation 12, the main's output slew rate (MR) and the subordinate's output slew rate (SR) in Volts/Time is determined by Equation 13.

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}} \quad (13)$$

For the coincident output tracking shown in Figure 28, the main's output slew rate (MR) is the same as the subordinate's output slew rate (SR), Equation 14.

$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(TOP)}}{R_{TR(TOP)} + R_{TR(BOT)}} \quad (14)$$

From Equation 14, we could easily find out that, in the coincident tracking, the subordinate regulator's TRACK/SS pin resistor divider is always the same as its feedback divider.

For the example shown in Figure 27, $R_{TR0(TOP)} = R_{TR1(TOP)} = R_{TR3(TOP)}$ = 60.4k and $R_{TR0(BOT)}$ = 90.9k, $R_{TR1(BOT)}$ = 60.4k and $R_{TR3(BOT)}$ = 121k are good combinations for coincident tracking for $V_{OUT2(MA)}$ = 1.8V, $V_{OUT0(SL)}$ = 1.0V, $V_{OUT1(SL)}$ = 1.2V and $V_{OUT3(SL)}$ = 0.9V.

The TRACK1 and TRACK2 pins have a 1.5µA current source on and the TRACK0 and TRACK3 pins have a 6µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from Equation 14 can be used. For example, where 60.4k and 121k are used for channel 3's resistive divider, 6.04k and 12.1k can be used to reduce the TRACK pin offset to a negligible value.

Multichannel Fault Management

Multichannel fault management is handled using the bidirectional $\overline{FAULT}$ pins. Figure 31 illustrates the connections between channels and the $\overline{FAULT}$ pins.

- The MFR_FAULTB*n*_PROPAGATE command acts like a programmable switch that allows faulted_off conditions from a particular channel (PAGE) to propagate to either $\overline{FAULT}$ output. The MFR_FAULTB*n*_RESPONSE command controls similar switches on the inputs to each channel that allow any channel to shut down in response to any combination of the $\overline{FAULT}$ pins. Channels responding to a $\overline{FAULT}$ pin pulling low will

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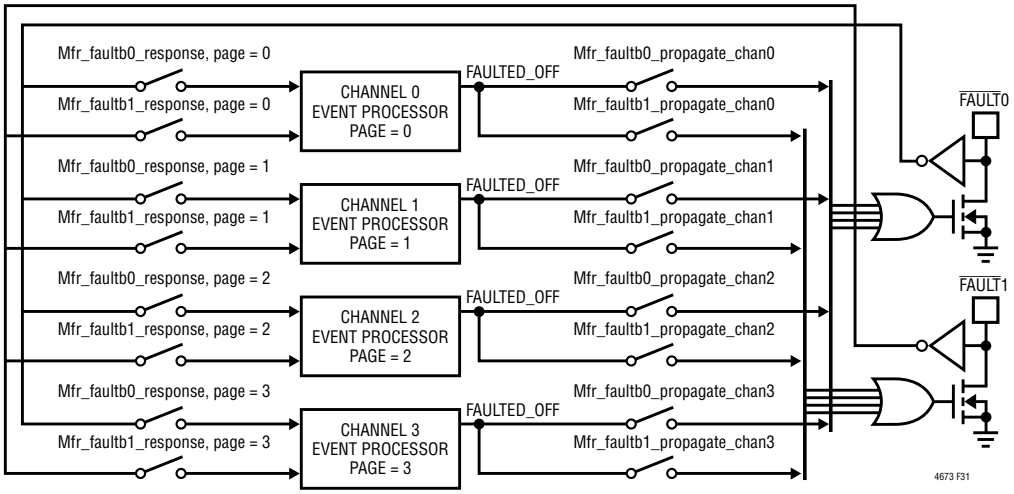

Figure 31. Channel Fault Management Block Diagram

attempt a new start sequence when the $\overline{\text{FAULT}}$ pin in question is released by the faulted channel.

- A $\overline{\text{FAULT}}$ pin can also be asserted low by an external driver in order to initiate an immediate off-sequence after a 10µs deglitch delay.

INTERCONNECT BETWEEN MULTIPLE ANALOG DEVICES POWER MANAGERS

Figure 32 shows how to interconnect the pins in a typical multi-LTM4673 array.

- All V_{INSNS} lines should be tied together in a star type connection at the point where V_{IN} is to be sensed. This will minimize timing errors for the case where the ON_OFF_CONFIG is configured to start the LTM4673 based on V_{IN} and ignore the CONTROL line and the OPERATION command. In multi-part applications that are sensitive to timing differences, it is recommended that the Vin_share_enable bit of the MFR_CONFIG_ALL_LTM4673 register be set high in order to allow SHARECLK to synchronize ON/OFF sequencing in response to the VIN_ON and VIN_OFF thresholds.
- Connecting all AUX$\overline{\text{FAULT}}$ lines together will allow selected faults on any DC/DC converter's output in the array to shut off a common input switch.
- $\overline{\text{ALERT}}$ is typically one line in an array of PMBus converters. The LTM4673 allows a rich combination of faults and warnings to be propagated to the $\overline{\text{ALERT}}$ pin.
- WDI/$\overline{\text{RESET}}$ can be used to put the LTM4673 in the power-on reset state. Pull WDI/$\overline{\text{RESET}}$ low for at least $t_{\overline{\text{RESET}}}$ to enter this state.
- The $\overline{\text{FAULT}}$ lines can be connected together to create fault dependencies. Figure 32 shows a configuration where a fault on any $\overline{\text{FAULT}}$ will pull all others low. This is useful for arrays where it is desired to abort a startup sequence in the event any channel does not come up (see Figure 33).
- PWRGD reflects the status of the outputs that are mapped to it by the MFR_PWRGD_EN command. Figure 32 shows all the PWRGD pins connected together, but any combination may be used.

Connecting the DC1613 USB to I²C/SMBus/PMBus Controller to the LTM4673 in System

The DC1613 USB to I²C/SMBus/PMBus Controller can be interfaced to the LTM4673s on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay software, provides a powerful way to debug an entire power system. Failures are quickly diagnosed using telemetry, fault status

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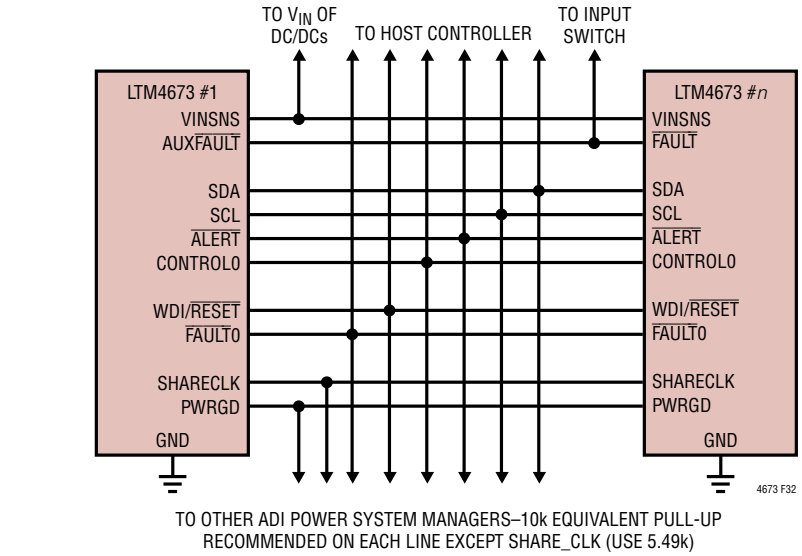

Figure 32. Typical Connections Between Multiple Analog Devices Power System Managers

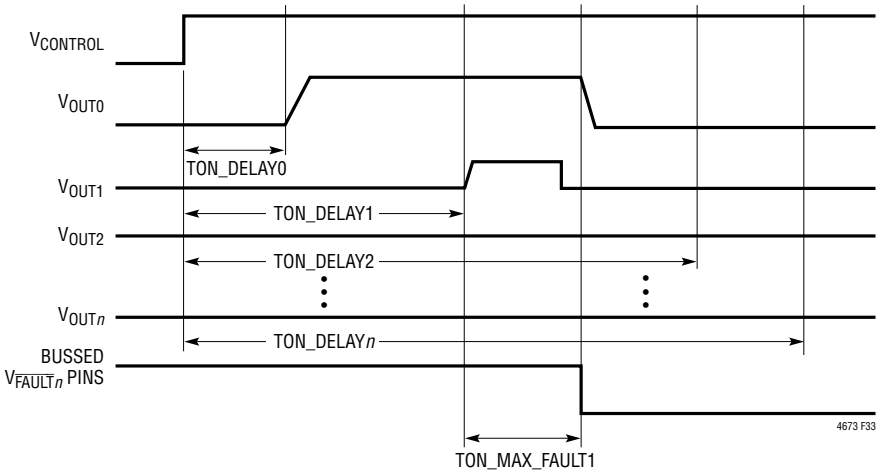

Figure 33. Aborted On-Sequence Due to Channel 1 Short

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registers and the fault log. The final configuration can be quickly developed and stored to the LTM4673's EEPROM.

Figure 34 and Figure 35 illustrate application schematics for powering, programming and communicating with one or more LTM4673's via the ADI I^2C/SMBus/PMBus controller regardless of whether or not system power is present.

Figure 34 shows the recommended schematic to use when the LTM4673 is powered by the system intermediate bus through its V_{IN_D} pin.

Figure 35 shows the recommended schematic to use when the LTM4673 is powered by the system 3.3V through its V_{DD33} and V_{IN_D} pins. The LTC4412 ideal OR'ing circuit allows either the controller or system to power the LTM4673.

Because of the controller's limited current sourcing capability, only the LTM4673s, their associated pull-up resistors and the I^2C/SMBus pull-up resistors should be powered from the ORed 3.3V supply. In addition, any device sharing I^2C/SMBus bus connections with the LTM4673 should not have body diodes between the SDA/SCL pins

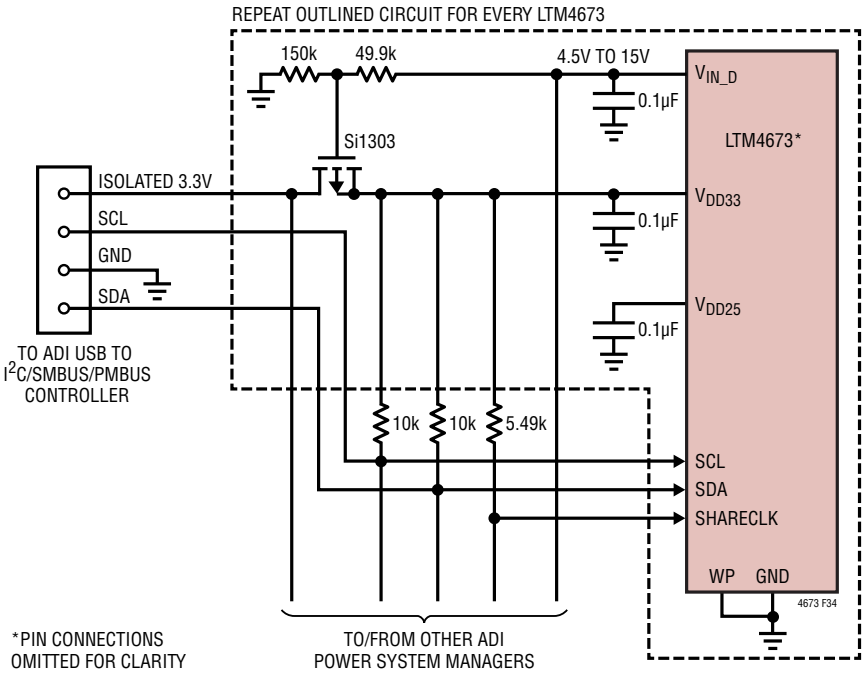

Figure 34. LTM4673 Connections When V_{IN_D} Is Used

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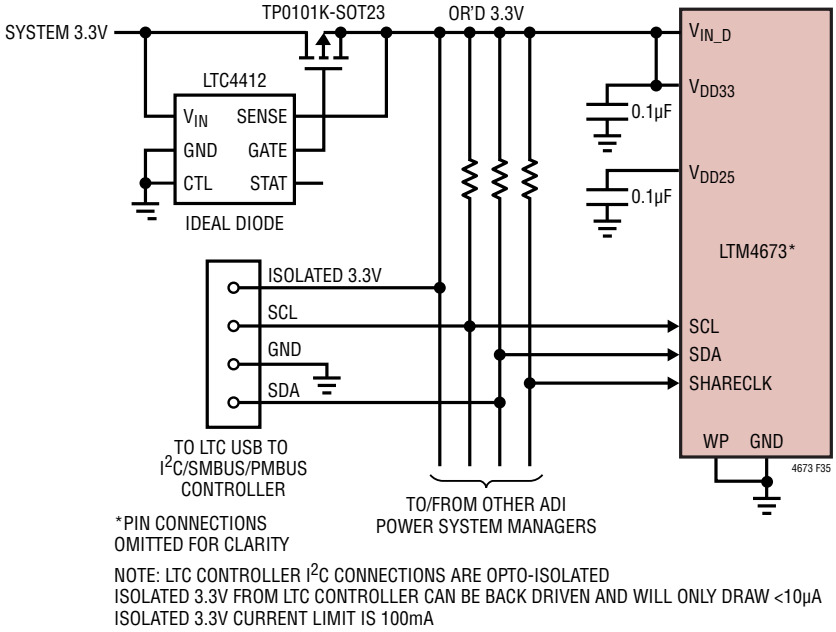

Figure 35. Connections when LTM4673 Is Powered Directly from 3.3V

and its V_{DD} node because this will interfere with bus communication in the absence of system power.

The ADI controller's I^2C/SMBus connections are opto-isolated from the PC's USB. The 3.3V from the controller and the LTM4673's V_{DD33} pin can be paralleled because the ADI LDOs that generate these voltages can be back driven and draw <10µA. The controller's 3.3V current limit is 100mA.

LTpowerPlay: AN INTERACTIVE GUI FOR POWER MANAGERS

LTpowerPlay is a powerful Windows based development environment that supports Analog Devices power manager ICs with EEPROM, including the LTM4673. The software supports a variety of different tasks. You can use LTpowerPlay to evaluate Linear Technology ICs by connecting to a demo board system. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build a multi-chip configuration file that can be saved and re-loaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program the power management scheme in a system.

LTpowerPlay utilizes Analog Devices DC1613 USB-to-I^2C/SMBus/PMBus Controller to communicate with one of many potential targets including the DC2022 demo board set, the DC1508 socketed programming board, or a customer target system. The software also provides an automatic update feature to keep the software current with the latest set of device drivers and documentation. A great deal of context sensitive help is available within LTpowerPlay along with several tutorial demos. Complete information is available here.

Four-Step Resistor Selection Procedure for Resistors between V_{DAC} and V_{FB} Pins

The following four-step procedure should be used to calculate the resistor values required for the application circuit shown in Figure 53. Alternatively, the LTpowerCAD software tool can be used to calculate R_{DAC} values.

1. Determine the bottom V_{FB} resistor value.

   The top V_{FB} feedback resistor is within the module and its resistance is 60.4k, the bottom V_{FB} resistor can be determined by the nominal output voltage (Equation 15).

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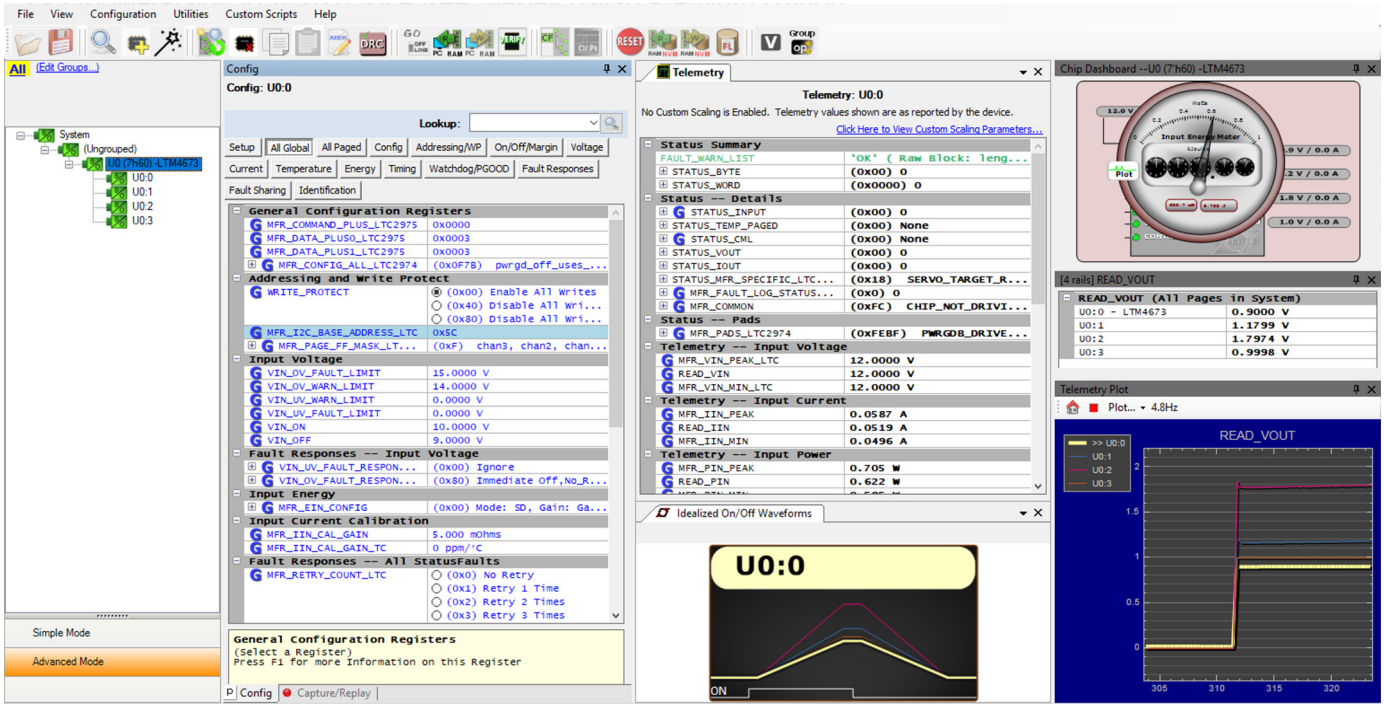

Figure 36. LTpowerPlay Snapshot

$$R_{FB(BOT)} = \frac{60.4k \bullet V_{FB}}{V_{DC(NOM)} - I_{FB} \bullet 60.4k - V_{FB}} \quad (15)$$

$V_{DC(NOM)}$ is the output voltage of the DC/DC converter when the LTM4673's V_{DAC0} pin is in a high impedance state. $R_{FB(BOT)}$ is a function of $V_{DC(NOM)}$, the voltage at the feedback node (V_{FB}) when the loop is in regulation, and the feedback node's input current (I_{FB}).

Using Channel 0 as an example, $V_{DC(NOM)}$ is 1.0V, I_{FB} = 50nA, V_{FB} = 0.6V, $R_{FB(BOT)}$ can be calculated as 90.9k

2. Solve for the value of R_{VDAC} that yields the maximum required DC/DC converter output voltage $V_{DC(MAX)}$.

   When V_{DAC0} is at 0V, the output of the DC/DC converter is at its maximum voltage (Equation 16).

$$R_{DAC} \leq \frac{60.4k \bullet V_{FB}}{V_{DC(MAX)} - V_{DC(NOM)}} \quad (16)$$

   For Channel 0, $V_{DC(NOM)}$ is 1.0V, set $V_{DC(MAX)}$ at 1.05V, V_{FB} = 0.6V, R_{DAC0} should not be greater than 715k. Let us set R_{DAC0} = 715k.

3. Solve for the minimum value of V_{DAC0} that's needed to yield the minimum required DC/DC converter output voltage $V_{DC(MIN)}$.

   The DAC has two full-scale settings, 1.38V and 2.65V. In order to select the appropriate full-scale setting, calculate the minimum required V_{FS_VDAC} output voltage (Equation 17).

$$V_{FS\_VDAC} > \left(V_{DC(NOM)} - V_{DC(MIN)}\right) \bullet \frac{R_{DAC}}{60.4k} + V_{FB} \quad (17)$$

   For Channel 0, $V_{DC(NOM)}$ is 1.0V, set $V_{DC(MIN)}$ at 0.95V, V_{FB} = 0.6V, V_{FS_VDAC0} should not be greater than 1.4V. Set V_{FS_VDAC} = 1.38V (MFR_CONFIG_LTM4673[1]=0)

4. Recalculate the minimum, nominal, and maximum DC/DC converter output voltages and the resulting margining resolution (Equation 18 to Equation 21).

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$$V_{DC(NOM)} = V_{FB} \bullet \left(1 + \frac{60.4k}{R_{FB(BOT)}}\right) + I_{FB} \bullet 60.4k \quad (18)$$

$$V_{DC(MIN)} = V_{DC(NOM)} - \frac{60.4k}{R_{DAC}} \bullet \left(V_{FS\_VDAC} - V_{FB}\right) \quad (19)$$

$$V_{DC(MAX)} = V_{DC(NOM)} + \frac{60.4k}{R_{DAC}} \bullet V_{FB} \quad (20)$$

$$V_{RES} = \frac{\frac{60.4k}{R_{DAC}} \bullet V_{FS\_VDAC}}{1023} \text{ V/DAC LSB} \quad (21)$$

For Channel 0, V_{FB} = 0.6V, I_{FB} = 50nA, $R_{FB(BOT)}$ = 90.9k, V_{FS_VDAC} = 1.38V. The nominal, minimum and maximum output voltage can be calculated as follows: $V_{DC(NOM)}$ = 1.0V, $V_{DC(MIN)}$ = 0.95V, $V_{DC(MAX)}$ = 1.05V. V_{RES} = 0.114mV/DAS LSB.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients in found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below.

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product, is determined with all of the component dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

A graphical representation of the aforementioned thermal resistances is given in Figure 37; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

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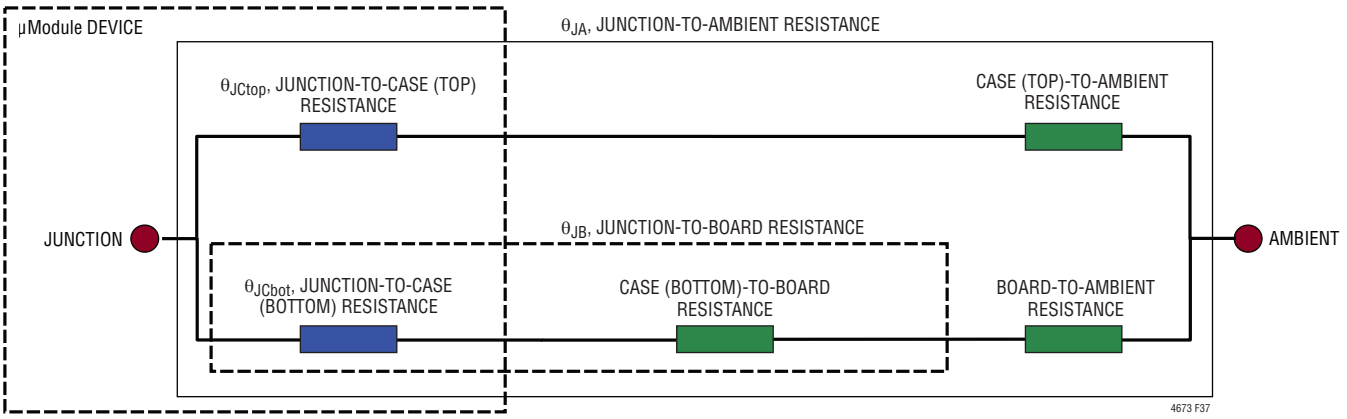

Figure 37. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED 51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed and correlated to the µModule model, then the θ_{JA} correlates quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This θ_{JA} value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1.0V, 1.5V, 3.3V and 5V power loss curves in Figure 38 to Figure 41 can be used in coordination with the load current derating curves in Figure 42 to Figure 51 for calculating an approximate θ_{JA} thermal resistance for the LTM4673 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the ambient temperature. These approximate

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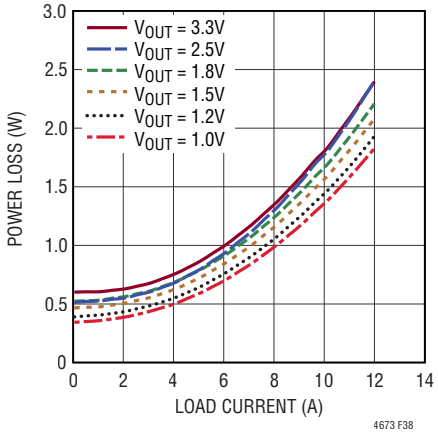

Figure 38. $5V_{IN}$ Output Power Loss for Channel 0 and 3

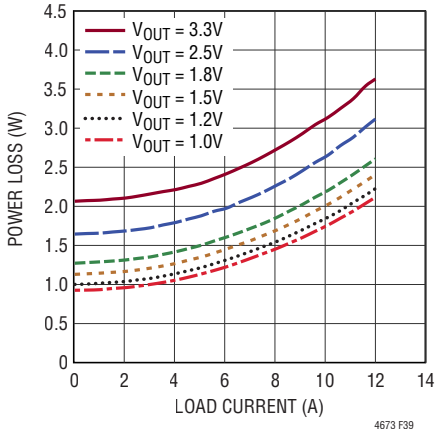

Figure 39. $12V_{IN}$ Output Power Loss for Channel 0 and 3

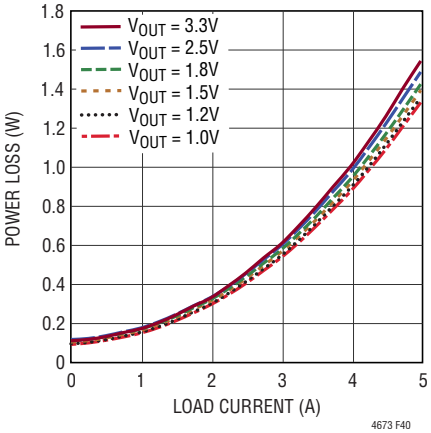

Figure 40. $5V_{IN}$ Output Power Loss for Channel 1 and 2

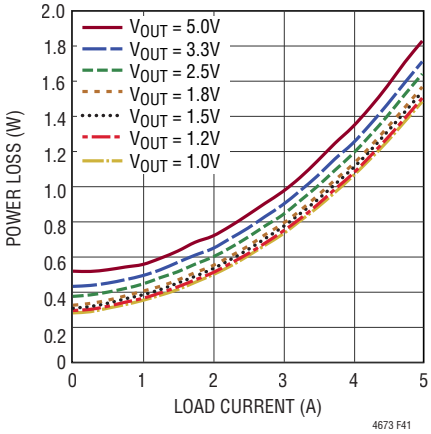

Figure 41. $12V_{IN}$ Output Power Loss for Channel 1 and 2

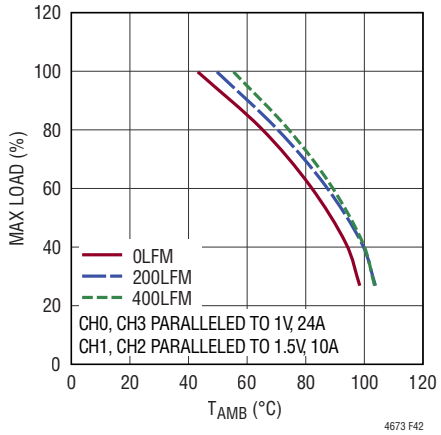

Figure 42. $12V_{IN}$ Derating Curve, No Heat Sink

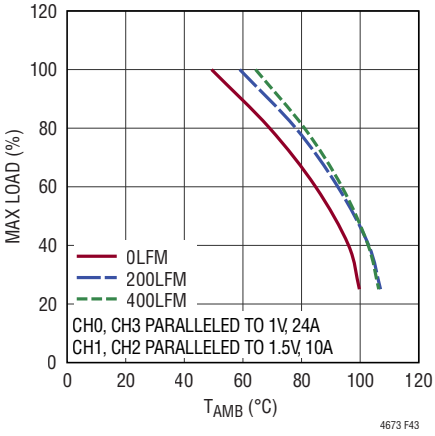

Figure 43. $12V_{IN}$ Derating Curve, with Heat Sink

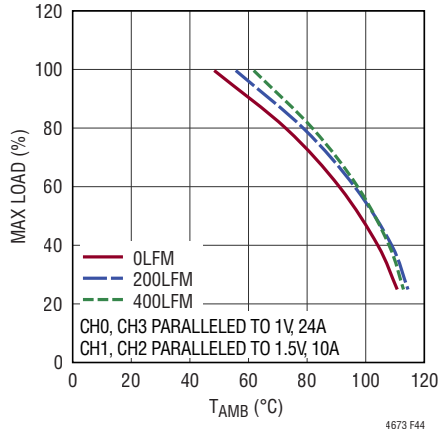

Figure 44. $5V_{IN}$ Derating Curve, No Heat Sink

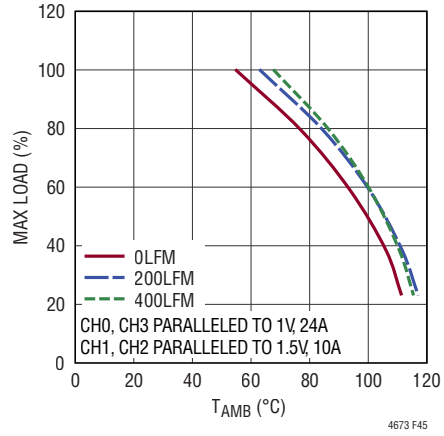

Figure 45. $5V_{IN}$ Derating Curve, with Heat Sink

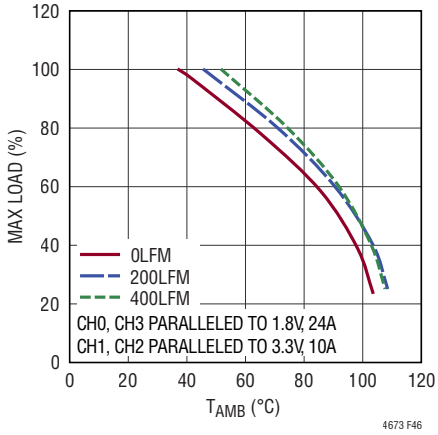

Figure 46. $5V_{IN}$ Derating Curve, No Heat Sink

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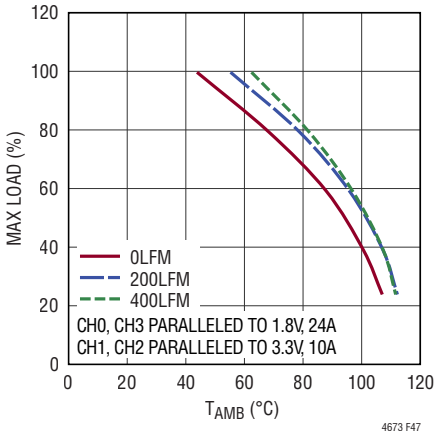

Figure 47. $5V_{IN}$ Derating Curve, No Heat Sink

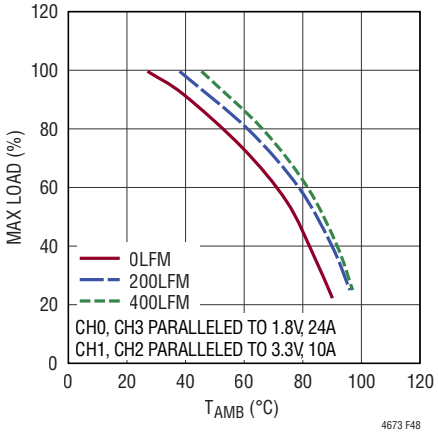

Figure 48. $12V_{IN}$ Derating Curve, No Heat Sink

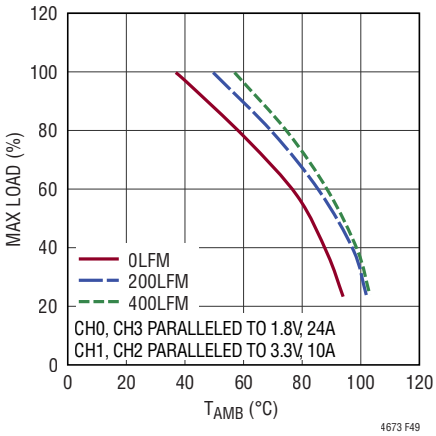

Figure 49. $12V_{IN}$ Derating Curve, with Heat Sink

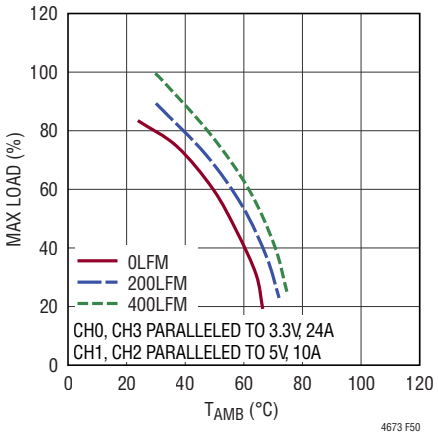

Figure 50. $12V_{IN}$ Derating Curve, No Heat Sink

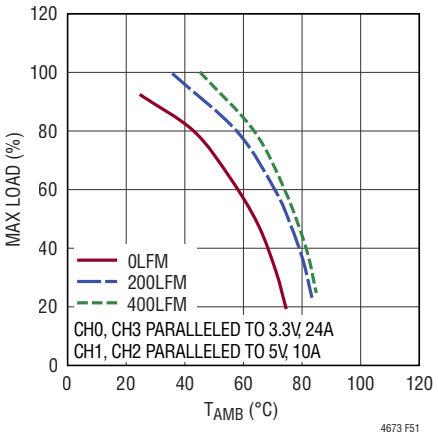

Figure 51. $12V_{IN}$ Derating Curve, with Heat Sink

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factors are: 1 for 40°C; 1.05 for 50°C; 1.1 for 60°C; 1.15 for 70°C; 1.2 for 80°C; 1.25 for 90°C; 1.3 for 100°C; 1.35 for 110°C and 1.4 for 120°C. The derating curves are plotted with the output current starting at 100% load for each paralleled output and the ambient temperature at 40°C. The output voltages are 1V, and 1.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 42, the load current is derated to ~14A for paralleled channels 0 and 3 and ~6A for paralleled channels 1 and 2 at ~80°C with no air or heat sink. The power loss for the 12V to 1.0V and 1.5V at this output load condition is about 5W. At room temperature, Channel 0 and 3 each have an estimated 1.3W loss at 7A according the $12V_{IN}$ to $1.0V_{OUT}$ curve in Figure 39. Channel 1 and 2 each have an estimated 0.8W loss at 3A according to the $12V_{IN}$ to $1.5V_{OUT}$ curve in Figure 41. The total room temperature loss is 4.2W. This 4.2W temperature loss is multiplied by 1.2, the multiplying factor at 80°C ambient, bringing power loss at this ambient temperature to 5W. If the 80°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 40°C divided by 5W equals 8°C/W θ_{JA} thermal resistance. Table 3 specifies a 8°C/W value which matches the calculation estimate. Table 3 through Table 5 provide equivalent thermal resistances for combinations of 1.0V, 1.5V 1.8V, 3.3V and 5V outputs with and without airflow and heat sinking. The derived thermal resistances in Table 3 through Table 5 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two-ounce copper for the two outer layers and one-ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The BGA heat sinks are listed in Table 4.

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Table 3. $V_{OUT0} = V_{OUT3} = 1V$, $V_{OUT1} = V_{OUT2} = 1.5V$

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figure 42, Figure 43	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	0	None	8
Figure 42, Figure 43	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	200	None	7
Figure 42, Figure 43	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	400	None	6.5
Figure 44, Figure 45	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	0	BGA Heat Sink	7
Figure 44, Figure 45	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	200	BGA Heat Sink	6
Figure 44, Figure 45	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	400	BGA Heat Sink	5.5

Table 4. $V_{OUT0} = V_{OUT3} = 1.8V$, $V_{OUT1} = V_{OUT2} = 3.3V$

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figure 46, Figure 47	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	0	None	8
Figure 46, Figure 47	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	200	None	7
Figure 46, Figure 47	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	400	None	6.5
Figure 48, Figure 49	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	0	BGA Heat Sink	7
Figure 48, Figure 49	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	200	BGA Heat Sink	6
Figure 48, Figure 49	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	400	BGA Heat Sink	5.5

Table 5. $V_{OUT0} = V_{OUT3} = 3.3V$, $V_{OUT1} = V_{OUT2} = 5V$

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figure 50	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	0	None	9
Figure 50	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	200	None	8
Figure 50	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	400	None	7
Figure 51	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	0	BGA Heat Sink	7.5
Figure 51	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	200	BGA Heat Sink	6
Figure 51	5, 12	Figure 38, Figure 39, Figure 40, Figure 41	400	BGA Heat Sink	5.5

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Table 6. Output Voltage Response vs Component Matrix (Refer to Figure 53) 0 to 25% Load Step Typical Measured Values

C_{IN} (CERAMIC)			C_{OUT} (CERAMIC)			C_{OUT} (BULK)		
VENDOR	VALUE	PART NUMBER	VENDOR	VALUE	PART NUMBER	VENDOR	VALUE	PART NUMBER
Murata	22µF, X5R, 25V, 1206	GRM31CR61E226KE15L	Murata	100µF, 6.3V, X5R, 1206	GRM31CR60J107KE39L	PANASONIC	330µF, 6.3V, 10mΩ	6TPF330M9L
			Murata	47µF	GRM31CR60J476ME19L			

V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{IN} (BULK)	C_{OUT1} (CERAMIC) (µF)	C_{OUT2} (BULK) (µF)	C_{TH} (pF)	R_{TH} (kΩ)	CFF (pF)	V_{IN} (V)	P-P DERIVATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (kΩ)
CH0 and CH3 Transient Response													
1	22 ×4	100 ×2	100 ×3	NA	2200	5	33	12	91.0	30	3	10	90.9
1	22 ×4	100 ×2	100	330	1000	8	NA	12	83	30	3	10	90.9
1.2	22 ×4	100 ×2	100 ×3	NA	2200	5	33	12	94.4	30	3	10	60.4
1.2	22 ×4	100 ×2	100	330	1000	8	NONE	12	89	30	3	10	60.4
1.5	22 ×4	100 ×2	100 ×3	NA	2200	5	33	12	103.8	30	3	10	40.2
1.5	22 ×4	100 ×2	100	330	1000	8	NONE	12	103.8	30	3	10	40.2
1.8	22 ×4	100 ×2	100 ×3	NA	2200	5	33	12	117.8	40	3	10	30.1
1.8	22 ×4	100 ×2	100	330	1000	8	NONE	12	114.5	40	3	10	30.1
2.5	22 ×4	100 ×2	100 ×3	NA	2200	5	33	12	154.0	40	3	10	19.1
2.5	22 ×4	100 ×2	100	330	1000	8	NONE	12	145.3	40	3	10	19.1
3.3	22 ×4	100 ×2	100 ×3	NA	2200	5	33	12	199.0	40	3	10	13.3
3.3	22 ×4	100 ×2	100	330	1000	8	NONE	12	189	40	3	10	13.3
CH1 and CH2 Transient Response													
1	22 ×4	100 ×2	47 ×2 + 10	NA	Internal	Internal	33	12	66.3	60	1.25	10	90.9
1.2	22 ×4	100 ×2	47 ×2 + 10	NA	Internal	Internal	33	12	69.6	60	1.25	10	60.4
1.5	22 ×4	100 ×2	47 ×2 + 10	NA	Internal	Internal	33	12	73.6	60	1.25	10	40.2
1.8	22 ×4	100 ×2	47 ×2 + 10	NA	Internal	Internal	33	12	83.0	70	1.25	10	30.1
2.5	22 ×4	100 ×2	47 ×2 + 10	NA	Internal	Internal	33	12	107.8	70	1.25	10	19.1
3.3	22 ×4	100 ×2	47 ×2 + 10	NA	Internal	Internal	33	12	146.0	70	1.25	10	13.3
5	22 ×4	100 ×2	47 ×2 + 10	NA	Internal	Internal	33	12	219.0	80	1.25	10	8.25

SAFETY CONSIDERATIONS

The LTM4673 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4673 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.

APPLICATIONS INFORMATION

- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- To minimize thermal voltages, route differential current sense inputs as close together as possible, and minimize vias.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie V_{OUT}, V_{OSNSN}^{+}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied to a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

LTM4671 is drop-in pin-compatible and is the non-PSM version of the LTM4673. It shares the same rectangular BGA footprint and pinout functions from pins A1 to W11. See Figure 52. The LTM4671 could be used in an existing design with LTM4673 to provide the same DC/DC converter performance if PSM functionality is not desired. No additional changes to the standard demo circuit are needed to utilize the LTM4671. The LTM4671 is the same quad-output (12A, 5A, 5A, 12A) DC/DC step down converter and channels can be paralleled to achieve higher current applications.

Figure 52 gives a good example of the recommended layout.

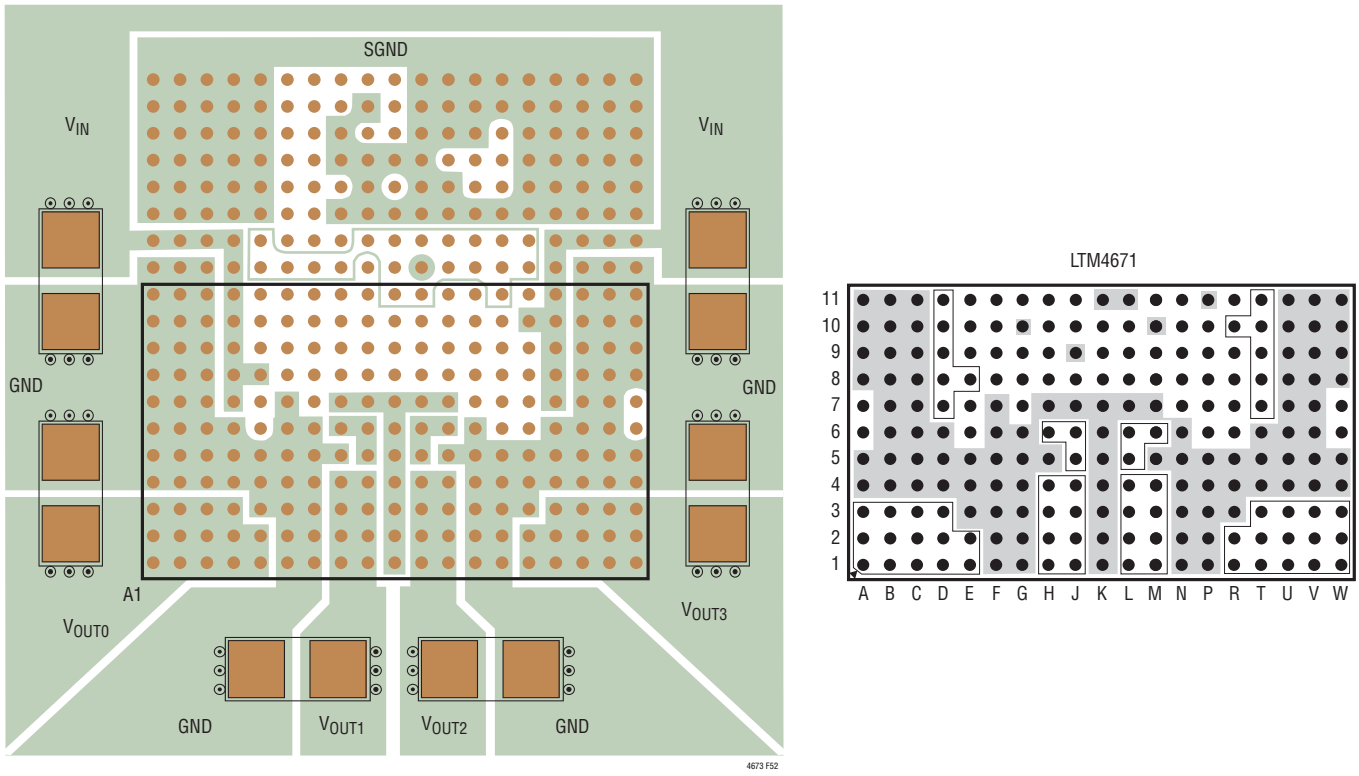


Figure 52. PCB Layout for LTM4673 and LTM4671, Package Top View

TYPICAL APPLICATIONS

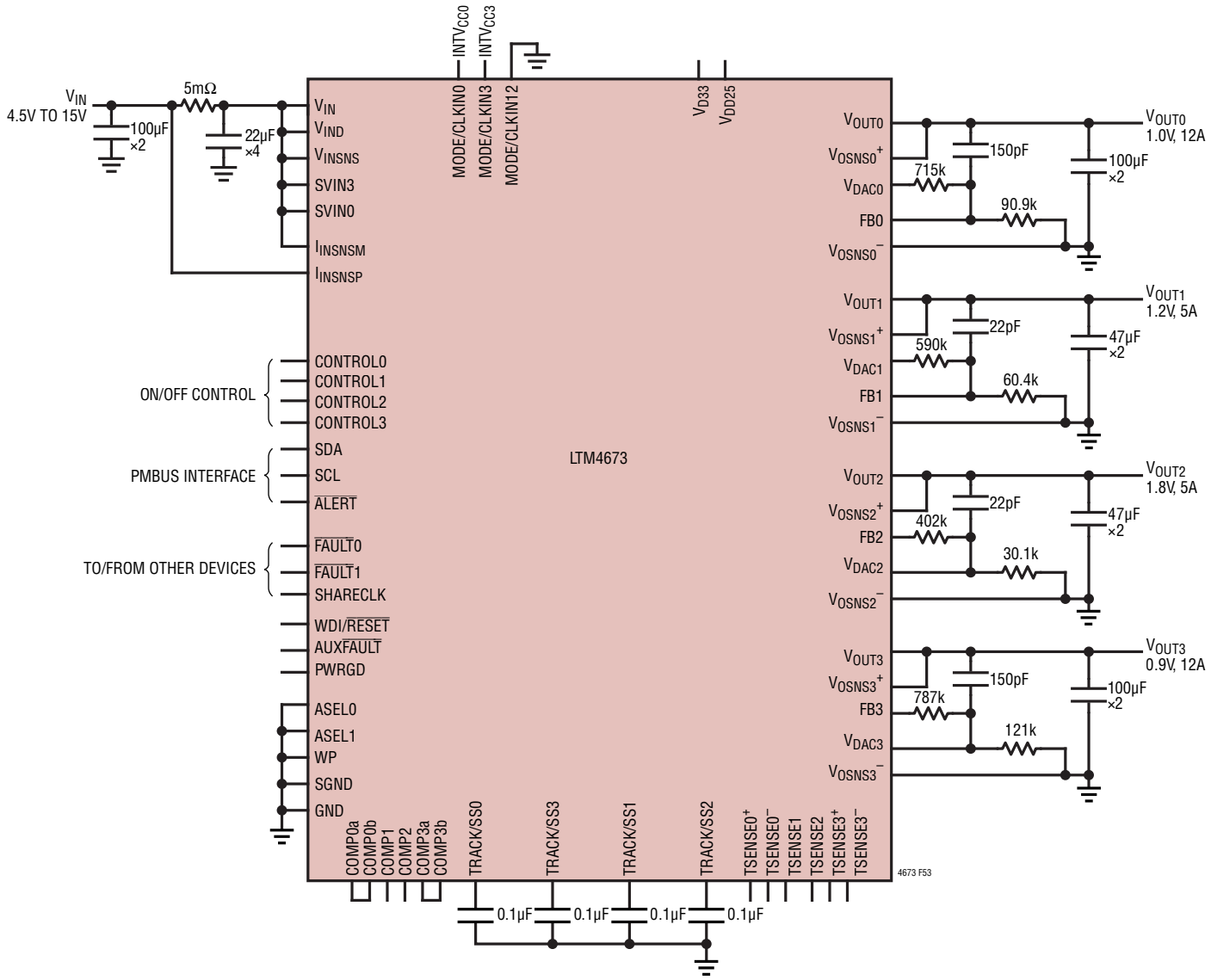
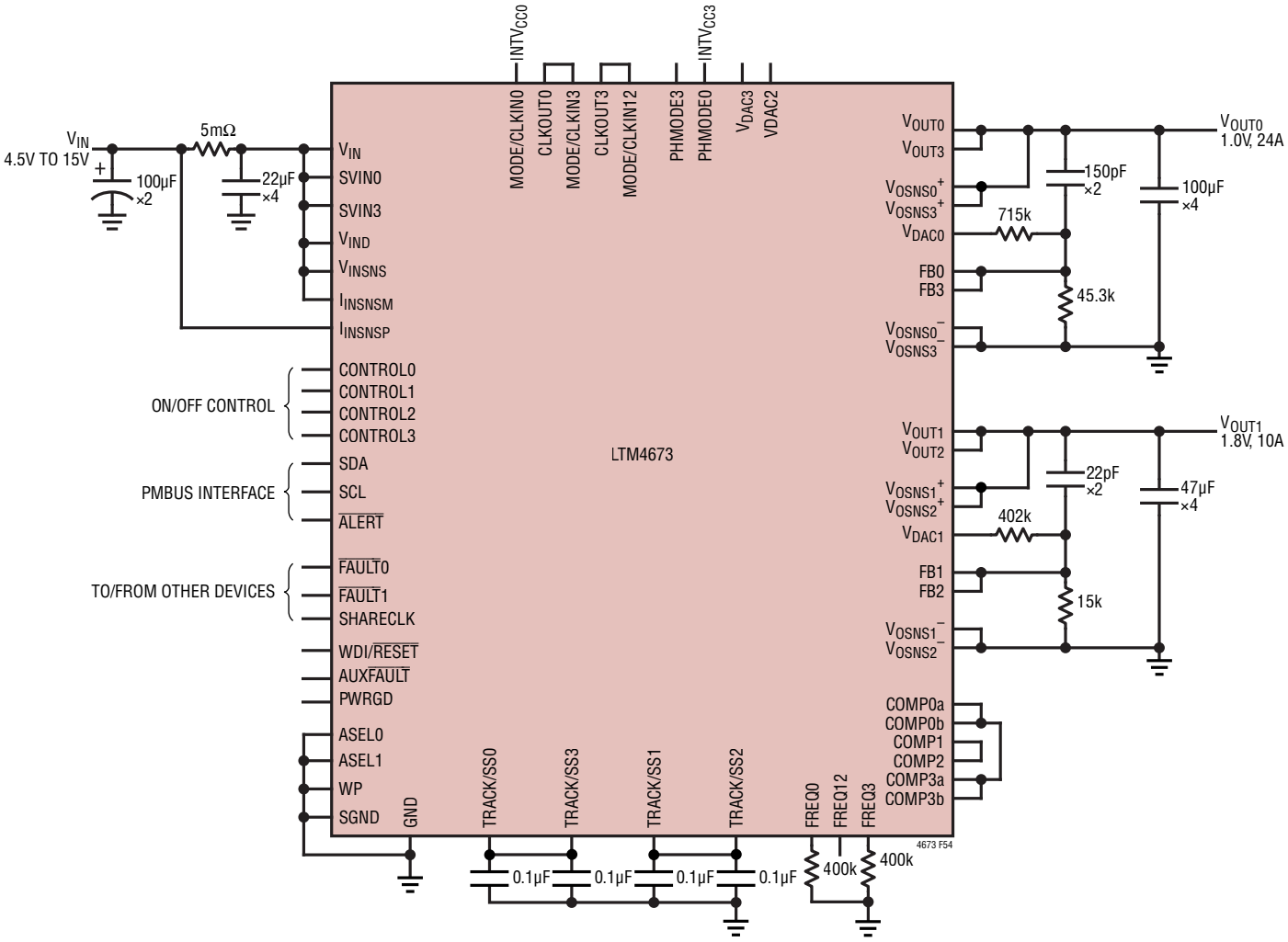


Figure 53. 4.5V to 15V Input, Quad Output Design

TYPICAL APPLICATIONS



	CH0	CH1	CH2	CH3
Phase Shift	90°	180°	90°	
Phase	0°	90°	270°	180°

Figure 54. Parallel Operation with 1MHz Clock and Interleaved Phases

TYPICAL APPLICATIONS

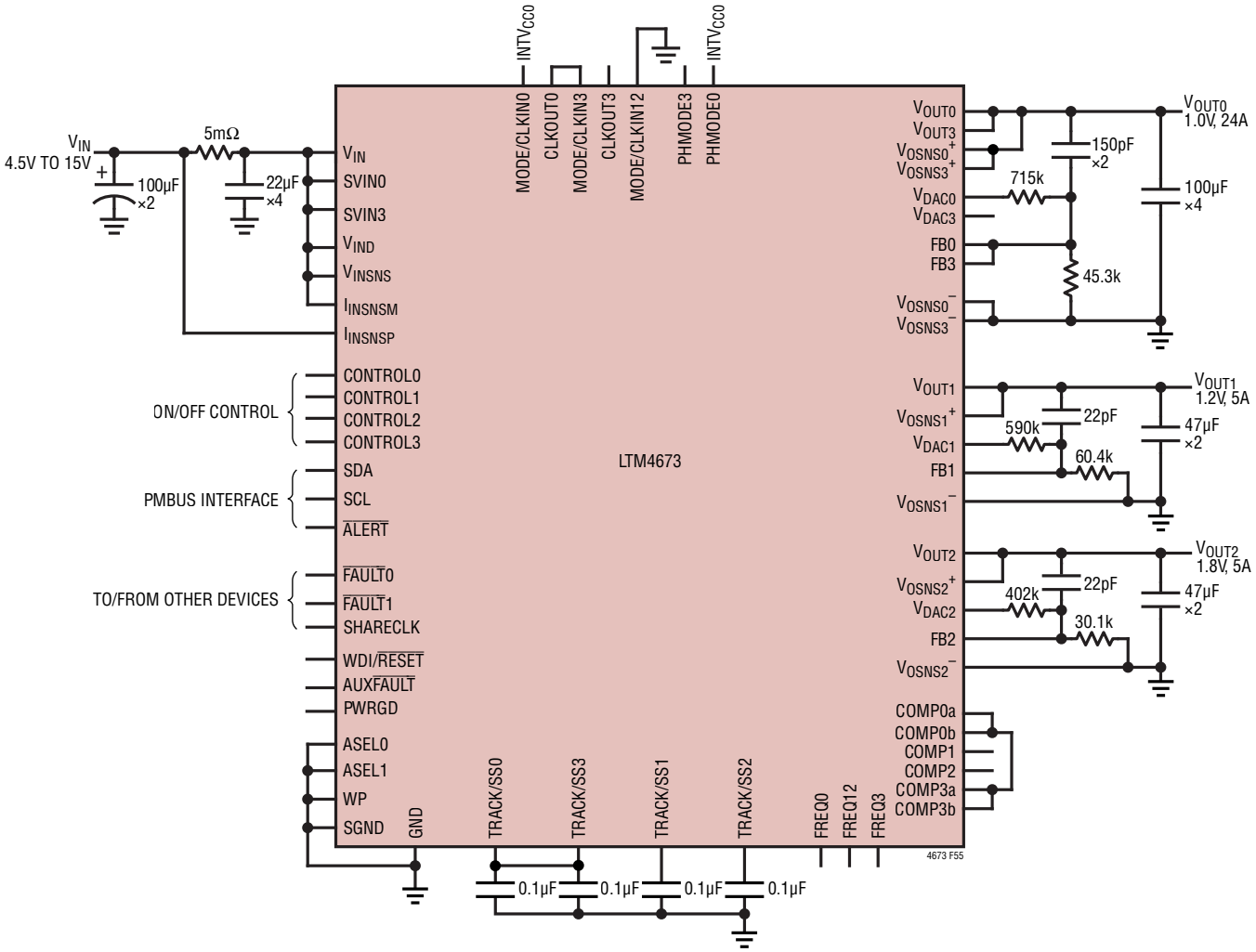


Figure 55. Two Single-Phase 5A Outputs and One Dual-Phase Single 24A Output

TYPICAL APPLICATIONS

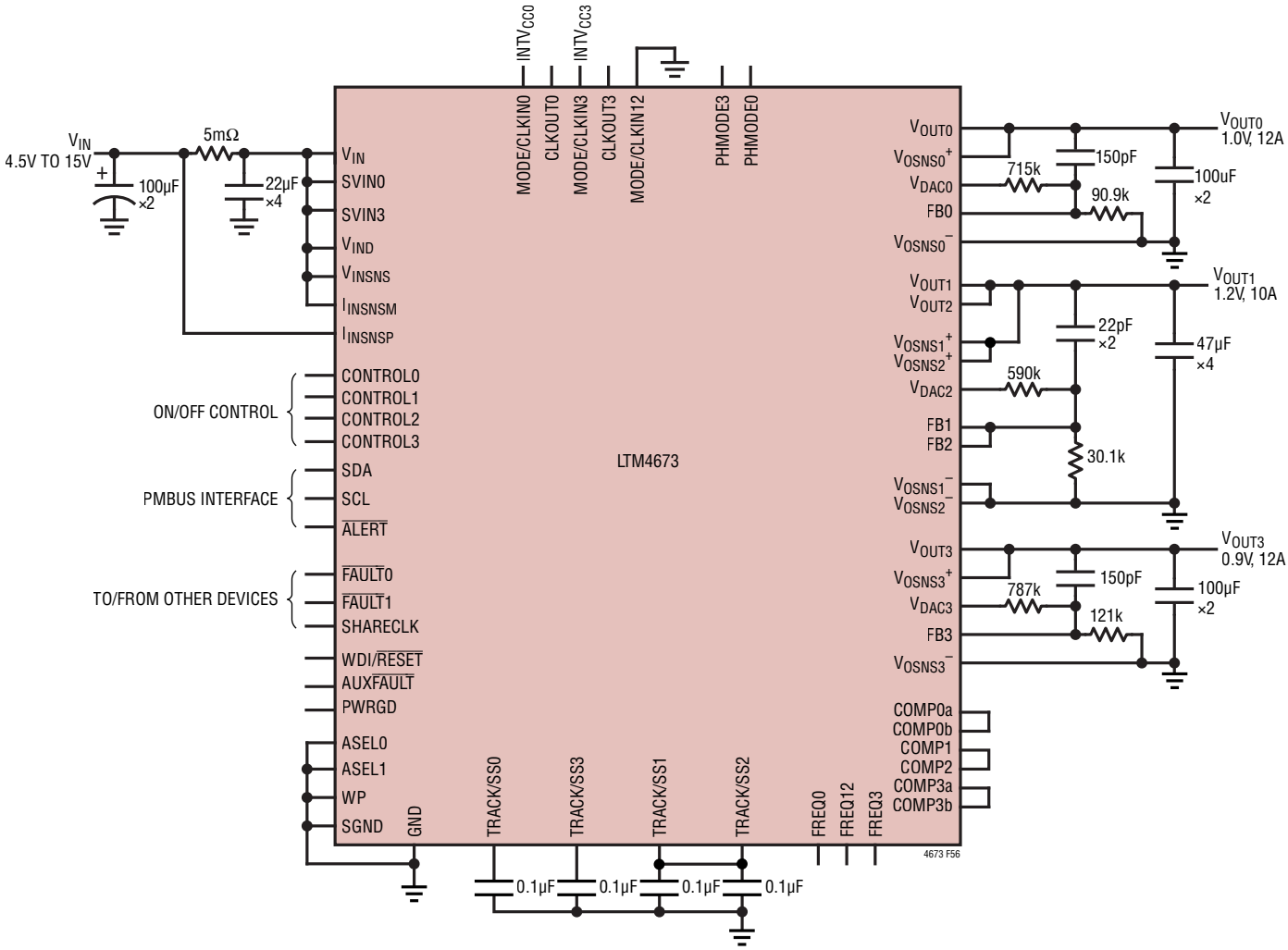


Figure 56. Two Single-Phase 12A Outputs and One Dual-Phase Single 10A Output

PMBus COMMAND DESCRIPTION

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	67
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	68
MFR_I2C_BASE_ADDRESS	0xE6	Base value of the I^2C/SMBus address byte.	R/W Byte	N	Reg		Y	0x5C	69
MFR_PAGE_FF_MASK	0xE4	Configuration defining which channels respond to global page commands (PAGE = 0xFF).	R/W Byte	N	Reg		Y	0x0F	68
MFR_COMMAND_PLUS	0xC8	Alternate access to block read and other data. Commands for all additional hosts.	R/W Word	N	Reg				69
MFR_DATA_PLUS0	0xC9	Alternate access to block read and other data. Data for additional host 0.	R/W Word	N	Reg				69
MFR_DATA_PLUS1	0xCA	Alternate access to block read and other data. Data for additional host 1.	R/W Word	N	Reg				69

PAGE

The LTM4673 has four pages that correspond to the four DC/DC converter channels that can be managed. Each DC/DC converter channel can be uniquely programmed by first setting the appropriate page.

Setting PAGE = 0xFF allows a simultaneous write to all pages for PMBus commands that support global page programming. The only commands that support PAGE = 0xFF are CLEAR_FAULTS, OPERATION and ON_OFF_CONFIG. See MFR_PAGE_FF_MASK for additional options. Reading any paged PMBus register with PAGE = 0xFF returns unpredictable data and will trigger a CML fault. Writes to pages that do not support PAGE = 0xFF with PAGE = 0xFF will be ignored and generate a CML fault.

PAGE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Page	Page operation. 0x00: All PMBus commands address channel/page 0. 0x01: All PMBus commands address channel/page 1. 0x02: All PMBus commands address channel/page 2. 0x03: All PMBus commands address channel/page 3. 0xXX: All non specified values reserved. 0xFF: A single PMBus write/send to commands that support this mode will simultaneously address all channel/pages with MFR_PAGE_FF_MASK enabled.

PMBus COMMAND DESCRIPTION

WRITE_PROTECT

The WRITE_PROTECT command provides protection against accidental programming of the LTM4673 command registers. All supported commands may have their parameters read, regardless of the WRITE_PROTECT setting, and the EEPROM contents can also be read regardless of the WRITE_PROTECT settings.

There are two levels of protection:

- Level 1: Nothing can be changed except the level of write protection itself. Values can be read from all pages. This setting can be stored to EEPROM.
- Level 2: Nothing can be changed except for the level of protection, channel ON/OFF state, and clearing of faults. Values can be read from all pages. This setting can be stored to EEPROM.

WRITE_PROTECT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Write_protect[7:0]	1000_0000b: Level 1 Protection – Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, and STORE_USER_ALL commands. 0100_0000b: Level 2 Protection – Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, STORE_USER_ALL, OPERATION, MFR_PAGE_FF_MASK and CLEAR_FAULTS commands. 0000_0000b: Enable writes to all commands. xxxx_xxxxb: All other values reserved.

WRITE-PROTECT Pin

The WP pin allows the user to write-protect the LTM4673's configuration registers. The WP pin is active high, and when asserted it provides Level 2 protection: all writes are disabled except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, STORE_USER_ALL, OPERATION, MFR_PAGE_FF_MASK and CLEAR_FAULTS commands. The most restrictive setting between the WP pin and WRITE_PROTECT command will override. For example if WP = 1 and WRITE_PROTECT = 0x80, then the WRITE_PROTECT command overrides, since it is the most restrictive.

MFR_PAGE_FF_MASK

The MFR_PAGE_FF_MASK command is used to select which channels respond when the global page command (PAGE = 0xFF) is in use.

MFR_PAGE_FF_MASK Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:4]	Reserved	Always returns 0000b
b[3]	Mfr_page_ff_mask_chan3	Channel 3 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses
b[2]	Mfr_page_ff_mask_chan2	Channel 2 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses
b[1]	Mfr_page_ff_mask_chan1	Channel 1 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses

PMBus COMMAND DESCRIPTION

MFR_PAGE_FF_MASK Data Contents

BIT(S)	SYMBOL	OPERATION
b[0]	Mfr_page_ff_mask_chan0	Channel 0 masking of global page command (PAGE = 0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses

MFR_I2C_BASE_ADDRESS

The MFR_I2C_BASE_ADDRESS command determines the base value for the I^2C/SMBus address byte. Offsets of 0 to 8 are added to this base address to generate the device I^2C/SMBus address. The part responds to the device address. For example, with the factory default MFR_I2C_BASE_ADDRESS of 5C, with both ASEL1 and ASEL0 High (Offset N=2), the device address would be 0x5C+2 = 0x5E.

MFR_I2C_BASE_ADDRESS Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Reserved	Read only, always returns 0.
b[6:0]	I2C_base_address	This 7-bit value determines the base value of the 7-bit I^2C/SMBus address. See Device Address in the Operation section.

MFR_COMMAND_PLUS

MFR_DATA_PLUS0 and MFR_DATA_PLUS1

MFR_STATUS_PLUS0, and MFR_STATUS_PLUS1

Similar to the PAGE register, these registers allow the user to indirectly address memory. These registers are useful to advanced users for reading or writing memory as described below.

Command Plus operations use a sequence of word commands to support the following:

- An alternate method for reading block data using sequential standard word reads.
- A peek operation that allows up to two additional hosts to read an internal register using PMBus word protocol where each host has a unique page.
- A poke operation that allows up to two additional hosts to write an internal register using PMBus word protocol where each host has a unique page.
- Peek, Poke and Command Plus block reads do not interfere with normal PMBus accesses or page values set by PAGE. This enables multi main support for up to 3 hosts.

MFR_COMMAND_PLUS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_command_plus_ reserved	Reserved. Always returns 0.
b[14]	Mfr_command_plus_id	Command plus host ID 0: Mfr_command_plus pointer and page are cached and used for all Mfr_data_plus0 accesses. 1: Mfr_command_plus pointer and page are cached and used for all Mfr_data_plus1 accesses.

PMBus COMMAND DESCRIPTION

MFR_COMMAND_PLUS Data Contents

b[13:9]	Mfr_command_plus_page	Page to be used when peeking or poking via Mfr_data_plus0 or Mfr_data_plus1. Allowed values are 0 through 3. This page value is cached separately for Mfr_data_plus0 and Mfr_data_plus1 based on the value of Mfr_command_plus_id when this register is written.
b[8:0]	Mfr_command_plus_pointer	Internal memory location accessed by Mfr_data_plus0 or Mfr_data_plus1. Mfr_data_plus0 and Mfr_data_plus1 pointers are cached separately. Legal values are listed in the CMD Code column of the PMBus COMMAND SUMMARY table. All other values are reserved, except for the special poke enable/disable values listed in the Enabling And Disabling Poke Operations section, and the command values listed below for Mfr_status_plus0 and Mfr_status_plus1.

MFR_DATA_PLUS0 and MFR_DATA_PLUS1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_data_plus0 Mfr_data_plus1	A read from this register returns data referenced by the last matching Mfr_command_plus write. More specifically, writes to Mfr_command_plus by host 0 update Mfr_data_plus0, and writes to Mfr_command_plus by host1 update Mfr_data_plus1. Multiple sequential reads while pointer = Mfr_fault_Log return the complete contents of the block read buffer. Block reads beyond the end of buffer return zeros. A write to this register will transfer the data to the location referenced by the last matching Mfr_command_plus_pointer when the Poke operation protocol described in the Poke Operation Using Mfr_data_plus0 section is followed.

MFR_STATUS_PLUS0 and MFR_STATUS_PLUS1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	
b[1]	Mfr_status_plus_block_peek_failed0 Mfr_status_plus_block_peek_failed1	Status of most recent block peek for matching host. 0: Last block peek was not aborted. 1: Last block peek was aborted due to an intervening fault log EEPROM write, MFR_FAULT_LOG_STORE command, or standard PMBus block read of MFR_FAULT_LOG. The intervening operation is always completed cleanly.
b[0]	Mfr_status_plus_poke_failed0 Mfr_status_plus_poke_failed1	Status of most recent poke for matching host. 0: Last poke operation did not fail. 1: Last poke operation failed because pokes were not enabled as described in Enabling and Disabling Poke Operations section.

MFR_STATUS_PLUS0 is at command location 0x2C, and MFR_STATUS_PLUS1 is at command location 0x2D. These correspond to reserved PMBus command locations. These two status registers can only be read via Command Plus peeks.

Reading Fault Log Using Command Plus and Mfr_data_plus0

Write Mfr_command_plus_pointer = 0xEE with Mfr_command_plus_page = 0 and Mfr_command_plus_id = 0.

Read data from Mfr_data_plus0; each read returns the next data word of the MFR_FAULT_LOG command:

- The first word read is Byte_count[15:0] = 0x00FF.
- The next set of words read is the Preamble with 2 bytes packed into a word. Refer to the Fault Log section for details.
- The next set of words read is the Cyclical Loop Data with 2 bytes per word. Refer to the Fault Log section for details.
- Extra reads return zero.
- Interleaved PMBus word and byte commands do not interfere with an ongoing Command Plus block read.
- Interleaved PMBus block reads of MFR_FAULT_LOG will interrupt this command.

PMBus COMMAND DESCRIPTION

Check status to be sure the data just read was all valid:

- Write Mfr_command_plus_pointer = 0x2C with Mfr_command_plus_page = 0 and Mfr_command_plus_id = 0.
- Read data from Mfr_data_plus0 and confirm that Mfr_status_plus_block_peek_failed0 = 0.

Reading Energy Using MFR_COMMAND_PLUS and MFR_DATA_PLUS0

Write Mfr_command_plus_pointer = 0xC0 with Mfr_command_plus_page = 0 and Mfr_command_plus_id = 0.

Read data from Mfr_data_plus_0; each read returns the next data word of the MFR_EIN command:

- Byte_count[15:0] = 0x000C
- Energy_value[15:0]
- Energy_value[31:16]
- Energy_value[47:32]
- Energy_time[15:0]
- Energy_time[31:16]
- Energy_time[47:32]

Peek Operation Using Mfr_data_plus0

Internal words and bytes may be read using Command Plus:

Write Mfr_command_plus_pointer = CMD_CODE with Mfr_command_plus_page = page and Mfr_command_plus_id = 0.

The CMD_CODE's are listed in the PMBus COMMAND SUMMARY table.

Read data from Mfr_data_plus0. Data is always read using a word read. Byte data is returned with upper byte set to 0.

Enabling and Disabling Poke Operations

Poke operations to Mfr_data_plus0 are enabled by writing Mfr_command_plus = 0x0BF6.

Poke operations to Mfr_data_plus0 are disabled by writing Mfr_command_plus = 0x01F6.

Poke operations to Mfr_data_plus1 are enabled by writing Mfr_command_plus = 0x4BF6.

Poke operations to Mfr_data_plus1 are disabled by writing Mfr_command_plus = 0x41F6.

Poke Operation Using Mfr_data_plus0

Internal words and bytes may be written using Command Plus:

Enable poke access for Mfr_data_plus0. This need only be done once after a power-up or WDI reset.

Write Mfr_command_plus_pointer = CMD_CODE with Mfr_command_plus_page = page and Mfr_command_plus_id = 0.

The CMD_CODEs are listed in the PMBus COMMAND SUMMARY table.

Write the new data value to MFR_DATA_PLUS0

Optionally check status to be sure data was written as desired:

- Write Mfr_command_plus_pointer = 0x2C with Mfr_command_plus_page = 0 and Mfr_command_plus_id = 0.

PMBus COMMAND DESCRIPTION

- Read data from Mfr_data_plus0 and confirm that Mfr_status_plus_poke_failed0 = 0.

Command Plus Operations Using Mfr_data_plus1

All the previous operations may be accessed via Mfr_data_plus1 by substituting Mfr_command_plus_id value with a 1. Poke operations must be enabled for Mfr_data_plus1.

ON/OFF CONTROL, MARGINING AND CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
OPERATION	0x01	Operating mode control. ON/OFF, Margin High and Margin Low	R/W Byte	Y	Reg		Y	0x80	72
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus ON/OFF command setting	R/W Byte	Y	Reg		Y	0x1E	73
MFR_CONFIG_LTM4673	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	Pg00:0x0088 Pg01:0x1088 Pg02:0x2088 Pg03:0x3088	74
MFR_CONFIG2_LTM4673	0xD9	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	77
MFR_CONFIG3_LTM4673	0xDA	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	76
MFR_CONFIG_ALL_LTM4673	0xD1	Configuration bits that are common to all pages	R/W Word	N	Reg		Y	0x0F7B	77

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the CONTROL pin and ON_OFF_CONFIG. This command register responds to the global page command (PAGE = 0xFF). The contents and functions of the data byte are shown in the following tables. A minimum t_{OFF_MIN} wait time must be observed between any OPERATION commands used to turn the unit off and then back on to give the ADC telemetry loop time to complete a full cycle.

OPERATION Data Contents (On_off_config_use_pmbus = 1)

SYMBOL	ACTION	OPERATION_ CONTROL[1:0]	OPERATION_ MARGIN[1:0]	OPERATION_ FAULT[1:0]	RESERVED (READ ONLY)
BIT(S)		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Turn off immediately	00	XX	XX	00
	Sequence on	10	00	XX	00
	Margin low (ignore faults and warnings)	10	01	01	00
	Margin low	10	01	10	00
	Margin high (ignore faults and warnings	10	10	01	00
	Margin high	10	10	10	00
	Sequence off with margin to nominal	01	00	XX	00
	Sequence off with margin low (ignore faults and warnings)	01	01	01	00
	Sequence off with margin low	01	01	10	00
	Sequence off with margin high (ignore faults and warnings)	01	10	01	00
	Sequence off with margin high	01	10	10	00
	Reserved	All remaining combinations			

PMBus COMMAND DESCRIPTION

OPERATION Data Contents (On_off_config_use_pmbus = 0)
ON/OFF

SYMBOL		OPERATION_ CONTROL[1:0]	OPERATION_ MARGIN[1:0]	OPERATION_ FAULT[1:0]	RESERVED (READ ONLY)
BITS	ACTION	b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Output at nominal	00, 01 or 10	00	XX	00
	Margin low (ignore faults and warnings)	00, 01 or 10	01	01	00
	Margin low	00, 01 or 10	01	10	00
	Margin high (ignore faults and warnings	00, 01 or 10	10	01	00
	Margin high	00, 01 or 10	10	10	00
	Reserved	All remaining combinations			

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of CONTROL pin input and PMBus commands needed to turn the LTM4673 ON/OFF, including the power-on behavior, as shown in the following table. This command register responds to the global page command (PAGE = 0xFF). After the part has initialized, an additional comparator monitors V_{INSNS}. The VIN_ON threshold must be exceeded before the output power sequencing can begin. After V_{IN} is initially applied, the part will typically require t_{INIT} to initialize and begin the TON_DELAY timer. The readback of voltages and currents may require an additional wait for t_{UPDATE_ADC}. A minimum t_{OFF_MIN} wait time must be observed for any CONTROL pin used toggle to turn the unit off and then back on.

ON_OFF_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:5]	Reserved	Don't care. Always returns 0.
b[4]	On_off_config_controlled_on	Control default autonomous power up operation. 0: Unit powers up regardless of the CONTROL pin or OPERATION value. Unit always powers up with sequencing. To turn unit on without sequencing, set TON_DELAY = 0. 1: Unit does not power up unless commanded by the CONTROL pin and/or the OPERATION command on the serial bus. If On_off_config[3:2] = 00, the unit never powers up.
b[3]	On_off_config_use_pmbus	Controls how the unit responds to commands received via the serial bus. 0: Unit ignores the Operation_control[1:0]. 1: Unit responds to Operation_control[1:0]. Depending on On_off_config_use_control, the unit may also require the CONTROL pin to be asserted for the unit to start.
b[2]	On_off_config_use_control	Controls how unit responds to the CONTROL pin. 0: Unit ignores the CONTROL pin. 1: Unit requires the CONTROL pin to be asserted to start the unit. Depending on On_off_config_use_pmbuS the OPERATION command may also be required to instruct the device to start.
b[1]	Reserved	Not supported. Always returns 1.
b[0]	On_off_config_control_fast_off	CONTROL pin turn off action when commanding the unit to turn off 0: Use the programmed TOFF_DELAY. 1: Turn off the output and stop transferring energy as quickly as possible. The device does not sink current in order to decrease the output voltage fall time.

PMBus COMMAND DESCRIPTION

MFR_CONFIG_LTM4673

This command is used to configure various manufacturer specific operating parameters for each channel.

MFR_CONFIG_LTM4673 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Reserved	Don't care. Always returns 0.
b[14]	Mfr_config_cascade_on	Configures channel's control pin for cascade sequence ON. There is no provision for cascade sequence OFF. See description for time based sequence OFF options.
b[13:12]	Mfr_config_controln_sel[1:0]	Selects the active control pin input (CONTROL0 , CONTROL1, CONTROL2 or CONTROL3) for this channel. 0: Select CONTROL0 pin. 1: Select CONTROL1 pin. 2: Select CONTROL2 pin. 3: Select CONTROL3 pin.
b[11]	Mfr_config_fast_servo_off	Disables fast servo when margining or trimming output voltages: 0: fast-servo enabled. 1: fast-servo disabled.
b[10]	Mfr_config_supervisor_resolution	Selects voltage supervisor resolution: 0: high resolution = 4mV/LSB, range for $V_{VSENSEP n} – V_{VSENSEM n}$ is 0 to 3.8V 1: low resolution = 8mV/LSB, range for $V_{VSENSEP n} – V_{VSENSEM n}$ is 0 to 6.0V
b[9:8]	Reserved	Always returns 0.
b[7]	Mfr_config_servo_continuous	Select whether the UNIT should continuously servo V_{OUT} after it has reached a new margin or nominal target. Only applies when Mfr_config_dac_mode = 00b. 0: Do not continuously servo VOUT after reaching initial target. 1: Continuously servo VOUT to target.
b[6]	Mfr_config_servo_on_warn	Control re-servo on warning feature. Only applies when Mfr_ config_dac_mode = 00b and Mfr_config_ servo_continuous = 0. 0: Do not allow the unit to re-servo when a V_{OUT} warning threshold is met or exceeded. 1: Allow the unit to re-servo VOUT to nominal target if $V_{OUT} \geq$ V(Vout_ov_warn_limit) or $V_{OUT} \leq$ V(Vout_uv_warn_limit).
b[5:4]	Mfr_config_dac_mode	Determines how DAC is used when channel is in the ON state and TON_RISE has elapsed. 00: Soft-connect (if needed) and servo to target. 01: DAC not connected. 10: DAC connected immediately using value from MFR_DAC command. If this is the configuration after a reset or RESTORE_USER_ALL, MFR_DAC will be undefined and must be written to desired value. 11: DAC is soft-connected. After soft-connect is complete MFR_DAC may be written.
b[3]	Mfr_config_vo_en_wpu_en	V_{OUT_EN} pin charge pumped, current-limited pull-up enable. 0: Disable weak pull-up. V_{OUT_EN} pin driver is three-stated when channel is on. 1: Use weak current-limited pull-up on V_{OUT_EN} pin when the channel is on.
b[2]	Mfr_config_vo_en_wpd_en	V_{OUT_EN} pin charge-pumped, current-limited pull-down enable. 0: Use a fast N-channel device to pull down V_{OUT_EN} pin when the channel is off for any reason. 1: Use weak current-limited pull-down to discharge V_{OUT_EN} pin when channel is off due to soft stop by the CONTROL pin and/or OPERATION command. If the channel is off due to a fault, use the fast pull-down on the V_{OUT_EN} pin.

PMBus COMMAND DESCRIPTION

MFR_CONFIG_LTM4673 Data Contents

BIT(S)	SYMBOL	OPERATION
b[1]	Mfr_config_dac_gain	DAC buffer gain. 0: Select DAC buffer gain dac_gain_0 (1.38V full-scale) 1: Select DAC buffer gain dac_gain_1 (2.65V full-scale)
b[0]	Mfr_config_ dac_pol	DAC output polarity. 0: Encodes negative (inverting) DC/DC converter trim input. 1: Encodes positive (non-inverting) DC/DC converter trim input.

MFR_CONFIG2_LTM4673

This command register determines whether V_{OUT} overvoltage or overcurrent faults from a given channel cause the AUX$\overline{FAULT}$ pin to be pulled low.

MFR_CONFIG2_LTM4673 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_auxfaultb_oc_fault_response_chan3	Response to channel 3 IOUT_OC_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[6]	Mfr_auxfaultb_oc_fault_response_chan2	Response to channel 2 IOUT_OC_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[5]	Mfr_auxfaultb_oc_fault_response_chan1	Response to channel 1 IOUT_OC_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[4]	Mfr_auxfaultb_oc_fault_response_chan0	Response to channel 0 IOUT_OC_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[3]	Mfr_auxfaultb_ov_fault_response_chan3	Response to channel 3 VOUT_OV_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[2]	Mfr_auxfaultb_ov_fault_response_chan2	Response to channel 2 VOUT_OV_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[1]	Mfr_auxfaultb_ov_fault_response_chan1	Response to channel 1 VOUT_OV_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[0]	Mfr_auxfaultb_ov_fault_response_chan0	Response to channel 0 VOUT_OV_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.

PMBus COMMAND DESCRIPTION

MFR_CONFIG3_LTM4673

This command register determines whether V_{OUT} undercurrent faults from a given channel cause the AUX$\overline{FAULT}$ pin to be pulled low. This command also allows tracking to be enabled on any channel.

MFR_CONFIG3_LTM4673 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_auxfaultb_uc_fault_response_chan3	Response to channel 3 IOUT_UC_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[6]	Mfr_auxfaultb_uc_fault_response_chan2	Response to channel 2 IOUT_UC_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[5]	Mfr_auxfaultb_uc_fault_response_chan1	Response to channel 1 IOUT_UC_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 =Do not pull AUX$\overline{FAULT}$ low.
b[4]	Mfr_auxfaultb_uc_fault_response_chan0	Response to channel 0 IOUT_UC_FAULT. 1 = Pull AUX$\overline{FAULT}$ low via fast pull-down. 0 = Do not pull AUX$\overline{FAULT}$ low.
b[3]	Mfr_track_en_chan3	Select if channel 3 is a subordinate in a tracked power supply system. 0: Channel is not a subordinate in a tracked power supply system. 1: Channel is a subordinate in a tracked power supply system. Setting this bit disables UV and UC detection during TOFF_DELAY.
b[2]	Mfr_track_en_chan2	Select if channel 2 is a subordinate in a tracked power supply system. 0: Channel is not a subordinate in a tracked power supply system. 1: Channel is a subordinate in a tracked power supply system. Setting this bit disables UV and UC detection during TOFF_DELAY.
b[1]	Mfr_track_en_chan1	Select if channel 1 is a subordinate in a tracked power supply system. 0: Channel is not a subordinate in a tracked power supply system. 1: Channel is a subordinate in a tracked power supply system. Setting this bit disables UV and UC detection during TOFF_DELAY.
b[0]	Mfr_track_en_chan0	Select if channel 0 is a subordinate in a tracked power supply system. 0: Channel is not a subordinate in a tracked power supply system. 1: Channel is a subordinate in a tracked power supply system. Setting this bit disables UV and UC detection during TOFF_DELAY.

PMBus COMMAND DESCRIPTION

MFR_CONFIG_ALL_LTM4673

This command is used to configure parameters that are common to all channels on the IC. They may be set or reviewed from any PAGE setting.

MFR_CONFIG_ALL_LTM4673 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:12]	Reserved	Don't care. Always returns 0.
b[11]	Mfr_config_all_pwrgd_off_uses_uv	Selects PWRGD de-assertion source for all channels. 0: PWRGD is de-asserted based on V_{OUT} being below or equal to POWER_GOOD_OFF. This option uses the ADC. Response time is approximately 100ms to 200ms. 1: PWRGD is de-asserted based on V_{OUT} being below or equal to VOUT_UV_LIMIT. This option uses the high speed supervisor. Response time is approximately 12µs.
b[10]	Mfr_config_all_fast_fault_log	Controls number of ADC readings completed before transferring fault log memory to EEPROM. 0: All ADC telemetry values will be updated before transferring fault log to EEPROM. Slower. 1: Telemetry values will be transferred from fault log to EEPROM within 24ms after detecting fault. Faster.
b[9]	Mfr_config_all_control3_pol	Selects active polarity of CONTROL3 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[8]	Mfr_config_all_control2_pol	Selects active polarity of CONTROL2 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[7]	Mfr_config_all_fault_log_enable	Enable fault logging to EEPROM in response to Fault. 0: Fault logging to EEPROM is disabled. 1: Fault logging to EEPROM is enabled.
b[6]	Mfr_config_all_vin_on_clr_faults_en	Allow VIN_ON rising edge to clear all latched faults. 0: VIN_ON clear faults feature is disabled. 1: VIN_ON clear faults feature is enabled.
b[5]	Mfr_config_all_control1_pol	Selects active polarity of CONTROL1 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).

PMBus COMMAND DESCRIPTION

MFR_CONFIG_ALL_LTM4673 Data Contents

BIT(S)	SYMBOL	OPERATION
b[4]	Mfr_config_all_control0_pol	Selects active polarity of CONTROL0 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[3]	Mfr_config_all_vin_share_enable	Allow this unit to hold Share-clock pin low when V_{IN} has not risen above VIN_ON or has fallen below VIN_OFF. When enabled this unit will also turn all channels off in response to Share-clock being held low. 0: Share-clock inhibit is disabled. 1: Share-clock inhibit is enabled.
b[2]	Mfr_config_all_pec_en	PMBus packet error checking enable. 0: PEC is accepted but not required. 1: PEC is enabled.
b[1]	Mfr_config_all_longer_pmbus_timeout	Increase PMBus timeout interval by a factor of 8. Recommended for fault logging. 0: PMBus timeout is not multiplied by a factor of 8. 1: PMBus timeout is multiplied by a factor of 8.
b[0]	Mfr_config_all_auxfaultb_wpu_dis	AUX$\overline{\text{FAULT}}$ charge-pumped, current-limited pull-up disable. 0: Use weak current-limited pull-up on AUX$\overline{\text{FAULT}}$ after power-up, as long as no faults have forced AUX$\overline{\text{FAULT}}$ off. 1: Disable weak pull-up. AUX$\overline{\text{FAULT}}$ driver is three-stated after power-up as long as no faults have forced AUX$\overline{\text{FAULT}}$ off.

PROGRAMMING USER EEPROM SPACE

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	79
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	79
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	79
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	80
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	80

PMBus COMMAND DESCRIPTION

STORE_USER_ALL and RESTORE_USER_ALL

STORE_USER_ALL, RESTORE_USER_ALL commands provide access to User EEPROM space. Once a command is stored in User EEPROM, it will be restored with explicit restore command, when the part emerges from power-on reset after power is applied, or after toggling the Reset pin. While either of these commands is being processed, the part will indicate it is busy, see Response When Part Is Busy on page 81.

STORE_USER_ALL. Issuing this command will store all operating memory commands with a corresponding EEPROM memory location.

RESTORE_USER_ALL. Issuing this command will restore all commands from EEPROM Memory. It is recommended that this command not be executed while a unit is enabled since all monitoring is suspended while the EEPROM is transferred to operating memory, and intermediate values from EEPROM may not be compatible with the values initially stored in operating memory.

Bulk Programming the User EEPROM Space

The MFR_EE_UNLOCK, MFR_EE_ERASE and MFR_EE_DATA commands provide a method for 3rd party EEPROM programming houses and end users to easily program the LTM4673 independent of any order dependencies or delays between PMBus commands. All data transfers are directly to and from the EEPROM and do not affect the volatile RAM space currently configuring the device.

The first step is to program a main reference part with the desired configuration. MFR_EE_UNLOCK and MFR_EE_DATA are then used to read back all the data in User EEPROM space as sequential words. This information is stored to the main programming HEX file. Subsequent parts may be cloned to match the main part using MFR_EE_UNLOCK, MFR_EE_ERASE and MFR_EE_DATA to transfer data from the main HEX file. These commands operate directly on the EEPROM independent of the part configurations stored in RAM space. During EEPROM access the part will indicate that it is busy as described below.

In order to support simple programming fixtures the bulk programming features only uses PMBus word and byte commands. The MFR_UNLOCK configures the appropriate access mode and resets an internal address pointer allowing a series of word commands to behave as a block read or write with the address pointer being incremented after each operation. PEC use is optional and is configured by the MFR_EE_UNLOCK operation.

MFR_EE_UNLOCK

The MFR_EE_UNLOCK command prevents accidental EEPROM access in normal operation and configures the required EEPROM bulk programming mode for bulk initialization, sequential writes, or reads. MFR_EE_UNLOCK augments the protection provided by write protect. Upon unlocking the part for the required operation, an internal address pointer is reset allowing a series of MFR_EE_DATA reads or writes to sequentially transfer data, similar to a block read or block write. The MFR_EE_UNLOCK command can clear or set PEC mode based on the desired level of error protection. An MFR_EE_UNLOCK sequence consists of writing two unlock codes using two byte-write commands. The following table documents the allowed sequences. Writing a non-supported sequence locks the part. Reading MFR_EE_UNLOCK returns the last byte written or zero if the part is locked.

PMBus COMMAND DESCRIPTION

MFR_EE_UNLOCK Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_unlock[7:0]	To unlock user EEPROM space for Mfr_ee_erase and Mfr_ee_data read or write operations with PEC allowed: Write 0x2b followed by 0xd4. To unlock user EEPROM space for Mfr_ee_erase and Mfr_ee_data read or write operations with PEC required: Write 0x2b followed by 0xd5. To unlock user and manufacturer EEPROM space for Mfr_ee_data read only operations with PEC allowed: Write 0x2b, followed by 0x91 followed by 0xe4. To unlock user and manufacturer EEPROM space for Mfr_ee_data read only operations with PEC required: Write 0x2b, followed by 0x91 followed by 0xe5.

MFR_EE_ERASE

The MFR_EE_ERASE command is used to erase the entire contents of the user EEPROM space and configures this space to accept new program data. Writing values other than 0x2B will lock the part. Reads return the last value written.

MFR_EE_ERASE Data contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_erase[7:0]	To erase the user EEPROM space and configure to accept new data: 1) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_erase commands with or without PEC. 2) Write 0x2B to Mfr_ee_erase. The part will indicate it is busy erasing the EEPROM by the mechanism detailed below.

MFR_EE_DATA

The MFR_EE_DATA command allows the user to transfer data directly to or from the EEPROM without affecting RAM space.

To read the user EEPROM space issue the appropriate Mfr_ee_unlock command and perform Mfr_ee_data reads until the EEPROM has been completely read. Extra reads will lock the part and return zero. The first read returns the 16-bit EEPROM packing revision ID that is stored in ROM. The second read returns the number of 16-bit words available; this is the number of reads or writes to access all memory locations. Subsequent reads return EEPROM data starting with lowest address.

To write to the user EEPROM space issue the appropriate Mfr_ee_unlock and Mfr_ee_erase commands followed by successive Mfr_ee_data word writes until the EEPROM is full. Extra writes will lock the part. The first write is to the lowest address.

Mfr_ee_data reads and writes must not be mixed.

PMBus COMMAND DESCRIPTION

MFR_EE_DATA Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_data[7:0]	To read user space 1) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_data commands with or without PEC. 2) Read Mfr_ee_data[0] = PackingId (MFR Specific ID). 3) Read Mfr_ee_data[1] = NumberOfUserWords (total number of 16-bit word available). 4) Read Mfr_ee_data[2] through Mfr_ee_data[NumberOfWord+1] (User EEPROM data contents) To write user space 1) Initialize the user memory using the sequence described for the MFR_EE_ERASE command. 2) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_data commands with or without PEC. 3) Write Mfr_ee_data[0] through Mfr_ee_data[NumberOfWord-1] (User EEPROM data content to be written) The part will indicate it is busy erasing the EEPROM by the mechanism detailed below.

Response When Part Is Busy

The part will indicate it is busy accessing the EEPROM by the following mechanism:

1) Clearing Mfr_common_busyb of the MFR_COMMON register. This byte can always be read and will never NACK a byte read request even if the part is busy.

2) NACKing commands other than MFR_COMMON.

MFR_EE Erase and Write Programming Time

The program time per word is typically 0.17ms and will require spacing the I^2C/SMBus writes at greater than 0.17ms to guarantee the write has completed. The Mfr_ee_erase command takes approximately 400ms. We recommend using MFR_COMMON for handshaking.

INPUT VOLTAGE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VIN_ON	0x35	Input voltage above which power conversion can be enabled.	R/W Word	N	L11	V	Y	4.5 0xCA40	81
VIN_OFF	0x36	Input voltage below which power conversion is disabled. All V_{OUT_EN} pins go off immediately or sequence off after TOFF_DELAY (See Mfr_track_en_chan*n*).	R/W Word	N	L11	V	Y	4.4 0xCA33	81
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at V_{INSNS} pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	81
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at V_{INSNS} pin.	R/W Word	N	L11	V	Y	14.0 0xD380	81
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at V_{INSNS} pin.	R/W Word	N	L11	V	Y	0 0x8000	81
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at V_{INSNS} pin.	R/W Word	N	L11	V	Y	0 0x8000	81

VIN_ON, VIN_OFF, VIN_OV_FAULT_LIMIT, VIN_OV_WARN_LIMIT, VIN_UV_WARN_LIMIT and VIN_UV_FAULT_LIMIT

These commands provide voltage supervising limits for the input voltage V_{INSNS}.

PMBus COMMAND DESCRIPTION

INPUT CURRENT AND ENERGY

COMMAND NAME		DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_EIN	0xC0	Input energy data bytes.	R Block	N	Reg			NA	83
MFR_EIN_CONFIG	0xC1	Configuration register for energy and input current.	R/W Byte	N	Reg		Y	0x00	83
MFR_IIN_CAL_GAIN_TC	0xC3	Temperature coefficient applied to IIN_CAL_GAIN.	R/W Word	N	CF	ppm	Y	0x0000	84
MFR_IIN_CAL_GAIN	0xE8	The nominal resistance of the current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	5.0 0xCA80	84

Energy Measurement and Reporting

Input energy measurement and monitoring supports the following:

- Input energy derived from the accumulated product of READ_VIN and READ_IIN.
- Reporting input energy value as a 48-bit integer in mJ. Returning value in Joules eliminates the need for the host to manage time.
- Reporting input energy time as a 48-bit integer in ms, where input energy time is the elapsed time since energy monitoring was last reset.
- Resetting time and energy accumulators whenever MFR_EIN_CONFIG is written.
- Wrapping of time and energy accumulators when full.
- An optional HD mode allowing the user to give priority to energy measurement by forcing the ADC to measure READ_VIN and READ_IIN between every other ADC measurement.
- Reporting energy and time values coherently.
- Ability to decrement energy to prevent rectification and accumulation of noise when the channel is off. Energy is not allowed to decrement below zero.

PMBus COMMAND DESCRIPTION

MFR_EIN

Read only. This 12-byte data block returns the input energy value and time. Once the block read starts, MFR_EIN updates are suspended until the block read completes. However, energy and time continue to accumulate internally during block reads.

Table 7. MFR_EIN Data Block Contents

DATA	BYTE*	DESCRIPTION
Energy_value [7:0]	0	Energy Value in mJ. This is the accumulated energy since Mfr_ein_config was last written.
Energy_value [15:8]	1	
Energy_value [23:16]	2	
Energy_value [31:24]	3	
Energy_value [39:32]	4	
Energy_value [47:40]	5	
Energy_time [7:0]	6	Energy Time in ms. This is the elapsed time since Mfr_ein_config was last written.
Energy_time [15:8]	7	
Energy_time [23:16]	8	
Energy_time [31:24]	9	
Energy_time [39:32]	10	
Energy_time [47:40]	11	

MFR_EIN_CONFIG

This command configures energy and input current related parameters.

MFR_EIN_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:3]	Mfr_ein_config_reserved	Don't care. Always returns 0.
b[2]	Mfr_ein_config_hd	Optimize ADC polling sequence for higher definition input energy measurement. 0: Standard ADC polling sequence 1: Read_vin and Read_iin measurements are interleaved between every other ADC measurement.
b[1:0]	Mfr_ein_config_iin_range	Input sense amplifier range setting. 0: High Range 1: Medium Range 2: Low Range 3: Reserved The range sets the Full-Scale Input Voltage Range (FS_IIN). Lower range settings have lower input referred noise.

PMBus COMMAND DESCRIPTION

MFR_IIN_CAL_GAIN

The MFR_IIN_CAL_GAIN command is used to set the ratio of the voltage at the input current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the same value as the resistance of the sense resistor (units are expressed in mΩ). MFR_IIN_CAL_GAIN is internally limited to values between 0.01mΩ to 1,000mΩ. The register readback value always returns what was last written and does not reflect internal limiting.

Calculations using IIN_CAL_GAIN are:

$$READ\_IIN = \frac{V_{IINSNSPn} - V_{IINSNSMn}}{(MFR\_IIN\_CAL\_GAIN) \bullet T_{CORRECTION}} \quad (22)$$

where:

$T_{CORRECTION} = [1 + MFR\_IIN\_CAL\_GAIN\_TC \bullet 1E^{-6} \bullet (READ\_TEMPERATURE\_2 - 25.0)]$

Note:

$T_{CORRECTION}$ is limited by hardware to a value between 0.25 and 4.0.

READ_TEMPERATURE_2 is the internal die temperature.

Mfr_ein_config_iin_range[1:0] may be used to minimize noise in systems with low sense resistor values.

MFR_IIN_CAL_GAIN_TC

The MFR_IIN_CAL_GAIN_TC sets the temperature coefficient of the MFR_IIN_CAL_GAIN register value in ppm/°C. This command uses the internal die temperature.

Refer to MFR_IIN_CAL_GAIN for details on proper usage.

MFR_IOUT_CAL_GAIN_TC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iin_cal_gain_tc	16-bit twos complement integer representing the temperature coefficient. Value = Y where Y = b[15:0] is a twos complement number. Example: Mfr_iin_cal_gain_tc = 3900ppm For b[15:0] = 0x0F3C Value = 3900

PMBus COMMAND DESCRIPTION

OUTPUT VOLTAGE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VOUT_MODE	0x20	Output voltage data format and mantissa exponent (2^{-13}).	R Byte	Y	Reg			0x13	86
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	Pg00: 1.0 0x2000 Pg01: 1.2 0x2666 Pg02: 1.8 0x399A Pg03: 0.9 0x1CCD	86
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	Pg00: 4.0 0x8000 Pg01: 6.0 0xC000 Pg02: 6.0 0xC000 Pg03: 4.0 0x8000	86
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	Pg00: 1.05 0x219A Pg01: 1.26 0x2852 Pg02: 1.89 0x3C7B Pg03: 0.945 0x1E3E	86
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	Pg00: 0.95 0x1E66 Pg01: 1.14 0x247A Pg02: 1.71 0x36B9 Pg03: 0.855 0x1B5C	86
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	Pg00: 1.10 0x2333 Pg01: 1.32 0x2A3D Pg02: 1.98 0x3F5D Pg03: 0.99 0x1FAE	86
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	Pg00: 1.07 0x2266 Pg01: 1.29 0x2947 Pg02: 1.94 0x3DEC Pg03: 0.97 0x1EF6	86
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	Pg00: 0.93 0x1D9A Pg01: 1.11 0x2385 Pg02: 1.67 0x3548 Pg03: 0.83 0x1AA4	86
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for Ton_max_fault and power good de-assertion.	R/W Word	Y	L16	V	Y	Pg00: 0.90 0x1CCD Pg01: 1.08 0x228F Pg02: 1.62 0x33D7 Pg03: 0.81 0x19EC	86
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	Pg00: 0.96 0x1EB8 Pg01: 1.15 0x24DD Pg02: 1.73 0x374C Pg03: 0.86 0x1BA6	86
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted when Mfr_config_all_pwrgd_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	Pg00: 0.94 0x1E14 Pg01: 1.13 0x2418 Pg02: 1.69 0x3625 Pg03: 0.85 0x1B13	86
MFR_VOUT_DISCHARGE_THRESHOLD	0xE9	Coefficient used to multiply VOUT_COMMAND in order to determine V_{OUT} off threshold voltage.	R/W Word	Y	L11		Y	2.0 0xC200	86
MFR_DAC	0xE0	Manufacturer register that contains the code of the 10-bit DAC.	R/W Word	Y	Reg			0x01FF	86

PMBus COMMAND DESCRIPTION

VOUT_MODE

This command is read only and specifies the mode and exponent for all commands with a L16 data format. See Data Formats on page 35.

VOUT_MODE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:5]	Vout_mode_type	Reports linear mode. Hard-wired to 000b.
b[4:0]	Vout_mode_parameter	Linear mode exponent. 5-bit two's complement integer. Hardwired to 0x13 (–13 decimal).

VOUT_COMMAND, VOUT_MAX, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, VOUT_OV_FAULT_LIMIT, VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT, POWER_GOOD_ON and POWER_GOOD_OFF

These commands provide various servo, margining and supervising limits for a channel's output voltage.

MFR_VOUT_DISCHARGE_THRESHOLD

This register contains the coefficient that multiplies VOUT_COMMAND in order to determine the OFF threshold voltage for the associated output. If the output voltage has not decayed below MFR_VOUT_DISCHARGE_THRESHOLD • VOUT_COMMAND prior to the channel being commanded to enter/re-enter the ON state, the Status_mfr_discharge bit in the STATUS_MFR_SPECIFIC register will be set and the $\overline{\text{ALERT}}$ pin will be asserted low. In addition, the channel will not enter the ON state until the output has decayed below its off-threshold voltage. Setting this to a value greater than 1.0 effectively disables DISCHARGE_THRESHOLD checking, allowing the channel to turn back on even if it has not decayed at all.

Other channels can be held-off if a particular output has failed to discharge by using the bidirectional $\overline{\text{FAULT}}$*n* pins (refer to the MFR_FAULTB*n*_RESPONSE and MFR_FAULTB*n*_PROPOGATE registers).

MFR_DAC

This command register allows the user to directly program the 10-bit DAC. Manual DAC writes require the channel to be in the ON state,TON_RISE to have expired and MFR_CONFIG_LTM4673 b[5:4] = 10b or 11b. Writing MFR_CONFIG_LTM4673 b[5:4] = 10b commands the DAC to hard connect with the value in Mfr_dac_direct_val. Writing b[5:4] = 11b commands the DAC to soft connect. Once the DAC has soft connected, Mfr_dac_direct_val returns the value that allowed the DAC to be connected without perturbing the power supply. MFR_DAC writes are ignored when MFR_CONFIG_LTM4673 b[5:4] = 00b or 01b.

MFR_DAC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:10]	Reserved	Read only, always returns 0.
b[9:0]	Mfr_dac_direct_val	DAC code value.

PMBus COMMAND DESCRIPTION

OUTPUT CURRENT COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R Word	Y	L11	mΩ	Y	Trimmed; (typical) Pg00: (2.85mΩ) Pg01: (15.5mΩ) Pg02: (15.5mΩ) Pg03: (2.85mΩ)	87
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	Pg00: 17 0xDA20 Pg01: 8 0xD200 Pg02: 8 0xD200 Pg03: 17 0xDA20	88
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	Pg00: 13 0xD340 Pg01: 6 0xCB00 Pg02: 6 0xCB00 Pg03: 13 0xD340	88
IOUT_UC_FAULT_LIMIT	0x4B	Output undercurrent fault limit. Used to detect a reverse current and must be a negative value.	R/W Word	Y	L11	A	Y	Pg00: –3 0xC500 Pg01: –1.5 0xBD00 Pg02: –1.5 0xBD00 Pg03: –3 0xC500	88
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient applied to IOUT_CAL_GAIN.	R Word	Y	CF	ppm	Y	3900 0x0F3C	88

IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the same value as the resistance of the resistor (units are expressed in mΩ). IOUT_CAL_GAIN is internally limited to values between 0.01mΩ to 1,000mΩ. The register readback value always returns what was last written and does not reflect internal limiting.

Calculations using IOUT_CAL_GAIN are:

$$V_{IOUT\_OC\_FAULT\_LIMIT} = IOUT\_OC\_FAULT\_LIMIT \bullet IOUT\_CAL\_GAIN \bullet T_{CORRECTION}$$

$$V_{IOUT\_UC\_FAULT\_LIMIT} = IOUT\_UC\_FAULT\_LIMIT \bullet IOUT\_CAL\_GAIN \bullet T_{CORRECTION}$$

where:

$$T_{CORRECTION} = (1 + MFR\_IOUT\_CAL\_GAIN\_TC \bullet 1E^{-6} \bullet (READ\_TEMPERATURE\_1 + MFR\_T\_SELF\_HEAT - 25.0))$$

$$READ\_IOUT = \frac{V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}}{(IOUT\_CAL\_GAIN) \bullet T_{CORRECTION}} \qquad (23)$$

Note:

$T_{CORRECTION}$ is limited by hardware to a value between 0.25 and 4.0.

READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if the associated T_{SENSE} network fails to detect a valid temperature. See READ_TEMPERATURE_1 for more information.

PMBus COMMAND DESCRIPTION

IOUT_OC_FAULT_LIMIT, IOUT_OC_WARN_LIMIT and IOUT_UC_FAULT_LIMIT

I_{OUT} supervisor fault and warning limits.

IOUT_OC_FAULT_LIMIT is internally limited to values greater or equal to zero. The register readback value always returns what was last written and does not reflect internal limiting.

IOUT_UC_FAULT_LIMIT is internally limited to values less than zero. The register readback value always returns what was last written and does not reflect internal limiting.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC is a paged command that sets the temperature coefficient of the IOUT_CAL_GAIN register value in ppm/°C. This command uses the temperature measured by the external temperature diode for the associated page.

Refer to IOUT_CAL_GAIN for details on proper usage.

MFR_IOUT_CAL_GAIN_TC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_cal_gain_tc	16-bit twos complement integer representing the temperature coefficient. Value = Y where Y = b[15:0] is a twos complement. Example: Mfr_iout_cal_gain_tc = 3900ppm For b[15:0] = 0x0F3C Value = 3900

EXTERNAL TEMPERATURE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit setting for the external temperature sensor.	R/W Word	Y	L11	°C	Y	128 0xF200	89
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor	R/W Word	Y	L11	°C	Y	125 0xEBE8	89
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	–20.0 0xDD80	89
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	–45.0 0xE530	89
MFR_TEMP_1_GAIN	0xF8	Inverse of external diode temperature non ideality factor. One LSB = 2^{-14}.	R/W Word	Y	CF		Y	1 0x4000	89
MFR_TEMP_1_OFFSET	0xF9	Offset value for the external temperature.	R/W Word	Y	L11	°C	Y	0 0x8000	89
MFR_T_SELF_HEAT	0xB8	Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor.	R Word	Y	L11	°C		NA	89
MFR_IOUT_CAL_GAIN_TAU_INV	0xB9	Inverse of time constant for Mfr_t_self_heat changes scaled by 4 • tCONV_SENSE.	R/W Word	Y	L11		Y	0.0 0x8000	89
MFR_IOUT_CAL_GAIN_THETA	0xBA	Thermal resistance from inductor core to point measured by external temperature sensor.	R/W Word	Y	L11	°C/W	Y	0.0 0x8000	89

PMBus COMMAND DESCRIPTION

OT_FAULT_LIMIT, OT_WARN_LIMIT, UT_WARN_LIMIT and UT_FAULT_LIMIT

These commands provide supervising limits for temperature as measured by the external diode.

MFR_TEMP_1_GAIN and MFR_TEMP_1_OFFSET

The MFR_TEMP_1_GAIN command specifies the inverse of the temperature sensor ideality factor. The MFR_TEMP_1_OFFSET allows an offset to be applied to the measured temperature.

Calculations using these paged commands are:

$$READ\_TEMPERATURE\_1 = T_{EXT} \bullet MFR\_TEMP\_1\_GAIN - 273.15 + MFR\_TEMP\_1\_OFFSET$$

where:

T_{EXT} = Measured external temperature in degrees Kelvin.

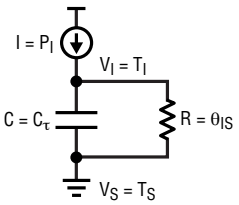
READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if the associated T_{SENSE} network fails to detect a valid temperature. Under these conditions MFR_TEMP_1_GAIN and MFR_TEMP_1_OFFSET will have no effect. See READ_TEMPERATURE_1 for more information.

MFR_TEMP_1_GAIN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_temp_1_gain[15:0]	16-bit integer representing inverse of temperature non-ideality factor. Value = Y • 2^{14} where Y = b[15:0] is an unsigned integer. Example: MFR_TEMP_1_GAIN = 1.0 For b[15:0] = 0x4000 Value = 16384 • 2^{-14} = 1.0

MFR_T_SELF_HEAT, MFR_IOUT_CAL_GAIN_TAU_INV and MFR_IOUT_CAL_GAIN_THETA

The LTM4673 uses an innovative (patent pending) algorithm to dynamically model the temperature rise from the external temperature sensor to the inductor core. This temperature rise is called MFR_T_SELF_HEAT and is used to calculate the final temperature correction required by IOUT_CAL_GAIN. The temperature rise is a function of the power dissipated in the inductor DCR, the thermal resistance from the inductor core to the remote temperature sensor and the thermal time constant of the inductor to board system. The algorithm simplifies the placement requirements for the external temperature sensor and compensates for the significant steady state and transient temperature error from the inductor core to the primary inductor heat sink.



P_I = CURRENT REPRESENTING THE POWER DISSIPATED BY THE INDUCTOR (V_{DCR} • READ_IOUT WHERE $V_{DCR} = (V_{ISENSEP} - V_{ISENSM})$)

C_τ = CAPACITANCE REPRESENTING THERMAL HEAT CAPACITY OF THE INDUCTOR (INCLUDED IN MFR_IOUT_CAL_GAIN_TAU_INV)

T_I = VOLTAGE REPRESENTING THE TEMPERATURE OF THE INDUCTOR

θ_{IS} = RESISTANCE REPRESENTING THE THERMAL RESISTANCE FROM THE DCR TO THE REMOTE TEMPERATURE SENSOR (MFR_IOUT_CAL_GAIN_THETA)

T_S = VOLTAGE REPRESENTING THE TEMPERATURE AT THE REMOTE TEMPERATURE SENSOR

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Figure 57. Electronic Analogy for Inductor Temperature Model

PMBus COMMAND DESCRIPTION

The best way to understand the self-heating effect inside the inductor is to model the system using the circuit analogy of Figure 57. The 1st order differential equation for the above model may be approximated by the following difference equation:

$P_I - T_I/\theta_{IS} = C_\tau\ \Delta T_I/\Delta t$ (Eq1) (when $T_S = 0$)

from which:

$\Delta T_I = \Delta t\ (P_I\ \theta_{IS} - T_I)/(\theta_{IS}\ C_\tau)$ (Eq2) or

$\Delta T_I = (P_I\ \theta_{IS} - T_I) \bullet \tau_{INV}$ (Eq3)

where

$\tau_{INV} = \Delta t/(\theta_{IS}\ C_\tau)$ (Eq4)

and Δt is the sample period of the external temperature ADC.

The LTM4673 implements the self-heating algorithm using Eq3 and Eq4 where:

$\Delta T_I = \Delta$MFR_T_SELF_HEAT

P_I = READ_IOUT • ($V_{ISENSEP} - V_{ISENSEM}$)

T_S = READ_TEMPERATURE_1

T_I = MFR_T_SELF_HEAT + T_S

$\Delta t = 4 \bullet t_{CONV\_SENSE}$. (One complete external temperature loop period)

τ_{INV} = MFR_IOUT_CAL_GAIN_TAU_INV

θ_{IS} = MFR_IOUT_CAL_GAIN_THETA

Initially self heat is set to zero. After each temperature measurement self heat is updated to be the previous value of self heat incremented or decremented by ΔMFR_T_SELF_HEAT.

The actual value of C_τ is not required. The important quantity is the thermal time constant $\tau_{INV} = (\theta_{IS}\ C_\tau)$. For example, if an inductor has a thermal time constant τ_{INV} = 5 seconds then:

MFR_IOUT_CAL_GAIN_TAU_INV = $(4 \bullet t_{CONV\_SENSE})/5 = 4 \bullet 66ms/5s = 0.0528$

Refer to the application section for more information on calibrating θ_{IS} and τ_{INV}.

READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if the associated T_{SENSE} network fails to detect a valid temperature. Under these conditions T_S = READ_TEMPERATURE_2 and the self-heating correction is applied using the internal die temperature. See READ_TEMPERATURE_1 for more information.

MFR_T_SELF_HEAT Data Content

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_t_self_heat	Values are limited to the range 0°C to 50°C.

MFR_IOUT_CAL_GAIN_THETA Data Content

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_cal_gain_theta	Values ≤ 0 set MFR_T_SELF_HEAT to zero.

PMBus COMMAND DESCRIPTION

MFR_IOUT_CAL_GAIN_TAU_INV Data Content

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_cal_gain_tau_inv	Values ≤ 0 set MFR_T_SELF_HEAT to zero. Values ≥ 1 set MFR_T_SELF_HEAT to MFR_IOUT_CAL_GAIN_THETA • READ_IOUT • ($V_{ISENSEP}$ – $V_{ISENSEM}$).

SEQUENCING TIMING LIMITS AND CLOCK SHARING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to RUN pin = ON.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	91
TON_RISE	0x61	Time from when the RUN pin goes high until the LTM4673 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	ms	Y	10.0 0xD280	91
TON_MAX_FAULT_LIMIT	0x62	Maximum time from RUN pin on assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	ms	Y	15.0 0xD3C0	91
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to RUN pin = OFF.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	91
MFR_RESTART_DELAY	0xDC	Delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W Word	N	L11	ms	Y	400 0xFB20	92

TON_DELAY, TON_RISE, TON_MAX_FAULT_LIMIT and TOFF_DELAY

These commands share the same format and provide sequencing and timer fault and warning delays in ms.

TON_DELAY sets the amount of time in milliseconds that a channel waits following the start of an ON sequence before its RUN pin enables a DC/DC converter. This delay is counted using SHARECLK only.

TON_RISE sets the amount of time in ms that elapses after the power supply has been enabled until the LTM4673's DAC soft connects and servos the output voltage to the desired level if Mfr_dac_mode = 00b. This delay is counted using SHARECLK only.

TON_MAX_FAULT_LIMIT is the maximum amount of time that the power supply being controlled by the LTM4673 can attempt to power up the output without reaching the VOUT_UV_FAULT_LIMIT. If it does not, then a TON_MAX_FAULT is declared. If the output reaches VOUT_UV_FAULT_LIMIT prior to TON_MAX_FAULT_LIMIT, the LTM4673 unmasks the VOUT_UV_FAULT_LIMIT threshold. (Note that a value of zero means there is no limit to how long the power supply can attempt to bring up its output voltage.) This delay is counted using SHARECLK only.

TOFF_DELAY is the amount of time that elapses after the CONTROL pin and/or OPERATION command is de-asserted until the channel is disabled (soft-off). This delay is counted using SHARECLK if available, otherwise the internal oscillator is used.

All of the above TON and TOFF delays are internally limited to 655ms, and rounded to the nearest 10µs. The read value of these commands always returns what was last written and does not reflect internal limiting.

PMBus COMMAND DESCRIPTION

MFR_RESTART_DELAY

This command essentially sets the off time of a CONTROL pin initiated restart. If the CONTROL pin is toggled off for at least 10µs then on, all dependent channels are disabled, held off for a time = Mfr_restart_delay, then sequenced back on. CONTROL pin transitions whose OFF time exceeds Mfr_restart_delay are not affected by this command. A value of all zeros disables this feature. This delay is counted using SHARECLK only.

This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

Clock Sharing

Multiple ADI PMBus devices can synchronize their clocks in an application by connecting together the open-drain SHARECLK input/outputs to a pull-up resistor as a wired OR. In this case the fastest clock will take over and synchronize all other chips to its falling edge.

SHARECLK can optionally be used to synchronize ON/OFF dependency on V_{IN} across multiple chips by setting the Mfr_config_all_vin_share_enable bit of the MFR_CONFIG_ALL register. When configured this way the chip will hold SHARECLK low when the unit is off for insufficient input voltage, and upon detecting that SHARECLK is held low the chip will disable all channels after a brief deglitch period. When the SHARECLK pin is allowed to rise, the chip will respond by beginning a start sequence. In this case the slowest VIN_ON detection will take over and synchronize other chips to its start sequence.

WATCHDOG TIMER AND POWER GOOD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_PWRGD_EN	0xD4	Configuration that maps WDI/$\overline{\text{RESET}}$ status and individual channel power good to the PWRGD pin.	R/W Word	N	Reg		Y	0x0000	92
MFR_POWERGOOD_ASSERTION_DELAY	0xE1	Power-good output assertion delay.	R/W Word	N	L11	ms	Y	100 0xEB20	93
MFR_WATCHDOG_T_FIRST	0xE2	First watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	93
MFR_WATCHDOG_T	0xE3	Watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	93

MFR_PWRGD_EN

This command register controls the mapping of the watchdog and channel power good status to the PWRGD pin.

MFR_PWRGD_EN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:9]	Reserved	Read only, always returns 0s.
b[8]	Mfr_pwrgd_en_wdog	Watchdog. 1 = Watchdog timer not-expired status is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = Watchdog timer does not affect the PWRGD pin.
b[7:4]	Reserved	Always returns 0000b.
b[3]	Mfr_pwrgd_en_chan3	Channel 3. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.

PMBus COMMAND DESCRIPTION

MFR_PWRGD_EN Data Contents

BIT(S)	SYMBOL	OPERATION
b[2]	Mfr_pwrgd_en_chan2	Channel 2. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.
b[1]	Mfr_pwrgd_en_chan1	Channel 1. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.
b[0]	Mfr_pwrgd_en_chan0	Channel 0. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.

MFR_POWERGOOD_ASSERTION_DELAY

This command register allows the user to program the delay from when the internal power-good signal becomes valid until the power-good output is asserted. This delay is counted using SHARECLK if available, otherwise the internal oscillator is used. This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

The power good de-assertion delay and threshold source is controlled by Mfr_config_all_pwrgd_off_uses_uv. Systems that require a fast power good de-assertion should set Mfr_config_all_pwrgd_off_uses_uv = 1. This uses the VOUT_UV_FAULT_LIMIT and the high speed comparator to de-assert the PWRGD pin. Systems that require a separate power good off threshold should set Mfr_config_all_pwrgd_off_uses_uv = 0. This uses the slower ADC polling loop and POWER_GOOD_OFF to de-assert the PWRGD pin.

Watchdog Operation

A non-zero write to the MFR_WATCHDOG_T register will reset the watchdog timer. Low-to-high transitions on the WDI/$\overline{\text{RESET}}$ pin also reset the watchdog timer. If the timer expires, $\overline{\text{ALERT}}$ is asserted and the PWRGD output is optionally de-asserted and then reasserted after MFR_PWRGD_ASSERTION_DELAY ms. Writing 0 to either the MFR_WATCH_DOG_T or MFR_WATCHDOG_T_FIRST registers will disable the timer.

MFR_WATCHDOG_T_FIRST and MFR_WATCHDOG_T

The MFR_WATCHDOG_T_FIRST register allows the user to program the duration of the first watchdog timer interval following assertion of the PWRGD pin, assuming the PWRGD pin reflects the status of the watchdog timer. If assertion of PWRGD is not conditioned by the watchdog timer's status, then MFR_WATCHDOG_T_FIRST applies to the first timing interval after the timer is enabled. Writing a value of 0ms to the MFR_WATCHDOG_T_FIRST register disables the watchdog timer. This delay is internally limited to 65 seconds and rounded to the nearest 1ms.

The MFR_WATCHDOG_T register allows the user to program watchdog timer intervals subsequent to the MFR_WATCHDOG_T_FIRST timing interval. Writing a value of 0ms to the MFR_WATCHDOG_T register disables the watchdog timer. This delay is internally limited to 655ms and rounded to the nearest 10µs.

Both timers operate on an internal clock independent of SHARECLK. The read value of both commands always returns what was last written and does not reflect internal limiting.

PMBus COMMAND DESCRIPTION

FAULT RESPONSES

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	94
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	94
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	95
IOUT_UC_FAULT_RESPONSE	0x4C	Action to be taken by the device when an output undercurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	95
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	96
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	96
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	96
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	96
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	97
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	N	L11	ms	Y	200 0xF320	97
MFR_RETRY_COUNT	0xF7	Retry count for all faulted off conditions that enable retry.	R/W Byte	N	Reg		Y	0x07	97

Clearing Latched Faults

Latched faults are reset by toggling the CONTROL pin, using the OPERATION command, or removing and reapplying the bias voltage to the V_{INSNS} pin. All fault and warning conditions result in the $\overline{ALERT}$ pin being asserted low and the corresponding bits being set in the status registers. The CLEAR_FAULTS command resets the contents of the status registers and de-asserts the $\overline{ALERT}$ output. The CLEAR_FAULTS does not clear a faulted off state nor allow a channel to turn back on.

VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE

The fault response documented here is for voltages that are measured by the high speed supervisor. These voltages are measured over a short period of time and may require a deglitch period. Note that in addition to the response described by these commands, the LTM4673 will also:

- Set the appropriate bit(s) in the STATUS_BYTE.
- Set the appropriate bit(s) in the STATUS_WORD.
- Set the appropriate bit in the corresponding STATUS_VOUT register, and
- Notify the host by pulling the $\overline{ALERT}$ pin low.

PMBus COMMAND DESCRIPTION

VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Vout_ov_fault_response_action, Vout_uv_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b: The unit continues operating for the delay time specified by bits[2:0] in increments of t_{S_VS}. See Electrical Characteristics Table. If the fault is still present at the end of the delay time, the unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chan*n*). After shutting down, the device responds according to the retry settings in bits [5:3]. 10b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chan*n*). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Vout_ov_fault_response_retry, Vout_uv_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next OFF-then-ON sequence on that channel.
b[2:0]	Vout_ov_fault_response_delay, Vout_uv_fault_response_delay	This sample count determines the amount of time a unit is to ignore a fault after it is first detected. Use this delay to deglitch fast faults. 000b: There is no additional deglitch delay applied to fault detection. 001b-111b: The fault is deglitched for deglitch period of b[2:0] samples at a sampling period of tS_VS (12.2µs typical).

IOUT_OC_FAULT_RESPONSE and IOUT_UC_FAULT_RESPONSE

The fault response documented here is for currents that are measured by the high speed supervisor. These currents are measured over a short period of time and may require a deglitch period. Note that in addition to the response described by these commands, the LTM4673 will also:

- Set the appropriate bit in the STATUS_BYTE.
- Set the appropriate bit in the STATUS_WORD.
- Set the appropriate bit in the corresponding STATUS_IOUT register, and
- Notify the host by pulling the $\overline{\text{ALERT}}$ pin low.

IOUT_OC_FAULT_RESONSE and IOUT_UC_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Iout_oc_fault_response_action, Iout_uc_fault_response_action	Response action: 00b and 01b: The unit continues operation without interruption. Note that the current will not be limited to the value of Iout_oc_fault_limit or Iout_uc_fault_limit. 10b: The unit continues operating for the delay time specified by bits [2:0]. If the fault is still present at the end of the delay time, the unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chan*n*). After shutting down, the device responds according to the retry settings in bits [5:3]. Note that the current will not be limited to the value of Iout_oc_fault_limit or Iout_uc_fault_limit. 11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chan*n*). After shutting down, the device responds according to the retry settings in bits [5:3].

PMBus COMMAND DESCRIPTION

IOUT_OC_FAULT_RESONSE and IOUT_UC_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[5:3]	Iout_oc_fault_response_retry, Iout_uc_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded off (by the control pin or operation command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next OFF-then-ON sequence on that channel.
b[2:0]	Iout_oc_fault_response_delay, Iout_uc_fault_response_delay	This sample count determines the amount of time a unit is to ignore a fault after it is first detected. Use this delay to deglitch fast faults. 000b: There is no additional deglitch delay applied to fault detection. 001b-111b: The fault is deglitched for the interval selected by b[2:0] as follows.

b[2:0]	Deglitch interval
001b	100µs
010b	1ms
011b	5ms
100b	10ms
101b	20ms
110b	50ms
111b	100ms

OT_FAULT_RESPONSE, UT_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE and VIN_UV_FAULT_RESPONSE

The fault response documented here is for values that are measured by the ADC. Note that in addition to the response described by these commands, the LTM4673 will also:

- Set the appropriate bit(s) in the STATUS_BYTE.
- Set the appropriate bit(s) in the STATUS_WORD.
- Set the appropriate bit in the corresponding STATUS_VIN or STATUS_TEMPERATURE register, and
- Notify the host by pulling the $\overline{\text{ALERT}}$ pin low.

OT_FAULT_RESPONSE, UT_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, VIN_UV_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ot_fault_response_action, Ut_fault_response_action, Vin_ov_fault_response_action, Vin_uv_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chan*n*). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Ot_fault_response_retry, Ut_fault_response_retry, Vin_ov_fault_response_retry, Vin_uv_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next OFF-then-ON sequence on that channel.
b[2:0]	Ot_fault_response_delay, Ut_fault_response_delay, Vin_ov_fault_response_delay, Vin_uv_fault_response_delay	Hard coded to 000b: There is no additional deglitch delay applied to fault detection.

PMBus COMMAND DESCRIPTION

TON_MAX_FAULT_RESPONSE

This command defines the LTM4673 response to a TON_MAX_FAULT. It may be used to protect against a short-circuited output at startup. After startup use VOUT_UV_FAULT_RESPONSE to protect against a short-circuited output.

The device also:

- Sets the HIGH_BYTE bit in the STATUS_BYTE,
- Sets the VOUT bit in the STATUS_WORD,
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT register, and
- Notifies the host by asserting $\overline{\text{ALERT}}$.

TON_MAX_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ton_max_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chan*n*). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Ton_max_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next OFF-then-ON sequence on that channel.
b[2:0]	Ton_max_fault_response_delay	Hard coded to 000b: There is no additional deglitch delay applied to fault detection.

MFR_RETRY_DELAY

This command determines the retry interval when the LTM4673 is in retry mode in response to a fault condition. This delay is counted using SHARECLK only. This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

MFR_RETRY_COUNT

The MFR_RETRY_COUNT is a global command that sets the number of retries attempted when any channel faults off with its fault response retry field set to a non zero value.

In the event of multiple or recurring retry faults on the same channel the total number of retries equals MFR_RETRY_COUNT. If a channel has not been faulted off for at least 16 seconds, its retry counter is cleared. Toggling a channel's CONTROL pin off then on or issuing OPERATION off then on commands will synchronously clear the retry count.

MFR_RETRY_COUNT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:3]	Reserved	Always returns zero.
b[2:0]	Mfr_retry_count [2:0]	0: No retries: 1-6: Number of retries. 7: Infinite retries. Changing the value might not take effect until the next OFF-then-ON sequence on that channel.

PMBus COMMAND DESCRIPTION

SHARED EXTERNAL FAULTS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_FAULTB0_PROPAGATE	0xD2	Configuration that determines if a channels faulted off state is propagated to the $\overline{\text{FAULT}}$0 pin.	R/W Byte	Y	Reg		Y	0x00	98
MFR_FAULTB1_PROPAGATE	0xD3	Configuration that determines if a channels faulted off state is propagated to the $\overline{\text{FAULT}}$1 pin.	R/W Byte	Y	Reg		Y	0x00	98
MFR_FAULTB0_RESPONSE	0xD5	Action to be taken by the device when the $\overline{\text{FAULT}}$0 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	98
MFR_FAULTB1_RESPONSE	0xD6	Action to be taken by the device when the $\overline{\text{FAULT}}$1 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	98

MFR_FAULTB0_PROPAGATE and MFR_FAULTB1_PROPAGATE

These manufacturer specific commands enable channels that have faulted off to propagate that state to the appropriate fault pin. MFR_FAULTB0_PROPAGATE allows any channel's faulted off state to propagate to the $\overline{\text{FAULT}}$0 pin. MFR_FAULTB1_PROPAGATE allows any channel's faulted off state to propagate to the $\overline{\text{FAULT}}$1 pin.

Note that pulling a fault pin low will have no effect for channels that have MFR_FAULTBn_RESPONSE set to 0. The channel continues operation without interruption. This fault response is called Ignore (0x0) in LTpowerPlay.

MFR_FAULT0_PROPAGATE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb0_propagate	Enable fault propagation. 0: Channel's faulted off state does not assert $\overline{\text{FAULT}}$0 low. 1 :Channel's faulted off state asserts $\overline{\text{FAULT}}$0 low.

MFR_FAULT1_PROPAGATE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb1_propagate	Enable fault propagation. 0: Channel's faulted off state does not assert $\overline{\text{FAULT}}$1 low. 1: Channel's faulted off state asserts $\overline{\text{FAULT}}$1 low.

MFR_FAULTB0_RESPONSE and MFR_FAULTB1_RESPONSE

These manufacturer specific commands share the same format and specify the response to assertions of the $\overline{\text{FAULT}}$ pins. MFR_FAULTB0_RESPONSE determines which channels shut off when the $\overline{\text{FAULT}}$ pin is asserted low and MFR_FAULTB1_RESPONSE determines which channels shut off when the $\overline{\text{FAULT}}$ pin is asserted low. When a channel shuts off in response to a $\overline{\text{FAULT}}$*n* pin, the $\overline{\text{FAULT}}$ pin is asserted low and the appropriate bit is set in the STATUS_MFR_SPECIFIC register. For a graphical explanation, see the switches on the left hand side of Figure 31: Channel Fault Management Block Diagram.

Faults will not propagate for channels that have MFR_FAULTB*n*_RESPONSE set to 0: The channel continues operation without interruption. Note that this fault response is called No Action in LTpowerPlay.

PMBus COMMAND DESCRIPTION

MFR_FAULTB0_RESPONSE and MFR_FAULTB1_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:4]	Reserved	Read only, always returns 0000b.
b[3]	Mfr_faultb0_response_chan3, Mfr_faultb1_response_chan3	Channel 3 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding $\overline{\text{FAULT}}$ pin is still asserted after 10µs. When the $\overline{\text{FAULT}}$ pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[2]	Mfr_faultb0_response_chan2, Mfr_faultb1_response_chan2	Channel 2 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding $\overline{\text{FAULT}}$ pin is still asserted after 10µs. When the $\overline{\text{FAULT}}$ pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[1]	Mfr_faultb0_response_chan1, Mfr_faultb1_response_chan1	Channel 1 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding $\overline{\text{FAULT}}$ pin is still asserted after 10µs. When the $\overline{\text{FAULT}}$ pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[0]	Mfr_faultb0_response_chan0, Mfr_faultb1_response_chan0	Channel 0 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding $\overline{\text{FAULT}}$ pin is still asserted after 10µs. When the $\overline{\text{FAULT}}$ pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.

FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	99
STATUS_BYTE	0x78	One-byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	100
STATUS_WORD	0x79	Two-byte summary of the unit's fault condition.	R Word	Y	Reg			NA	100
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	101
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	101
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	101
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	102
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	102
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	103
MFR_PADS	0xE5	Current state of selected digital I/O pads.	R/W Word	N	Reg			NA	103
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	104

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear status bits that have been set. This command clears all fault and warning bits in all unpaged status registers, and paged status registers selected by the current PAGE setting. At the same time, the device negates (clears, releases) its contribution to $\overline{\text{ALERT}}$.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. See Clearing Latched Faults for more information.

If the fault is present after the fault is cleared, the fault status bit will be set again and the host notified by the usual means.

Note: this command responds to the global page command. (PAGE=0xFF)

PMBus COMMAND DESCRIPTION

STATUS_BYTE

The STATUS_BYTE command returns the summary of the most critical faults or warnings which have occurred, as shown in the following table. STATUS_BYTE is a subset of STATUS_WORD and duplicates the same information.

STATUS_BYTE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_byte_busy	Same as Status_word_busy.
b[6]	Status_byte_off	Same as Status_word_off.
b[5]	Status_byte_vout_ov	Same as Status_word_vout_ov.
b[4]	Status_byte_iout_oc	Same as Status_word_iout_oc.
b[3]	Status_byte_vin_uv	Same as Status_word_vin_uv.
b[2]	Status_byte_temp	Same as Status_word_temp.
b[1]	Status_byte_cml	Same as Status_word_cml.
b[0]	Status_byte_high_byte	Same as Status_word_high_byte.

STATUS_WORD

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate detailed status register.

The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command.

STATUS_WORD Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Status_word_vout	An output voltage fault or warning has occurred. See STATUS_VOUT.
b[14]	Status_word_iout	An output current fault or warning has occurred. See STATUS_IOUT.
b[13]	Status_word_input	An input voltage fault or warning has occurred. See STATUS_INPUT.
b[12]	Status_word_mfr	A manufacturer specific fault has occurred. See STATUS_MFR._SPECIFIC.
b[11]	Status_word_power_not_good	The PWRGD pin, if enabled, is negated. Power is not good.
b[10]	Status_word_fans	Not supported. Always returns 0.
b[9]	Status_word_other	Not supported. Always returns 0.
b[8]	Status_word_unknown	Not supported. Always returns 0.
b[7]	Status_word_busy	Device busy when PMBus command received. See OPERATION: Processing Commands.
b[6]	Status_word_off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. The off-bit is clear if unit is allowed to provide power to the output.
b[5]	Status_word_vout_ov	An output overvoltage fault has occurred.
b[4]	Status_word_iout_oc	An output overcurrent fault has occurred.
b[3]	Status_word_vin_uv	A V_{IN} undervoltage fault has occurred.
b[2]	Status_word_temp	A temperature fault or warning has occurred. See STATUS_TEMPERATURE.
b[1]	Status_word_cml	A communication, memory or logic fault has occurred. See STATUS_CML.
b[0]	Status_word_high_byte	A fault/warning not listed in b[7:1] has occurred.

PMBus COMMAND DESCRIPTION

STATUS_VOUT

The STATUS_VOUT command returns the summary of the output voltage faults or warnings which have occurred, as shown in the following table:

STATUS_VOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_vout_ov_fault	Overvoltage fault.
b[6]	Status_vout_ov_warn	Overvoltage warning.
b[5]	Status_vout_uv_warn	Undervoltage warning
b[4]	Status_vout_uv_fault	Undervoltage fault.
b[3]	Status_vout_max_warn	VOUT_MAX warning. An attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command. After being cleared, Status_vout_max_warn will not report additional warnings until a channel state transition (off-then-on) has been performed or a valid output voltage, lower than allowed by VOUT_MAX, has been set.
b[2]	Status_vout_ton_max_fault	TON_MAX_FAULT sequencing fault.
b[1]	Status_vout_toff_max_warn	Not supported. Always returns 0.
b[0]	Status_vout_tracking_error	Not supported. Always returns 0.

STATUS_IOUT

The STATUS_IOUT command returns the summary of the output current faults or warnings which have occurred, as shown in the following table:

STATUS_IOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_iout_oc_fault	Overcurrent fault.
b[6]	Status_iout_oc_uv_fault	Not Supported. Always returns 0.
b[5]	Status_iout_oc_warn	Overcurrent warning
b[4]	Status_iout_uc_fault	Undercurrent fault.
b[3]	Status_iout_curr_share_fault	Not Supported. Always returns 0.
b[2]	Status_pout_power_limiting	Not Supported. Always returns 0.
b[1]	Status_pout_overpower_fault	Not Supported. Always returns 0.
b[0]	Status_pout_overpower_warn	Not Supported. Always returns 0.

STATUS_INPUT

The STATUS_INPUT command returns the summary of the V_{IN} faults or warnings which have occurred, as shown in the following table:

STATUS_INPUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_input_ov_fault	V_{IN} overvoltage fault
b[6]	Status_input_ov_warn	V_{IN} overvoltage warning
b[5]	Status_input_uv_warn	V_{IN} undervoltage warning
b[4]	Status_input_uv_fault	V_{IN} undervoltage fault
b[3]	Status_input_off	Unit is off for insufficient input voltage.
b[2]	IIN overcurrent fault	Not supported. Always returns 0.

PMBus COMMAND DESCRIPTION

STATUS_INPUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[1]	IIN overcurrent warn	Not supported. Always returns 0.
b[0]	PIN overpower warn	Not supported. Always returns 0.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns the summary of the temperature faults or warnings which have occurred, as shown in the following table. Note that this information is paged and refers to the temperature of the associated external diode.

STATUS_TEMPERATURE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_temperature_ot_fault	Overtemperature fault.
b[6]	Status_temperature_ot_warn	Overtemperature warning.
b[5]	Status_temperature_ut_warn	Undertemperature warning.
b[4]	Status_temperature_ut_fault	Undertemperature fault.
b[3]	Reserved	Reserved. Always returns 0.
b[2]	Reserved	Reserved. Always returns 0.
b[1]	Reserved	Reserved. Always returns 0.
b[0]	Reserved	Reserved. Always returns 0.

STATUS_CML

The STATUS_CML command returns the summary of the communication, memory and logic faults or warnings which have occurred, as shown in the following table:

STATUS_CML Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_cml_cmd_fault	1 = An illegal or unsupported command fault has occurred. 0 = No fault has occurred.
b[6]	Status_cml_data_fault	1 = Illegal or unsupported data received. 0 = No fault has occurred.
b[5]	Status_cml_pec_fault	1 = A packet error check fault has occurred. Note: PEC checking is always active in the LTM4673. Any extra byte received before a STOP will set Status_cml_pec_fault unless the extra byte is a matching PEC byte. 0 = No fault has occurred.
b[4]	Status_cml_memory_fault	1 = A fault has occurred in the EEPROM. 0 = No fault has occurred.
b[3]	Status_cml_processor_fault	Not supported, always returns 0.
b[2]	Reserved	Reserved, always returns 0.
b[1]	Status_cml_pmbus_fault	1 = A communication fault other than ones listed in this table has occurred. This is a catch all category for illegally formed I^2C/SMBus commands (Example: An address byte with read =1 received immediately after a START). 0 = No fault has occurred.
b[0]	Status_cml_unknown_fault	Not supported, always returns 0.

PMBus COMMAND DESCRIPTION

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command returns manufacturer specific status flags. Bits marked CHANNEL = All are not paged. Bits marked STICKY = Yes stay set until a CLEAR_FAULTS is issued or the channel is commanded on by the user. Bits marked ALERT = Yes pull $\overline{\text{ALERT}}$ low when the bit is set. Bits marked OFF = Yes indicate that the event can be configured elsewhere to turn the channel off.

STATUS_MFR_SPECIFIC Data Contents

BIT(S)	SYMBOL	OPERATION	CHANNEL	STICKY	ALERT	OFF
b[7]	Status_mfr_discharge	1 = A V_{OUT} discharge fault occurred while attempting to enter the ON state. 0 = No V_{OUT} discharge fault has occurred.	Current Page	Yes	Yes	Yes
b[6]	Status_mfr_fault1_in	This channel attempted to turn on while the $\overline{\text{FAULT}}$1 pin was asserted low, or this channel has shut down at least once in response to a $\overline{\text{FAULT}}$1 pin asserting low since the last CONTROL pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command. If Mfr_track_en_chan*n* is set, Status_mfr_fault1_in may also be set for the channel causing the fault.	Current Page	Yes	Yes	Yes
b[5]	Status_mfr_fault0_in	This channel attempted to turn on while the $\overline{\text{FAULT}}$0 pin was asserted low, or this channel has shut down at least once in response to a $\overline{\text{FAULT}}$0 pin asserting low since the last CONTROL pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command. If Mfr_track_en_chan*n* is set, Status_mfr_fault0_in may also be set for the channel causing the fault.	Current Page	Yes	Yes	Yes
b[4]	Status_mfr_servo_target_reached	Servo target has been reached.	Current Page	No	No	No
b[3]	Status_mfr_dac_connected	DAC is connected and driving V_{DAC} pin.	Current Page	No	No	No
b[2]	Status_mfr_dac_saturated	A previous servo operation terminated with maximum or minimum DAC value.	Current Page	Yes	No	No
b[1]	Status_mfr_auxfaultb_faulted_off	AUX$\overline{\text{FAULT}}$ has been de-asserted due to a V_{OUT} or I_{OUT} fault.	All	No	No	No
b[0]	Status_mfr_watchdog_fault	1 = A watchdog fault has occurred. 0 = No watchdog fault has occurred.	All	Yes	Yes	No

MFR_PADS

The MFR_PADS command provides read-only access of digital pads (pins). The input values are before any deglitching logic.

MFR_PADS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_pads_pwrgd_drive	0 = PWRGD pad is being driven low by this chip. 1 = PWRGD pad is not being driven low by this chip.
b[14]	Mfr_pads_alertb_drive	0 = $\overline{\text{ALERT}}$ pad is being driven low by this chip. 1 = $\overline{\text{ALERT}}$ pad is not being driven low by this chip.
b[13:12]	Mfr_pads_faultb_drive[1:0]	bit[1] used for $\overline{\text{FAULT}}$0 pad, bit[0] used for $\overline{\text{FAULT}}$1 pad as follows: 0 = $\overline{\text{FAULT}}$ pad is being driven low by this chip. 1 = $\overline{\text{FAULT}}$ pad is not being driven low by this chip.
b[11:10]	Reserved[1:0]	Always returns 00b.
b[9:8]	Mfr_pads_asel1[1:0]	11: Logic high detected on ASEL1 input pad. 10: ASEL1 input pad is floating. 01: Reserved. 00: Logic low detected on ASEL1 input pad.

PMBus COMMAND DESCRIPTION

MFR_PADS Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Mfr_pads_asel0[1:0]	11: Logic high detected on ASEL0 input pad. 10: ASEL0 input pad is floating. 01: Reserved. 00: Logic low detected on ASEL0 input pad.
b[5]	Mfr_pads_control1	1: Logic high detected on CONTROL1 pad. 0: Logic low detected on CONTROL1 pad.
b[4]	Mfr_pads_control0	1: Logic high detected on CONTROL0 pad. 0: Logic low detected on CONTROL0 pad.
b[3:2]	Mfr_pads_faultb[1:0]	bit[1] used for $\overline{\text{FAULT}}$0 pad, bit[0] used for $\overline{\text{FAULT}}$1 pad as follows: 1: Logic high detected on $\overline{\text{FAULT}}$ pad. 0: Logic low detected on $\overline{\text{FAULT}}$ pad.
b[1]	Mfr_pads_control2	1: Logic high detected on CONTROL2 pad. 0: Logic low detected on CONTROL2 pad.
b[0]	Mfr_pads_control3	1: Logic high detected on CONTROL3 pad. 0: Logic low detected on CONTROL3 pad.

MFR_COMMON

This command returns status information for the alert, device busy, share-clock pin (SHARECLK) and the write-protect pin (WP).

This is the only command that may still be read when the LTM4673 is busy processing an EEPROM or other command. It may be polled by the host to determine when the LTM4673 is available to process a PMBus command. A busy device will always acknowledge its address but will NACK the command byte and set Status_byte_busy and Status_word_busy when it receives a command that it cannot immediately process. $\overline{\text{ALERT}}$ will not be asserted low in this case.

MFR_COMMON Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_common_alertb	Returns alert status. 1: $\overline{\text{ALERT}}$ is de-asserted high. 0: $\overline{\text{ALERT}}$ is asserted low.
b[6]	Mfr_common_busyb	Returns device busy status. 1: The device is available to process PMBus commands. 0: The device is busy and will NACK PMBus commands.
b[5:2]	Reserved	Read only, always returns 1s.
b[1]	Mfr_common_share_clk	Returns the status of the share-clock pin. 1: Share-clock pin is being held low. 0: Share-clock pin is active.
b[0]	Mfr_common_write_protect	Returns the status of the write-protect pin. 1: Write-protect pin is high. 0: Write-protect pin is low.

PMBus COMMAND DESCRIPTION

TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	105
READ_IIN	0x89	DC/DC converter input current.	R Word	Y	L11	A		NA	105
READ_PIN	0x97	DC/DC converter input power.	R Word	Y	L11	W		NA	105
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	105
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	106
READ_TEMPERATURE_1	0x8D	Power stage temperature sensor. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	106
READ_TEMPERATURE_2	0x8E	Control IC die temperature.	R Word	N	L11	°C		NA	106
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	106
MFR_READ_IOUT	0xBB	Alternate data format for READ_IOUT. One LSB = 2.5mA.	R Word	Y	CF	2.5mA		NA	107
MFR_IIN_PEAK	0xC4	Maximum measured value of READ_IIN	R Word	Y	L11	A		NA	106
MFR_IIN_MIN	0xC5	Minimum measured value of READ_IIN.	R Word	Y	L11	A		NA	106
MFR_PIN_PEAK	0xC6	Maximum measured value of READ_PIN.	R Word	Y	L11	W		NA	106
MFR_PIN_MIN	0xC7	Minimum measured value of READ_PIN.	R Word	Y	L11	W		NA	106
MFR_IOUT_SENSE_VOLTAGE	0xFA	Absolute value of VISENSEP – VISENSEM. One LSB = 3.05µV.	R Word	Y	CF	3.05µV		NA	108
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN.	R Word	N	L11	V		NA	108
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT.	R Word	Y	L16	V		NA	108
MFR_IOUT_PEAK	0xD7	Maximum measured value of READ_IOUT.	R Word	Y	L11	A		NA	108
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	108
MFR_VIN_MIN	0xFC	Minimum measured value of READ_VIN.	R Word	N	L11	V		NA	108
MFR_VOUT_MIN	0xFB	Minimum measured value of READ_VOUT.	R Word	Y	L16	V		NA	108
MFR_IOUT_MIN	0xD8	Minimum measured value of READ_IOUT.	R Word	Y	L11	A		NA	108
MFR_TEMPERATURE_1_MIN	0xFD	Minimum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	109

READ_VIN

This command returns the most recent ADC measured value of the input voltage at the V_{INSNS} pin.

READ_IIN

This command returns the most recent ADC measured value of the input current derived from the voltage difference between the I_{INSNSP} and I_{INSNSM} pins. The READ_IIN value reported is automatically corrected to account for the range selected by Mfr_ein_config_iin_range[1:0].

READ_PIN

This command returns the most recent ADC measured value of the input power in watts. This is the product of READ_IIN and READ_VIN.

READ_VOUT

This command returns the most recent ADC measured value of the channel's output voltage.

PMBus COMMAND DESCRIPTION

READ_IOUT

This command returns the most recent ADC measured value of the channel's output current.

MFR_IIN_PEAK

This command returns the maximum ADC measured value of the input current. This register is reset to 0x7C00 (-2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_IIN_MIN

This command returns the minimum ADC measured value of the input current. This register is reset to 0x7BFF (approximately 2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_PIN_PEAK

This command returns the maximum ADC measured value of the input power. This register is reset to 0x7C00 (-2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_PIN_MIN

This command returns the minimum ADC measured value of the input power. This register is reset to 0x7BFF (approximately 2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

READ_TEMPERATURE_1

This command returns the most recent measured value of the power stage temperature sensor in °C. This value is used for all temperature related operations and calculations. This command is paged. READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if the associated T_{SENSE} network fails to detect a valid temperature.

The T_{SENSE} network will fail to detect a valid temperature under the following conditions:

The T_{SENSE} pin is shorted to a constant voltage.

The sense diode has an ideality factor greater than N_TS max.

READ_TEMPERATURE_2

This command returns the most recent ADC measured value of control IC die temperature in °C as determined by the control IC's internal temperature sensor. This register is for information purposes and does not generate any faults, warnings, or affect any other registers or internal calculations unless it is used as READ_TEMPERATURE_1. This command is not paged.

READ_TEMPERATURE_2 is substituted for READ_TEMPERATURE_1 if a channel's T_{SENSE} network fails to detect a valid temperature.

READ_POUT

This command returns the most recent ADC measured value of the channel's output power in watts.

PMBus COMMAND DESCRIPTION

MFR_READ_IOUT

This command returns the most recent ADC measured value of the channel's output current, using a custom format that provides better numeric representation granularity than the READ_IOUT command for currents whose absolute value is between 2A and 82A.

MFR_READ_IOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_read_iout[15:0]	Channel output current expressed in custom format for improved resolution at high currents. Value = Y • 2.5 where Y = b[15:0] is a signed two's-complement number. Example: MFR_READ_IOUT = 5mA For b[15:0] = 0x0002 Value = 2 • 2.5 = 5mA

The granularity of the returned value is always 2.5mA, and the return value is limited to ±81.92A. Use the READ_IOUT command for larger currents. Note that the accuracy of the returned value is always limited by the ADC Characteristics listed in the Electrical Characteristics section.

Comparison of Granularity Due to Numeric Format

CURRENT RANGE	READ_IOUT GRANULARITY	MFR_READ_IOUT GRANULARITY
$31.25mA \le I_{OUT} < 62.5mA$	61µA	2.5mA
$62.5mA \le I_{OUT} < 125mA$	122µA	2.5mA
$125mA \le I_{OUT} < 250mA$	244µA	2.5mA
$250mA \le I_{OUT} < 500mA$	488µA	2.5mA
$0.5A \le I_{OUT} < 1A$	977µA	2.5mA
$1A \le I_{OUT} < 2A$	1.95mA	2.5mA
$2A \le I_{OUT} < 4A$	3.9mA	2.5mA
$4A \le I_{OUT} < 8A$	7.8mA	2.5mA
$8A \le I_{OUT} < 16A$	15.6mA	2.5mA
$16A \le I_{OUT} < 32A$	31.3mA	2.5mA
$32A \le I_{OUT} < 64A$	62.5mA	2.5mA
$64A \le I_{OUT} < 82A$	125mA	2.5mA
$82A \le I_{OUT} < 128A$	125mA	Saturated
$128A \le I_{OUT} < 256A$	250mA	Saturated

PMBus COMMAND DESCRIPTION

MFR_IOUT_SENSE_VOLTAGE

This command returns the absolute value of the voltage measured between $I_{SENSEP}n$ and $I_{SENSEM}n$ during the last READ_IOUT ADC conversion without any temperature correction.

MFR_IOUT_SENSE_VOLTAGE Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_sense_voltage	Absolute value of raw voltage conversion measured between $I_{SENSEPn}$ and $I_{SENSEMn}$. Value = Y • 0.025 • 2^{-13} where Y = b[15:0] is an unsigned integer. Example: MFR_IOUT_SENSE_VOLTAGE = 1.544mV For b[15:0] = 0x1FA=506 Value = 506 • 0.025 • 2^{-13} = 1.544mV

MFR_VIN_PEAK

This command returns the maximum ADC measured value of the input voltage. This register is reset to 0x7C00 (-2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_VOUT_PEAK

This command returns the maximum ADC measured value of the channel's output voltage. This register is reset to 0xF800 (0.0) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_IOUT_PEAK

This commands returns the maximum ADC measured value of the channel's output current. This register is reset to 0x7C00 (-2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_TEMPERATURE_1_PEAK

This command returns the maximum measured value of the external diode temperature in °C. This register is reset to 0x7C00 (-2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_VIN_MIN

This command returns the minimum ADC measured value of the input voltage. This register is reset to 0x7BFF (approximately 2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_VOUT_MIN

This command returns the minimum ADC measured value of the channel's output voltage. This register is reset to 0xFFFF (7.9999) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed. Updates are disabled when Margin Low (Ignore Faults and Warnings) is enabled.

MFR_IOUT_MIN

This command returns the minimum ADC measured value of the channel's output current. This register is reset to 0x7BFF (approximately 2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

PMBus COMMAND DESCRIPTION

MFR_TEMPERATURE_1_MIN

This command returns the minimum measured value of the power stage temperature sensor in °C. This register is reset to 0x7BFF (approximately 2^{25}) when the LTM4673 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

FAULT LOGGING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	109
MFR_FAULT_LOG_RESTORE	0xEB	Command a transfer of the fault log previously stored in EEPROM back to RAM.	Send Byte	N				NA	109
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	110
MFR_FAULT_LOG_STATUS	0xED	Fault logging status.	R Byte	N	Reg		Y	NA	110
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	110

Fault Log Operation

A conceptual diagram of the fault log is shown in Figure 58. The fault log provides black box capability for the LTM4673. During normal operation the contents of the status registers, the output voltage/current/temperature readings, the input voltage readings, as well as peak and min values of these quantities, are stored in a continuously updated buffer in RAM. You can think of the operation as being similar to a strip chart recorder. When a fault occurs, the contents are written into EEPROM for non volatile storage. The EEPROM fault log is then locked. The part can be powered down with the fault log available for reading at a later time.

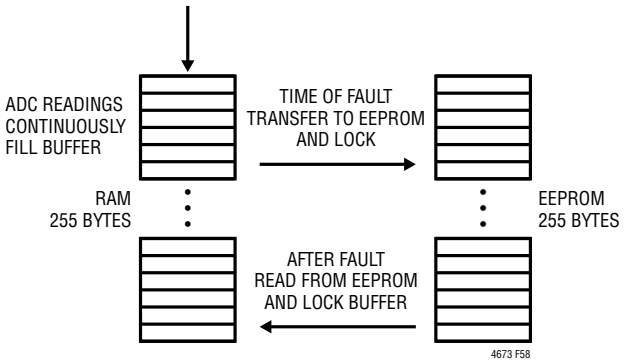


Figure 58. Fault Logging

MFR_FAULT_LOG_STORE

This command allows the user to transfer data from the RAM buffer to EEPROM.

MFR_FAULT_LOG_RESTORE

This command allows the user to transfer a copy of the fault-log data from the EEPROM to the RAM buffer. After a restore the RAM buffer is locked until a successful Mfr_fault_log read.

PMBus COMMAND DESCRIPTION

MFR_FAULT_LOG_CLEAR

This command initializes the EEPROM block reserved for fault logging. Any previous fault log stored in EEPROM will be erased by this operation and logging of the fault log RAM to EEPROM will be enabled. Make sure that Mfr_fault_log_status_ram = 0 before issuing the MFR_FAULT_LOG_CLEAR command.

MFR_FAULT_LOG_STATUS

This register is used to manage fault log events. The Mfr_fault_log_status_eeprom bit is set after a MFR_FAULT_LOG_STORE command or a faulted-off event triggers a transfer of the fault log from RAM to EEPROM. This bit is cleared by a MFR_FAULT_LOG_CLEAR command.

Mfr_fault_log_status_ram is set after a MFR_FAULT_ LOG_RESTORE to indicate that the data in the RAM has been restored from EEPROM and not yet read using a MFR_FAULT_LOG command. This bit is cleared only by a successful execution of an MFR_FAULT_LOG command.

MFR_FAULT_LOG_STATUS Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	Read only, always returns 0s.
b[1]	Mfr_fault_log_status_ram	Fault log RAM status: 0: The fault log RAM allows updates. 1: The fault log RAM is locked until the next Mfr_fault_log read.
b[0]	Mfr_fault_log_status_eeprom	Fault log EEPROM status: 0: The transfer of the fault log RAM to the EEPROM is enabled. 1: The transfer of the fault log RAM to the EEPROM is inhibited.

MFR_FAULT_LOG

Read only. This 2040-bit (255-byte) data block contains a copy of the RAM buffer fault log. The RAM buffer is continuously updated after each ADC conversion as long as Mfr_fault_log_status_eeprom is clear.

With Mfr_config_fault_log_enable = 1 and Mfr_fault_log_status_eeprom = 0, the RAM buffer is transferred to EEPROM whenever an LTM4673 fault causes a channel to latch off or a MFR_FAULT_LOG_STORE command is received. This transfer is delayed until the ADC has updated its READ values for all channels when Mfr_config_all_fast_fault_log is clear, otherwise it happens within 24ms. This optional delay can be used to ensure that the slower ADC monitored values are all updated for the case where a fast supervisor detected fault initiates the transfer to EEPROM.

Mfr_fault_log_status_eeprom is set high after the RAM buffer is transferred to EEPROM and not cleared until a Mfr_fault_log_clear is received, even if the LTM4673 is reset or powered down. Fault log EEPROM transfers are not initiated as a result of Status_mfr_discharge events.

During a Mfr_fault_log read, data is returned one byte at a time as defined in Table 8. The fault log data is partitioned into two sections. The first section is referred to as the preamble and contains the Position_last pointer, time information and peak and min values. The second section contains a chronological record of telemetry and requires Position_last for proper interpretation. The fault log stores approximately 300ms seconds of telemetry. To prevent timeouts during block reads, it is recommended that Mfr_config_all_longer_pmbus_timeout be set to 1.

PMBus COMMAND DESCRIPTION

Table 8. Data Block Contents

DATA	BYTE*	DESCRIPTION
Position_last[7:0]	0	Position of fault log pointer when fault occurred.
SharedTime[7:0]	1	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments.
SharedTime[15:8]	2	
SharedTime[23:16]	3	
SharedTime[31:24]	4	
SharedTime[39:32]	5	
SharedTime[40]	6	
Mfr_vout_peak0[7:0]	7	
Mfr_vout_peak0[15:8]	8	
Mfr_vout_min0[7:0]	9	
Mfr_vout_min0[15:8]	10	
Mfr_temperature_peak0[7:0]	11	
Mfr_temperature_peak0[15:8]	12	
Mfr_temperature_min0[7:0]	13	
Mfr_temperature_min0[15:8]	14	
Mfr_iout_peak0[7:0]	15	
Mfr_iout_peak0[15:8]	16	
Mfr_iout_min0[7:0]	17	
Mfr_iout_min0[15:8]	18	
Mfr_vin_peak[7:0]	19	
Mfr_vin_peak[15:8]	20	
Mfr_vin_min[7:0]	21	
Mfr_vin_min[15:8]	22	
Mfr_iin_peak[7:0]	23	
Mfr_iin_peak[15:8]	24	
Mfr_iin_min[7:0]	25	
Mfr_iin_min[15:8]	26	
Mfr_pin_peak[7:0]	27	
Mfr_pin_peak[15:8]	28	
Mfr_pin_min[7:0]	29	
Mfr_pin_min[15:8]	30	
Mfr_vout_peak1[7:0]	31	
Mfr_vout_peak1[15:8]	32	
Mfr_vout_min1[7:0]	33	
Mfr_vout_min1[15:8]	34	
Mfr_temperature_peak1[7:0]	35	
Mfr_temperature_peak1[15:8]	36	
Mfr_temperature_min1[7:0]	37	
Mfr_temperature_min1[15:8]	38	

Table 8. Data Block Contents

DATA	BYTE*	DESCRIPTION
Mfr_iout_peak1[7:0]	39	
Mfr_iout_peak1[15:8]	40	
Mfr_iout_min1[7:0]	41	
Mfr_iout_min1[15:8]	42	
Mfr_vout_peak2[7:0]	43	
Mfr_vout_peak2[15:8]	44	
Mfr_vout_min2[7:0]	45	
Mfr_vout_min2[15:8]	46	
Mfr_temperature_peak2[7:0]	47	
Mfr_temperature_peak2[15:8]	48	
Mfr_temperature_min2[7:0]	49	
Mfr_temperature_min2[15:8]	50	
Mfr_iout_peak2[7:0]	51	
Mfr_iout_peak2[15:8]	52	
Mfr_iout_min2[7:0]	53	
Mfr_iout_min2[15:8]	54	
Mfr_vout_peak3[7:0]	55	
Mfr_vout_peak3[15:8]	56	
Mfr_vout_min3[7:0]	57	
Mfr_vout_min3[15:8]	58	
Mfr_temperature_peak3[7:0]	59	
Mfr_temperature_peak3[15:8]	60	
Mfr_temperature_min3[7:0]	61	
Mfr_temperature_min3[15:8]	62	
Mfr_iout_peak3[7:0]	63	
Mfr_iout_peak3[15:8]	64	
Mfr_iout_min3[7:0]	65	
Mfr_iout_min3[15:8]	66	
Status_vout0[7:0]	67	
Status_iout0[7:0]	68	
Status_mfr_specific0[7:0]	69	
Status_vout1[7:0]	70	
Status_iout1[7:0]	71	
Status_mfr_specific1[7:0]	72	
Status_vout2[7:0]	73	
Status_iout2[7:0]	74	
Status_mfr_specific2[7:0]	75	
Status_vout3[7:0]	76	
Status_iout3[7:0]	77	
Status_mfr_specific3[7:0]	78	
		71 bytes for preamble

PMBus COMMAND DESCRIPTION

Table 8. Data Block Contents

DATA	BYTE*	DESCRIPTION
Fault_log [Position_last]	79	
Fault_log [Position_last-1]	80	
...		
Fault_log [Position_last-170]	237	
Reserved	238 to 254	
		Number of loops: (238 to 79)/58 = 2.7

*Note that PMBus data byte numbers start at 1 rather than 0.
See Figure 13 Block Read.

The data returned between bytes 79 and 237 of the previous table is interpreted using Position_last and the following table. The key to identifying the data located in byte 79 is to locate the DATA corresponding to POSITION = Position_last in the next table. Subsequent bytes are identified by decrementing the value of POSITION. For example: If Position_last = 8 then the first data returned in a block read is Status_temperature of page 0 followed by Read_temperature_1[15:8] of page 0 followed by Read_temperature_1[7:0] of page 0 and so on. See Table 9.

Table 9. Interpreting Cyclical Loop Data

POSITION	DATA
0	Read_temperature_2[7:0]
1	Read_temperature_2[15:8]
2	Read_vout0[7:0]
3	Read_vout0[15:8]
4	Status_vout0[7:0]
5	Status_mfr_specific0[7:0]
6	Read_temperature_1_0[7:0]
7	Read_temperature_1_0[15:8]
8	Status_temperature0[7:0]
9	Status_iout0[7:0]
10	Read_iout0[7:0]
11	Read_iout0[15:8]
12	Read_pout0[7:0]
13	Read_pout0[15:8]
14	Read_vin[7:0]
15	Read_vin[15:8]
16	Status_input[7:0]
17	0x0
18	Read_iin[7:0]

Table 9. Interpreting Cyclical Loop Data

POSITION	DATA
19	Read_iin[15:8]
20	Read_pin[7:0]
21	Read_pin[15:8]
22	Read_vout1[7:0]
23	Read_vout1[15:8]
24	Status_vout1[7:0]
25	Status_mfr_specific1[7:0]
26	Read_temperature_1_1[7:0]
27	Read_temperature_1_1[15:8]
28	Status_temperature1[7:0]
29	Status_iout1[7:0]
30	Read_iout1[7:0]
31	Read_iout1[15:8]
32	Read_pout1[7:0]
33	Read_pout1[15:8]
34	Read_vout2[7:0]
35	Read_vout2[15:8]
36	Status_vout2[7:0]
37	Status_mfr_specific2[7:0]
38	Read_temperature_1_2[7:0]
39	Read_temperature_1_2[15:8]
40	Status_temperature2[7:0]
41	Status_iout2[7:0]
42	Read_iout2[7:0]
43	Read_iout2[15:8]
44	Read_pout2[7:0]
45	Read_pout2[15:8]
46	Read_vout3[7:0]
47	Read_vout3[15:8]
48	Status_vout3[7:0]
49	Status_mfr_specific3[7:0]
50	Read_temperature_1_3[7:0]
51	Read_temperature_1_3[15:8]
52	Status_temperature3[7:0]
53	Status_iout3[7:0]
54	Read_iout3[7:0]
55	Read_iout3[15:8]
56	Read_pout3[7:0]
57	Read_pout3[15:8]
	Total Bytes = 58

PMBus COMMAND DESCRIPTION

MFR_FAULT_LOG Read Example

The following table fully decodes a sample fault log read with Position_last = 13 to help clarify the cyclical nature of the operation.

Data Block Contents

PREAMBLE INFORMATION

BYTE NUMBER DECIMAL	BYTE NUMBER HEX		DATA	DESCRIPTION
0	00		Position_last[7:0] = 13	Position of fault-log pointer when fault occurred.
1	01		SharedTime[7:0]	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments.
2	02		SharedTime[15:8]	
3	03		SharedTime[23:16]	
4	04		SharedTime[31:24]	
5	05		SharedTime[39:32]	
6	06		SharedTime[40]	
7	07		Mfr_vout_peak0[7:0]	
8	08		Mfr_vout_peak0[15:8]	
9	09		Mfr_vout_min0[7:0]	
10	0A		Mfr_vout_min0[15:8]	
11	0B		Mfr_temperature_peak0[7:0]	
12	0C		Mfr_temperature_peak0[15:8]	
13	0D		Mfr_temperature_min0[7:0]	
14	0E		Mfr_temperature_min0[15:8]	
15	0F		Mfr_iout_peak0[7:0]	
16	10		Mfr_iout_peak0[15:8]	
17	11		Mfr_iout_min0[7:0]	
18	12		Mfr_iout_min0[15:8]	
19	13		Mfr_vin_peak_[7:0]	
20	14		Mfr_vin_peak_[15:8]	
21	15		Mfr_vin_min_[7:0]	
22	16		Mfr_vin_min_[15:8]	
23	17		Mfr_iin_peak[7:0]	
24	18		Mfr_iin_peak[15:8]	
25	19		Mfr_iin_min[7:0]	
26	1A		Mfr_iin_min[15:8]	
27	1B		Mfr_pin_peak[7:0]	
28	1C		Mfr_pin_peak[15:8]	
29	1D		Mfr_pin_min[7:0]	

PREAMBLE INFORMATION

BYTE NUMBER DECIMAL	BYTE NUMBER HEX		DATA	DESCRIPTION
30	1E		Mfr_pin_min[15:8]	
31	1F		Mfr_vout_peak1[7:0]	
32	20		Mfr_vout_peak1[15:8]	
33	21		Mfr_vout_min1[7:0]	
34	22		Mfr_vout_min1[15:8]	
35	23		Mfr_temperature_peak1[7:0]	
36	24		Mfr_temperature_peak1[15:8]	
37	25		Mfr_temperature_min1[7:0]	
38	26		Mfr_temperature_min1[15:8]	
39	27		Mfr_iout_peak1[7:0]	
40	28		Mfr_iout_peak1[15:8]	
41	29		Mfr_iout_min1[7:0]	
42	2A		Mfr_iout_min1[15:8]	
43	2B		Mfr_vout_peak2[7:0]	
44	2C		Mfr_vout_peak2[15:8]	
45	2D		Mfr_vout_min2[7:0]	
46	2E		Mfr_vout_min2[15:8]	
47	2F		Mfr_temperature_peak2[7:0]	
48	30		Mfr_temperature_peak2[15:8]	
49	31		Mfr_temperature_min2[7:0]	
50	32		Mfr_temperature_min2[15:8]	
51	33		Mfr_iout_peak2[7:0]	
52	34		Mfr_iout_peak2[15:8]	
53	35		Mfr_iout_min2[7:0]	
54	36		Mfr_iout_min2[15:8]	
55	37		Mfr_vout_peak3[7:0]	
56	38		Mfr_vout_peak3[15:8]	
57	39		Mfr_vout_min3[7:0]	
58	3A		Mfr_vout_min3[15:8]	
59	3B		Mfr_temperature_peak3[7:0]	
60	3C		Mfr_temperature_peak3[15:8]	

PMBus COMMAND DESCRIPTION

PREAMBLE INFORMATION

BYTE NUMBER DECIMAL	BYTE NUMBER HEX		DATA	DESCRIPTION
61	3D		Mfr_temperature_ min3[7:0]	
62	3E		Mfr_temperature_ min3[15:8]	
63	3F		Mfr_iout_peak3[7:0]	
64	40		Mfr_iout_peak3[15:8]	
65	41		Mfr_iout_min3[7:0]	
66	42		Mfr_iout_min3[15:8]	
67	43		Status_vout0[7:0]	
68	44		Status_iout0[7:0]	
69	45		Status_temperature0[7:0]	
70	46		Status_vout1[7:0]	
71	47		Status_iout1[7:0]	
72	48		Status_temperature1[7:0]	
73	49		Status_vout2[7:0]	
74	4A		Status_iout2[7:0]	
75	4B		Status_temperature2[7:0]	
76	4C		Status_vout3[7:0]	
77	4D		Status_iout3[7:0]	
78	4E		Status_temperature3[7:0]	End of Preamble

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 0	54 BYTES PER LOOP
79	4F	13	Read_pout0[15:8]	Position_last
80	50	12	Read_pout0[7:0]	
81	51	11	Read_iout0[15:8]	
82	52	10	Read_iout0[7:0]	
83	53	9	Status_iout0[7:0]	
84	54	8	Status_ temperature0[7:0]	
85	55	7	Read_ temperature_1_0[15:8]	
86	56	6	Read_ temperature_1_0[7:0]	
87	57	5	Status_mfr_ specific0[7:0]	
88	58	4	Status_vout0[7:0]	
89	59	3	Read_vout0[15:8]	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 0	54 BYTES PER LOOP
90	5A	2	Read_vout0[7:0]	
91	5B	1	Read_ temperature_2[15:8]	
92	5C	0	Read_ temperature_2[7:0]	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 1	54 BYTES PER LOOP
93	5D	57	Read_pout3[15:8]	
94	5E	56	Read_pout3[7:0]	
95	5F	55	Read_iout3[15:8]	
96	60	54	Read_iout3[7:0]	
97	61	53	Status_iout3[7:0]	
98	62	52	Status_ temperature3[7:0]	
99	63	51	Read_ temperature_1_3[15:8]	
100	64	50	Read_ temperature_1_3[7:0]	
101	65	49	Status_mfr_ specific3[7:0]	
102	66	48	Status_vout3[7:0]	
103	67	47	Read_vout3[15:8]	
104	78	46	Read_vout3[7:0]	
105	69	45	Read_pout2[15:8]	
106	6A	44	Read_pout2[7:0]	
107	6B	43	Read_iout2[15:8]	
108	6C	42	Read_iout2[7:0]	
109	6D	41	Status_iout2[7:0]	
110	6E	40	Status_ temperature2[7:0]	
111	6F	39	Read_ temperature_1_2[15:8]	
112	70	38	Read_ temperature_1_2[7:0]	
113	71	37	Status_mfr_ specific2[7:0]	
114	72	36	Status_vout2[7:0]	
115	73	35	Read_vout2[15:8]	

PMBus COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 1	54 BYTES PER LOOP
116	74	34	Read_vout2[7:0]	
117	75	33	Read_pout1[15:8]	
118	76	32	Read_pout1[7:0]	
119	77	31	Read_iout1[15:8]	
120	78	30	Read_iout1[7:0]	
121	79	29	Status_iout1[7:0]	
122	7A	28	Status_ temperature2[7:0]	
123	7B	27	Read_ temperature_1_1[15:8]	
124	7C	26	Read_ temperature_1_1[7:0]	
125	7D	25	Status_mfr_ specific1[7:0]	
126	7E	24	Status_vout1[7:0]	
127	7F	23	Read_vout1[15:8]	
128	80	22	Read_vout1[7:0]	
129	81	21	Read_pin[15:8]	
130	82	20	Read_pin[7:0]	
131	83	19	Read_in[15:8]	
132	84	18	Read_in[7:0]	
133	85	17	0x0	
134	86	16	Status_input[7:0]	
135	87	15	Read_vin[15:8]	
136	88	14	Read_vin[7:0]	
137	89	13	Read_pout0[15:8]	
138	8A	12	Read_pout0[7:0]	
139	8B	11	Read_iout0[15:8]	
140	8C	10	Read_iout0[7:0]	
141	8D	9	Status_iout0[7:0]	
142	8E	8	Status_ temperature0[7:0]	
143	8F	7	Read_ temperature_1_0[15:8]	
144	90	6	Read_ temperature_1_0[7:0]	
145	91	5	Status_mfr_ specific0[7:0]	
146	92	4	Status_vout0[7:0]	
147	93	3	Read_vout0[15:8]	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 1	54 BYTES PER LOOP
148	94	2	Read_vout0[7:0]	
149	95	1	Read_ temperature_2[15:8]	
150	96	0	Read_ temperature_2[7:0]	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	54 BYTES PER LOOP
151	97	57	Read_pout3[15:8]	
152	98	56	Read_pout3[7:0]	
153	99	55	Read_iout3[15:8]	
154	9A	54	Read_iout3[7:0]	
155	9B	53	Status_iout3[7:0]	
156	9C	52	Status_ temperature3[7:0]	
157	9D	51	Read_ temperature_1_3[15:8]	
158	9E	50	Read_ temperature_1_3[7:0]	
159	9F	49	Status_mfr_ specific3[7:0]	
160	A0	48	Status_vout3[7:0]	
161	A1	47	Read_vout3[15:8]	
162	A2	46	Read_vout3[7:0]	
163	A3	45	Read_pout2[15:8]	
164	A4	44	Read_pout2[7:0]	
165	A5	43	Read_iout2[15:8]	
166	A6	42	Read_iout2[7:0]	
167	A7	41	Status_iout2[7:0]	
168	A8	40	Status_ temperature2[7:0]	
169	A9	39	Read_ temperature_1_2[15:8]	
170	AA	38	Read_ temperature_1_2[7:0]	
171	AB	37	Status_mfr_ specific2[7:0]	
172	AC	36	Status_vout2[7:0]	

PMBus COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	54 BYTES PER LOOP
173	AD	35	Read_vout2[15:8]	
174	AE	34	Read_vout2[7:0]	
175	AF	33	Read_pout1[15:8]	
176	B0	32	Read_pout1[7:0]	
177	B1	31	Read_iout1[15:8]	
178	B2	30	Read_iout1[7:0]	
179	B3	29	Status_iout1[7:0]	
180	B4	28	Status_ temperature2[7:0]	
181	B5	27	Read_ temperature_1_1[15:8]	
182	B6	26	Read_ temperature_1_1[7:0]	
183	B7	25	Status_mfr_ specific1[7:0]	
184	B8	24	Status_vout1[7:0]	
185	B9	23	Read_vout1[15:8]	
186	BA	22	Read_vout1[7:0]	
187	BB	21	Read_pin[15:8]	
188	BC	20	Read_pin[7:0]	
189	BD	19	Read_in[15:8]	
190	BE	18	Read_in[7:0]	
191	BF	17	0x0	
192	C0	16	Status_input[7:0]	
193	C1	15	Read_vin[15:8]	
194	C2	14	Read_vin[7:0]	
195	C3	13	Read_pout0[15:8]	
196	C4	12	Read_pout0[7:0]	
197	C5	11	Read_iout0[15:8]	
198	C6	10	Read_iout0[7:0]	
199	C7	9	Status_iout0[7:0]	
200	C8	8	Status_ temperature0[7:0]	
201	C9	7	Read_ temperature_1_0[15:8]	
202	CA	6	Read_ temperature_1_0[7:0]	
203	CB	5	Status_mfr_ specific0[7:0]	
204	CC	4	Status_vout0[7:0]	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	54 BYTES PER LOOP
205	CD	3	Read_vout0[15:8]	
206	CE	2	Read_vout0[7:0]	
207	CF	1	Read_ temperature_2[15:8]	
208	D0	0	Read_ temperature_2[7:0]	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	54 BYTES PER LOOP
209	D1	57	Read_pout3[15:8]	
210	D2	56	Read_pout3[7:0]	
211	D3	55	Read_iout3[15:8]	
212	D4	54	Read_iout3[7:0]	
213	D5	53	Status_iout3[7:0]	
214	D6	52	Status_ temperature_3[7:0]	
215	D7	51	Read_ temperature_1_3[15:8]	
216	D8	50	Read_ temperature_1_3[7:0]	
217	D9	49	Status_mfr_ specific3[7:0]	
218	DA	48	Status_vout3[7:0]	
219	DB	47	Read_vout3[15:8]	
220	DC	46	Read_vout3[7:0]	
221	DD	45	Read_pout2[15:8]	
222	DE	44	Read_pout2[7:0]	
223	DF	43	Read_iout2[15:8]	
224	E0	42	Read_iout2[7:0]	
225	E1	41	Status_iout2[7:0]	
226	E2	40	Status_ temperature2[7:0]	
227	E3	39	Read_ temperature_1_2[15:8]	
228	E4	38	Read_ temperature_1_2[7:0]	

PMBus COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	54 BYTES PER LOOP
229	E5	37	Status_mfr_ specific2[7:0]	
230	E6	36	Status_vout2[7:0]	
231	E7	35	Read_vout2[15:8]	
232	E8	34	Read_vout2[7:0]	
233	E9	33	Read_pout1[15:8]	
234	EA	32	Read_pout1[7:0]	
235	EB	31	Read_iout1[15:8]	
236	EC	30	Read_iout1[7:0]	
237	ED	29	Status_iout1[7:0]	Last valid fault log byte
238	EE		0x00	Bytes EE – FE return 0x00
239	EF		0x00	
240	F0		0x00	
241	F1		0x00	
242	F2		0x00	

CYCLICAL MUX LOOP DATA

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	54 BYTES PER LOOP
243	F3		0x00	
244	F4		0x00	
245	F5		0x00	
246	F6		0x00	
247	F7		0x00	
248	F8		0x00	
249	F9		0x00	
250	FA		0x00	
251	FB		0x00	
252	FC		0x00	
253	FD		0x00	
254	FE		0x00	This is PMBus byte 255. It must be read to clear Mfr_fault_log_ status_ram.

PMBus COMMAND DESCRIPTION

IDENTIFICATION/INFORMATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	118
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	118
MFR_SPECIAL_ID	0xE7	Manufacturer code for identifying the LTM4673.	R Word	N	Reg		Y	0x448X	119
MFR_SPECIAL_LOT	0xE8	Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value.	R Byte	Y	Reg		Y	NA	119

CAPABILITY

The CAPABILITY command provides a way for a host system to determine some key capabilities of the LTM4673.

CAPABILITY Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Capability_pec	Hard coded to 1 indicating Packet Error Checking is supported. Reading the Mfr_config_all_pec_en bit will indicate whether PEC is currently required.
b[6:5]	Capability_scl_max	Hard coded to 01b indicating the maximum supported bus speed is 400kHz.
b[4]	Capability_smb_alert	Hard coded to 1 indicating this device does have an $\overline{\text{ALERT}}$ pin and does support the SMBus Alert Response Protocol.
b[3:0]	Reserved	Always returns 0.

PMBus_REVISION

PMBus_REVISION Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	PMBus_rev	Reports the PMBus standard revision compliance. This is hard-coded to 0x11 for revision 1.1.

PMBus COMMAND DESCRIPTION

MFR_SPECIAL_ID

This register contains the manufacturer ID for the LTM4673. Always returns 0x448X.

MFR_SPECIAL_LOT

These paged registers contain information that identifies the user configuration that was programmed at the factory. Contact the factory to request a custom factory programmed user configuration and special lot number.

USER SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	NA	119
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	119
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	NA	119
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	119
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	119
MFR_LTC_RESERVED_1	0xB5	Manufacturer reserved.	R/W Word	Y	Reg		Y	NA	119
MFR_LTC_RESERVED_2	0xBC	Manufacturer reserved.	R/W Word	Y	Reg			NA	119

USER_DATA_00, USER_DATA_01, USER_DATA_02, USER_DATA_03, USER_DATA_04, MFR_LTC_RESERVED_1 and MFR_LTC_RESERVED_2

These registers are provided as user scratchpad and additional manufacturer reserved locations.

USER_DATA_03 and USER_DATA_04 are available for user scratchpad use. These 10 bytes (1 unpaged word plus 4-paged words) might be used for traceability or revision information such as serial number, board model number, assembly location, or assembly date.

PACKAGE DESCRIPTION

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT0}	B1	V_{OUT0}	C1	V_{OUT0}	D1	V_{OUT0}	E1	V_{OUT0}
A2	V_{OUT0}	B2	V_{OUT0}	C2	V_{OUT0}	D2	V_{OUT0}	E2	V_{OUT0}
A3	V_{OUT0}	B3	V_{OUT0}	C3	V_{OUT0}	D3	V_{OUT0}	E3	GND
A4	GND	B4	GND	C4	GND	D4	GND	E4	GND
A5	GND	B5	GND	C5	GND	D5	GND	E5	GND
A6	$TSENSE0^-$	B6	GND	C6	GND	D6	GND	E6	PHMODE0
A7	$TSENSE0^+$	B7	GND	C7	GND	D7	V_{IN}	E7	$INTV_{CC0}$
A8	GND	B8	GND	C8	GND	D8	V_{IN}	E8	V_{IN}
A9	GND	B9	GND	C9	GND	D9	V_{IN}	E9	SV_{IN0}
A10	GND	B10	GND	C10	GND	D10	V_{IN}	E10	CLKOUT0
A11	GND	B11	GND	C11	GND	D11	V_{IN}	E11	PWRGD0
A12	GND	B12	GND	C12	GND	D12	V_{IN}	E12	GND
A13	V_{IN}	B13	V_{IN}	C13	V_{IN}	D13	V_{IN}	E13	GND
A14	SGND	B14	SGND	C14	SGND	D14	SGND	E14	SGND
A15	SGND	B15	SGND	C15	SGND	D15	SGND	E15	SGND
A16	SGND	B16	SGND	C16	SGND	D16	SGND	E16	SGND
A17	SGND	B17	SGND	C17	SGND	D17	SGND	E17	SGND
A18	SGND	B18	SGND	C18	SGND	D18	SGND	E18	SGND
A19	SGND	B19	SGND	C19	SGND	D19	SGND	E19	SGND

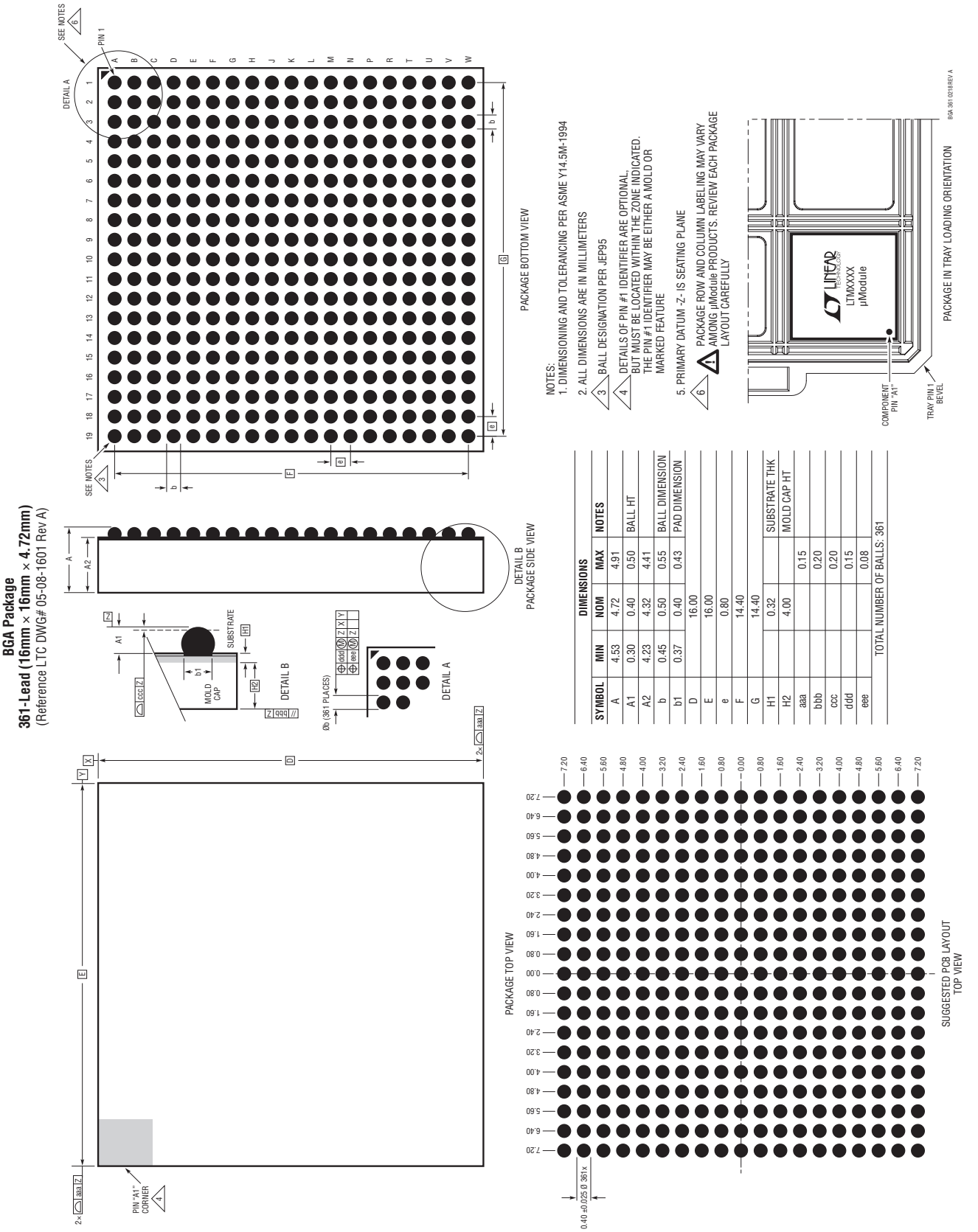
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
F1	GND	G1	GND	H1	V_{OUT1}	J1	V_{OUT1}	K1	GND
F2	GND	G2	GND	H2	V_{OUT1}	J2	V_{OUT1}	K2	GND
F3	GND	G3	GND	H3	V_{OUT1}	J3	V_{OUT1}	K3	GND
F4	GND	G4	GND	H4	V_{OUT1}	J4	V_{OUT1}	K4	GND
F5	GND	G5	GND	H5	GND	J5	V_{IN}	K5	GND
F6	GND	G6	GND	H6	V_{IN}	J6	V_{IN}	K6	GND
F7	GND	G7	TRACK/SS1	H7	GND	J7	GND	K7	GND
F8	V_{OSNS0}^-	G8	V_{OSNS0}^+	H8	PWRGD1	J8	RUN1	K8	TMON
F9	TRACK/SS0	G9	FB0	H9	FB1	J9	GND	K9	$INTV_{CC12}$
F10	FREQ0	G10	GND	H10	COMP0a	J10	V_{OSNS1}^+	K10	FREQ12
F11	RUN0	G11	MODE/CLKIN0	H11	COMP0b	J11	COMP1	K11	GND
F12	GND	G12	GND	H12	GND	J12	V_{OSNS1}^-	K12	GND
F13	$\overline{ALERT}$	G13	CONTROL0	H13	ASEL0	J13	GND	K13	GND
F14	SCL	G14	CONTROL1	H14	SGND	J14	SGND	K14	SGND
F15	SDA	G15	WP	H15	TSENSE2	J15	SGND	K15	ASEL1
F16	$\overline{FAULT}$1	G16	$\overline{FAULT}$0	H16	SGND	J16	SGND	K16	SGND
F17	CONTROL3	G17	CONTROL2	H17	SGND	J17	TSENSE1	K17	AUX$\overline{FAULT}$
F18	SHARECLK	G18	WDI/$\overline{RESET}$	H18	V_{IN_D}	J18	SGND	K18	V_{INSNS}
F19	PWRGD	G19	V_{DD25}	H19	V_{DD25}	J19	V_{DD33}	K19	DNC

PACKAGE DESCRIPTION

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
L1	V_{OUT2}	M1	V_{OUT2}	N1	GND	P1	GND	R1	V_{OUT3}
L2	V_{OUT2}	M2	V_{OUT2}	N2	GND	P2	GND	R2	V_{OUT3}
L3	V_{OUT2}	M3	V_{OUT2}	N3	GND	P3	GND	R3	GND
L4	V_{OUT2}	M4	V_{OUT2}	N4	GND	P4	GND	R4	GND
L5	V_{IN}	M5	GND	N5	GND	P5	GND	R5	GND
L6	V_{IN}	M6	V_{IN}	N6	GND	P6	CLKOUT3	R6	PHMODE3
L7	GND	M7	GND	N7	TRACK/SS2	P7	RUN3	R7	PWRGD3
L8	RUN2	M8	PWRGD2	N8	COMP3b	P8	FREQ3	R8	MODE/CLKIN3
L9	MODE/CLKIN12	M9	FB2	N9	COMP3a	P9	TRACK/SS3	R9	SV_{IN3}
L10	V_{OSNS2}^{+}	M10	GND	N10	FB3	P10	V_{OSNS3}^{-}	R10	V_{IN}
L11	GND	M11	COMP2	N11	V_{OSNS3}^{+}	P11	GND	R11	$INTV_{CC3}$
L12	V_{OSNS2}^{-}	M12	GND	N12	GND	P12	GND	R12	GND
L13	GND	M13	GND	N13	GND	P13	GND	R13	GND
L14	SGND	M14	SGND	N14	SGND	P14	SGND	R14	SGND
L15	SGND	M15	SGND	N15	V_{DAC1}	P15	V_{DAC0}	R15	SGND
L16	SGND	M16	V_{DAC2}	N16	I_{INSNSP}	P16	I_{INSNSM}	R16	SGND
L17	SGND	M17	SGND	N17	SGND	P17	V_{DAC3}	R17	SGND
L18	SGND	M18	SGND	N18	SGND	P18	SGND	R18	SGND
L19	SGND	M19	SGND	N19	SGND	P19	SGND	R19	SGND

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
T1	V_{OUT3}	U1	V_{OUT3}	V1	V_{OUT3}	W1	V_{OUT3}
T2	V_{OUT3}	U2	V_{OUT3}	V2	V_{OUT3}	W2	V_{OUT3}
T3	V_{OUT3}	U3	V_{OUT3}	V3	V_{OUT3}	W3	V_{OUT3}
T4	GND	U4	GND	V4	GND	W4	GND
T5	GND	U5	GND	V5	GND	W5	GND
T6	GND	U6	GND	V6	GND	W6	$TSENSE3^{+}$
T7	V_{IN}	U7	GND	V7	GND	W7	$TSENSE3^{-}$
T8	V_{IN}	U8	GND	V8	GND	W8	GND
T9	V_{IN}	U9	GND	V9	GND	W9	GND
T10	V_{IN}	U10	GND	V10	GND	W10	GND
T11	V_{IN}	U11	GND	V11	GND	W11	GND
T12	V_{IN}	U12	GND	V12	GND	W12	GND
T13	V_{IN}	U13	V_{IN}	V13	V_{IN}	W13	V_{IN}
T14	SGND	U14	SGND	V14	SGND	W14	SGND
T15	SGND	U15	SGND	V15	SGND	W15	SGND
T16	SGND	U16	SGND	V16	SGND	W16	SGND
T17	SGND	U17	SGND	V17	SGND	W17	SGND
T18	SGND	U18	SGND	V18	SGND	W18	SGND
T19	SGND	U19	SGND	V19	SGND	W19	SGND

PACKAGE DESCRIPTION



SYMBOL	DIMENSIONS MIN	NOM	MAX	NOTES
A	4.53	4.72	4.91	
A1	0.30	0.40	0.50	BALL HT
A2	4.23	4.32	4.41	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		16.00		
E		16.00		
e		0.80		
F		14.40		
G		14.40		
H1	0.32			SUBSTRATE THK
H2	4.00			MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
	TOTAL NUMBER OF BALLS: 361			

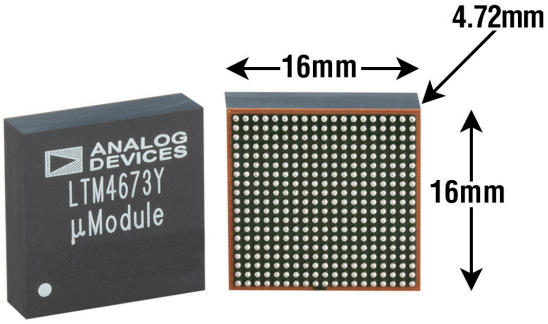
Rev. A

REVISION HISTORY

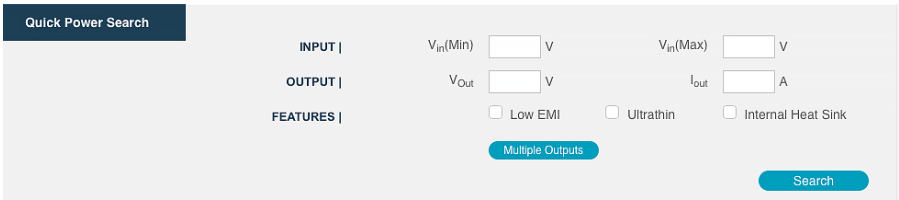
REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/23	Changed master to main and slave to subordinate.	All
		Removed TSENSE*n* and added Note 17 to Absolute Maximum Ratings section.	4
		Updated Pin Functions description for V_{OSNSn}^+ and V_{OSNSn}^-.	18, 19
		Updated Equation 5, added Equation 6 and corrected Equation 7.	37, 38
		Updated text and corrected Figure 23 pin names in the Multichannel Parallel Operation section.	44
		Updated text about parallel operation in Layout Checklist/Example section.	62
		Updated Figure 53: Changed resistor values connected to V_{DAC0}, FB0, FB1 and FB2, V_{DAC3}, FB3.	63
		Updated Figure 54: Changed resistor value from 90.9k to 45.3k. Tied V_{OSNS0}^+ to V_{OSNS3}^+, V_{OSNS1}^+ to V_{OSNS2}^+, TRACK/SS0 to TRACK/SS3, TRACK/SS1 to TRACK/SS2.	64
		Updated Figure 55: Changed resistor value from 90.9k to 45.3k. Tied V_{OSNS0}^+ to V_{OSNS3}^+, TRACK/SS0 to TRACK/SS3.	65
		Updated Figure 56: Changed resistor values from 787k to 715k, 121k to 90.9k, 715k to 787k, 90.9 to 121k. Changed V_{OUT0} to 1.0V, V_{OUT1} to 1.2V, V_{OUT3} to 0.9V. Tied V_{OSNS1}^+ to V_{OSNS2}^+, TRACK/SS1 to TRACK/SS2.	66

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4671	Quad µModule Regulator with Configurable Dual 12A, Dual 5A Output Array	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 3.3V for Dual 12A Rails, 0.6V ≤ V_{OUT} ≤ 5.5V for Dual 5A Rails, 9.5mm × 16mm × 4.72mm BGA
LTM4644	Quad 4A µModule Regulator	4.5V ≤ V_{IN} ≤ 14V, 0.6V ≤ V_{OUT} ≤ 5.5V, 9mm × 15mm × 5.01mm BGA
LTM4622	Ultrathin, Dual 2.5A or Single 5A µModule Regulator	3.6V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4705	Dual 5A or Single 10A µModule Regulator	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 7.5mm × 3.22mm BGA
LTM4646	Dual 10A or Single 20A µModule Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 11.25mm × 15mm × 5.01mm BGA
LTM4662	Dual 15A or Single 30A µModule Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 11.25mm × 15mm × 5.74mm BGA
LTM4650A	Dual 25A or Single 50A µModule Regulator	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.5V, 16mm × 16mm × 4.41mm LGA, 16mm × 16mm × 5.01mm BGA
LTM4657	8A µModule Regulator	3.1V ≤ V_{IN} ≤ 20V, 0.5V ≤ V_{OUT} ≤ 5.5V. 6.25mm × 6.25mm × 3.87mm BGA
LTM4626	12A µModule Regulator	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V. 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule Regulator	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V. 6.25mm × 6.25mm × 5.02mm BGA