RS9116 n-Link™ and WiSeConnect™ Single Chip Wi-Fi® and Dual-Mode Bluetooth® 5 Wireless Connectivity Solutions

QFN (7 x 7 x 0.85) mm

Overview

1.1 Features

Wi-Fi

- Compliant to single-spatial stream IEEE 802.11 b/g/n with single band support
- Support for 20 MHz channel bandwidth
- Transmit power up to +20 dBm with integrated PA
- Receive sensitivity as low as -98.5 dBm
- Data Rates: 802.11b: Up to 11 Mbps; 802.11g: Up to 54 Mbps; 802.11n: MCS0 to MCS7
- Operating Frequency Range: 2412 MHz – 2484 MHz

Bluetooth

- Transmit power up to +20 dBm with integrated PA
- Receive sensitivity:- LE: -95 dBm, LR 125 Kbps: -106 dBm
- Compliant to dual-mode Bluetooth 5
- <8 mA transmit current in Bluetooth 5 mode, 2 Mbps data rate
- Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps, 3 Mbps
- Operating Frequency Range: 2.402 GHz - 2.480 GHz
- Bluetooth 2.1 + EDR, Bluetooth Low Energy 4.0 / 4.1 / 4.2 / 5.0
- Bluetooth Low Energy 1 Mbps, 2 Mbps and Long Range modes
- Bluetooth Low Energy Secure connections
- Bluetooth Low Energy supports central role and peripheral role concurrently
- Bluetooth auto rate and auto TX power adaptation
- Scatternet* with two slave roles while still being visible

RF Features

- Integrated baseband processor with calibration memory, RF transceiver, high-power amplifier, balun and T/R switch
- Dual external antenna (diversity supported)

Power Consumption

- Wi-Fi Standby Associated mode current: 55 uA @ 1 second beacon listen interval
- Wi-Fi 1 Mbps Listen current: 14 mA
- Wi-Fi LP chain Rx current: 19 mA
- Deep sleep current <1 uA, Standby current (RAM retention) < 10 uA

Operating Conditions

- Wide operating supply range: 1.75 V to 3.63 V
- Operating temperature: -40 ºC to +85 ºC (Industrial grade)

Size

- QMS: 7 mm x 7 mm x 0.85 mm

Evaluation Kit

- Single Band EVK: RS9116X-SB-EVK1

Software Operating Modes

- Hosted mode (n-Link™): Wi-Fi stack, Bluetooth stack and profiles and all network stacks reside on the host processor
- Embedded mode (WiSeConnect™): Wi-Fi stack, TCP/IP stack, IP modules, Bluetooth stack and some profiles reside in RS9116; Some of the Bluetooth profiles reside in the host processor

Hosted Mode (n-Link™)

- Available host interfaces: SDIO 2.0 and USB HS
- Application data throughput up to 50 Mbps (Hosted Mode) in 802.11n with 20MHz bandwidth.
- Host drivers for Linux
- Support for Client mode, Access point mode (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

Embedded Mode (WiSeConnect™)

- Available host interface: UART, SPI, and USB CDC

- Support for Embedded Client mode, Access Point mode (Up to 8 clients), Concurrent Client and Access Point mode, and Enterprise Security
- Supports advanced security features: WPA/WPA2-Personal and Enterprise
- Integrated TCP/IP stack, HTTP/HTTPS, SSL/TLS, MQTT
- Bluetooth inbuilt stack support for L2CAP, RFCOMM, SDP, SPP, GAP
- Bluetooth profile support for GAP, SDP, SPP, GATT, L2CAP, RFCOMM
- Wireless firmware update and provisioning
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

Security

- Accelerators: AES128/256 in Embedded Mode
- WPA/WPA2-Personal, WPA/WPA2 Enterprise for Client

Software and Regulatory Certification

- Wi-Fi Alliance*
- Bluetooth Qualification*

* For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

All power and performance numbers are under ideal conditions.

1.2 Applications

Wearables

Smart Watches, Wristbands, Fitness Monitors, Smart Glasses, etc.

Smart Home

Smart Locks, Motion/Entrance Sensors, Water Leak sensors, Smart plugs/switches, LED lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.

Other Consumer Applications

Toys, Anti-theft tags, Smart dispensers, Weighing scales, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.

Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)

Healthcare Tags, Medical patches/pills, Infusion pumps, Sensors/actuators in Manufacturing, Electronic Shelf labels, Agricultural sensors, Product tracking tags, Smart Meters, Parking sensors, Street LED lighting, Automotive After-market, Security Cameras, etc.

1.3 Description

Silicon Labs' RS9116 single band QMS provide a comprehensive multi-protocol wireless connectivity solution including 802.11 b/g/n (2.4 GHz), and dual-mode Bluetooth 5. The SoC offers high throughput, extended range with power-optimized performance. The SoCs are FCC, IC, and ETSI/CE (including EN 300 328-v2.2.2) certifiable.

1.4 Block Diagrams

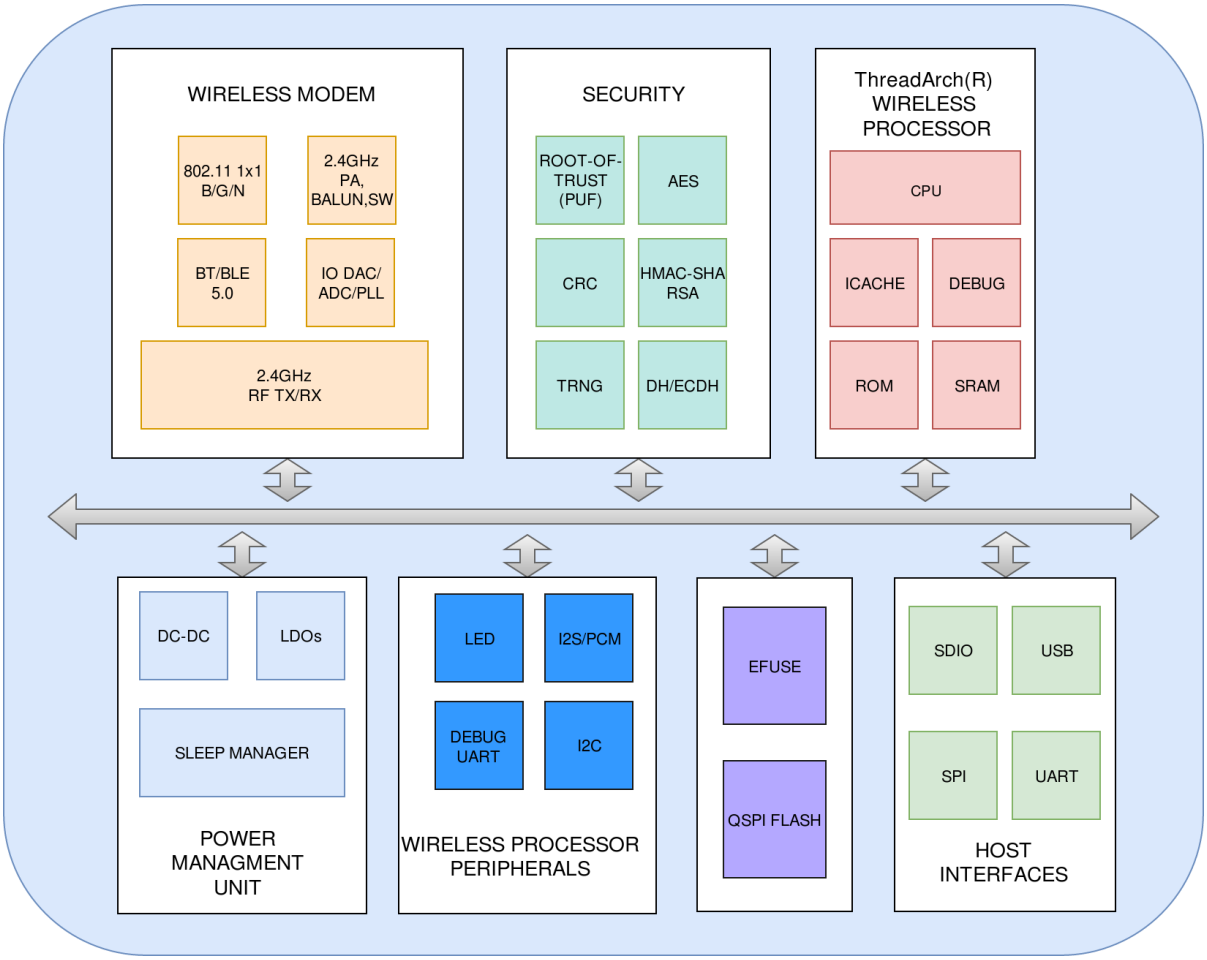

Figure 1 RS9116 Connectivity Hardware Block Diagram

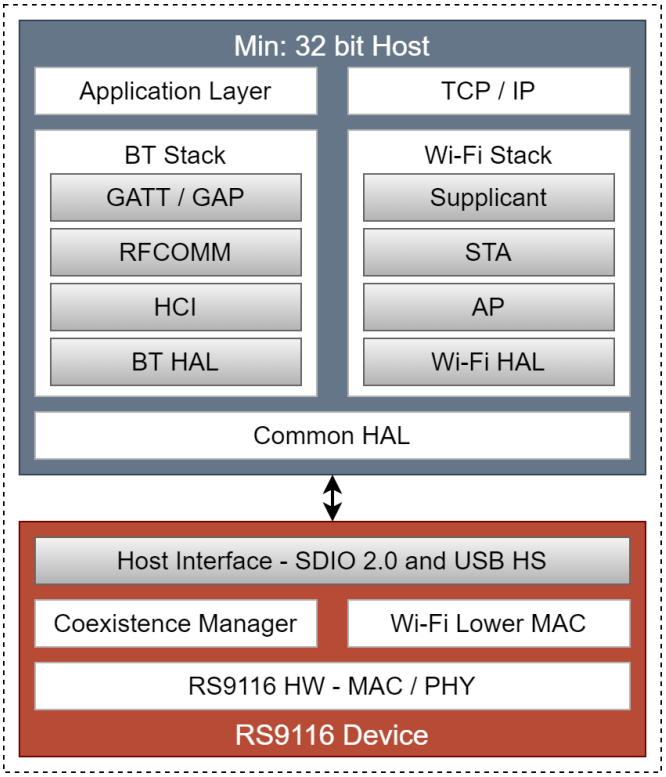

Figure 2 Hosted Software Architecture

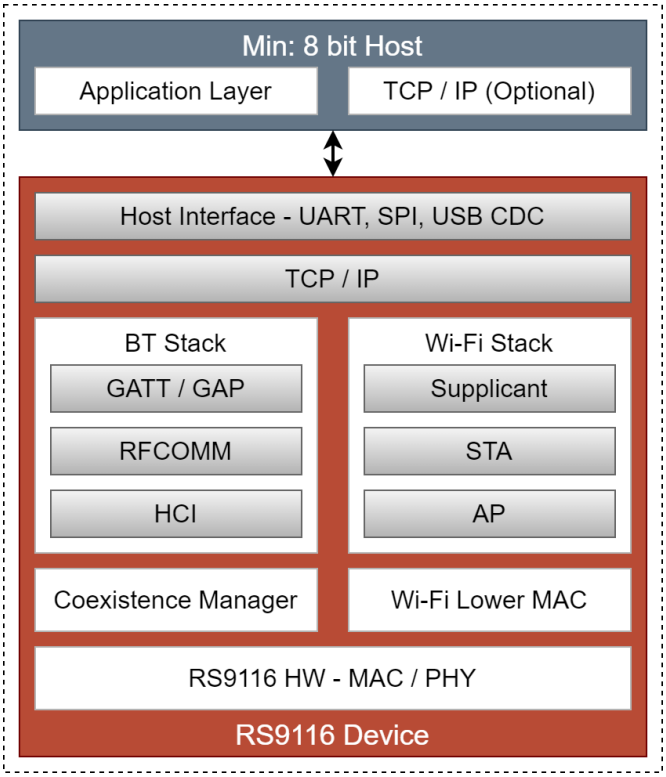

Figure 3 Embedded Software Architecture

Customer can connect multiple hosts, but only one host interface can be active after power-on.

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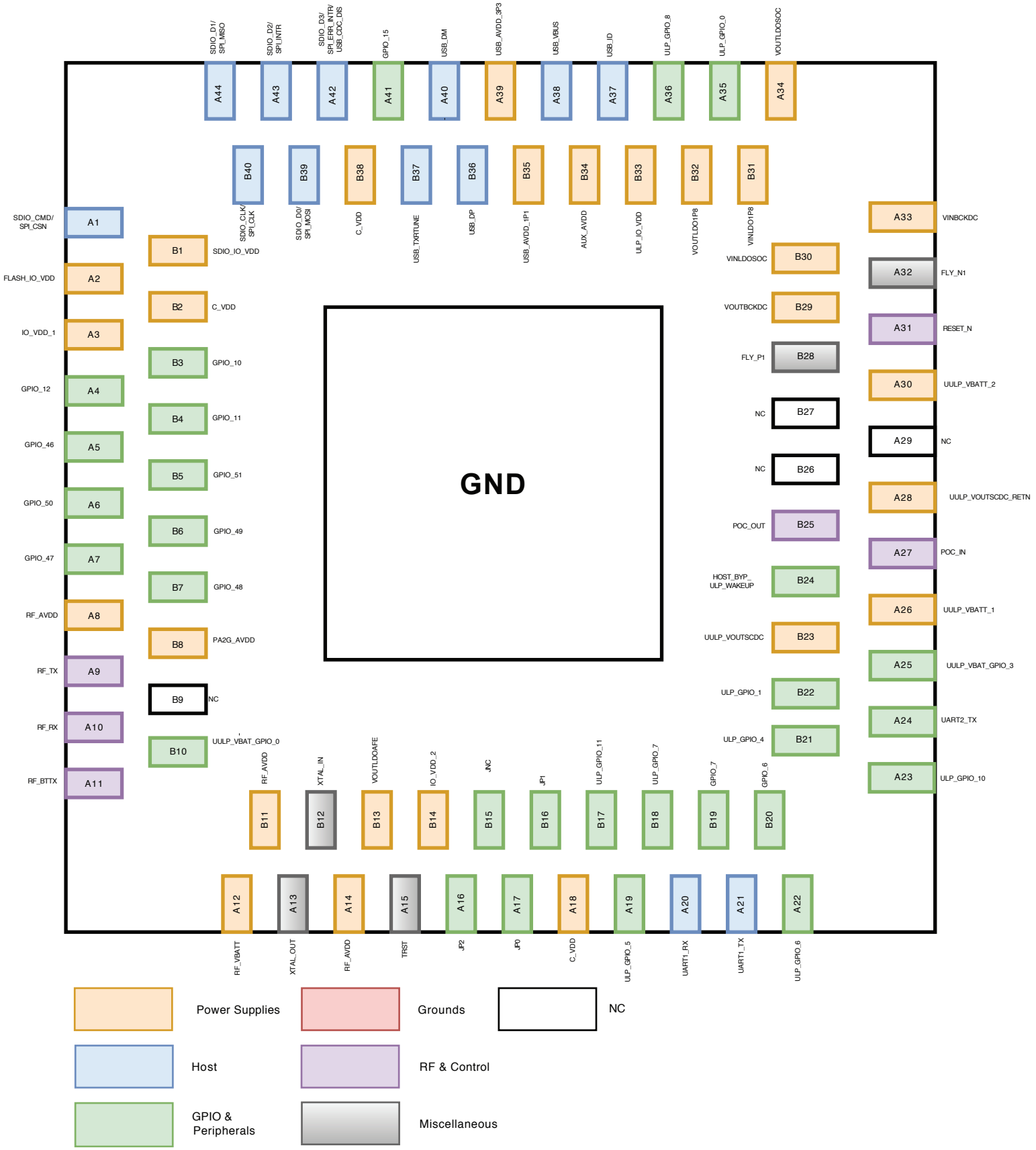
2 RS9116 QMS Soc Pinout and Pin Description

2.1 Pin Diagram

RS9116X-SBXX-QMS-ABC



2.2 Pin Description

2.2.1 RF & Control Interfaces

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
RF_TX	A9	PA2G_AVDD	Output	NA	2.4 GHz RF Output.
RF_RX	A10	RF_AVDD	Inout	NA	2.4 GHz RF Input/Output.
RF_BTTX	A11	RF_AVDD	Output	NA	Bluetooth 10 dBm RF Output.
RESET_N	A31	UULP_VBATT_2	Input	NA	Active-low reset asynchronous reset signal.
POC_IN	A27	UULP_VBATT_1	Input	NA	Power On Control Input.
POC_OUT	B25	UULP_VBATT_1	Output	NA	Power On Control Output.

Table 1 Chip Packages - RF & Control Interfaces

2.2.2 Power & Ground Pins

Pin Name	Type	QMS Pin Number	Direction	Description
UULP_VBATT_1	Power	A26	Input	Always-on VBATT Power supply to the UULP domains.
UULP_VBATT_2	Power	A30	Input	Always-on VBATT Power supply to the UULP domains.
RF_VBATT	Power	A12	Input	Always-on VBATT Power supply to the RF.
VINBCKDC	Power	A33	Input	Power supply for the on-chip Buck.
VOUTBCKDC	Power	B29	Output	Output of the on-chip Buck.
VINLDOSOC	Power	B30	Input	Power supply for SoC LDO. Connect to VOUTBCKDC as per the Reference Schematics.
VOUTLDOSOC	Power	A34	Output	Output of SoC LDO.
VINLDO1P8	Power	B31	Input	Power supply for 1.8V LDO.
VOUTLDO1P8	Power	B32	Output	Output of 1.8V LDO.

Pin Name	Type	QMS Pin Number	Direction	Description
VOUTLDOAFE	Power	B13	Output	Output of AFE LDO.
FLASH_IO_VDD	Power	A2	Input	I/O Supply for Flash. Connect to VOUTLDO1P8 as per the Reference Schematics.
IO_VDD_1	Power	A3	Input	I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
IO_VDD_2	Power	B14	Input	I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
SDIO_IO_VDD	Power	B1	Input	I/O Supply for SDIO I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
ULP_IO_VDD	Power	B33	Input	I/O Supply for ULP GPIOs.
PA2G_AVDD	Power	B8	Input	Power supply for the 2.4 GHz RF Power Amplifier.
RF_AVDD	Power	A8, A14, B11	Input	Power supply for the 2.4 GHz RF and AFE. Connect to VOUTBCKDC as per the Reference Schematics.
PLL_AVDD	Power	NA	Input	Power supply for the on-chip PLLs. Connect to VOUTBCKDC as per the Reference Schematics.
AUX_AVDD	Power	B34	Output	Output supply for the Analog peripherals.
UULP_VOUTSCDC	Power	B23	Output	UULP Switched Cap DCDC Output.
UULP_VOUTSCDC_RETN	Power	A28	Output	UULP Retention Supply Output.
UULP_AVDD	Power	NA	Input	Power supply for the always-on digital and ULP peripherals. Connect to UULP_VOUTSCDC as per the Reference Schematics.
C_VDD	Power	B2, A18, B38	Input	Power supply for the digital core. Connect to the VOUTLDOSOC as per the Reference Schematics.
USB_AVDD_3P3	Power	A39	Input	Power Supply for the USB interface.
USB_AVDD_1P1	Power	B35	Input	Power supply for the USB core.
PMU_AGND	Ground	GND Paddle	GND	Ground corresponding to PMU_AVDD.
VSSBCKDC	Ground	GND Paddle	GND	Ground corresponding to VINBCKDC and VOUTBCKDC

Pin Name	Type	QMS Pin Number	Direction	Description
IO_DGND	Ground	GND Paddle	GND	Ground corresponding to the I/O power supply pins.
PA_AGND	Ground	GND Paddle	GND	Ground corresponding to the RF Power Amplifier supply.
RF_AGND	Ground	GND Paddle	GND	Ground corresponding to the RF supply.
RFPLL_AGND	Ground	GND Paddle	GND	Ground corresponding to the supply for PLL in the RF.
PLL_AGND	Ground	GND Paddle	GND	Ground corresponding to the on-chip PLL's supply.
VBATT_AGND	Ground	GND Paddle	GND	Ground corresponding to the VBATT supply.
UULP_VBATT_AGND_1	Ground	GND Paddle	GND	Ground corresponding to the UULP_VBATT_1 supply.
UULP_VBATT_AGND_2	Ground	GND Paddle	GND	Ground corresponding to the UULP_VBATT_2 supply.
UULP_AGND	Ground	GND Paddle	GND	Ground corresponding to the UULP_AVDD supply.
AUX_AGND	Ground	GND Paddle	GND	Ground corresponding to the AUX_AVDD supply.
GND	Ground	GND Paddle	GND	Common ground pins.

Table 2 Chip Packages - Power and Ground Pins

2.2.3 Host & Peripheral Interfaces

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
GPIO_6	B20	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • I2S_DOUT - I2S interface output data. • PCM_DOUT - PCM interface output data.
GPIO_7	B19	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ

<table>
<tr><th>Pin Name</th><th>QMS Pin Number</th><th>QMS I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>This pin can be configured by software to be any of the following
I2S_CLK - I2S interface clock.
PCM_CLK - PCM interface clock.</td></tr>
<tr><td>GPIO_8/ UART1_RX</td><td>A20</td><td>IO_VDD_1</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>UART</td><td>UART1_RX - UART Host interface serial input.</td><td>HighZ</td></tr><tr><td>Non UART</td><td>HighZ</td><td>HighZ</td></tr></table>The UART interface is supported only in WiSeConnect™.</td></tr>
<tr><td>GPIO_9/ UART1_TX</td><td>A21</td><td>IO_VDD_1</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>UART</td><td>UART1_TX - UART Host interface serial output.</td><td>HighZ</td></tr><tr><td>Non UART</td><td>HighZ</td><td>HighZ</td></tr></table>The UART interface is supported only in WiSeConnect™.</td></tr>
<tr><td>GPIO_10</td><td>B3</td><td>IO_VDD_1</td><td>Inout</td><td>HighZ</td><td>Default: HighZ
Sleep: HighZ
This pin can be configured by software to be any of the following
I2S_DIN: I2S interface input data.
PCM_DIN - PCM interface input data.</td></tr>
<tr><td>GPIO_11</td><td>B4</td><td>IO_VDD_1</td><td>Inout</td><td>HighZ</td><td>Default: HighZ.
Sleep: HighZ</td></tr>
</table>

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					This pin can be configured by software to be any of the following • I2S_WS: I2S interface Word Select. • PCM_FSYNC: PCM interface Frame Synchronization signal.
GPIO_12	A4	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • UART1_RTS - UART interface Request to Send, if UART Host Interface flow control is enabled. The UART interface is supported only in WiSeConnect™.
GPIO_15	A41	IO_VDD_1	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • UART1_CTS - UART interface Clear to Send, if UART Host Interface flow control is enabled. • UART1_TRANSPARENT_MODE - UART Host interface Transparent Mode, Indication that chip has entered into TRANSPERENT_MODE • TSF_SYNC - Transmit Synchronization Function signal to indicate to the Host when a packet is transmitted. The signal is toggled once at the end of every transmitted packet.

<table>
<tr><th>Pin Name</th><th>QMS Pin Number</th><th>QMS I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>The UART interface is supported only in WiSeConnect™.</td></tr>
<tr><td>SDIO_CLK/SPI_CLK</td><td>B40</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>SDIO</td><td>SDIO_CLK - SDIO interface clock</td><td>HighZ</td></tr><tr><td>SPI</td><td>SPI_CLK - SPI Slave interface clock</td><td>HighZ</td></tr><tr><td>Non-SDIO, SPI</td><td>HighZ</td><td>HighZ</td></tr></table>The SPI interface is supported only in WiSeConnect™.</td></tr>
<tr><td>SDIO_CMD/SPI_CSN</td><td>A1</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>SDIO</td><td>SDIO_CMD - SDIO interface CMD signal</td><td>HighZ</td></tr><tr><td>SPI</td><td>SPI_CSN - Active-low Chip Select signal of SPI Slave interface</td><td>HighZ</td></tr><tr><td>Non-SDIO, SPI</td><td>HighZ</td><td>HighZ</td></tr></table>The SPI interface is supported only in WiSeConnect™.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>QMS Pin Number</th><th>QMS I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td>SDIO_D0/SPI_MOSI</td><td>B39</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D0 - SDIO interface Data0 signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_MOSI - SPI Slave interface Master-Out-Slave-In signal</td><td>HighZ</td></tr>
<tr><td>Non-SDIO, SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
The SPI interface is supported only in WiSeConnect™.
</td></tr>
<tr><td>SDIO_D1/SPI_MISO</td><td>A44</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D1 - SDIO interface Data1 signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_MISO - SPI Slave interface Master-In-Slave-Out signal</td><td>HighZ</td></tr>
<tr><td>Non-SDIO, SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
The SPI interface is supported only in WiSeConnect™.
</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>QMS Pin Number</th><th>QMS I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td>SDIO_D2/SPI_INTR</td><td>A43</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D2 - SDIO interface Data2 signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_INTR - SPI Slave interface Interrupt Signal to the Host</td><td>HighZ</td></tr>
<tr><td>Non-SDIO, SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
The SPI interface is supported only in WiSeConnect™.
</td></tr>
<tr><td>SDIO_D3/SPI_ERR_INTR/USB_CDC_DIS</td><td>A42</td><td>SDIO_IO_VDD</td><td>Inout</td><td>Pullup</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D3 - SDIO interface Data3 signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_ERR_INTR - SPI Bus Error Interrupt Signals</td><td>HighZ</td></tr>
<tr><td>USB</td><td>USB_CDC_DIS - USB-CDC Active-High Disable Signal</td><td>HighZ</td></tr>
<tr><td>Non-SDIO, SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
</td></tr>
</table>

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					The SPI interface is supported only in WiSeConnect™.
GPIO_46	A5	IO_VDD_1	Inout	HighZ	<table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>ANT_SEL - Antenna Select 1</td><td>HighZ</td></tr></table>
GPIO_47	A7	IO_VDD_1	Inout	HighZ	<table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>ANT_SEL_B - Antenna Select 2</td><td>HighZ</td></tr></table>
GPIO_48	B7	IO_VDD_1	Inout	HighZ	<table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>BT_ANT_SEL - Antenna Select for Bluetooth RF Chain</td><td>HighZ</td></tr></table>
GPIO_49	B6	IO_VDD_1	Inout	HighZ	<table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>HighZ</td><td>HighZ</td></tr></table>
GPIO_50	A6	IO_VDD_1	Inout	HighZ	<table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>HighZ</td><td>HighZ</td></tr></table>

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
GPIO_51	B5	IO_VDD_1	Inout	HighZ	<table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>**RS9116W-SB00-QMS-ABC**</td><td>HighZ</td><td>HighZ</td></tr></table>
ULP_GPIO_0	A35	ULP_IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following for **RS9116X-SB00-QMS-ABC** • WLAN_ACTIVE*: Active-High signal to indicate to an external Bluetooth IC that WLAN transmission is active. Part of the 3-wire coexistence interface. *This pin is intended to act as WLAN_ACTIVE for wireless coexistence. It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions.
ULP_GPIO_1	B22	ULP_IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following for **RS9116X-SB00-QMS-ABC** • BT_ACTIVE*: Active-High signal from an external Bluetooth IC that it is transmitting. Part of the 3-wire coexistence interface. *This pin is intended to act as BT_ACTIVE for Bluetooth coexistence. It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions.

<table>
<tr><th>Pin Name</th><th>QMS Pin Number</th><th>QMS I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td>ULP_GPIO_4</td><td>B21</td><td>ULP_IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>HighZ</td><td>HighZ</td></tr></table></td></tr>
<tr><td>ULP_GPIO_5</td><td>A19</td><td>ULP_IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>LP_WAKEUP_IN</td><td>HighZ</td></tr></table>This pin can be configured by software to be any of the following for RS9116W-SB00-QMS-ABC
LP_WAKEUP_IN: This is LP Powersave Wakeup indication to Device from HOST
HOST_WAKEUP_INDICATION: This is used as an indication from Host to the device that host is ready to take the packet and Device can transfer the packet to host. This is supported only in UART host mode.
The UART interface is supported only in WiSeConnect™.</td></tr>
<tr><td>ULP_GPIO_6</td><td>A22</td><td>ULP_IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>HighZ</td><td>HighZ</td></tr></table>This pin can be configured by software to be any of the following for RS9116W-SB00-QMS-ABC.
WAKEUP_FROM_Dev* - Used as a wakeup indication to host from device.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>QMS Pin Number</th><th>QMS I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>• BT_PRIORITY**: Active-high signal from an external Bluetooth IC that indicates that the Bluetooth transmissions are a higher priority.

*For Wake-on-Wireless feature, it is recommended to use an external weak pull-down or pull-up resistor. It is recommended to use weak pull-down resistor in new designs. Software has to be configured suitably for using either pull-down or pull-up resistor.

**This pin is intended to act as BT_PRIORITY for Bluetooth coexistence. It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions.</td></tr>
<tr><td>ULP_GPIO_7</td><td>B18</td><td>ULP_IO_VDD</td><td>Inout</td><td>HighZ</td><td><table><tr><th>Part Number</th><th>Default</th><th>Sleep</th></tr><tr><td>RS9116W-SB00-QMS-ABC</td><td>HighZ</td><td>HighZ</td></tr></table></td></tr>
<tr><td>ULP_GPIO_8</td><td>A36</td><td>ULP_IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: HighZ

Sleep: HighZ

This pin can be configured by software to be any of the following

• LED0: Control signal to an external LED.
* LED0 functionality currently not available in WiSeConnect™ modules</td></tr>
<tr><td>ULP_GPIO_9/ UART2_TX</td><td>A24</td><td>ULP_IO_VDD</td><td>Inout</td><td>HighZ</td><td>Default: UART2_TX- Debug UART Interface serial output

Sleep: HighZ</td></tr>
</table>

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					UART2_TX: Debug UART interface serial output.
ULP_GPIO_10	A23	ULP_IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • I2C_SCL: I2C interface clock.
ULP_GPIO_11	B17	ULP_IO_VDD	Inout	HighZ	**Default:** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • I2C_SDA: I2C interface data.
UULP_VBAT_GPIO_0	B10	UULP_VBATT_1	Output	High	**Default :** EXT_PG_EN **Sleep**: SLEEP_IND_FROM_DEV / EXT_PG_EN This pin can be configured by software to be any of the following • SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode. • EXT_PG_EN: Active-high enable signal to an external power gate which can be used to control the power supplies other than Always-ON VBATT Power Supplies in ULP Sleep mode.
UULP_VBAT_GPIO_2/ HOST_BYP_ULP_WAKE UP	B24	UULP_VBATT_1	Input	HighZ	**Default:** HOST_BYP **Sleep**: ULP_WAKEUP This signal has two functionalities – one during the bootloading process and one

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the chip should wake up from it's Ultra Low Power (ULP) sleep mode. The bootloader bypass functionality is supported only in WiSeConnect™.
UULP_VBAT_GPIO_3	A25	UULP_VBATT_1	Inout	HighZ	**Default :** HighZ **Sleep**: XTAL_32KHZ_IN / SLEEP_IND_FROM_DEV This pin can be configured by software to be any of the following • XTAL_32KHZ_IN: This pin can be used to feed external clock from a host processor or from external crystal oscillator. • SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode.
JP0	A17	IO_VDD_2	Input	Pullup	**Default:** JP0 **Sleep**: HighZ JP0 - Reserved. Connect to a test point for debugging purposes.
JP1	B16	IO_VDD_2	Input	Pullup	**Default:** JP1 **Sleep**: HighZ JP1 - Reserved. Connect to a test point for debugging purposes.

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
JP2	A16	IO_VDD_2	Input	Pullup	**Default:** JP2 **Sleep**: HighZ JP2 - Reserved. Connect to a test point for debugging purposes.
JNC	B15	IO_VDD_2	NC	Pullup	**Default:** JNC **Sleep**: HighZ JNC - Reserved. Connect to a test point for debugging purposes.
USB_DP	B36	USB_AVDD_3P3	Inout	NA	Positive data channel from the USB connector.
USB_DM	A40	USB_AVDD_3P3	Inout	NA	Negative data channel from the USB connector.
USB_ID	A37	USB_AVDD_3P3	Input	NA	ID signal from the USB connector.
USB_TXRTUNE	B37	USB_AVDD_3P3	Input	NA	USB Transmitter resistor tune analog signal which needs to be connected to an external 200 Ω resistor to adjusts the USB's high-speed source impedance.
USB_VBUS	A38	USB_AVDD_3P3	Input	NA	5V USB VBUS signal from the USB connector. This pin is used just for detecting USB.

Table 3 Chip Packages - Host and Peripheral Interfaces

1. **"Default"** state refers to the state of the device after initial boot loading and firmware loading is complete.
2. **"Sleep"** state refers to the state of the device after entering Sleep state which is indicated by Active-Low "SLEEP_IND_FROM_DEV" signal.
3. Please refer to **"RS9116 nLink Technical Reference Manual"** for software programming information in hosted mode.
4. Please refer to **"RS9116 Wireless SAPI Manual"** for software programming information in embedded mode.
5. There are some functionalities, such as SLEEP_IND_FROM_DEV, that are available on multiple pins. However, these pins have other multiplexed functionalities. Any pin can be used based on the required functionality. Customer has to note the default states before using appropriate pin.

2.2.4 Miscellaneous Pins

Pin Name	QMS Pin Number	QMS I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
FLY_P1	B28	UULP_VBATT_1	Input	NA	Fly Capacitor for Switched cap DCDC.
FLY_N1	A32	UULP_VBATT_1	Input	NA	Fly Capacitor for Switched cap DCDC.
XTAL_IN	B12	RF_VBATT	Input	NA	Input to the on-chip oscillator from the external 40 MHz crystal.
XTAL_OUT	A13	RF_VBATT	Output	NA	The output of the on-chip oscillator to the external 40 MHz crystal.
TRST	A15	IO_VDD_2	Input	HighZ	Test signal. Connect to Ground.
NC	A29,B9,B26,B27	NA	NA	NA	No connect.

Table 4 Chip Packages - Miscellaneous Pins

3 RS9116 QMS SoC Specifications

3.1 Absolute Maximum Ratings

Functional operation above maximum ratings is not guaranteed and may damage the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Units
T_{store}	Storage temperature	-40	+125	°C
$T_{j(max)}$	Maximum junction temperature	-	+125	°C
UULP_VBATT_1	Always-on VBATT supply to the UULP Domains	-0.5	3.63	V
UULP_VBATT_2	Always-on VBATT supply to the UULP Domains	-0.5	3.63	V
RF_VBATT	Always-on VBATT Power supply to the RF	-0.5	3.63	V
VINBCKDC	Power supply for the on-chip Buck	-0.5	3.63	V
VINLDOSOC	Power supply for SoC LDO	-0.5	1.8	V
VINLDO1P8	Power supply for 1.8V LDO	-0.5	3.63	V
FLASH_IO_VDD	I/O supply for Flash	-0.5	3.63	V
IO_VDD_1	I/O supplies for GPIOs	-0.5	3.63	V
IO_VDD_2	I/O supplies for GPIOs	-0.5	3.63	V
SDIO_IO_VDD	I/O supplies for SDIO I/Os.	-0.5	3.63	V
ULP_IO_VDD	I/O supplies for ULP GPIOs	-0.5	3.63	V
PA2G_AVDD	Power supply for the 2.4 GHz RF Power Amplifier	-0.5	3.63	V
RF_AVDD	Power supply for the 2.4 GHz RF and AFE	-0.5	1.98	V
PLL_AVDD	Power supply for the on-chip PLLs	-0.5	1.98	V
UULP_AVDD	Power supply for the always-on digital and ULP peripherals	-0.5	1.21	V
C_VDD	Power supply for the digital core	-0.5	1.26	V
USB_AVDD_3P3	Power supply for the USB interface	-0.5	3.63	V
USB_AVDD_1P1	Power supply for the USB core	-0.5	1.26	V
I_{max}	Maximum Current consumption in TX mode	-	400	mA
P_{max}	RF Power Level Input to the chip on pins RF pins	-	10	dBm
I_{Pmax}	Peak current rating for power supply	-	500	mA

Table 5 Absolute Maximum Ratings

3.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_{ambient}$	Ambient temperature	-40	25	85	°C

Symbol	Parameter	Min.	Typ.	Max.	Units
UULP_VBATT_1	Always-on VBATT supply to the UULP Domains	1.75/3.0	1.85/3.3	1.98/3.63	V
UULP_VBATT_2	Always-on VBATT supply to the UULP Domains	1.75/3.0	1.85/3.3	1.98/3.63	V
RF_VBATT	Always-on VBATT Power supply to the RF	1.75/3.0	1.85/3.3	1.98/3.63	V
VINBCKDC	Power supply for the on-chip Buck	1.75/3.0	1.85/3.3	1.98/3.63	V
VINLDOSOC	Power supply for SoC LDO	1.1	1.35	1.55	V
VINLDO1P8	Power supply for 1.8V LDO	1.75/3.0	1.85/3.3	1.98/3.63	V
FLASH_IO_VDD	I/O supply for Flash	1.65	1.85	1.98	V
IO_VDD_1	I/O supply for GPIOs	1.65/3.0	1.85/3.3	1.98/3.63	V
IO_VDD_2	I/O supply for GPIOs	1.65/3.0	1.85/3.3	1.98/3.63	V
SDIO_IO_VDD	I/O Supply for SDIO I/Os	1.65/3.0	1.85/3.3	1.98/3.63	V
ULP_IO_VDD	I/O Supply for ULP GPIOs.	1.65/3.0	1.85/3.3	1.98/3.63	V
PA2G_AVDD	Power supply for the 2.4 GHz RF Power Amplifier	3.0	3.3	3.63	V
RF_AVDD	Power supply for the 2.4 GHz RF and AFE	1.3	1.4	1.8	V
PLL_AVDD	Power supply for the on-chip PLLs	1.3	1.4	1.8	V
UULP_AVDD	Power supply for the always-on digital and ULP peripherals	0.95	1.0	1.21	V
C_VDD	Power supply for the digital core (Low Power Mode) Power supply for the digital core (High Performance Mode)	0.95 0.99	1.0 1.1	1.05 1.21	V V
USB_AVDD_3P3	Power supply for the USB interface	3.0	3.3	3.63	V
USB_AVDD_1P1	Power supply for the USB core	0.99	1.1	1.21	V

Table 6 Recommended Operating Conditions

3.3 DC Characteristics

3.3.1 Reset Pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage @3.3V	0.8 * VDD	-	-	V
	High level input voltage @1.8V	1.17	-	-	V
V_{IL}	Low level input voltage @3.3V	-	-	0.3 * VDD	V
	Low level input voltage @1.8V	-	-	0.63	V
V_{hys}	Hysteresis voltage	0.05 * VDD	-	-	V

Table 7 Reset Pin

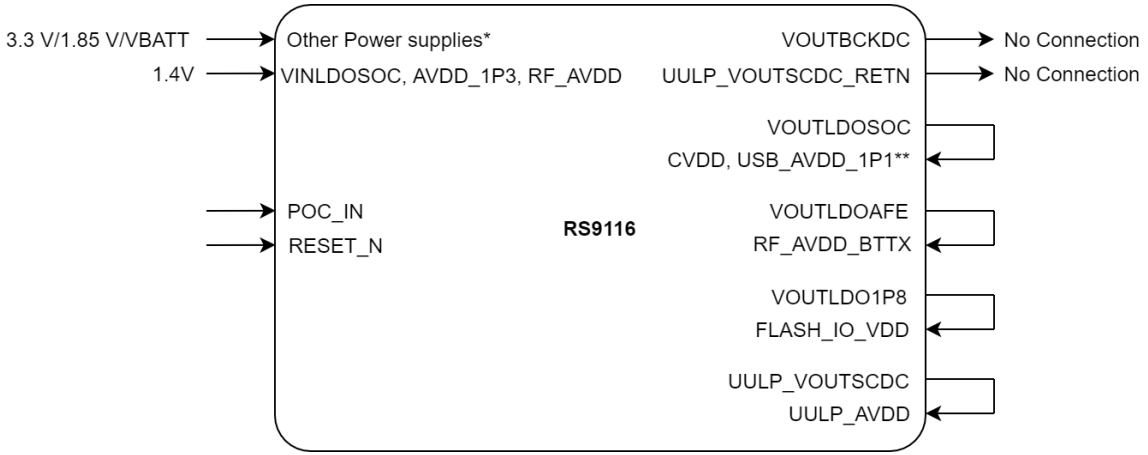
3.3.2 Power Sequence

The POC_IN and RESET_N signals should be controlled from external sources such as R/C circuits, and/or other MCU's GPIOs. However POC_OUT can be connected to POC_IN, if the supply voltage is 3.3V. Below waveforms show power sequence (Up & Down) requirements under various application needs. Note that below waveforms are not to scale.

3.3.2.1 Power-Up and Down Sequence with External 1.4V supply and POC_IN

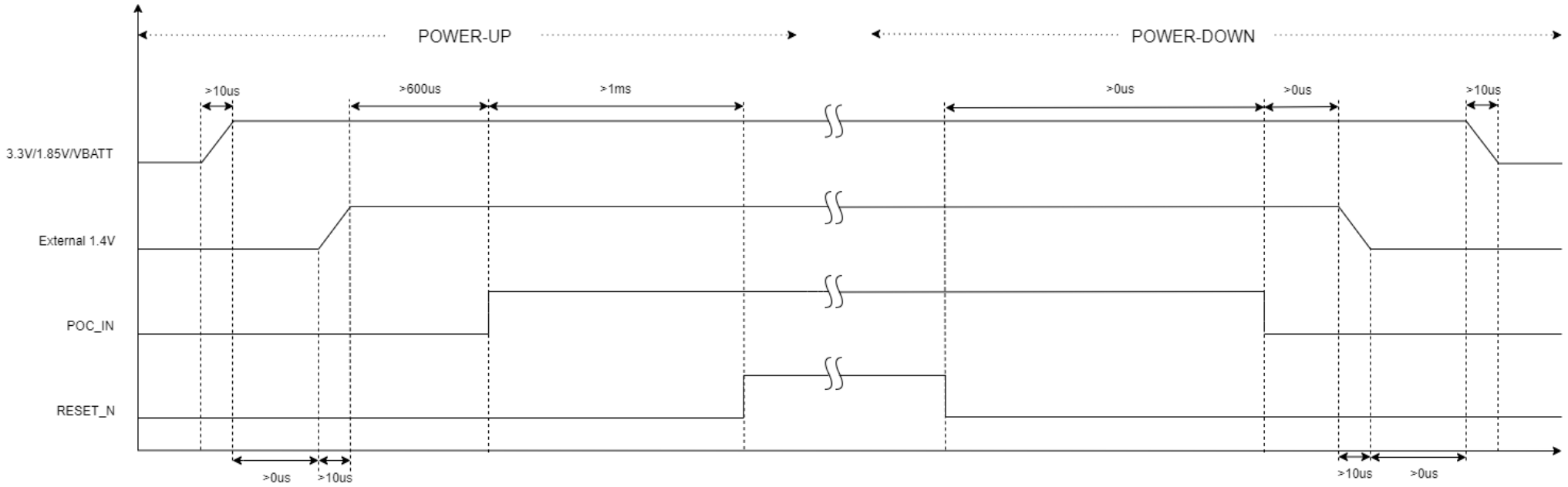
The diagram below shows connections of various power supply voltages, POC_IN and RESET_N. These connections can be used when:

- System PMU (outside RS9116) can provide 1.4V supply, and hence the internal Buck regulator in RS9116 can be disabled.
- The 1.1V supply is still derived from LDO SoC (internal to RS9116).
- POC_IN is controlled externally.



NOTE:

1. Above shown is a typical connection diagram. Some of the supply pins shown above may or may not be present in the IC/Module. Check the Pinout table in this datasheet and connect accordingly.
2. * = Provide the supply voltages as per the specifications mentioned in this datasheet.
3. ** = USB power supply input connection is required if USB interface is present and used. Else, follow the connection as shown in Reference Schematics.



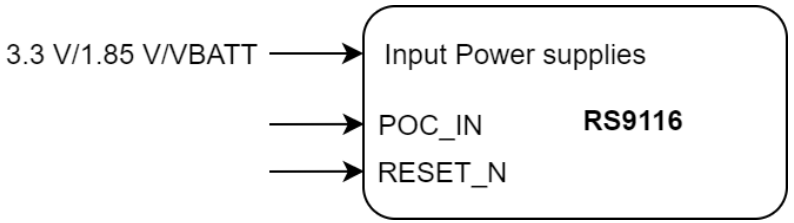
NOTE:

1. 3.3 V/1.85 V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.
2. Above POC_IN waveform is applicable if it is externally driven. Else, that particular waveform can be ignored, and the RESET_N timing can be considered after/before external power supplies ramp-up/down.

3.3.2.2 Power-Up and Down Sequence with External POC_IN

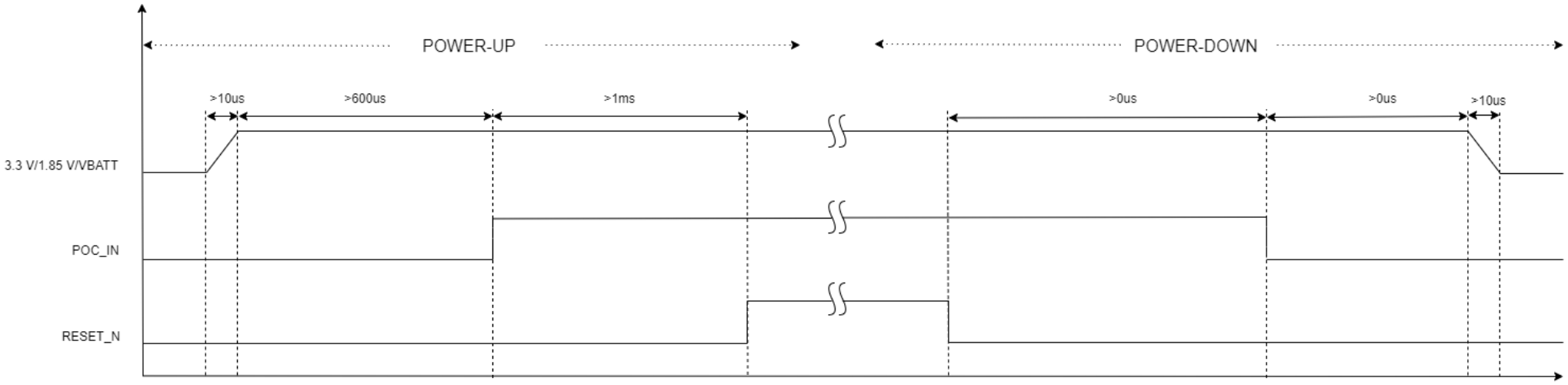
The diagram below shows connections of various power supply voltages, POC_IN and RESET_N. These connections can be used when:

- System PMU cannot provide 1.4V or 1.1V supplies and the internal buck and LDO of RS9116 are used.
- POC_IN is controlled externally.



NOTE:

1. Above shown is a typical connection diagram. Check the Reference Schematics for connections of other power supplies.



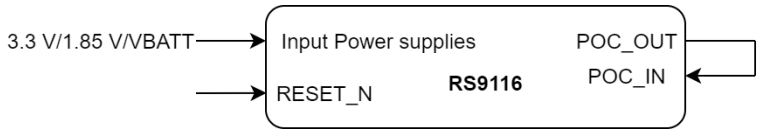
NOTE:

1. 3.3 V/1.85 V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.

3.3.2.3 Power-Up and Down Sequence with POC_IN connected internally

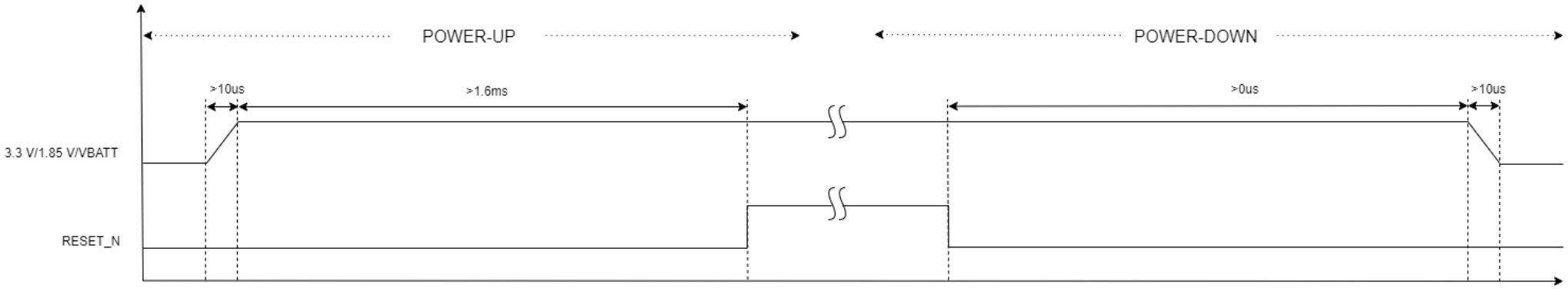
The diagram below shows connections of various power supply voltages, POC_IN and RESET_N. The typical applications of this connection can be as follows. This connection is **Not Recommended for New Design**.

- System cannot provide external 1.4V & 1.1V supplies and the internal buck and LDO of RS9116 are used.
- POC_IN is looped back from POC_OUT.



NOTE:

1. Above shown is a typical connection diagram. Check the Reference Schematics for connections of other power supplies.
2. POC_OUT can be connected to POC_IN if the supply voltage is 3.3V only. Else, POC_IN has to be driven externally.
3. This connection is **Not Recommended for New Design**, and it is recommended to drive POC_IN externally as shown in the above section. If POC_IN cannot be driven externally, then an RC circuit delay can be provided in between POC_IN and POC_OUT, for delaying the POC_OUT signal reaching POC_IN.



NOTE:

1. 3.3 V/1.85 V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.

3.3.3 Digital Input Output Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage @3.3V	2.0	-	-	V
	High level input voltage @1.8V	1.17	-	-	V
V_{IL}	Low level input voltage @3.3V	-	-	0.8	V
	Low level input voltage @1.8V	-	-	0.63	V
V_{hys}	Hysteresis voltage	0.1 VDD	-	-	V
V_{OL}	Low level output voltage	-	-	0.4	V
V_{OH}	High level output voltage	VDD-0.4	-	-	V
I_{OL}	Low level output current (programmable)	-	4.0	-	mA
I_{OH}	High level output current (programmable)	-	4.0	-	mA

Table 8 Digital I/O Signals

All numbers are at typical operating conditions unless otherwise stated.

3.3.4 USB

Parameter	Conditions	Min.	Typ.	Max.	Units
Vcm DC (DC level measured at receiver connector)	HS Mode LS/FS Mode	-0.05 0.8	-	0.5 2.5	V
Crossover Voltages	LS Mode FS Mode	1.3 1.3	-	2 2	V
Power supply ripple noise (Analog 3.3V)	< 160 MHz	-50	-	50	mV

Table 9 USB

3.3.5 Pin Capacitances

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{io}	Input/output capacitance, digital pins only	-	-	2.0	pF

Table 10 Pin Capacitances

3.4 AC Characteristics

3.4.1 Clock Specifications

RS9116 chipsets require two primary clocks:

- Low frequency 32 kHz clock for sleep manager and RTC
    - Internal 32 kHz RC clock is used for applications with low timing accuracy requirements
    - 32 kHz crystal clock is used for applications with high timing accuracy requirements
- High frequency 40 MHz clock for the ThreadArch® processor, baseband subsystem and the radio

The chipsets have integrated internal oscillators including crystal oscillators to generate the required clocks. Integrated crystal oscillators enable the use of low-cost passive crystal components. Additionally, in a system where an external clock source is already present, the clock can be reused. The following are the recommended options for the clocks for different functionalities:

Functionality	Default Clock option	Other Clock option	Comments
Wi-Fi or Wi-Fi + BLE Connectivity	Internal 32 kHz RC oscillator calibrated to <200ppm	32 kHz XTAL oscillator input on UULPGPIO.	32 kHz XTAL Oscillator clock is optional. No significant power consumption impact on connected power numbers (<10uA).
Wi-Fi + BT or Wi-Fi + BT + BLE Connectivity with low power Audio Streaming operation (A2DP Source)	32 kHz XTAL oscillator input on UULPGPIO	Internal 32 kHz RC oscillator calibrated to <200ppm	32 kHz XTAL Oscillator clock is important for Low-power Audio Streaming operation (A2DP Source).

There is no impact on sleep/deep-sleep power consumption with/without 32 kHz XTAL oscillator clock

32 kHz XTAL sources:

Option 1: From Host MCU/MPU LVCMOS rail to rail clock input on UULPGPIO

Option 2: External Xtal oscillator providing LVCMOS rail to rail clock input on UULPGPIO (Nano-drive clock should not be supplied).

3.4.1.1 32 kHz Clock

The 32 kHz clock selection can be done through software. RC oscillator clock is not suited for high timing accuracy applications and can increase system current consumption in duty-cycled power modes.

3.4.1.1.1 RC Oscillator

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		32.0		kHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage		1.2		%
Jitter	RMS value of Edge jitter (TIE)		91		ns
Peak Period Jitter	Peak value of Cycle Jitter with 6σ variation		789		ns

Table 11 32 kHz RC Oscillator

3.4.1.1.2 32 kHz External Oscillator

An external 32 kHz low-frequency clock can be fed through the XTAL_32KHZ_IN functionality.

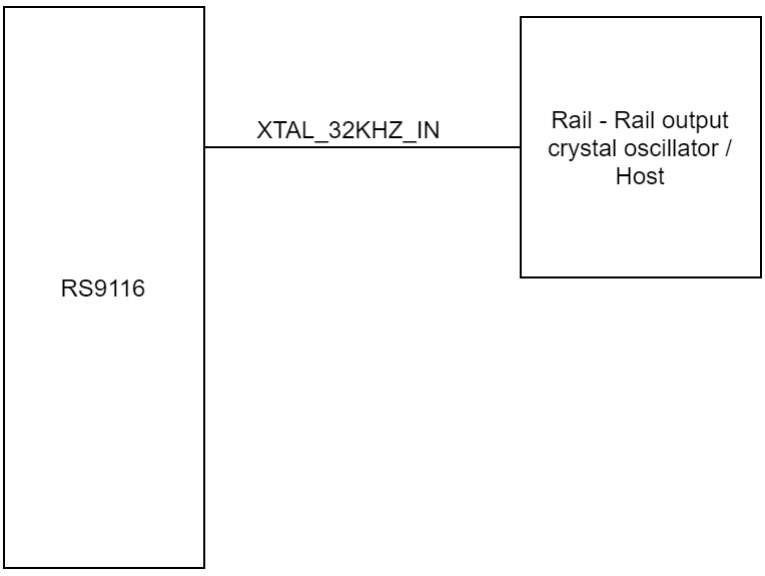


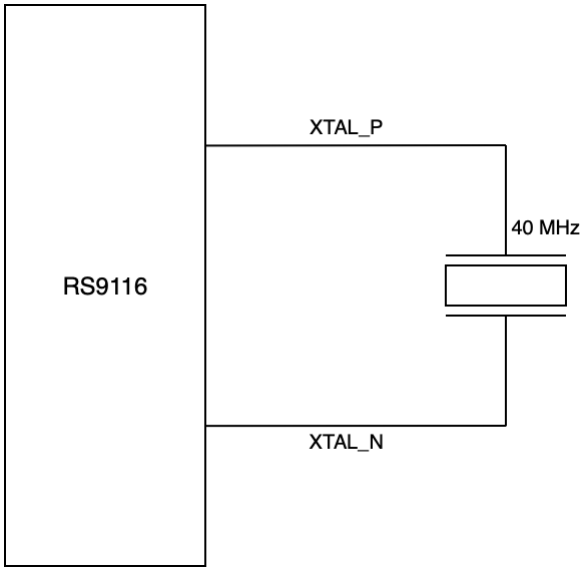
Figure 4 External 32 kHz Oscillator - Rail to Rail

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		32.768		kHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage	-100		100	ppm
Duty cycle	Input duty cycle	30	50	70	%
V_{AC}	Input AC peak-peak voltage swing at input pin.	-0.3	-	VBATT +/- 10%	Vpp

Table 12 32 kHz External Oscillator Specifications

3.4.1.2 40 MHz Clock

The 40 MHz internal oscillator mode can be used by connecting a 40 MHz crystal between the pins XTA L_P and XTAL_N. Load capacitance is integrated inside the chipset and calibrated and the calibrated value can be stored in eFuse using calibration software.



Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		40		MHz
Mode	Mode of Operation		Fundamental		
Resonance	Series or Parallel Resonance		Parallel		
Drive	Drive Level	100			uW
F_{osc_Acc}	Frequency Variation with Temp and Voltage	-20		20	ppm
ESR	Equivalent series resistance			60	Ω
Load cap	Load capacitance range	7		10	pF

Table 13 40 MHz Crystal Specifications

Wi-Fi standards mention a maximum variation of +/- 20 ppm for clock. This +/- 20 ppm includes variation due to crystal Process, Voltage, Temperature, and Aging. It is recommended for the user to have sufficient margin below this ppm. If the ppm variation due to Voltage, Temperature, and Aging is close to +/- 20 ppm, the trimming of Crystal for process is a useful option. If ppm is higher than 20 ppm, the user needs to trim/calibrate across Voltage, Temperature, and Aging, and ensure ppm is lower than 20 ppm with sufficient margin.

3.4.2 SDIO 2.0 Slave

3.4.2.1 Full Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{sdio}	SDIO_CLK	-	-	25	MHz
T_s	SDIO_DATA/SDIO_CMD, input setup time	4	-	-	ns
T_h	SDIO_DATA/SDIO_CMD, input hold time	1	-	-	ns
T_{od}	SDIO_DATA/SDIO_CMD, clock to output delay	-	-	13	ns
C_L	Output Load	5	-	10	pF

Table 14 AC Characteristics - SDIO 2.0 Slave Full Speed Mode

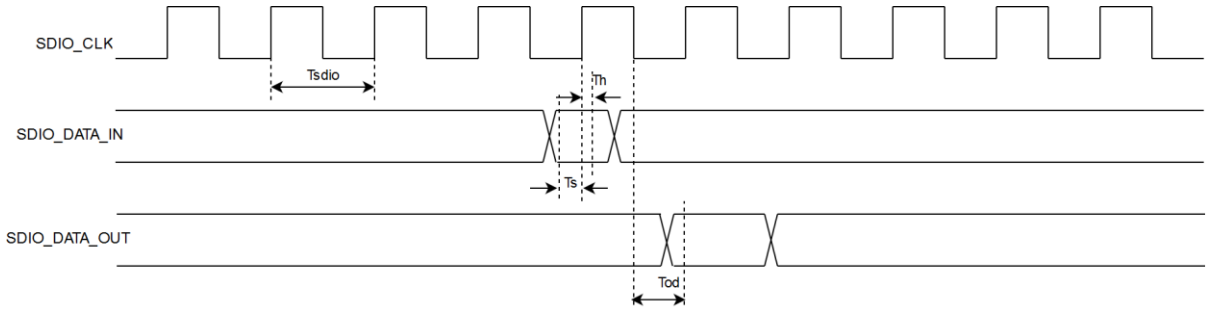


Figure 5 Interface Timing Diagram for SDIO 2.0 Slave Full Speed Mode

3.4.2.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{sdio}	SDIO_CLK	25	-	50	MHz
T_s	SDIO_DATA/SDIO_CMD, input setup time	4	-	-	ns
T_h	SDIO_DATA/SDIO_CMD, input hold time	1	-	-	ns
T_{od}	SDIO_DATA/SDIO_CMD, clock to output delay	2.5	-	13	ns
C_L	Output Load	5	-	10	pF

Table 15 AC Characteristics - SDIO 2.0 Slave High Speed Mode

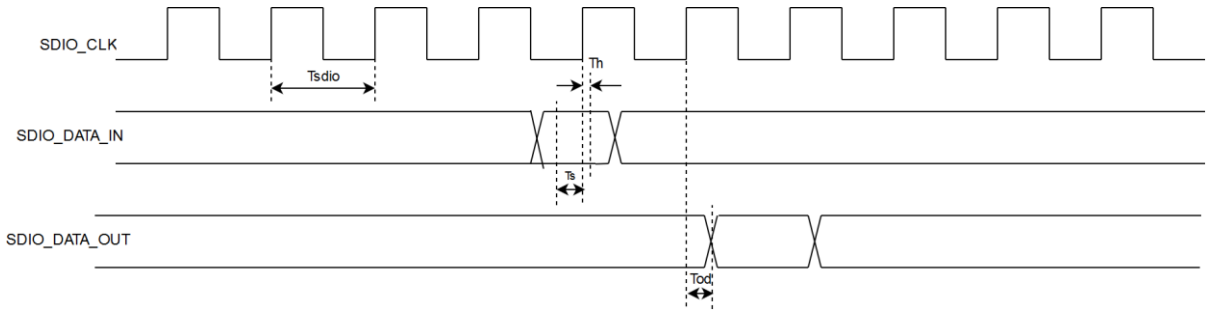


Figure 6 Interface Timing Diagram for SDIO 2.0 Slave High Speed Mode

3.4.3 SPI Slave

3.4.3.1 Low Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	0	-	25	MHz
T_{cs}	SPI_CS to output delay	-	-	7.5	ns
T_{cst}	SPI CS to input setup time	4.5	-	-	-
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	-	-	8.75	ns
C_L	Output Load	5	-	10	pF

Table 16 AC Characteristics - SPI Slave Low Speed Mode

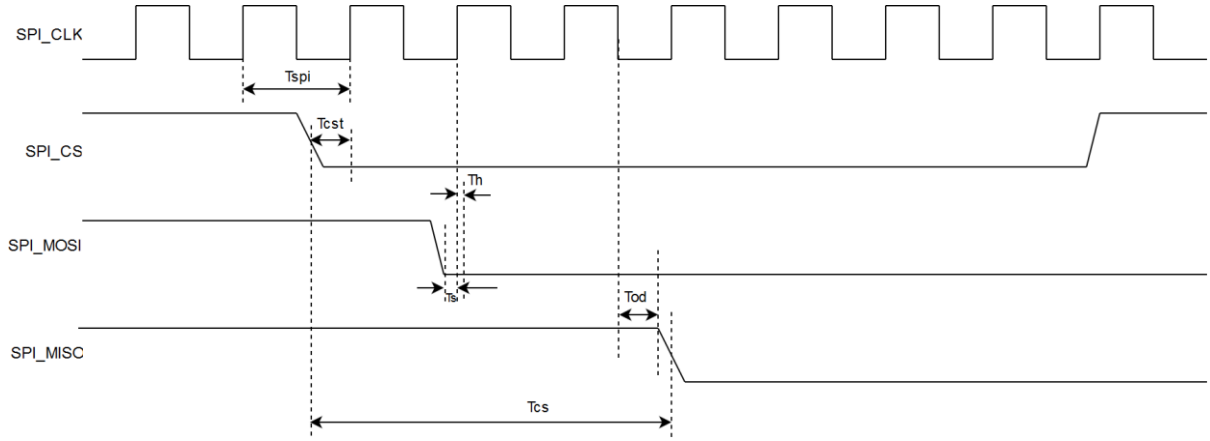


Figure 7 Interface Timing Diagram for SPI Slave Low Speed Mode

3.4.3.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	25	-	80	MHz
T_{cs}	SPI_CS to output delay	-	-	7.5	ns
T_{cst}	SPI CS to input setup time	4.5	-	-	-
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	2.5	-	8.75	ns
C_L	Output Load	5	-	10	pF

Table 17 AC Characteristics - SPI Slave High Speed Mode

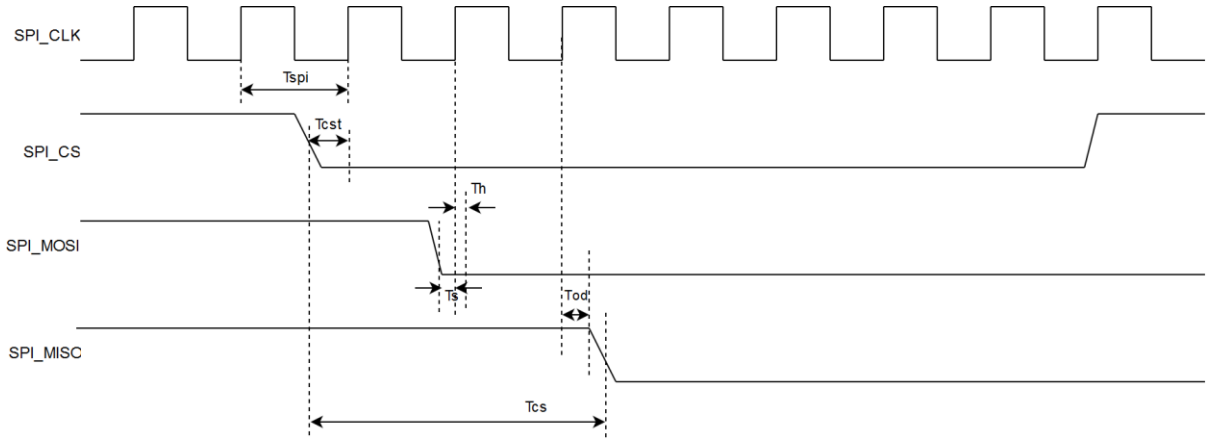


Figure 8 Interface Timing Diagram for SPI Slave High Speed Mode

3.4.3.3 Ultra High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	-	-	100	MHz
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	1.5	-	8.75	ns
C_L	Output Load	5	-	10	pF

Table 18 AC Characteristics - SPI Slave Ultra High Speed Mode

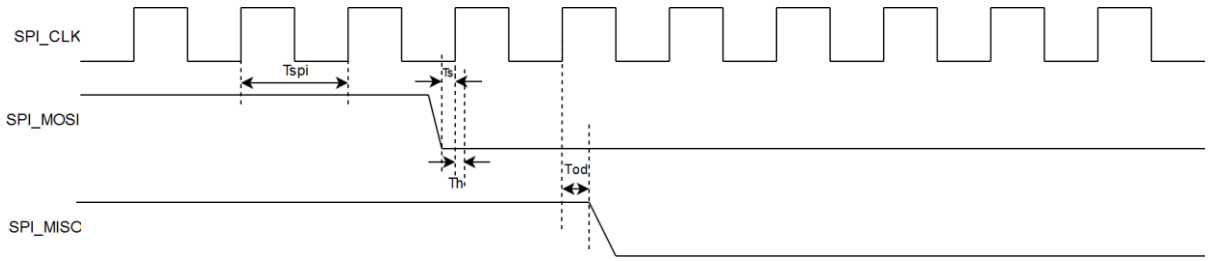


Figure 9 Interface Timing Diagram for SPI Slave Ultra High Speed Mode

3.4.4 USB

3.4.4.1 Low Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_r	Rise Time	75	-	300	ns
T_f	Fall Time	75	-	300	ns
Jitter	Jitter	-	-	10	ns

Table 19 AC Characteristics - USB Low Speed Mode

3.4.4.2 Full Speed Mode

Parameter	Parameter	Min.	Typ.	Max.	Unit
T_r	Rise Time	4	-	20	ns

Parameter	Parameter	Min.	Typ.	Max.	Unit
T_f	Fall Time	4	-	20	ns
Jitter	Jitter	-	-	1	ns

Table 20 AC Characteristics - USB Full Speed Mode

3.4.4.3 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_r	Rise Time	0.5	-	-	ns
T_f	Fall Time	0.5	-	-	ns
Jitter	Jitter	-	-	0.1	ns

Table 21 AC Characteristics - USB High Speed Mode

3.4.5 UART

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{uart}	CLK	0	-	20	MHz
T_{od}	Output delay	0	-	10	ns
T_s	Input setup time	0	-	5	ns
C_L	Output load	5	-	25	pF

Table 22 AC Characteristics - UART

3.4.6 I2C Master and Slave

3.4.6.1 Fast Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2c}	SCL	100	-	400	KHz
T_{low}	clock low period	1.3	-	-	us
T_{high}	clock high period	0.6	-	-	us
T_{sstart}	start condition, setup time	0.6	-	-	us
T_{hstart}	start condition, hold time	0.6	-	-	us
T_s	data, setup time	100	-	-	ns
T_{sstop}	stop condition, setup time	0.6	-	-	us
C_L	Output Load	5	-	10	pF

Table 23 AC Characteristics - I2C Fast Speed Mode

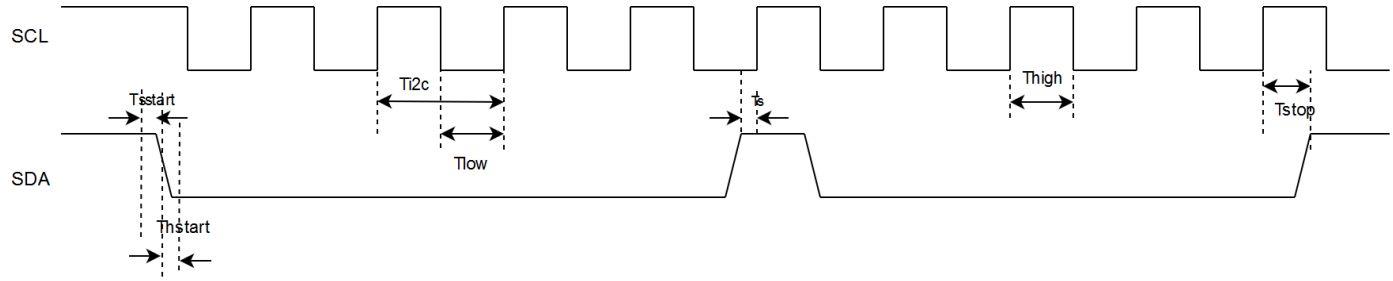


Figure 10 Interface Timing Diagram for I2C Fast Speed Mode

3.4.6.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2c}	SCL	0.4	-	3.4	MHz
T_{low}	clock low period	160	-	-	ns
T_{high}	clock high period	60	-	-	ns
T_{sstart}	start condition, setup time	160	-	-	ns
T_{hstart}	start condition, hold time	160	-	-	ns
T_s	data, setup time	10	-	-	ns
T_h	data, hold time	0	-	70	ns
T_{sstop}	stop condition, setup time	160	-	-	ns
C_L	Output Load	5	-	10	pF

Table 24 AC Characteristics - I2C High Speed Mode

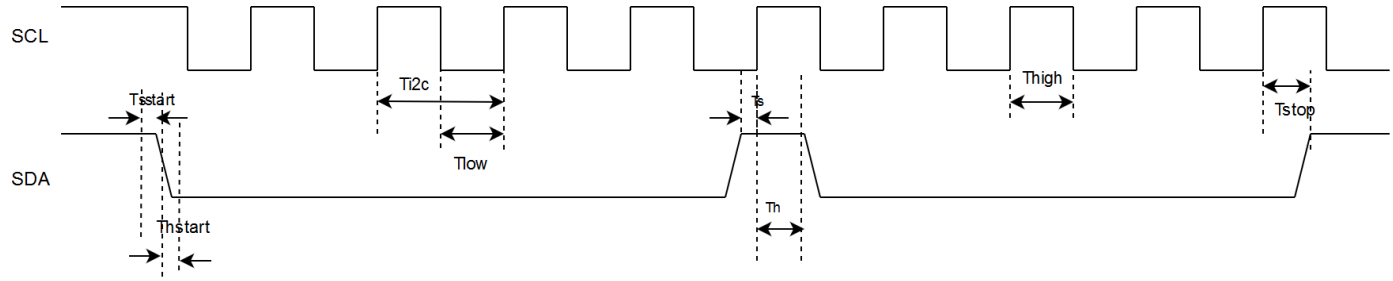


Figure 11 Interface Timing Diagram for I2C High Speed Mode

3.4.7 I2S/PCM Master and Slave

3.4.7.1 Master Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	25	MHz
T_s	i2s_din,i2s_ws setup time	10	-	-	ns
T_h	i2s_din,i2s_ws hold time	0	-	-	ns

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{od}	i2s_dout output delay	0	-	12	ns
C_L	i2s_dout output load	5	-	10	pF

Table 25 AC Characteristics – I2S/PCM Master Mode

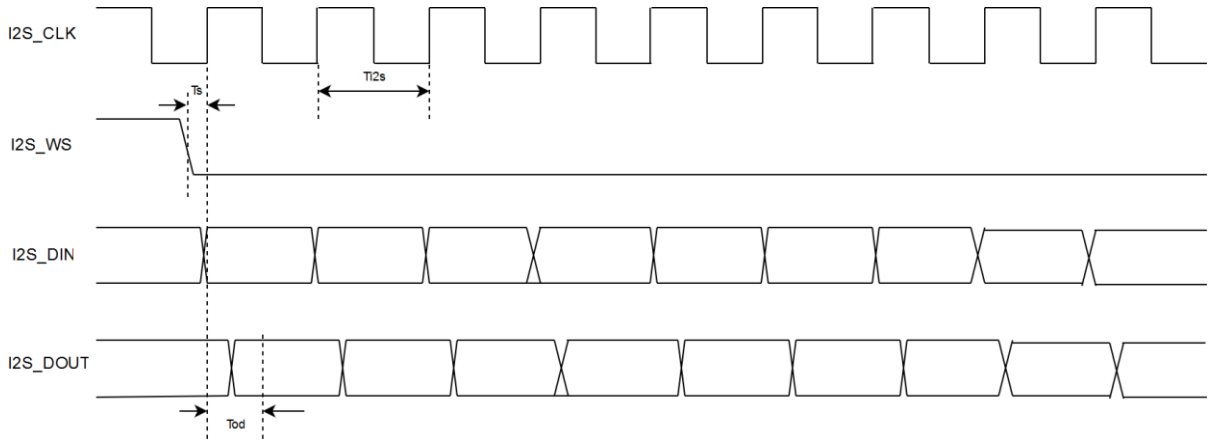


Figure 12 Interface Timing Diagram for I2S Master Mode

3.4.7.2 Slave Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	25	MHz
T_s	i2s_din,i2s_ws setup time	8	-	-	ns
T_h	i2s_din,i2s_ws hold time	0	-	-	ns
T_{od}	i2s_dout output delay	0	-	17	ns
C_L	i2s_dout output load	5	-	10	pF

Table 26 AC Characteristics - I2S/PCM Slave Mode

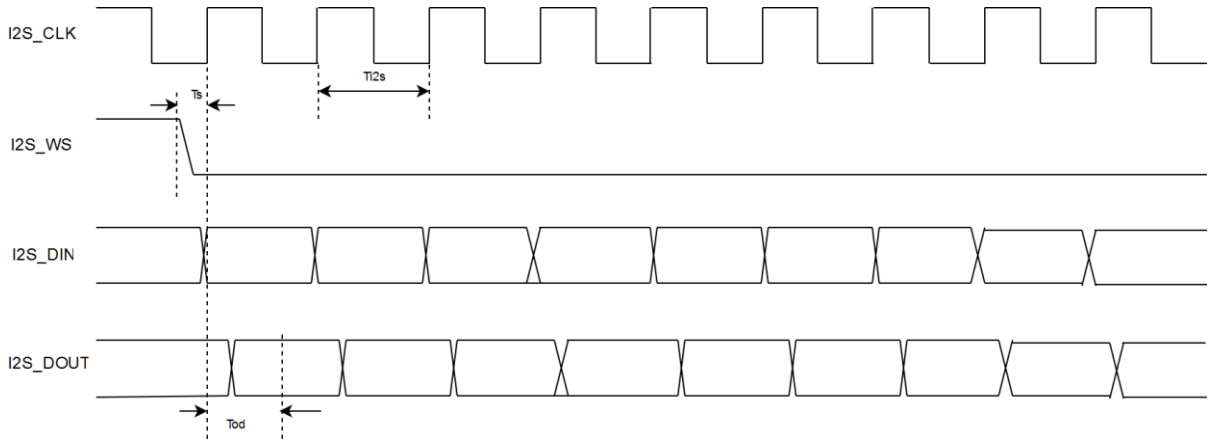


Figure 13 Interface Timing Diagram for I2S Slave Mode

3.4.8 GPIO pins

Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
T_{rf}	Rise time	Pin configured as output; SLEW = 1(fast mode)	1.0	-	2.5	ns
T_{ff}	Fall time	Pin configured as output; SLEW = 1(fast mode)	0.9	-	2.5	ns
T_{rs}	Rise time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	4.3	ns
T_{fs}	Fall time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	4.0	ns
T_{r}	Rise time	Pin configured as input	0.3	-	1.3	ns
T_{f}	Fall time	Pin configured as input	0.2	-	1.2	ns

Table 27 AC Characteristics - GPIO Pins

3.5 RF Characteristics

In the sub-sections below,

- All receiver sensitivity and transmit power numbers are at chip pin for the QMS package. The value at the antenna port will be lower depending on the front-end loss.
- All numbers are measured at typical operating conditions unless otherwise stated.

3.5.1 WLAN 2.4 GHz Transmitter Characteristics

3.5.1.1 Transmitter characteristics with 3.3V Supply

- TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions.
- The transmit power numbers are based on average performance across all channels.

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM	DSSS - 1 Mbps	EVM< -9 dB	-	20	-	dBm
	DSSS - 2 Mbps	EVM< -9 dB	-	20	-	dBm
	CCK- 5.5 Mbps	EVM< -9 dB	-	20	-	dBm
	CCK - 11 Mbps	EVM< -9 dB	-	19.5	-	dBm
	OFDM - 6 Mbps	EVM< -5 dB	-	20	-	dBm
	OFDM - 9 Mbps	EVM< -8 dB	-	20	-	dBm
	OFDM - 12 Mbps	EVM< -10 dB	-	20	-	dBm

Parameter	Condition	Notes	Min	Typ	Max	Units
	OFDM - 18 Mbps	EVM< -13 dB	-	20	-	dBm
	OFDM - 24 Mbps	EVM< -16 dB	-	19	-	dBm
	OFDM - 36 Mbps	EVM< -19 dB	-	17	-	dBm
	OFDM - 48 Mbps	EVM< -22 dB	-	16	-	dBm
	OFDM - 54 Mbps	EVM< -25 dB (see note section)	-	15	-	dBm
	MCS0 Mixed Mode	EVM< -5 dB	-	19.5	-	dBm
	MCS1 Mixed Mode	EVM< -10 dB	-	20	-	dBm
	MCS2 Mixed Mode	EVM< -13 dB	-	20	-	dBm
	MCS3 Mixed Mode	EVM< -16 dB	-	19	-	dBm
	MCS4 Mixed Mode	EVM< -19 dB	-	17	-	dBm
	MCS5 Mixed Mode	EVM< -22 dB	-	16	-	dBm
	MCS6 Mixed Mode	EVM< -25 dB (see note section)	-	16	-	dBm
	MCS7 Mixed Mode	EVM< -27 dB (see note section)	-	14	-	dBm
Transmitter Emissions (6 Mbps @ Maximum Power)	776-794 MHz	CDMA2000	-	-141	-	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	-	-159	-	dBm/Hz
	1450–1495 MHz	DAB	-	-151	-	dBm/Hz
	1570–1580 MHz	GPS	-	-148	-	dBm/Hz
	1592--1610 MHz	GLONASS	-	-130	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-128	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-110	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-121	-	dBm/Hz
	1910–1930 MHz	TDSCDMA,LTE	-	-132	-	dBm/Hz

Parameter	Condition	Notes	Min	Typ	Max	Units
	1930–1990 MHz	GSM1900, CDMAOne,WCDMA	-	-130	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-130	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-128	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-106	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-95	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-115	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-124	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-126	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-145	-	dBm/Hz
Harmonic Emissions (1 Mbps @ Maximum Power)	2nd Harmonic	-	-	-19.6	-	dBm/MHz
	3rd Harmonic	-	-	-10.5	-	dBm/MHz

Table 28 Transmitter characteristics with 3.3 V Supply

1. There is a variation of up to 2 dB in power across channels.
2. To meet FCC emission limits, band edge channels (1 and 11) TX power has to be reduced up to 5 dB in lower data rates and up to 3 dB in higher data rates. The radiated power in band edge is a strong function of the antenna properties. Refer to the AN1337 application note for note details on the certifications.
3. The output power may degrade up to 3 dB over the operating temperature range of -40 °C to +85 °C.
4. There may be a reduction in EVM of up to 1 dB in 54 Mbps data rate, 2 dB in MCS6 data rate, and 4 dB in MCS7 data rate.
5. *IEEE spectral mask limits may be crossed in lower data rates in some channels, and if required power may be backed off by 1-2 dB.*

3.5.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25°C. Parameters are measured at chip port on channel 1(2412 MHz)

- All WLAN receiver sensitivity numbers and adjacent channel numbers are at < 10% PER limit. Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11 n data rates.
- For WLAN ACI cases, the desired signal power is 3 dB above standard defined sensitivity level.

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity for 20MHz Bandwidth(1)	1 Mbps DSSS	-	-98.5	-	dBm
	2 Mbps DSSS	-	-93	-	dBm
	5.5 Mbps CCK	-	-90	-	dBm
	11 Mbps CCK	-	-88	-	dBm
	6 Mbps OFDM	-	-93	-	dBm
	9 Mbps OFDM	-	-92	-	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-89	-	dBm
	24 Mbps OFDM	-	-85.5	-	dBm
	36 Mbps OFDM	-	-82.5	-	dBm
	48 Mbps OFDM	-	-78	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
	MCS0 Mixed Mode	-	-91.5	-	dBm
	MCS1 Mixed Mode	-	-89.5	-	dBm
	MCS2 Mixed Mode	-	-87	-	dBm
	MCS3 Mixed Mode	-	-84.5	-	dBm
	MCS4 Mixed Mode	-	-80.5	-	dBm
	MCS5 Mixed Mode	-	-76.5	-	dBm
	MCS6 Mixed Mode	-	-74.5	-	dBm
	MCS7 Mixed Mode	-	-73	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	0	-	dBm
	802.11g	-	-10	-	dBm
	802.11n	-	-10	-	dBm
RSSI Accuracy Range		-3	-	3	dB
Blocking level for 3 dB RX Sensitivity Degradation(Data rate 6Mbps OFDM, Desired signal at -79dBm)	776–794 MHz	-	-14	-	dBm
	824–849 MHz	-	-14	-	dBm
	880–915 MHz	-	-16	-	dBm
	1710–1785 MHz	-	-13	-	dBm
	1850–1910 MHz	-	-18	-	dBm
	1920–1980 MHz	-	-20	-	dBm
	2300–2400 MHz	-	-58	-	dBm
	2570–2620 MHz	-	-24	-	dBm
	2545–2575 MHz	-	-24	-	dBm
Return Loss		-10	-	-	dB
Adjacent Channel Interference	1 Mbps DSSS	-	36	-	dB
	11 Mbps DSSS	-	37	-	dB
	6 Mbps OFDM	-	38	-	dB
	54 Mbps OFDM	-	22	-	dB
	MCS0 Mixed Mode	-	38	-	dB
	MCS7 Mixed Mode	-	20	-	dB
	1 Mbps DSSS	-	44	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Units
Alternate Adjacent Channel Interference	11 Mbps DSSS	-	35	-	dB
	6 Mbps OFDM	-	46	-	dB
	54 Mbps OFDM	-	30	-	dB
	MCS0 Mixed Mode	-	46	-	dB
	MCS7 Mixed Mode	-	28	-	dB

Table 29 WLAN 2.4 GHz Receiver Characteristics on HP RF Chain

1. Receive sensitivity may be degraded by up to 4 dB for channels 6,7,8,11,12,13 and 14 due to the desensitization of the receiver by harmonics of the system clock (40 MHz).
2. There may be a degradation of up to 2 dB across the operating temperature range of -40 °C to +85 °C.

3.5.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25°C. Parameters are measured at chip port on channel 1(2412 MHz)

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity for 20MHz Bandwidth(1)	1 Mbps DSSS	-	-96.5	-	dBm
	2 Mbps DSSS	-	-89.5	-	dBm
	5.5 Mbps CCK	-	-88	-	dBm
	11 Mbps CCK	-	-84.5	-	dBm
	6 Mbps OFDM	-	-89.5	-	dBm
	9 Mbps OFDM	-	-89.5	-	dBm
	12 Mbps OFDM	-	-89.5	-	dBm
	18 Mbps OFDM	-	-86.5	-	dBm
	24 Mbps OFDM	-	-83.5	-	dBm
	36 Mbps OFDM	-	-79	-	dBm
	MCS0 Mixed Mode	-	-88.5	-	dBm
	MCS1 Mixed Mode	-	-87.5	-	dBm
	MCS2 Mixed Mode	-	-85.5	-	dBm
	MCS3 Mixed Mode	-	-82.5	-	dBm
	MCS4 Mixed Mode	-	-78.5	-	dBm
Maximum Input Level for PER below 10%	802.11 b	-	-10	-	dBm
	802.11g	-	-10	-	dBm
	802.11n	-	-10	-	dBm
RSSI Accuracy Range		-3	-	3	dB

Parameter	Condition/Notes	Min	Typ	Max	Units
Blocking level for 3 dB RX Sensitivity Degradation(Data rate 6Mbps OFDM, Desired signal at -79dBm)	776–794 MHz	-	-14	-	dBm
	824–849 MHz	-	-19	-	dBm
	880–915 MHz	-	-16	-	dBm
	1710–1785 MHz	-	-14	-	dBm
	1850–1910 MHz	-	-14	-	dBm
	1920–1980 MHz	-	-23	-	dBm
	2300–2400 MHz	-	-26	-	dBm
	2570–2620 MHz	-	-23	-	dBm
	2545–2575 MHz	-	-22	-	dBm
Return Loss		-10	-	-	dB
Adjacent Channel Interference	1 Mbps DSSS	-	40	-	dB
	11 Mbps DSSS	-	36	-	dB
	6 Mbps OFDM	-	42	-	dB
	36 Mbps OFDM	-	30	-	dB
	MCS0 Mixed Mode	-	40	-	dB
	MCS4 Mixed Mode	-	30	-	dB
Alternate Adjacent Channel Interference	1 Mbps DSSS	-	50	-	dB
	11 Mbps DSSS	-	38	-	dB
	6 Mbps OFDM	-	48	-	dB
	36 Mbps OFDM	-	38	-	dB
	MCS0 Mixed Mode	-	48	-	dB
	MCS4 Mixed Mode	-	36	-	dB

Table 30 WLAN 2.4 GHz Receiver Characteristics on LP RF Chain

1. Receive sensitivity may be degraded by up to 4 dB for channels 6,7,8,11,12,13 and 14 due to the desensitization of the receiver by harmonics of the system clock (40 MHz).
2. There may be a degradation of up to 2 dB across the operating temperature range of -40 °C to +85 °C.

3.5.4 Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain

3.5.4.1 Transmitter characteristics with 3.3 V Supply

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are measured at chip port.(1)

- For Bluetooth C/I cases, the desired signal power is 3 dB above standard defined sensitivity level.

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power	BR		-	14	-	dBm
	EDR 2Mbps		-	14	-	dBm
	EDR 3Mbps		-	14	-	dBm
	LE 1Mbps		-	20	-	dBm
	LE 2Mbps		-	20	-	dBm
	LR 500 Kbps		-	20	-	dBm
	LR 125 Kbps		-	20	-	dBm
Power Control Step	BR, EDR		-	3	-	dB
Adjacent Channel Power |M-N| = 2	BR		-	-	-20	dBm
	EDR		-	-	-20	dBm
	LE		-	-	-20	dBm
	LR		-	-	-20	dBm
Adjacent Channel Power |M-N| > 2	BR		-	-	-40	dBm
	EDR		-	-	-40	dBm
	LE		-	-	-30	dBm
	LR		-	-	-30	dBm
BR Modulation Characteristics	DH1		-25	-	25	kHz
	DH3		-40	-	40	kHz
	DH5		-40	-	40	kHz
	Drift Rate		-20	-	20	kHz/50 us
	Δf1 Avg		140	-	175	kHz
	Δf2 Max		115	-		kHz
EDR Modulation Characteristics	RMS DEVM, EDR2			24		%
	RMS DEVM, EDR3			6		%
	99% DEVM, EDR2			37		%
	99% DEVM, EDR3			20		%
	peak DEVM,EDR2			49		%
	peak DEVM,EDR3			13		%
BLE Modulation Characteristics	Δf1 Avg		225	-	275	kHz
	Δf2 Max		185	-	-	kHz
	Δf2 Avg/Δf1 Avg		0.8	1.2	-	-
	776-794 MHz	CDMA2000	-	-161	-	dBm/Hz

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmitter Emissions (BR @Maximum output power)	869–960 MHz	CDMAOne, GSM850	-	-161	-	dBm/Hz
	1450–1495 MHz	DAB	-	-158	-	dBm/Hz
	1570–1580 MHz	GPS	-	-159	-	dBm/Hz
	1592--1610	GLONASS	-	-159(2)	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-115	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-148	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-148	-	dBm/Hz
	1910–1930 MHz	TDSCDMA,LTE	-	-132	-	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne, WCDMA	-	-148	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-148	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-138	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-141	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-135	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-141	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-142	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-138	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-144	-	dBm/Hz

Table 31 Bluetooth Transmitter characteristics with 3.3 V Supply

1. There is a variation of up to 2 dB in power across channels.
2. Noise-floor is -159 dBm/Hz with spurious tone power of -65 dBm at 1601.33 MHz when transmitted signal is at 2402 MHz
3. The output power may degrade up to 3 dB over the operating temperature range of -40 °C to +85 °C.

3.5.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

TA = 25°C. Parameters are measured at chip port and applicable to PA2G_AVDD/VINBCKDC=3.3V

- For Bluetooth C/I cases, the desired signal power is 3 dB above standard defined sensitivity level.

Parameter	Condition/Notes	Min	Typ	Max	Units
Transmit Power	LE 1Mbps	-	-	-0.5	dBm
	LE 2Mbps	-	-	-0.5	dBm
	LR 500 Kbps	-	-	-0.5	dBm
	LR 125 kbps	-	-	-0.5	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
Adjacent Channel Power |M-N| = 2	LE	-	-	-20	dBm
	LR	-	-	-20	dBm
Adjacent Channel Power |M-N| > 2	LE	-	-	-30	dBm
	LR	-	-	-30	dBm
BR Modulation Characteristics	DH1	-25	-	25	kHz
	DH3	-40	-	40	kHz
	DH5	-40	-	40	kHz
	Drift Rate	-20	-	20	kHz
	Δf1 Avg	140	-	175	kHz
	Δf2 Max	115	-	-	kHz
BLE Modulation Characteristics	Δf1 Avg	225	-	275	kHz
	Δf2 Max	185	-	-	kHz
	Δf2 Avg/Δf1 Avg	0.8	1.2	-	-

Table 32 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

1. There is a variation of up to 2 dB in power across channels.
2. Noise-floor is -159dBm/Hz with spurious tone power of -65dBm at 1601.33 MHz when transmitted signal is at 2402 MHz
3. The output power may degrade up to 3 dB over the operating temperature range of -40 °C to +85 °C.

3.5.6 Bluetooth Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25°C. Parameters are measured at chip port and applicable to PA2G_AVDD/VINBCKDC=3.3V

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off[1],[2]	BR (1 Mbps), 339 bytes, DH5 Packet, BER= 0.1%	-	-93.5	-	dBm
	EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01%	-	-94	-	dBm
	EDR3 (3 Mbps), 1020 bytes, 3-DH5 Packet, BER= 0.01%	-	-88	-	dBm
	LE (1 Mbps), 37 bytes, PER=30.8%	-	-95	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-93	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-102	-	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-106	-	dBm
Maximum Input Level	BR, EDR2, EDR3,BER= 0.1%	-	-16	-	dBm
	LE 1Mbps, 2Mbps,PER=30.8%	-	-8	-	dBm
	LR 500kps, 125kbps,PER=30.8%	-	-8	-	dBm
C/I Performance	BR, co-channel, BER=0.1%	9	-	-	dB
	BR, adjacent +1/-1 MHz, BER=0.1%	-2	-	-	dB
	BR, adjacent +2/-2 MHz BER=0.1%	-19	-	-	dB
	BR, adjacent >=|±3| MHz BER=0.1%	-19	-	-	dB
	BR, Image channel BER=0.1%	-11	-	-	dB
	BR, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR2, co-channel BER=0.1%	11	-	-	dB
	EDR2, adjacent +1/-1 MHz BER=0.1%	-2	-	-	dB
	EDR2, adjacent +2/-2 MHz BER=0.1%	-17	-	-	dB
	EDR2, adjacent >=|±3| MHz BER=0.1%	-17	-	-	dB
	EDR2, Image channel BER=0.1%	-9	-	-	dB
	EDR2, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR3, co-channel BER=0.1%	19	-	-	dB
	EDR3, adjacent +1/- MHz BER=0.1%	3	-	-	dB
	EDR3, adjacent +2/-2 MHz BER=0.1%	-12	-	-	dB
	EDR3, adjacent >=|±3| MHz BER=0.1%	-12	-	-	dB
	EDR3, Image channel BER=0.1%	-2	-	-	dB
	EDR3, adjacent to Image channel BER=0.1%	-15	-	-	dB
	LE 1Mbps, co-channel PER=30.8%	-	10	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	2	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	-3	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	-22	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Units
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	-25	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	-21	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	-27	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	-34	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-24	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	-34	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	-21	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	10	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	-4	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	-4	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	-13	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	-18	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	-33	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	-13	-	dB
	LE 2Mbps, +2MHz adjacent to Image channel PER=30.8%	-	-25	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	-4	-	dB

Table 33 Bluetooth Receiver Characteristics on HP RF Chain

1. **BR,EDR:** Receiver sensitivity is degraded by up to 6 dB for channels 38,78 due to the desensitization of the receiver by harmonics of the system clock (40MHz)
2. **BLE,LR:** Receiver sensitivity is degraded by up to 5 dB for channels 19,29,30,39 due to the desensitization of the receiver by harmonics of the system clock (40MHz)
3. There may be a degradation of up to 2 dB across the operating temperature range of -40 °C to +85 °C.

3.5.7 Bluetooth Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25°C. Parameters are measured at chip port and applicable to PA2G_AVDD/VINBCKDC=3.3V

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off[1],[2]	BR (1 Mbps), 339 bytes, DH5 Packet BER= 0.1%	-	-90	-	dBm
	EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01%	-	-90.5	-	dBm
	LE (1 Mbps), 37 bytes, PER=30.8%	-	-93.5	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-91	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-100.5	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-104.5	-	dBm
Maximum Input Level	BR, EDR2 BER= 0.1%	-	-10	-	dBm
	LE 1Mbps, 2Mbps PER=30.8%	-	-10	-	dBm
	LR 500kps, 125kbps PER=30.8%	-	-10	-	dBm
BER Floor		-	1e-4	-	%
C/I Performance	BR, co-channel BER= 0.1%	9	-	-	dB
	BR, adjacent +1/-1 MHz, BER=0.1%	-2	-	-	dB
	BR, adjacent +2/-2 MHz BER=0.1%	-19	-	-	dB
	BR, adjacent >=|±3| MHz BER=0.1%	-19	-	-	dB
	BR, Image channel BER=0.1%	-11	-	-	dB
	BR, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR2, co-channel BER=0.1%	11	-	-	dB
	EDR2, adjacent +1/-1 MHz BER=0.1%	-2	-	-	dB
	EDR2, adjacent +2/-2 MHz BER=0.1%	-17	-	-	dB
	EDR2, adjacent >=|±3| MHz BER=0.1%	-17	-	-	dB
	EDR2, Image channel BER=0.1%	-9	-	-	dB
	EDR2, adjacent to Image channel BER=0.1%	-22	-	-	dB
	LE 1Mbps, co-channel PER=30.8%	-	10	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	2	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	-2	-	dB

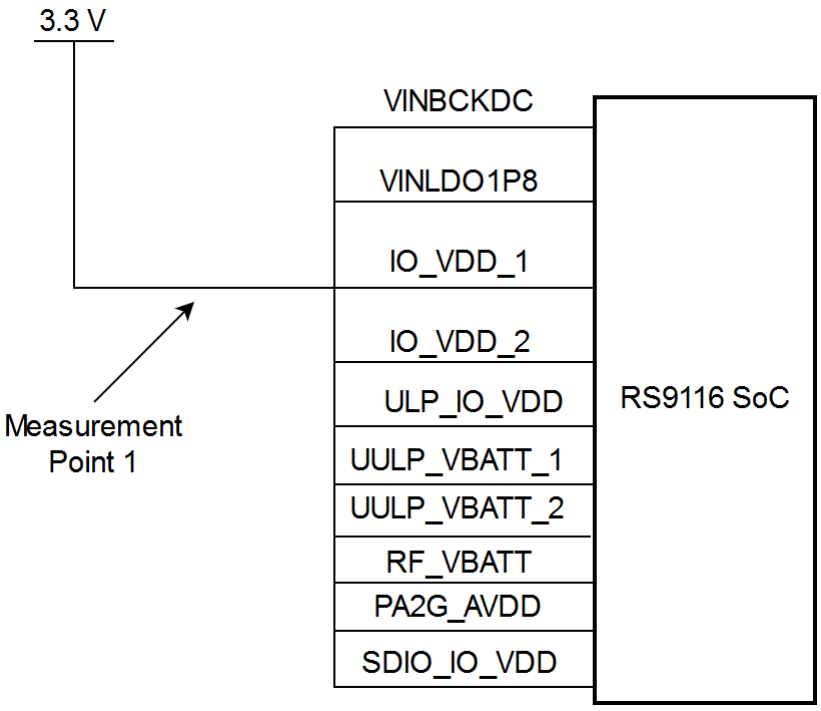
Parameter	Condition/Notes	Min	Typ	Max	Units
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	-22	-	dB
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	-24	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	-21	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	-27	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	-34	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-27	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	-35	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	-21	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	10	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	-5	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	-3	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	-12	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	-18	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	-34	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	-12	-	dB
	LE 2Mbps, +2MHz adjacent to Image channel PER=30.8%	-	-24	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	-5	-	dB

Table 34 Bluetooth Receiver Characteristics on LP RF Chain

1. **BR,EDR:** Receiver sensitivity is degraded by up to 6 dB for channels 38,78 due to the desensitization of the receiver by harmonics of the system clock (40MHz)
2. **BLE,LR:** Receiver sensitivity is degraded by up to 5 dB for channels 19,29,30,39 due to the desensitization of the receiver by harmonics of the system clock (40MHz)
3. There may be a degradation of up to 2 dB across the operating temperature range of -40 °C to +85 °C.

3.6 Typical Current Consumption

3.6.1 3.3 V



3.6.1.1 WLAN 2 GHz

Parameter	Description	Value	Units
1 Mbps Listen	LP Chain	13.82	mA
1 Mbps RX Active	LP Chain	19.67	mA
6 Mbps RX Active	HP Chain	48.2	mA
72 Mbps RX Active	HP Chain	48.2	mA
11 Mbps TX Active	Tx Power = Maximum (20dBm) Tx Power = 10dBm	270 130	mA mA
6 Mbps TX Active	Tx Power = Maximum (20dBm) Tx Power = 10dBm	285 130	mA mA
54 Mbps TX Active	Tx Power = Maximum (17dBm) Tx Power = 10dBm	200 130	mA mA
72 Mbps TX Active	Tx Power = Maximum (14dBm) Tx Power = 10dBm	180 130	mA mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA
Standby Associated, DTIM = 1		293	uA

Parameter	Description	Value	Units
Standby Associated, DTIM = 3		119	uA
Standby Associated, DTIM = 10		51	uA

3.6.1.2 Bluetooth BR and EDR

Parameter	Description	Value	Units
TX Active Current, 1 Mbps BR	LP chain, Tx Power = 0 dBm HP chain, Tx Power = Maximum (14 dBm)	9.9 130	mA mA
RX Active Current, 1 Mbps BR	LP chain HP chain	10.2 26.7	mA mA
TX Active Current, 2 Mbps EDR	HP chain, Tx Power = Maximum (14 dBm)	130	mA
RX Active Current, 2 Mbps EDR	LP chain HP chain	10.2 26.7	mA mA
TX Active Current, 3 Mbps EDR	HP chain, Tx Power = Maximum (14 dBm)	140	mA
RX Active Current, 3 Mbps EDR	HP chain	26.7	mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA

3.6.1.3 Bluetooth LE

Parameter	Description	Value	Units
TX Active Current	LP chain, Tx Power = 0 dBm LP Chain, Tx Power = 4 dBm HP Chain, Tx Power = Maximum (20 dBm)	8.9 - 190	mA mA mA
RX Active Current	LP chain HP chain	10.9 26.7	mA mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA
Advertising, Unconnectable	Advertising on all 3 channels Advertising Interval = 1.28s	22.4	uA

Parameter	Description	Value	Units
	Tx Power = 0 dBm, LP chain		
Advertising, Connectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = 0 dBm, LP chain	30.1	uA
Connected	Connection Interval = 1.28s No Data Tx Power = 0 dBm, LP chain	21.8	uA
Connected	Connection Interval = 200ms No Data Tx Power = 0 dBm, LP chain	72	uA

4 RS9116 QMS SoC Detailed Description

4.1 Overview

RS9116 is an ultra-low-power, single spatial stream, 802.11n + BT/BLE5.0 Convergence SoC. The RS9116 chipset family provides low-cost CMOS integration of a multi-threaded MAC processor (ThreadArch®), baseband digital signal processing, analog front-end, calibration eFuse, 2.4GHz RF transceiver, integrated power amplifier, and Quad-SPI Flash thus providing a fully-integrated solution for a range of hosted and embedded wireless applications. With Silicon Labs' embedded four-threaded processor and on-chip ROM and RAM, these chipsets enable integration into low-cost and zero host load applications. With an integrated PMU and support for a variety of digital peripherals, RS9116 enables very low-cost implementations for wireless hosted and embedded applications. It can be connected to a host processor through SDIO, USB, SPI or UART interfaces. Wireless firmware upgrades and provisioning are supported.

4.2 Chipset Features

4.2.1 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n with single band support
- Support for 20 MHz channel bandwidth
- Transmit power up to +20 dBm with integrated PA
- Receive sensitivity as low as -98.5 dBm
- Data Rates: 802.11b: Up to 11 Mbps; 802.11g: Up to 54 Mbps; 802.11n: MCS0 to MCS7
- Operating Frequency Range: 2412 MHz – 2484 MHz

4.2.1.1 MAC

- Conforms to IEEE 802.11b/g/n/j standards for MAC
- Dynamic selection of fragment threshold, data rate, and antenna depending on the channel statistics
- Hardware accelerators for WEP 64/128-bit and AES
- WPA, WPA2, and WMM support
- AMPDU and AMSDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS)

4.2.1.2 Baseband Processing

- Supports DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates (6, 9, 12, 18, 24, 36, 48, 54 Mbps, MCS0 to MCS7), and Short GI in Hosted mode
- Supports IEEE 802.11n single-stream modes with data rates up to 150 Mbps
- Supports long, short, and HT preamble modes
- High-performance multipath compensation in OFDM, DSSS, and CCK modes

4.2.2 Bluetooth

- Transmit power up to +20 dBm with integrated PA
- Receive sensitivity:- LE: -95 dBm, LR 125 Kbps: -106 dBm
- Compliant to dual-mode Bluetooth 5
- <8 mA transmit current in Bluetooth 5 mode, 2 Mbps data rate
- Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps, 3 Mbps
- Operating Frequency Range: 2.402 GHz - 2.480 GHz
- Bluetooth 2.1 + EDR, Bluetooth Low Energy 4.0 / 4.1 / 4.2 / 5.0

- Bluetooth Low Energy 1 Mbps, 2 Mbps and Long Range modes
- Bluetooth Low Energy Secure connections
- Bluetooth Low Energy supports central role and peripheral role concurrently
- Bluetooth auto rate and auto TX power adaptation
- Scatternet* with two slave roles while still being visible

> * For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

4.2.2.1 MAC

4.2.2.1.1 Link Manager

- Creation, modification & release of logical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- Services the data transport requests from L2CAP and provides required QOS
- Support for security using ECDH hardware accelerator

4.2.2.1.2 Link Controller

- Encodes and decodes header of BT packets
- Manages flow control, acknowledgment, retransmission requests, etc.
- Stores the last packet status for all logical transports
- Chooses between SCO & ACL buffers depending on the control information coming from BBP resource manager
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

4.2.2.1.3 Host Controller

- Receives & decodes commands received from the Bluetooth Host.
- Propagates the decoded commands to respective modules
- Responsible for transmitting and receiving packets from and to Host
- Formats the responses coming from other modules of Bluetooth Controller as events and sends them to the Host.

4.2.2.1.4 Device Manager

- Controls Scan & Connection processes
- Controls all BT Device operations except data transport operations
- Storing link keys
- BT Controller state transition management
- Slot synchronization & management
- Access contract management
- Scheduler

4.2.2.2 Baseband Processing

- Supports GFSK (1 Mbps), EDR-DQPSK, EDR-D8PSK
- Supports BLE and Bluetooth long range

- Supports Data rates up to 3 Mbps

4.2.3 RF Transceiver

- Integrated 2.4 GHz transceiver with highly programmable operating modes
- Internal oscillator with 40 MHz crystal
- Inbuilt automatic boot up and periodic calibration enables ease of integration

4.2.4 Host Interfaces

- SDIO
    - Version 2.0-compatible
    - Supports SD-SPI, 1-bit, and 4-bit SDIO modes
    - Operation up to a maximum clock speed of 50 MHz
- SPI Interface
    - Operation up to a maximum clock speed of 100 MHz
- USB 2.0
    - Supports 480Mbps “High Speed” (HS), 12Mbps “Full Speed” (FS) and 1.5Mbps “Low Speed” (LS) serial data transmission
    - Support USB CDC and device mode
- UART
    - Supports variable baud rates between 9600 and 3686400 bps
    - AT command interface for configuration and data transmission/reception

NOTE: Hosted mode (n-Link) supports USB 2.0 and SDIO. Embedded Mode (WiSeConnect) supports SPI, USB CDC, and UART.

4.2.4.1 Auto Host detection

RS9116 detects the host interface automatically after connecting to respective host controllers like SDIO, SPI, UART, USB and USB-CDC. SDIO/SPI host interface is detected through the hardware packet exchanges. UART host interface is detected through the software based-on the received packets on the UART interface. USB-Device mode interface is detected through the hardware based-on VBUS signal level. The host interface detection between USB & USB-CDC will be taken care by the firmware based on the USB_CDC_DIS GPIO. This Host configuration is stored in always-on domain registers after detection (on power up) and reused this information at each wakeup.

4.2.5 Wireless Coexistence Manager

- Arbitration between Wi-Fi, Bluetooth, and Bluetooth Low Energy
- Application aware arbitration
- Adaptive frequency hopping (AFH) in Bluetooth is based on WLAN channel usage
- Pre inter thread interrupts generation for radio switching
- QoS assurance across different traffics

4.2.6 Software

The RS9116 software package supports 802.11 b/g/n Client, Access Point (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security, dual-mode BT 5.0 functionality on a variety of host platforms and operating systems. The software package includes complete firmware, reference drivers, application profiles and configuration graphical user interface (GUI) for Linux operating systems. The Wi-Fi driver has support for a simultaneous access point, and client mode. Bluetooth host driver utilizes Opensource host stacks like BlueZ for Linux. The application layer supports all profiles supported by BlueZ on Linux. It has a wireless coexistence manager to arbitrate between protocols.

The RS9116 software package is available in two flavors

- **Hosted mode (n-Link™):** Wi-Fi stack, Bluetooth stack and profiles, and all network stacks reside on the host processor. Support for multiple Virtual Access Points available.
- **Embedded mode (WiSeConnect™):** Wi-Fi stack, TCP/IP stack, IP modules, Bluetooth stack and some profiles reside in RS9116; Some of the Bluetooth profiles reside in the host processor

NOTE: Please refer to the Software Manuals (TRM and PRM) in RS9116 Document Library for more details.

4.2.6.1 Hosted Mode (n-Link™)

- Available host interfaces: SDIO 2.0 and USB HS
- Application data throughput up to 50 Mbps (Hosted Mode) in 802.11n with 20MHz bandwidth.
- Host drivers for Linux
- Support for Client mode, Access point mode (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

4.2.6.2 Embedded Mode (WiSeConnect™)

- Available host interface: UART, SPI, and USB CDC
- Support for Embedded Client mode, Access Point mode (Up to 8 clients), Concurrent Client and Access Point mode, and Enterprise Security
- Supports advanced security features: WPA/WPA2-Personal and Enterprise
- Integrated TCP/IP stack, HTTP/HTTPS, SSL/TLS, MQTT
- Bluetooth inbuilt stack support for L2CAP, RFCOMM, SDP, SPP, GAP
- Bluetooth profile support for GAP, SDP, SPP, GATT, L2CAP, RFCOMM
- Wireless firmware update and provisioning
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

* For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

4.2.7 Security

RS9116 supports multiple levels of security capabilities available for the development of IoT devices.

- Accelerators: AES128/256 in Embedded Mode
- WPA/WPA2-Personal, WPA/WPA2 Enterprise for Client

* For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

4.2.8 System Power Supply Configurations

RS9116 chipsets support highly flexible power supply configurations for various application scenarios. Few application scenarios are below

- 3.3V single supply - A single 3.3V supply derived from the system PMU can be input to all I/O supplies.
- 1.85V single supply - A single 1.85V supply derived from the system PMU can be input to all I/O supplies. The maximum transmitter power is reduced in 1.85V single supply mode.

- 1.85V and 3.3V supply - A 1.85V supply derived from the system PMU can be input to all I/O supplies except PA2G_AVDD. A 3.3V supply derived from system PMU can be fed to the power amplifier supply pin PA2G_AVDD. In this mode, I/O's can operate at 1.85V without a penalty in the maximum transmit power
- Wide input supply - In a system without a PMU, a primary cell can be connected to all the I/O pins including PA2G_AVDD. In this mode, the maximum output power is a function of the primary cell voltage.

4.2.9 Power Management

The RS9116 chipsets have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the chipset to operate from a wide variety of input sources.

- LC DC-DC switching converter for RF and Digital blocks
    - Wide input voltage range (1.85 to 3.6V) on pin VINBCKDC
    - Output - 1.4V and 300mA maximum load on pin VOUTBCKDC
- SC DC-DC - Switching converter for Always-ON core logic domain
    - Wide input voltage range (1.85 to 3.6V) on pin UULP_VBATT_1 and UULP_VBATT_2
    - Output - 1.05V
- LDO SOC - Linear regulator for digital blocks
    - Input - 1.4V from LC DC-DC or external regulated supply on pin VINLDOSOC
    - Output - 1.15V and 300mA maximum load on pin VOUTLDOSOC
- LDO RF and AFE - Linear regulator for RF and AFE
    - Input - 1.4V from LC DC-DC or external regulated supply on pin RF_AVDD
    - Output - 1.1V and 20mA maximum load on pin VOUTLDOAFE
- LDO FLASH - Linear regulator for internal and external Flash
    - Input - Wide input voltage range (1.85 to 3.6V) on pin VINLDO1P8
    - Output - 1.8V and 20mA maximum load on pin VOUTLDO1P8

4.2.9.1 Output Voltage Ranges

Pin Description	Supply Voltage (V)	
	Min	Max
VOUTLDOSOC	1.05	1.2
VOUTBCKDC	1.25	1.55
VOUTLDO1P8	1.75	2.0
VOUTLDOAFE	1.0	1.2
UULP_VOUTSCDC	1.02	1.122
UULP_VOUTSCDC_RETN	0.715	1.122

Min. and Max. specifications of various output voltages

The output voltages from the IC/module will be reflected as per specifications only after the firmware is loaded.

4.2.10 Low power modes

It supports Ultra-low power consumption with multiple power modes to reduce the system energy consumption.

- Dynamic Voltage and Frequency Scaling
- Low Power (LP) mode with only the host interface active

- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to LP or ULP modes

4.2.10.1 ULP Mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a 32 kHz low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.
- Analog Comparator Based wakeup - Exit sleep state on an event at the analog comparator.
- RTC Timer wakeup - Exit Sleep state on timeout of RTC timer
- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout.

ULP mode is not supported in the USB interface mode

4.2.10.2 LP Mode

In Low Power mode, Network processor maintains system state and gate all internal high frequency clocks. But host interface is ready to accept any command from host controller.

The LP mode supports the following wake-up options:

- Host Request - Exit sleep state on a command from HOST controller. whenever a command from the host is received, the processor serves the request with minimum latency and the clock is gated immediately after the completion of the operation to reduce power consumption
- GPIO based wakeup - Wakeup can be initiated through a GPIO pin
- Timeout wakeup - Exit sleep state after the programmed timeout value

4.2.11 Memory

4.2.11.1 On-chip Memory

The ThreadArch® processor has the following memory:

- On-chip SRAM for the wireless stack.
- 512Kbytes of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions.
- 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with quad SPI flash memory.
- eFuse of 512 bytes (used to store primary boot configuration, security and calibration parameters)

5 RS9116 QMS SoC Reference Schematics, BOM and Layout Guidelines

1. Customers should include provision for programming or updating the firmware at manufacturing.
2. If using UART, we recommend bringing out the SPI lines to test points, so designers could use the faster interface for programming the firmware as needed.
3. If using SPI as host interface, then firmware programming or update can be done through the host MCU, or if designer prefers to program standalone at manufacturing, then it is recommended to have test points on the SPI signals.

5.1 SDIO/SPI/UART

5.1.1 Schematics

The below diagram shows the typical schematic with SDIO/SPI/UART Host Interface and Internal Flash.

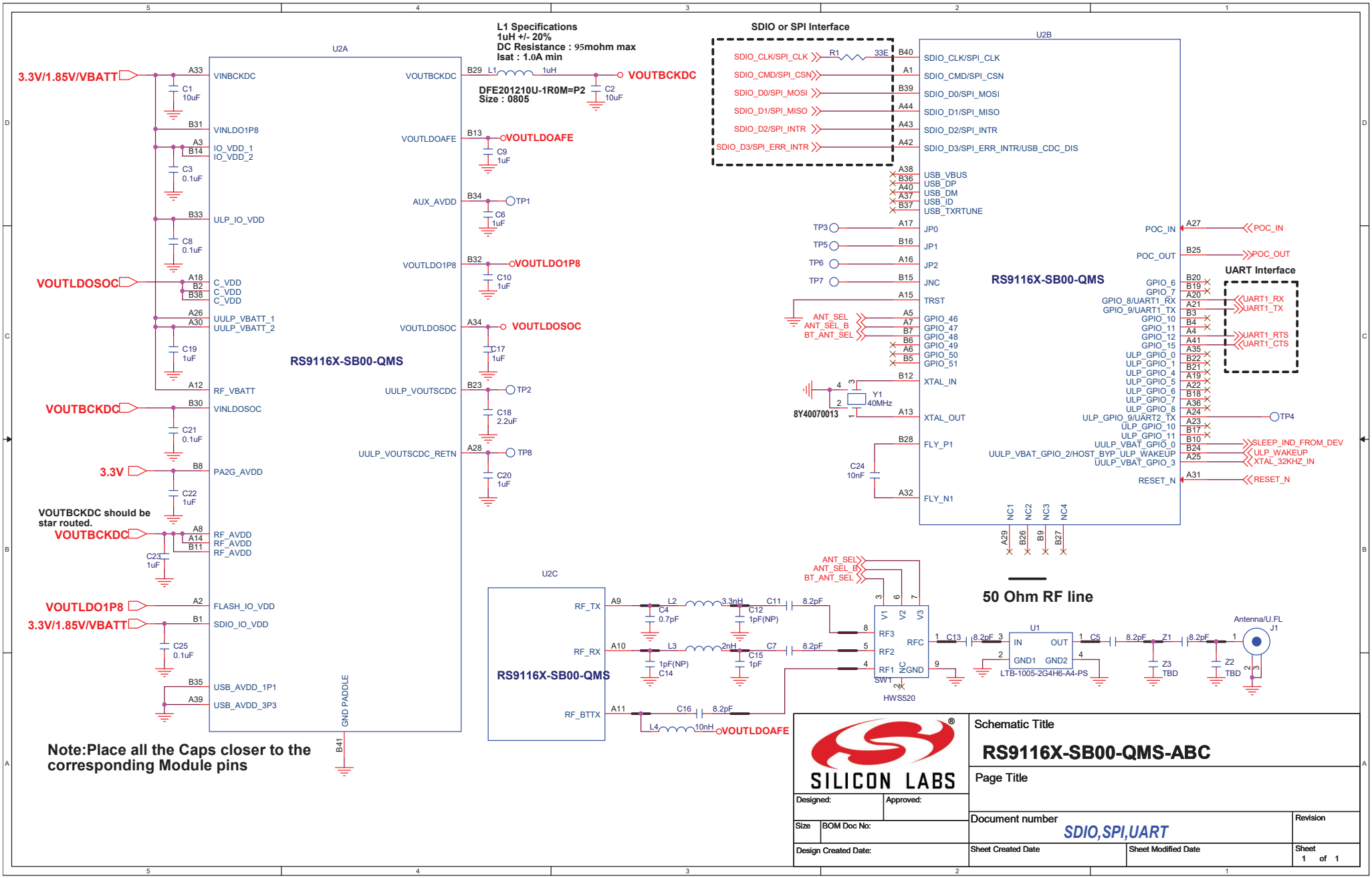


Figure 14 Schematics for QMS SoC with SDIO/SPI/UART Host Interface

1. PA2G_AVDD can be driven by 3.3V source irrespective of other sources for Maximum Transmit Output power.
2. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
3. SDIO_IO_VDD can be driven by a different source irrespective of other sources to support different interfaces.
4. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification, version 2.0.
5. In SPI mode, ensure that the input signals, SPI_CS and SPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset. SPI_INTR is the interrupt signal driven by the slave device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required. The following action can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.
    a. To use the signal in the Active-high or Active-low mode, ensure that, during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the SPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
    b. The Host processor needs to be disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.
6. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.
7. Resistor "**R1**" should not be populated if UART is used as Host Interface.

5.1.2 Bill of Materials

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
1	2	C1,C2	10uF	CAP CER 10UF 10V X5R 0805	0805	Murata	GRM21BR61A106KE19L
2	8	C6,C9,C10,C17,C19,C20,C22,C23	1uF	CAP CER 1UF 10V 10% X5R 0402	0402	Murata	GRM155R61A105KE15D
3	1	C4	0.7pF	CAP CER 0.7PF 50V C0G/NP0 0201	0201	Murata	GRM0335C1HR70WA01D
4	6	Z1,C5,C7,C11,C13,C16	8.2pF	CER CHP 8.2P +/-0.25P C0G 0201 25V	0201	Murata	GRM0335C1E8R2CD01D

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
5	4	C3,C8,C21,C25	0.1uF	CAP CER 0.1UF 10V X5R 0402	0402	Murata	GRM155R61A104KA01D
6	1	C15	1pF	CAP CER 1PF 25V C0G/NP0 0201	0201	Murata	GJM0335C1E1R0WB01D
7	1	C18	2.2uF	CAP CER 2.2UF 6.3V X5R 0402	0402	Murata	GRM155R60J225KE95D
8	1	C24	10nF	CAP CER 10000PF 25V X5R 0201	0201	Murata	GRM033R61E103KA12D
9	1	J1		Antenna/U.FL			
10	1	L1	1uH	FIXED IND 1UH 2.0A 95 MOHM SMD	0805	Murata	DFE201210U-1R0M=P2
11	1	L2	3.3nH	FIXED IND 3.3NH 450MA 250 MOHM	0201	Murata	LQP03TN3N3B02D
12	1	L3	2nH	FIXED IND 2NH 600MA 150 MOHM SMD	0201	Murata	LQP03TN2N0C02D
13	1	L4	10nH	FIXED IND 10NH 250MA 700 MOHM	0201	Murata	LQP03TN10NJ02D
14	1	R1	33E	RES SMD 33 OHM 5% 1/10W	0402	Panasonic	ERJ-2GEJ330X
15	1	SW1		GaAs 0.5-6GHz SP3T Switch	USON8L	Hexawave	HWS520
16	1	U1	BPF	Multi Layer band Pass layer	SMD	Mag Layers	LTB-1005-2G4H6-A4-PS
17	1	U2		Silicon Labs Single Band Chip		Silicon Labs	RS9116N-SB00-QMS-B00 / RS9116W-SB00-QMS-B24 / RS9116W-SB00-QMS-B2A
18	1	Y1	40MHz	40MHz Crystal	2x1.6mm	TXC	8Y40070013
19	2	Z2,Z3		Optional Capacitors for Antenna Matching	0201		

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
20	2	C12,C14	1pF(NP)		0201		

Table 35 Bill of Materials for QMS SoC with SDIO/SPI/UART Host Interface

5.2 USB/USB-CDC

5.2.1 Schematics

The below diagram shows the typical schematic with USB/USB-CDC Host Interface and Internal Flash.

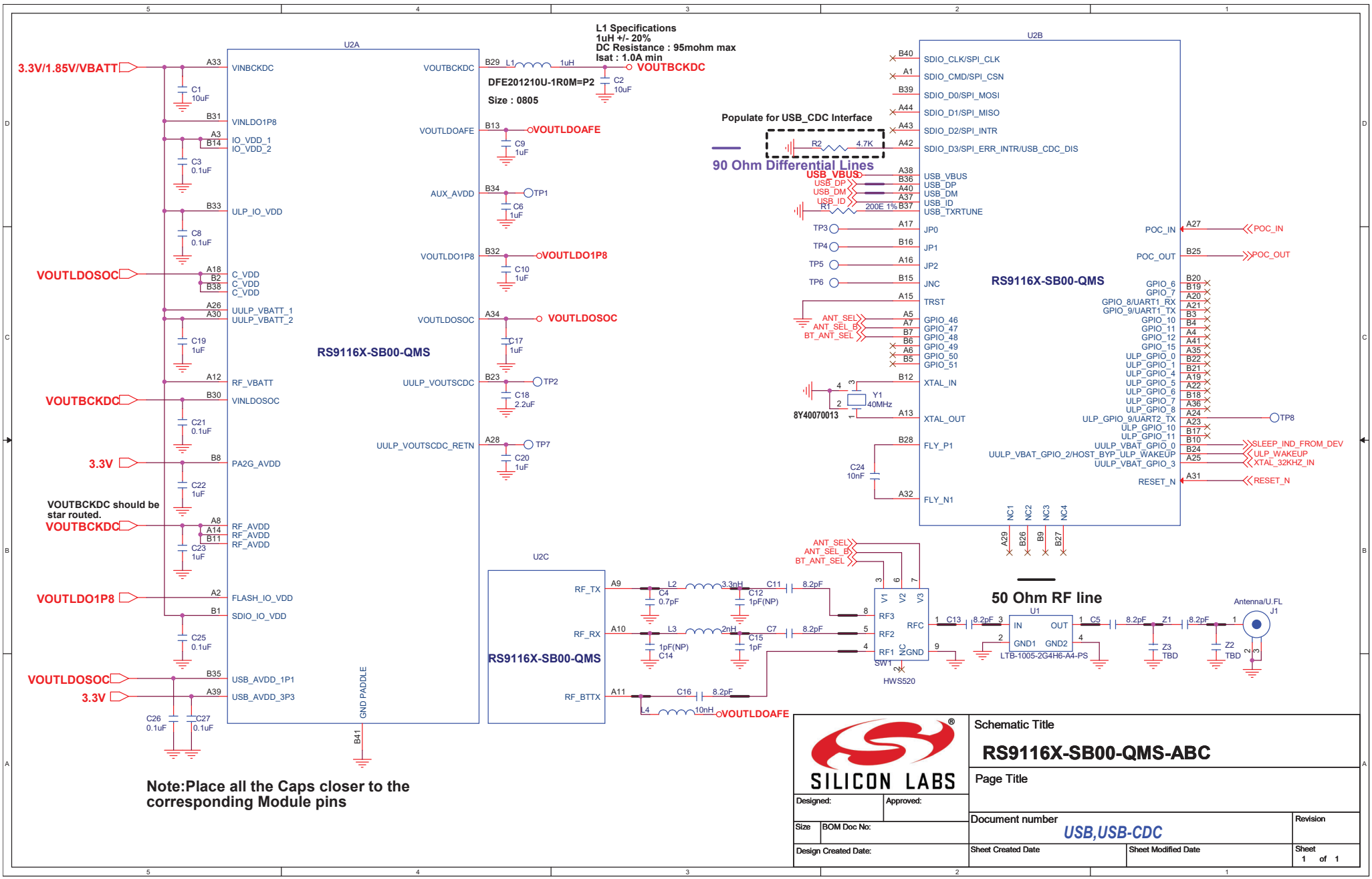


Figure 15 Schematics for QMS SoC with USB/USB-CDC Host Interface

1. PA2G_AVDD can be driven by 3.3V source irrespective of other sources for Maximum Transmit Output power.
2. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
3. Ensure that the pin USB_CDC_DIS is left unconnected to ensure normal USB functionality.
4. Resistor "**R2**" should not be populated if normal USB is used as Host Interface.

5.2.2 Bill of Materials

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
1	2	C1,C2	10uF	CAP CER 10UF 10V X5R 0805	0805	Murata	GRM21BR61A106KE19L
2	8	C6,C9,C10,C17,C19,C20,C22,C23	1uF	CAP CER 1UF 10V 10% X5R 0402	0402	Murata	GRM155R61A105KE15D
3	1	C4	0.7pF	CAP CER 0.7PF 50V C0G/NP0 0201	0201	Murata	GRM0335C1HR70WA01D
4	6	Z1,C5,C7,C11,C13,C16	8.2pF	CER CHP 8.2P +/-0.25P C0G 0201 25V	0201	Murata	GRM0335C1E8R2CD01D
5	6	C3,C8,C21,C25,C26,C27	0.1uF	CAP CER 0.1UF 10V X5R 0402	0402	Murata	GRM155R61A104KA01D
6	1	C15	1pF	CAP CER 1PF 25V C0G/NP0 0201	0201	Murata	GJM0335C1E1R0WB01D
7	1	C18	2.2uF	CAP CER 2.2UF 6.3V X5R 0402	0402	Murata	GRM155R60J225KE95D
8	1	C24	10nF	CAP CER 10000PF 25V X5R 0201	0201	Murata	GRM033R61E103KA12D
9	1	J1		Antenna/U.FL			

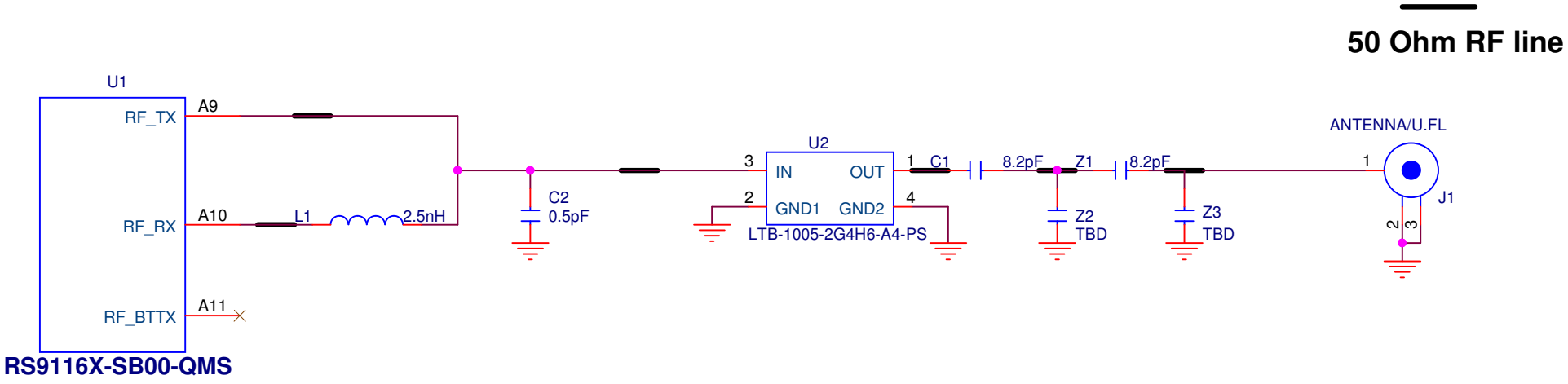
S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
10	1	L1	1uH	FIXED IND 1UH 2.0A 95 MOHM SMD	0805	Murata	DFE201210U-1R0M=P2
11	1	L2	3.3nH	FIXED IND 3.3NH 450MA 250 MOHM	0201	Murata	LQP03TN3N3B02D
12	1	L3	2nH	FIXED IND 2NH 600MA 150 MOHM SMD	0201	Murata	LQP03TN2N0C02D
13	1	L4	10nH	FIXED IND 10NH 250MA 700 MOHM	0201	Murata	LQP03TN10NJ02D
14	1	R1	200E	RES SMD 200 OHM 1% 1/16W 0402	0402	Yageo	RC0402FR-07200RL
15	1	R2	4.7K	RES SMD 4.7K OHM 1% 1/16W 0402	0402	Yageo	RC0402FR-074K7L
16	1	SW1		GaAs 0.5-6GHz SP3T Switch	USON8L	Hexawave	HWS520
17	1	U1	BPF	Multi Layer band Pass layer	SMD	Mag Layers	LTB-1005-2G4H6-A4-PS
18	1	U2		Silicon Labs Single Band Chip		Silicon Labs	RS9116N-SB00-QMS-B00 / RS9116W-SB00-QMS-B24 / RS9116W-SB00-QMS-B2A
19	1	Y1	40MHz	40MHz Crystal	2x1.6mm	TXC	8Y40070013
20	2	Z2,Z3		Optional Capacitors for Antenna Matching	0201		
21	2	C12,C14	1pF(NP)		0201		

Table 36 USB Bill of Materials for QMS SoC

5.3 Reduced Front-End Option

5.3.1 Schematics

The below diagram shows the typical schematic for reduced Front-End option.



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Title

RS9116X-SB00-QMS-ABC

Size | Document Number

Sheet 1 of 1

Figure 16 Reduced Front-End Schematics for QMS SoC

1. There is a degradation of 1dB in Transmit Output Power and Receive Sensitivity with the above Front-End.

5.4 Layout Guidelines for QMS SoC

The following guidelines outline the integration of the QMS SoC :

1. The following Supply Pins needs to be STAR routed from the Supply Source
    a. VINBCKDC
    b. VINLDO1P8
    c. IO_VDD_1, IO_VDD_2
    d. ULP_IO_VDD
    e. UULP_VBATT_1
    f. UULP_VBATT_2
    g. RF_VBATT
    h. PA2G_AVDD
    i. SDIO_IO_VDD
2. The RF_OUT signal of Filter may be directly connected to an on-board chip antenna or terminated in an RF connector of any form factor for enabling the use of external antennas.
3. There need to be DC blocking capacitors (8.2pF) on RF_OUT of Filter if connected to Antenna
4. The RF trace should have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, dielectric constant of the material, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
5. To evaluate transmit and receive performance like Tx Power and EVM, Rx sensitivity and the like, an RF connector would be required. A suggestion is to place a 'microwave coaxial connector with switch' between RF_OUT of Filter and the antenna.
6. The layout guidelines for BUCK are :

    Minimise the loop area formed by inductor switching node, output capacitors & input capacitors. This helps keep high current paths as short as possible. Keeping high current paths shorter and wider would help decrease trace inductance & resistance. This would significantly help increase the efficiency in high current applications. This reduced loop area would also help in reducing the radiated EMI that may affect nearby components.

    a. VINBCKDC Capacitor should be very close to the Chip Pin & the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
    b. Buck Inductor should be close to Chip VOUTBCKDC pin and buck capacitor should be placed closed to the Inductor, the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
    c. The Ground Plane underneath the Buck Inductor in the Top Layer should be made as an isolated copper patch and should descend down to the Second Layer (Main Ground) through multiple Vias.
    d. The path from VOUTBCKDC to VINLDOSOC is a high current path. The Trace should be as short & wide as possible and is recommended to run Grounded Shield Traces on either side of this High Current Trace
    e. The Capacitor on VINLDOSOC should be very close to the Chip Pin & the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.

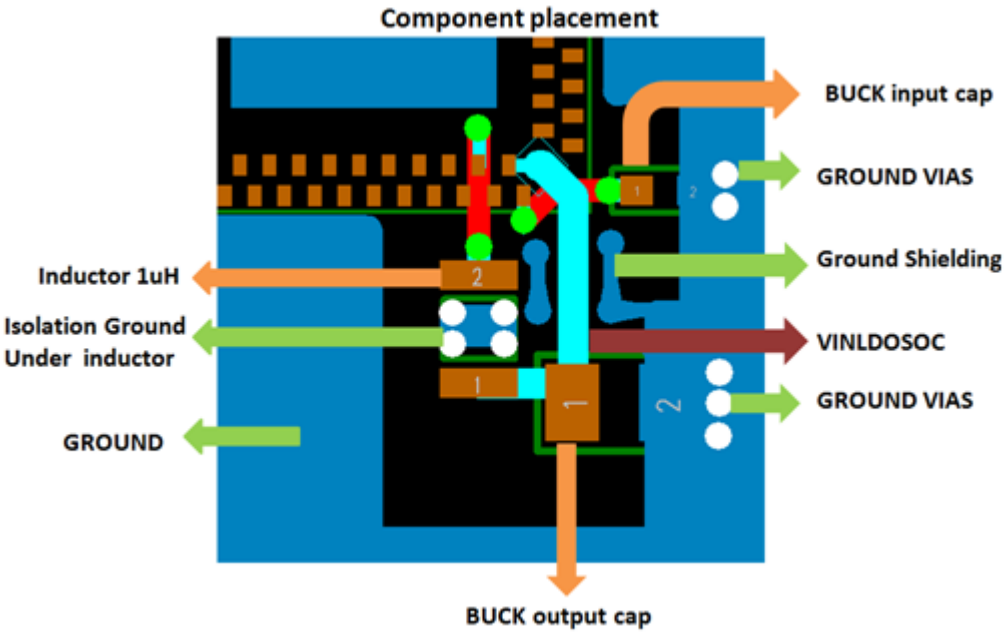


Figure 17 BUCK layout guidelines

7. For USB, it is recommended that the components and their values in the BoM be adhered to.
8. It is highly recommended that the two USB differential signals (USB_DP and USB_DN) be routed in parallel with a spacing (say, a) which achieves 90 Ω of differential impedance, 45 Ω for each trace.

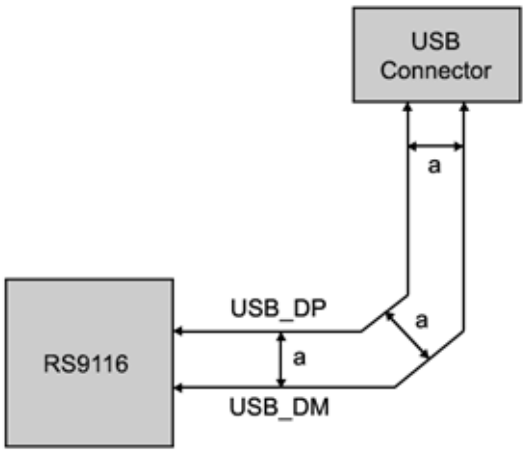


Figure 18 Spacing between USB_DP and USB_DM

9. In order to minimize crosstalk between the two USB differential signals (USB_DP and USB_DN) and other signal traces routed close to them, it is recommended that a minimum spacing of 3 x a be maintained for low-speed non-periodic signals and a minimum spacing of 7 x a be maintained for high-speed periodic signals.

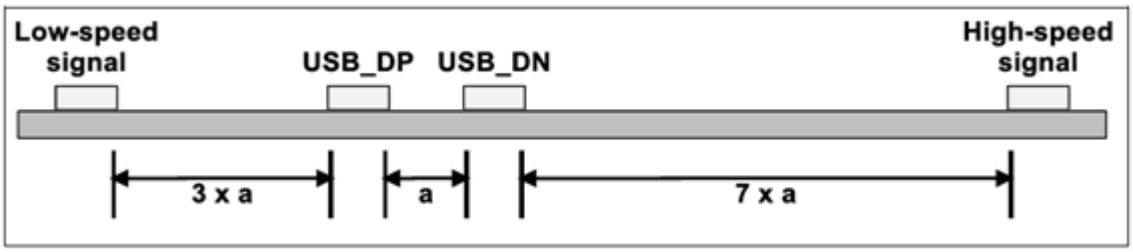


Figure 19 Spacing for Low-speed and High-speed signals around USB_DP/USB_DN

10. It is recommended that the total trace length of the signals between the RS9116 chip and the USB connector be less than 450mm
11. If the USB high-speed signals are routed on the Top layer, best results will be achieved if Layer2 is a Ground plane. Furthermore, there must be only one ground plane under high-speed signals in order to avoid the high-speed signals crossing to another ground plane

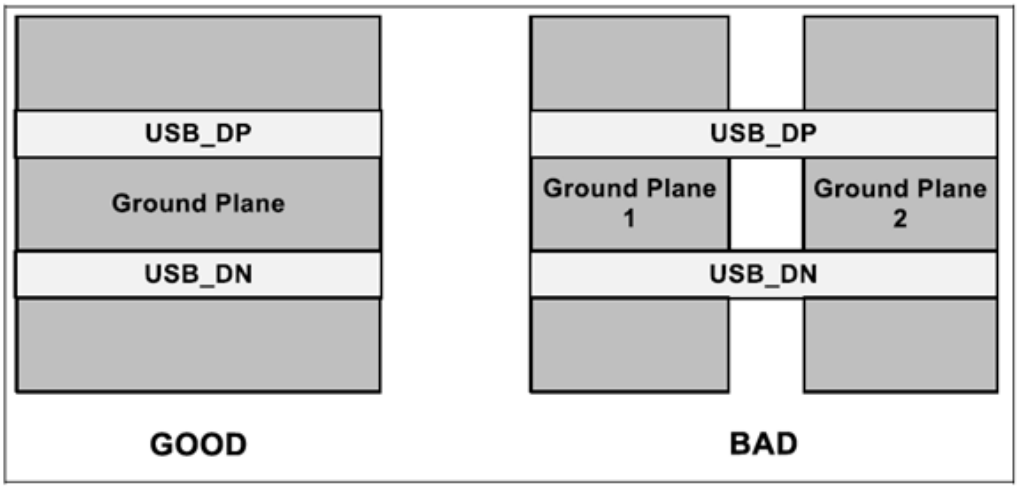


Figure 20 USB Signals and the Ground Plane

12. Each GND pin must have a separate GND via.
13. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.
14. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.
15. Add GND copper pour underneath IC/Module in all layers, for better thermal dissipation.

6 Chip Packages

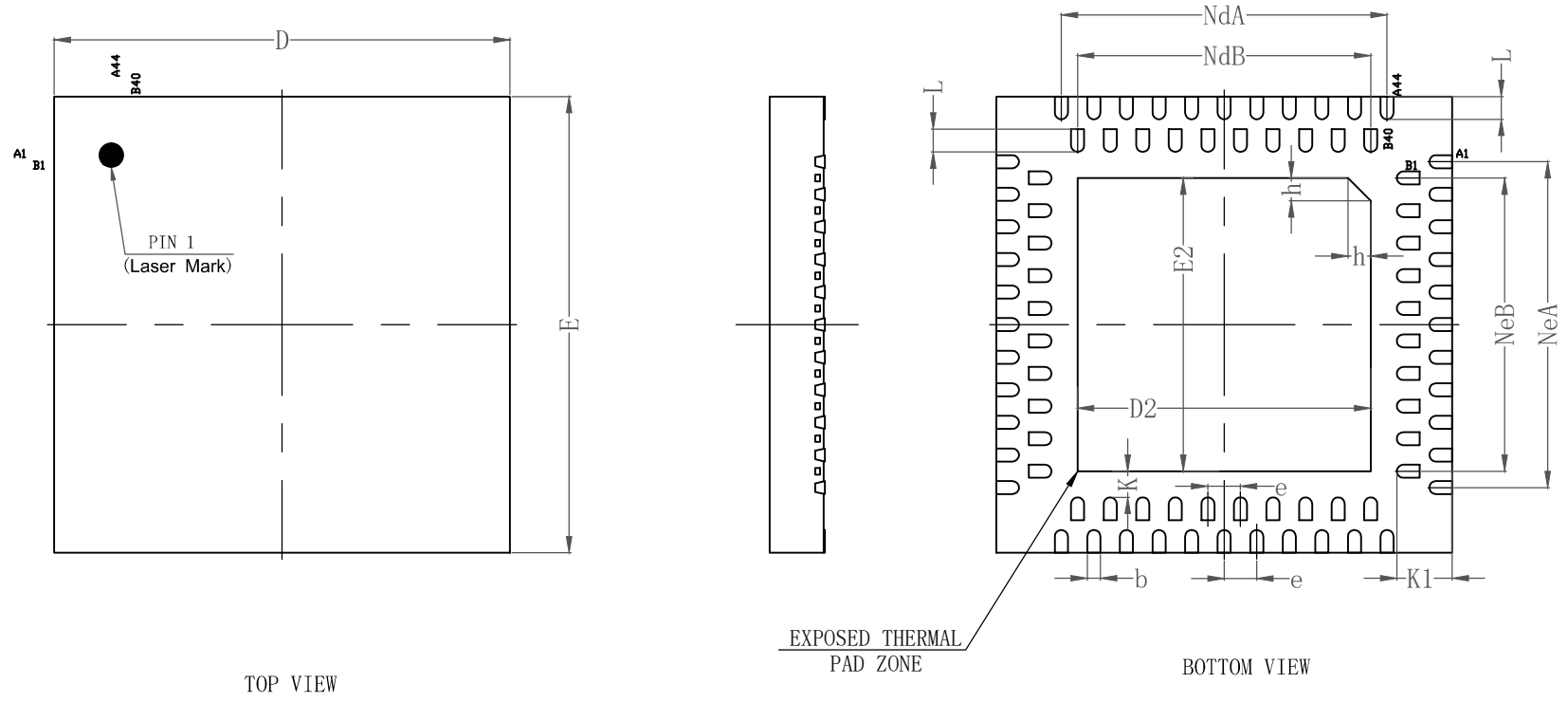
6.1 Chip with Package Code QMS

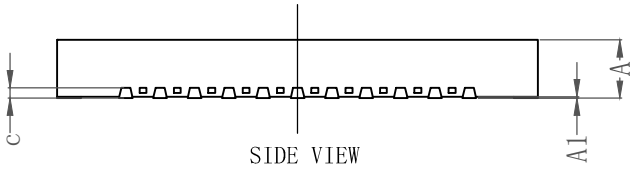
6.1.1 Package Dimensions

Parameter	Value (LxWxH)	Units
Package Dimensions	7 x 7 x 0.85	mm
Tolerance	±0.1	mm

Table 37 Package Dimensions - QMS

6.1.2 Package Outline





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.152REF		
D	6.90	7.00	7.10
D2	4.40	4.50	4.60
e	0.50BSC		
NdA	5.00BSC		
NdB	4.50BSC		
E	6.90	7.00	7.10
E2	4.40	4.50	4.60
NeA	5.00BSC		
NeB	4.50BSC		
L	0.30	0.35	0.40
K	0.35	0.40	0.45
K1	0.80	0.85	0.90
h	0.30	0.35	0.40

Figure 21 Package Outline - QMS

6.1.3 PCB Landing Pattern

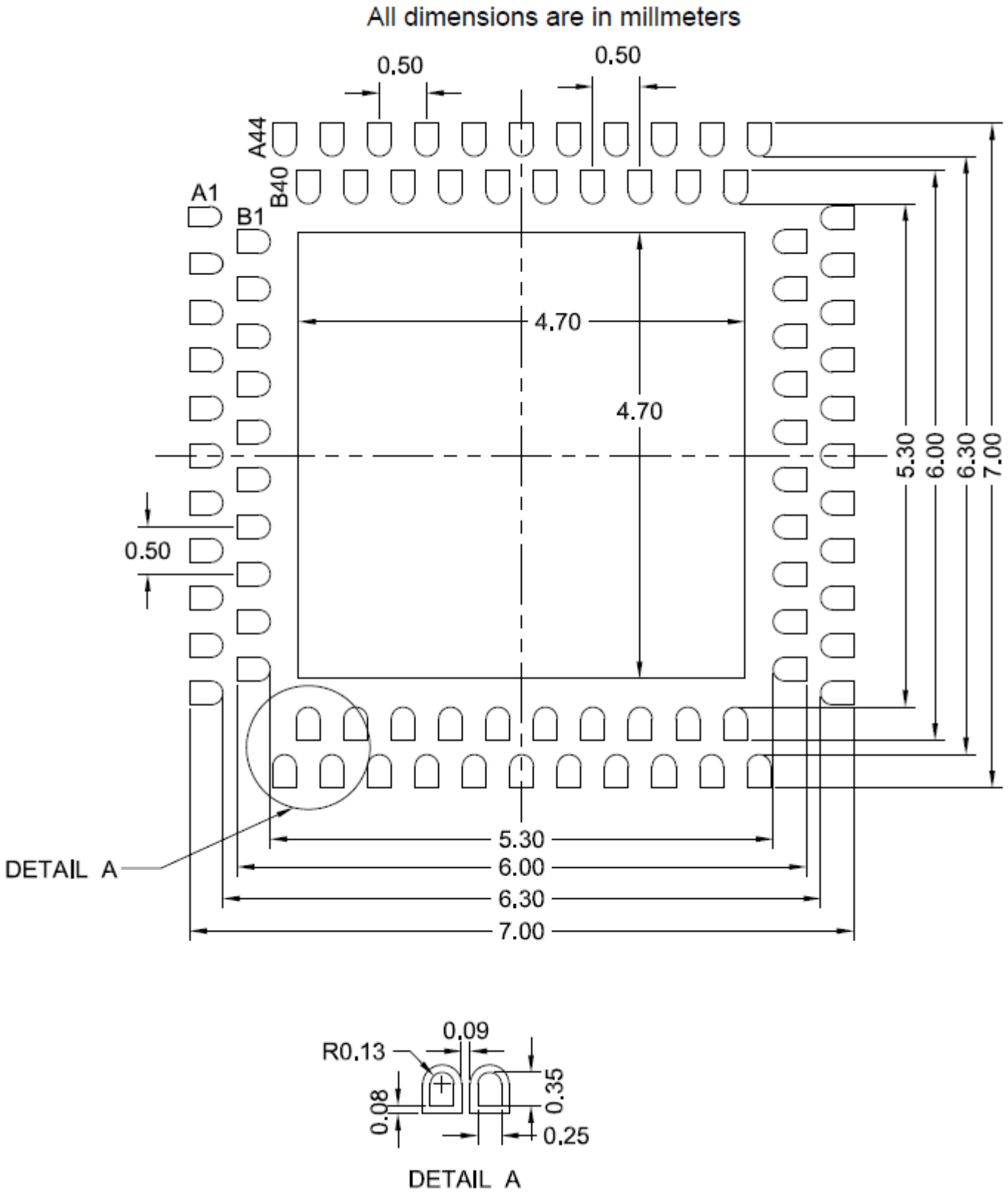


Figure 22 PCB Landing Pattern - QMS

7 RS9116 QMS SoC Ordering Information

7.1 Chip Packages

Package Code	Package Type, Pins	Dimension, Pitch (mm)	Frequency Band
QMS	QFN, 84	7 x 7 x 0.85	Single Band (2.4 GHz)

Table 38 Chip Package Options

7.2 Ordering Information

Part Number	Wireless and Memory
Hosted Connectivity (n-Link)	
RS9116N-SB00-QMS-B00	SBW + BT 5 with internal flash; Rev 1.4 Silicon
Embedded Connectivity (WiSeConnect)	
RS9116W-SB00-QMS-B24	SBW + BT 5 with internal flash; Rev 1.4 Silicon; Firmware version: 1.2.24
RS9116W-SB00-QMS-B2A	SBW + BT 5 with internal flash; Rev 1.4 Silicon; Firmware version: 2.0 or higher

Table 39 Part Ordering Options

- SBW: Single Band Wi-Fi (2.4 GHz).
- Customer should include provision for programming or updating the firmware at manufacturing.

8 RS9116 QMS SoC Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating, and developing products and applications using RS9116. These documents are available in RS9116 Document Library on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

For further assistance, you can contact Silicon Labs Technical Support here.

8.1 Resource Location

RS9116 Document Library : https://docs.silabs.com/rs9116/

Technical Support : http://www.silabs.com/support/

9 RS9116 QMS SoC Revision History

Revision No.	Version No.	Date	Changes
1	1.0	April 2019	Initial version
2	1.0.1	May, 2019	Updated host based schematics. Combined SDIO, SPI & UART host interfaces into one schematic.Combined USB and USB-CDC host interfaces into one schematic
3	1.0.2	May, 2019	• Updated the Antenna Control Pins for WMS. Modified Schematics and Pinout Description. • Updated 32 Khz external oscillator specifications • Updated the Schematics for UART_RTS and UART_CTS Pin correction.
4	1.0.3	May, 2019	Removed 32KHz XTAL Pins and used UULP GPIO for feeding in the External Clock. Updated the below sections for the same • Pinout Description. • Specifications • Reference Schematics
5	1.0.4	July, 2019	• Corrected the description of 32KHz external clock in Specifications section. • Renamed LP_WAKEUP to LP_WAKEUP_IN and changed its description in Pinout section. • Added host detection details in Detailed description
6	1.0.5	October, 2019	• POC reset control description changed to remove the1.75V –2.15V text. For connectivity SoC, externalPOC_in and reset control is now recommended for any operating voltage. • Power consumption Table for 3.3V operation reverted to the correct version for single band chip (same as1.0.3). This was corrupted in 1.0.4 version (got wronglyreplaced with dual-band package table for power consumption at 3.3V
7	1.0.6	November, 2019	Bluetooth ACI specs corrected (earlier version shows under Typ - should have been under “Min”)
8	1.0.7	July, 2020	• Added note about voltage applied on external Buck Regulator for Typical Current Consumption at 1.85V. • Updated 40 MHz clock specifications. • Updated LED0 software configuration note for ULP_GPIO_8 under Pin Description. • Mentioned need for weak pull up resistor under Pin Description to use Wake-on-Wireless feature on ULP_GPIO_6. • Updated "Digital Input Output Signals" to separate readings at 3.3V and 1.8V. • Updated Applications section. • Updated Wireless Co-Existence modes in Features list. • The number of center roles supported by BLE changed from 8 to 6. • Added a note under Pin Description regarding functionalities that are available on multiple Pins, and their proper usage. Eg. SLEEP_IND_FROM_DEV

Revision No.	Version No.	Date	Changes
			• Updated Generic PCB Layout Guidelines. • Updated Power Sequence Diagrams under DC Characteristics for POC_IN and POC_OUT. • Features list updated. • Reflow profile diagram updated. • Updated Typical values for BLE ACI characteristics. • Updated GPIO pin descriptions. • Updated Bluetooth EDR 2 Mbps LP Chain Receiver specification. • Removed Legacy Bluetooth Tx on LP Chain. • Updated WLAN 2.4 GHz 1.85V Transmitter specifications.
9	1.0.8	August, 2020	• Updated datasheet to reflect data specific to QFN. • Updated Features List, removed redundant information. • Updated Applications, and Software Architecture Diagrams. • Updated pin descriptions - ULP_GPIO_0 and ULP_GPIO_6. • Updated RF Tx and Rx numbers based on latest tests. • Updated Software section with latest information. • Rebranded to Silicon Labs.
10	1.0.9	August, 2020	• Updated Device Information with new nomenclature to include Silicon revision, and firmware version. • Updated nomenclature in Pinout diagram, and Pin descriptions. • Updated schematics to include the new nomenclature. • SoC Ordering information updated with new OPNs; Device Nomenclature diagram updated.
11	1.0.10	June, 2021	• SoC image updated with Silicon Labs logo. • Added note under Software Architecture diagram on connecting and using multiple hosts at the same time. • Included EN 300 328-v2.2.2 certifiable info. • Removed redundant section ‘Device Information’. Same information is available in section ‘Ordering Information’. • Pin names updated for consistency; included actual pin names along with signals; updated pins: UART1_RX, UART1_TX, UART2_TX, HOST_BYP_ULP_WAKEUP • ULP_GPIOs in Pin Description referenced to ULP_IO_VDD instead of IO_VDD_1. • Updated note on Wake-on-Wireless feature, under Description for pin ULP_GPIO_6. • Removed ESD and Latch Up information from Absolute Ratings table. • Updated Min. and Max. values for RF related pins to reflect both 1.8 V and 3.3 V related values in Recommended Operating Conditions. • Updated Min. and Max. values for IO pins to reflect both 1.8 V and 3.3 V related minimum (1.65/3.0), and maximum (1.98/3.6) values in Recommended Operating Conditions.

Revision No.	Version No.	Date	Changes
			• Power-Up and Down Sequence with POC_IN connected internally. Included statement that this connection is NRND. • Updated V_{IH}, V_{OH} to show only Min. values; V_{IL}, V_{OL} to show only Max. values; I_{OL}, I_{OH} to show only Typ. values. • Updated 32 kHz External Crystal Oscillator specifications to reflect correct Min and Max values for V_{ac}. • Updated 40 MHz crystal specifications with additional parameters – Mode of Operation, Resonance, Drive Level. • Timing data included for SDIO_CMD. • Recommended Operating Conditions for PA2G_AVDD pin updated. • Added caveats to the RF Characteristics. • Updated RF Specification section to include numbers at 3.3 V only. • Updated Note for IEEE spectral mask effects. Added mention of AN1337 application note for certification details. • Included output voltage power ranges under Power Management. • Typical Current Consumption section updated to include values at 3.3 V only. • Removed section on Serial Flash; QMS does not support External Flash. • Schematics updated to reflect correct voltage for PA2G_AVDD pin. • Reference Schematics updated to show DC Resistance at 95mohm max (from 70), and Isat at 1.0A min (from 1.5). • Updated Murata's 1uH inductor part in Schematics and BOM from DFE201210**S**-1R0M=P2 to DFE201210**U**-1R0M=P2. • Updated description for DFE201210S-1R0M=P2 in BOM to FIXED IND 1UH 2.0A 95 MOHM SMD (from 2.3A 70 MOHM SMD). • Removed External Flash reference schematics. • Updated Layout Guidelines: RF_OUT replaced with "RF_OUT signal of Filter". • Removed Device Nomenclature. • Removed Reflow Profile, Soldering and Baking instructions. Information available through the web based RFI system. • Datasheet updated from Preliminary to Full Production.

Table 40 Revision History

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

IoT Portfolio
www.silabs.com/IoT

SW/HW
www.silabs.com/simplicity

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