ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at www.onsemi.com

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

April 2015

FAN53202
5 A, 2.4 MHz, Digitally Programmable TinyBuck® Regulator

Features

- Up to 91% Efficiency
- Quiescent Current in PFM Mode: 60 µA (Typical)
- Digitally Programmable Output Voltage:
  - 0.6-1.3875 V in 12.5 mV Steps
- Best-in-Class Load Transient
- Continuous Output Current Capability: 5 A
- 2.5 V to 5.5 V Input Voltage Range
- Programmable Slew Rate for Voltage Transitions
- Fixed-Frequency Operation: 2.4 MHz
- I^2C-Compatible Interface Up to 3.4 Mbps
- Internal Soft-Start
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 20-Bump Wafer-Level Chip Scale Package (WLCSP)

Applications

- Application, Graphic, and DSP Processors
  - ARM™, Krait™, OMAP™, NovaThor™, ARMADA™
- Hard Disk Drives
- Tablets, Netbooks, Ultra-Mobile PCs
- Smart Phones
- Gaming Devices

All trademarks are the property of their respective owners.

Description

The FAN53202 is a step-down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5 V to 5.5 V. The output voltage is programmed through an I^2C interface capable of operating up to 3.4 MHz.

Using a proprietary architecture with synchronous rectification, the FAN53202 is capable of delivering 5 A continuous at over 80% efficiency, while maintaining over 80% efficiency at load currents as low as 10 mA. The device can also support a 7 A 500 ms pulse. The regulator operates at a nominal fixed frequency of 2.4 MHz, which reduces the value of the external components to 330 nH for the inductor and as low as 22 µF for the output capacitor. Additional output capacitance can be added to improve regulation during load transients without affecting stability. Inductance up to 1.2 µH may be used with additional output capacitance.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in Power-Save Mode with a typical quiescent current of 60 µA. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 2.4 MHz. In Shutdown Mode, the supply current drops below 1 µA, reducing power consumption. PFM Mode can be disabled if constant frequency is desired. The FAN53202 is available in a 20-bump, 1.6 x 2 mm, WLCSP.

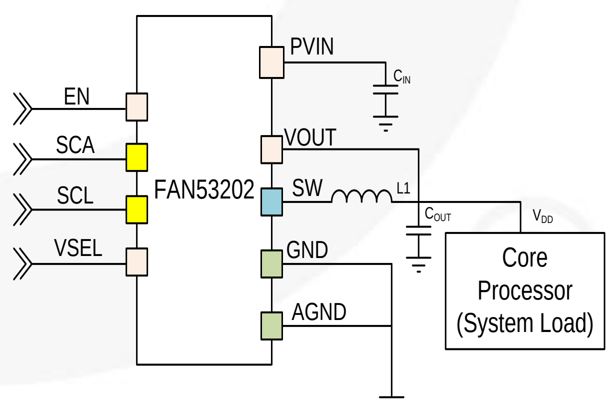


Figure 1. Typical Application

Ordering Information

Part Number	Power-Up Defaults		I2C Slave Address	Max Pulse Current (500ms)	Temperature Range	Package	Packing Method	Device Marking
	VSEL0	VSEL1						
FAN53202UC23X	1.15 V	1.15 V	C0	7.0 A	-40 to 85°C	WLCSP-20	Tape & Reel	CK

Pin Configuration

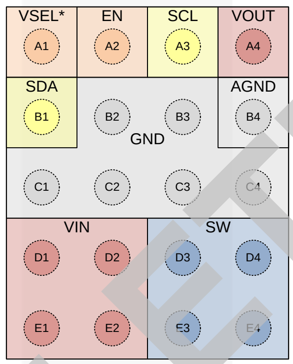


Figure 2. Top View

Pin Definitions

Pin #	Name	Description
A1	VSEL	**Voltage Select**. When this pin is LOW, V_{OUT} is set by the VSEL0 register. When this pin is HIGH, V_{OUT} is set by the VSEL1 register.
A2	EN	**Enable**. The device is in Shutdown Mode when this pin is LOW. All register values are kept during shutdown. All registers go to default values when EN pin is LOW.
A3	SCL	**I²C Serial Clock**
A4	VOUT	**VOUT**. Sense pin for VOUT. Connect to COUT.
B1	SDA	**I²C Serial Data**
B2, B3, C1 – C4	GND	**Ground**. Low-side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
B4	AGND	**Analog Ground**. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
D1, D2, E1, E2	VIN	**Power Input Voltage**. Connect to the input power source. Connect to C_{IN} with minimal path.
D3, D4, E3, E4	SW	**Switching Node**. Connect to the inductor.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Voltage on SW, VIN Pins	IC Not Switching	-0.3	7.0	V
		IC Switching	-0.3	6.5	
	Voltage on All Other Pins	IC Not Switching	-0.3	V_{IN}(1)	V
V_{OUT}	Voltage on VOUT Pin		-0.3	3.0	V
V_{INOV_SLEW}	Maximum Slew Rate of V_{IN} > 6.5 V, PWM Switching			100	V/ms
ESD	Electrostatic Discharge Protection Level	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	2500		V
		Charged Device Model per JESD22-C101	1500		
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
1. Lesser of 7 V or V_{IN}+0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage Range	2.5		5.5	V
I_{OUT}	Output Current	0		5	A
L	Inductor		0.33		µH
C_{IN}	Input Capacitor		10		µF
C_{OUT}	Output Capacitor		44		µF
T_A	Operating Ambient Temperature	-40		+85	°C
T_J	Operating Junction Temperature	-40		+125	°C

Thermal Properties

Symbol	Parameter	Min.	Typ.	Max.	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance(2)		38		°C/W

Note:
2. *See Thermal Considerations in the Application Information section.*

Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.5 V to 5.5 V, T_A=-40°C to +85°C, unless otherwise noted. Typical values are at T_A=25°C, V_{IN} = 5V and EN=HIGH.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
I_Q	Quiescent Current	I_{LOAD}=0		60	100	µA
I_{SD}	H/W Shutdown Supply Current	EN=GND		0.1	5.0	µA
	S/W Shutdown Supply Current	EN= V_{IN}, BUCK_ENx=0		41	75	µA
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} Rising		2.35	2.45	V
V_{UVHYST}	Under-Voltage Lockout Hysteresis			350		mV
EN, VSEL, SDA, SCL						
V_{IH}	HIGH-Level Input Voltage		1.1			V
V_{IL}	LOW-Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			160		mV
I_{IN}	Input Bias Current for Logic Pin	Input Tied to GND or 1.8V		0.01	1.00	µA
PGOOD						
I_{OUTL}	PGOOD Pull-Down Current				1	mA
I_{OUTH}	PGOOD HIGH Leakage Current			0.01	1.00	µA
V_{OUT} Regulation						
V_{REG}	V_{OUT} DC Accuracy	$I_{OUT(DC)}$=0 to 5A, Auto Mode, 2.5 V ≤ V_{IN} ≤ 4.5 V	-2.0		4.0	%
Power Switch and Protection						
I_{LIMPK}	P-MOS Peak Current Limit	Open Loop	8.5	10.0	11.5	A
V_{SDWN}	Input OVP Shutdown	Rising Threshold		6.15		V
		Falling Threshold	5.50	5.85		V
Frequency Control						
f_{SW}	Oscillator Frequency (FPWM)		2.05	2.40	2.75	MHz
R_{OFF}	VOUT Pull-Down Resistance, Disabled	EN=0 or V_{IN}<V_{UVLO}		160		Ω

Note:
3. Monotonicity assured by design.

System Characteristics

The following table is verified by design and verified while using the following external components: L = 0.33 µH, DFE252012F (TOKO), CIN = C2012X5R1A106M (TDK), C_{OUT} = 2 x C2012X5R0J226M (TDK) These parameters are not verified in production. Minimum and maximum values are at V_{IN} = 2.5 V to 5.5 V, V_{EN} = 1.8 V, T_A = -40°C to +85°C; circuit of Figure 1, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.6V, V_{EN} = 1.8 V.

Symbol	Parameter		Min.	Typ.	Max.	Unit
ΔV_{OUT1}	Load Regulation	I_{OUT} = 0 A to 2.5 A, V_{IN} = 3.8 V (Auto)		0.3		%/A
		I_{OUT} = 1 A to 5 A, V_{IN} = 3.8 V (PWM)		0.1		
ΔV_{OUT2}	Line Regulation	3.6 V ≤ V_{IN} ≤ 4.0 V, I_{OUT} = 3 A		0.03		%/V
V_{OUT_RIPPLE}	Ripple Voltage	V_{IN} = 3.8 V, I_{OUT} = 100 mA, PFM Mode		15		mV
		V_{IN} = 3.8 V, I_{OUT} = 2000 mA, PWM Mode		5		
η	Efficiency	P_{VIN} = 3.6 V, V_{OUT} = 1.15 V, I_{OUT} = 100 mA		87		%
		P_{VIN} = 3.6 V, V_{OUT} = 1.15 V, I_{OUT} = 500 mA		89		
		P_{VIN} = 3.6 V, V_{OUT} = 1.15 V, I_{OUT} = 2 A		89		
T_{SS}	Soft-Start	EN High to 95% of Target_ $V_{OUT.}$ (1.15 V), R_{LOAD} = 50 Ω		340		µs
ΔV_{OUT_LOAD}	Load Transient	I_{OUT} = 0.1 A ⇔ 1.2 A, T_R= T_F =100 ns		±40		mV
ΔV_{OUT_LINE}	Line Transient	V_{IN} = 3.0 V⇔3.6 V, T_R = T_F = 10 µs, I_{OUT} = 500 mA		±25		mV
T_{LIMIT}	Thermal Shutdown			150		°C

Typical Characteristics

Unless otherwise specified, V_{IN} = 3.6 V, V_{OUT} = 1.15 V, V_{EN} = 1.8 V, T_A = 25°C; circuit and components according to Figure 1.

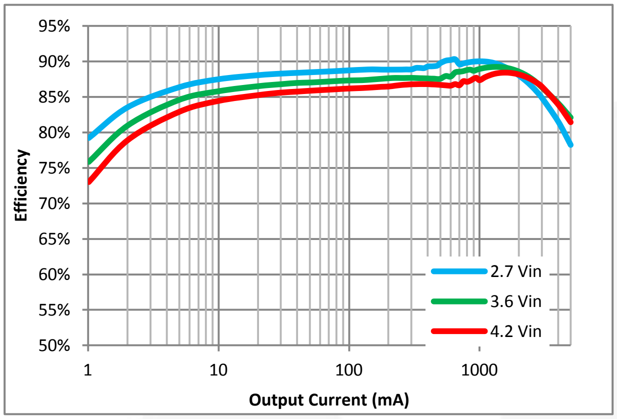


Figure 3. Efficiency vs. Load Current and Input Voltage

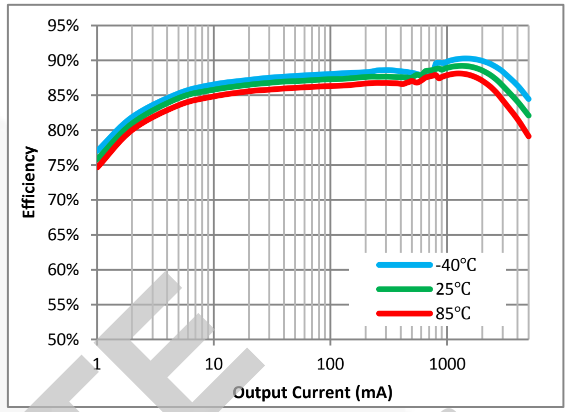


Figure 4. Efficiency vs. Load Current and Temperature

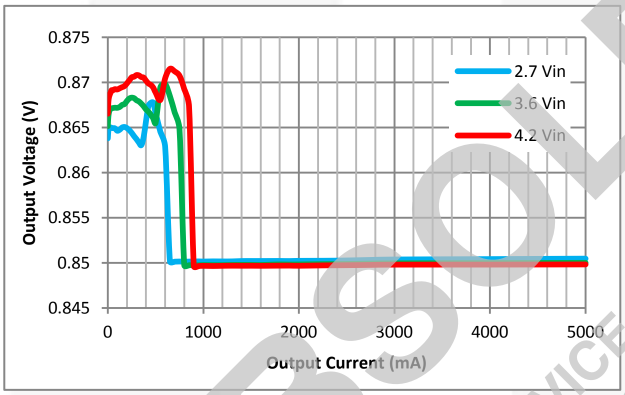


Figure 5. Output Regulation vs. Load Current and Input Voltage, V_{OUT}=0.85 V

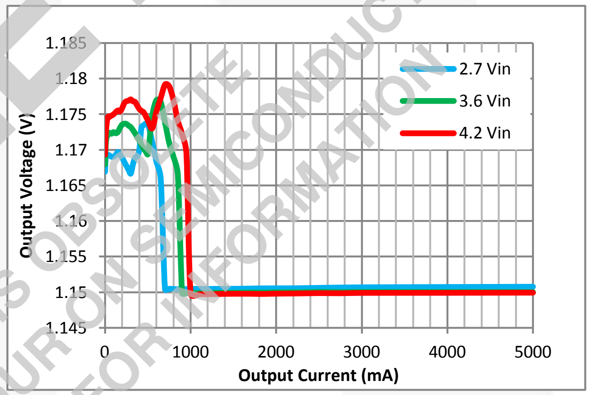


Figure 6. Output Regulation vs. Load Current and Input Voltage, V_{OUT}=1.15 V

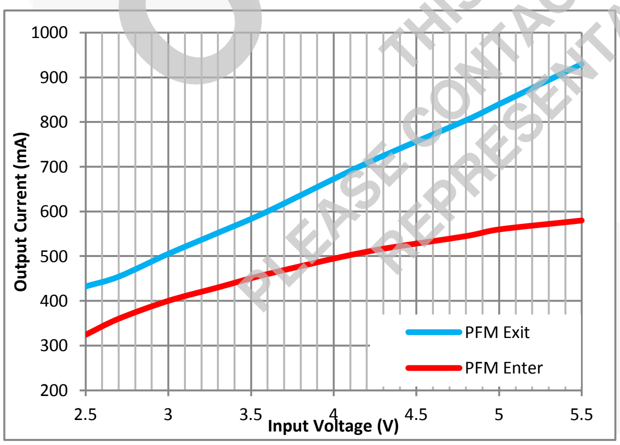


Figure 7. PFM Entry / Exit Level vs. Input Voltage, V_{OUT}=0.85 V

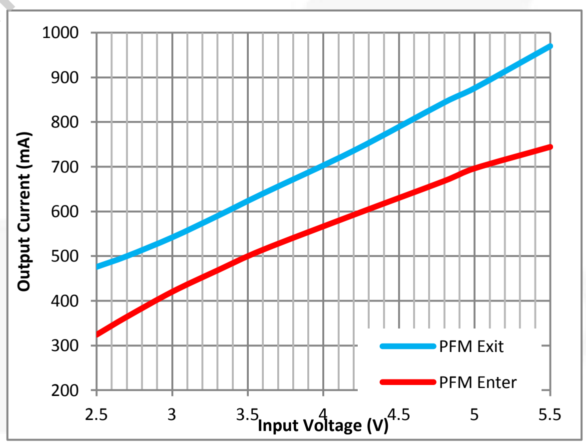


Figure 8. PFM Entry / Exit Level vs. Input Voltage, V_{OUT}=1.15 V

Typical Characteristics (Continued)

Unless otherwise specified, V_{IN} = 3.6 V, V_{OUT} = 1.15 V, V_{EN} = 1.8 V, T_A = 25°C; circuit and components according to Figure 1.

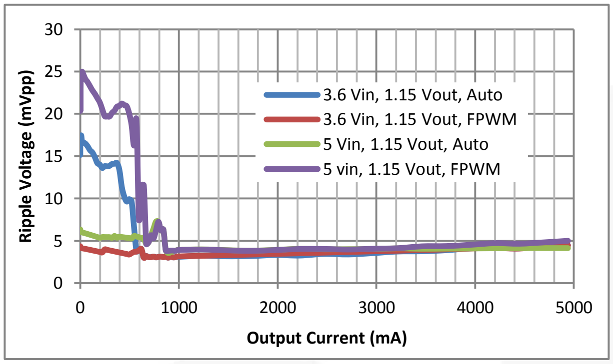


Figure 9. Output Ripple vs. Load Current

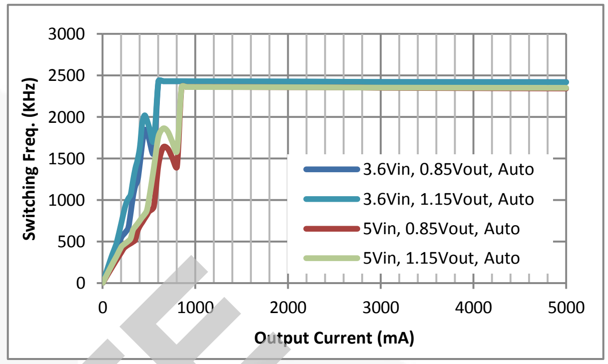


Figure 10. Frequency vs. Load Current

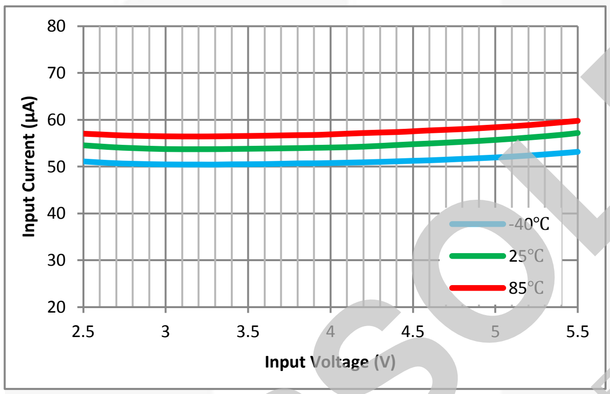


Figure 11. Quiescent Current vs. Input Voltage and Temperature, Auto PWM

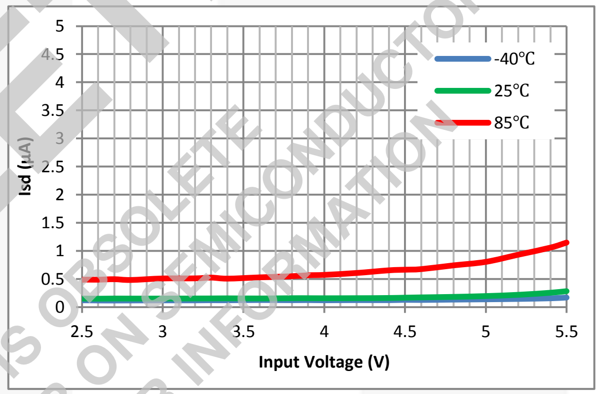


Figure 12. Shutdown Current vs. Input Voltage and Temperature

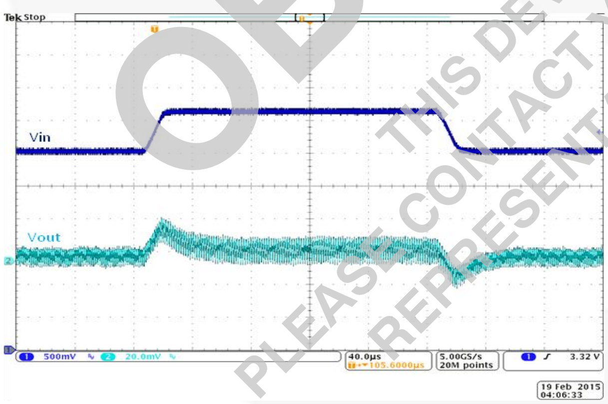


Figure 13. Line Transient, V_{IN} = 3.0 V ⇔ 3.6 V, T_R=T_F=10 µs Auto Mode I_{OUT} = 250 mA

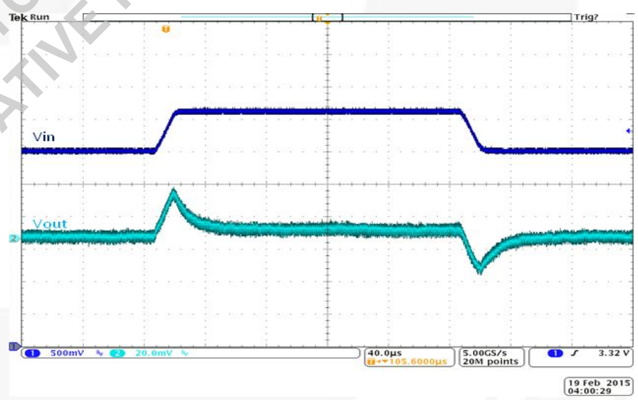


Figure 14. Line Transient, V_{IN} = 3.0 V ⇔ 3.6 V, T_R=T_F=10 µs Auto Mode I_{OUT} = 2 A

Typical Characteristics (Continued)

Unless otherwise specified, V_{IN} = 3.6 V, V_{OUT} = 1.15 V, V_{EN} = 1.8 V, T_A = 25°C; circuit and components according to Figure 1.

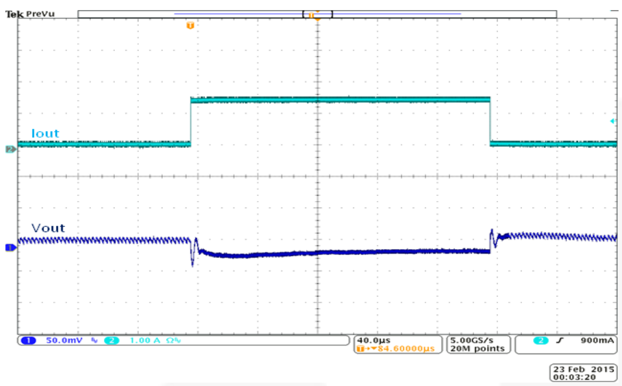


Figure 15. Load Transient, I_{OUT} = 0.1 A ⇔1.6 A, Auto Mode T_R = T_F = 100 ns

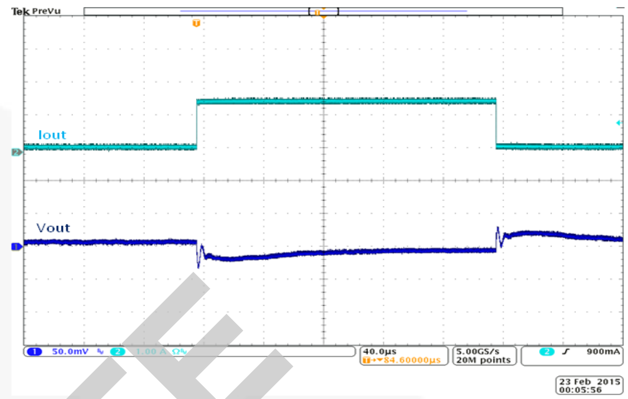


Figure 16. Load Transient, I_{OUT} = 0.1 A ⇔1.6 A, FPWM Mode T_R = T_F = 100 ns

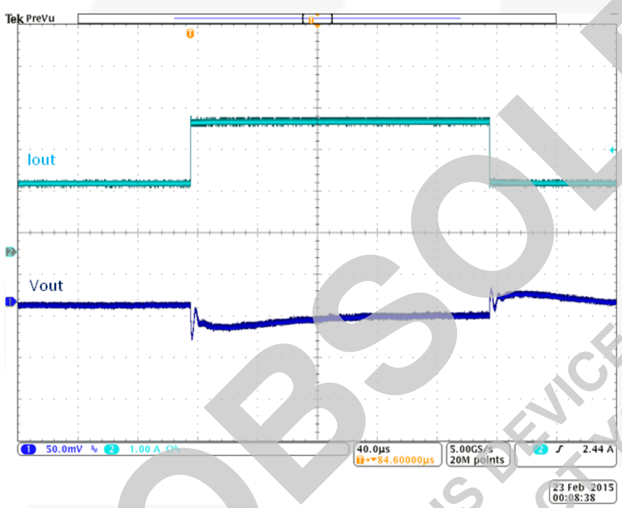


Figure 17. Load Transient, I_{OUT} = 1.5 A ⇔ 3 A, Auto Mode T_R = T_F = 100 ns

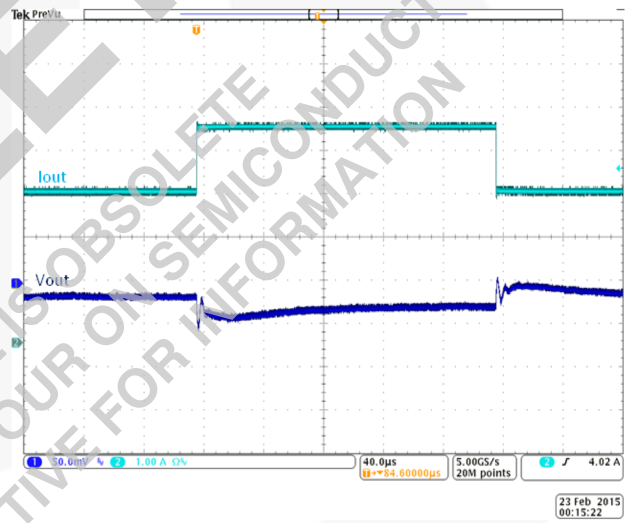


Figure 18. Load Transient, I_{OUT} = 3.5 A ⇔ 5 A, Auto Mode T_R = T_F = 100 ns

Operation Description

The FAN53202 is a step-down switching voltage regulator that delivers a programmable output voltage from an input voltage supply of 2.5 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53202 is capable of delivering 5 A at over 80% efficiency. The regulator operates at a nominal frequency of 2.4 MHz at full load, which reduces the value of the external components to 330 nH for the output inductor and 22 µF for the output capacitor. High efficiency is maintained at light load with single-pulse PFM.

The FAN53202 integrates an I^2C-compatible interface, allowing transfers up to 3.4 Mbps. This communication interface can be used to:

- Dynamically re-program the output voltage in 12.5 mV
- Reprogram the mode to enable or disable PFM;
- Control voltage transition slew rate; or
- Enable / disable the regulator.

Control Scheme

The FAN53202 uses a proprietary non-linear, fixed-frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53202 operates in Discontinuous Current Diode (DCM) single-pulse PFM, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is relatively seamless, providing a smooth transition between DCM and CCM Modes.

PFM can be disabled by programming the MODE bit HIGH in the VSEL registers.

Enable and Soft-Start

When the EN pin is LOW; the IC is shutdown, all internal circuits are off, and the part draws very little current. In this state, I^2C cannot be written to or read from. All registers are reset to default values when EN pin is LOW.

When the OUTPUT_DISCHARGE bit in the CONTROL register is enabled (logic HIGH) and the EN pin is LOW or the BUCK_ENx bit is LOW, a load is connected from VOUT to GND to discharge the output capacitors.

Raising EN while the BUCK_ENx bit is HIGH activates the part and begins the soft-start cycle. During soft-start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. Synchronous rectification is inhibited during soft-start, allowing the IC to start into a pre-charged capacitive load.

If large output capacitance values are used, the regulator may fail to start. Maximum C_{OUT} capacitance for successfully starting with a heavy constant-current load is approximately:

$$C_{OUTMAX} \approx (I_{LIMPK} - I_{LOAD}) \bullet \frac{320\mu}{V_{OUT}} \qquad (1)$$

where C_{OUTMAX} is expressed in µF and I_{LOAD} is the load current during soft-start, expressed in A.

If the regulator is at its current limit for 16 consecutive current limit cycles, the regulator shuts down and enters 3-state before reattempting soft-start 1700 ms later. This limits the duty cycle of full output current during soft-start to prevent excessive heating.

The IC allows for software enable of the regulator, when EN is HIGH, through the BUCK_EN bits. BUCK_EN0 and BUCK_EN1 are both initialized HIGH.

Table 1. Hardware and Software Enable

Pins		BITS		
EN	VSEL	BUCK_EN0	BUCK_EN1	Output
0	X	X	X	OFF
1	0	0	X	OFF
1	0	1	X	ON
1	1	X	0	OFF
1	1	X	1	ON

VSEL Pin and I^2C Programming Output Voltage

The output voltage is set by the NSELx control bits in VSEL0 and VSEL1 registers. The output voltage is given as:

$$V_{OUT} = 0.60V + NSELx \bullet 12.5mV \qquad (2)$$

Output voltage can also be controlled by toggling the VSEL pin LOW or HIGH. VSEL LOW corresponds to VSEL0 and VSEL HIGH corresponds to VSEL1. Upon POR, VSEL0 and VSEL1 are reset to their default voltages, shown in Table 5.

Transition Slew Rate Limiting

When transitioning from a low- to high-voltage, the IC can be programmed for one of eight possible slew rates using the SLEW bits in the CONTROL register (Table 5 and Table 6).

Table 2. Transition Slew Rate

Decimal	Bin	Slew Rate	
0	000	80	mV / µs
1	001	40	mV / µs
2	010	20	mV / µs
3	011	10	mV / µs
4	100	5	mV / µs
5	101	2.5	mV / µs
6	110	1.25	mV / µs
7	111	0.625	mV / µs

Transitions from high to low voltage rely on the output load to discharge VOUT to the new set point. Once the high-to-low transition begins, the IC stops switching until VOUT has reached the new set point.

Under-Voltage Lockout

When EN is HIGH, the under-voltage lockout keeps the part from operating until the input supply voltage rises HIGH enough to properly operate. This ensures proper operation of the regulator during startup or shutdown.

Input Over-Voltage Protection (OVP)

When V_{IN} exceeds V_{SDWN} (about 6.2 V) the IC stops switching to protect the circuitry from internal spikes above 6.5 V. An internal filter prevents the circuit from shutting down due to noise spikes.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching this point, the high-side switch turns off, preventing high currents from causing damage. Sixteen consecutive current limit cycles in current limit cause the regulator to shut down and stay off for about 1700 µs before attempting a restart.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 17°C hysteresisI^2C Interface

I^2C Interface

The FAN53202's serial interface is compatible with Standard, Fast, Fast Plus, and HS Mode I^2C-Bus® specifications. The FAN53202's SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I^2C Slave Address

In hex notation, the slave address assumes a 0 LS Bit. The hex slave address is C0.

Table 3. I^2C Slave Address

Hex	Bits							
	7	6	5	4	3	2	1	0
C0	1	1	0	0	0	0	0	R/$\overline{W}$

Other slave addresses can be assigned. Contact a Fairchild Semiconductor representative.

Bus Timing

As shown in Figure 19, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

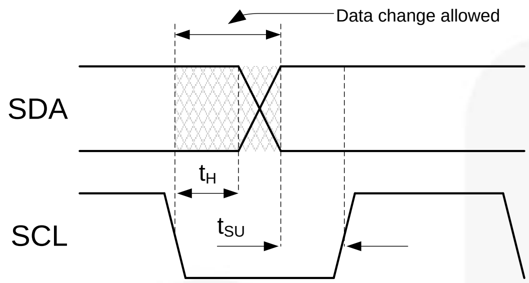


Figure 19. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 20

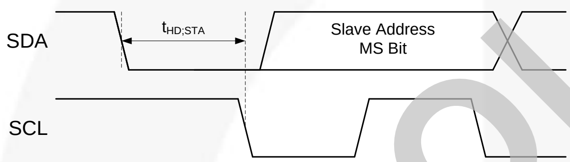


Figure 20. START Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 21.

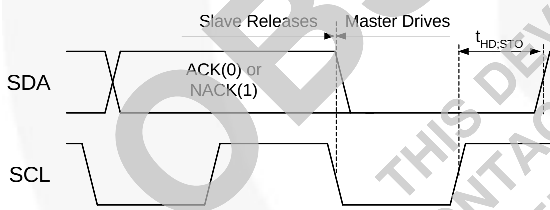


Figure 21. STOP Bit

During a read from the FAN53202, the master issues a REPEATED START after sending the register address, and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 22.

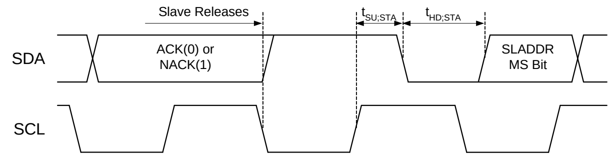


Figure 22. REPEATED START Timing

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical, except the bus speed for HS mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition. The master code is sent in Fast or Fast-Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition (Figure 20 that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 21) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 22) Read and Write Transactions.

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 4. I²C Bit Definitions for Figure 23 & Figure 24

Symbol	Definition
R	REPEATED START, *see Figure 22*
P	STOP, *see Figure 21*
S	START, *see Figure 20*
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	REPEATED START, *see Figure 22*
P	STOP, *see Figure 21*

	7 bits	0		8 bits	0	8 bits	0	
S	Slave Address	0	A	Reg Addr	A	Data	A	P

Figure 23. Write Transaction

	7 bits	0		8 bits	0		7 bits	0		8 bits	1	
S	Slave Address	0	A	Reg Addr	A	R	Slave Address	1	A	Data	$\overline{A}$	P

Figure 24. Read Transaction

Register Description

Table 5. Map

Hex Address	Name	Function
00	VSEL0	Controls V_{OUT} settings when VSEL pin = 0
01	VSEL1	Controls V_{OUT} settings when VSEL pin = 1
02	CONTROL	Determines whether V_{OUT} output discharge is enabled and also the slew rate of positive transitions
03	ID1	Read-only register identifies vendor and chip type
04	ID2	Read-only register identifies die revision
05	MONITOR	Indicates device status

Table 6. Bit Definitions

The following table defines the operation of each register bit. Bold indicates power-on default values.

Bit	Name	Value	Description
VSEL0	**R/W**	**Register Address: 00**	
7	BUCK_EN0	**1**	Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent.
6	MODE0	**0**	Allow Auto-PFM Mode during light load.
		1	Forced PWM Mode.
5:0	NSEL0		Sets V_{OUT} value from 0.6V to 1.3875 V in 12.5 mV steps
VSEL1	**R/W**	**Register Address: 01**	
7	BUCK_EN1	**1**	Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent.
6	MODE1	**0**	Allow AUTO-PFM Mode during light load.
		1	Forced PWM Mode.
5:0	NSEL1		Sets V_{OUT} value from 0.6V to 1.3875 V in 12.5 mV steps
CONTROL	**R/W**	**Register Address: 02**	
7	OUTPUT_DISCHARGE	0	When the regulator is disabled, V_{OUT} is not discharged.
		1	When the regulator is disabled, V_{OUT} discharges through an internal pull-down.
6:4	SLEW	**000**	Sets the slew rate for positive voltage transitions *(see Table 2).*
3	Reserved	**0**	Always reads back 0
2	Reserved	**0**	Always reads back 0
1:0	Reserved	**00**	Always reads back 00
ID1	**R**	**Register Address: 03**	
7:5	VENDOR	**100**	Signifies Fairchild as the IC vendor
4	Reserved	**0**	Always reads back 0
3:0	DIE_ID	**0000**	Refer to ordering information
ID2	**R**	**Register Address: 04**	
7:4	Reserved	**0000**	Always reads back 0000
3:0	DIE_REV	**1100**	IC mask revision
MONITOR	**R**	**Register Address: 05**	
7	PGOOD	0	1: buck is enabled and soft-start is completed
6:0	Not used	**000 0000**	Always reads back 000 0000

Application Information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy-handling capability of the application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}} \right) \quad (3)$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current such that:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad (4)$$

The FAN53202 is optimized for operation with L=330 nH, but is stable with inductances up to 1.0 µH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so will lower the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin-effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^{\ 2} + \frac{\Delta I^2}{12}} \quad (5)$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs as well as the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Table 7. Effects of Inductor Value (from 330 nH Recommended) on Regulator Performance

$I_{MAX(LOAD)}$	ΔV_{OUT} (Eq.(7))	Transient Response
Increase	Decrease	Degraded

Inductor Current Rating

The current limit circuit can allow substantial peak currents to flow through L1 under worst-case conditions. If it is possible for the load to draw such currents, the inductor should be capable of sustaining the current or failing in a safe manner.

For space-constrained applications, a lower current rating for L1 can be used. The FAN53202 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor.

Output Capacitor and V_{OUT} Ripple

The reference BOM suggests 0805 capacitors, but 0603 capacitors may be used if space is at a premium. Due to voltage effects, the 0603 capacitors have a lower in-circuit capacitance than the 0805 package, which can degrade transient response and output ripple.

Increasing C_{OUT} has negligible effect on loop stability and can be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is calculated by:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1-D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right] \quad (6)$$

where C_{OUT} is the effective output capacitance.

The capacitance of C_{OUT} decreases at higher output voltages, which results in higher ΔV_{OUT}. Equation (6) is only valid for Continuous Current Mode (CCM) operation, which occurs when the regulator is in PWM Mode.

For large C_{OUT} values, the regulator may fail to start under a load. If an inductor value greater than 1.0 µH is used, at least 30 µF of C_{OUT} should be used to ensure stability.

The lowest ΔV_{OUT} is obtained when the IC is in PWM Mode and, therefore, operating at 2.4 MHz. In PFM Mode, f_{SW} is reduced, causing ΔV_{OUT} to increase.

ESL Effects

The Equivalent Series Inductance (ESL) of the output capacitor network should be kept low to minimize the square-wave component of output ripple that results from the division ratio C_{OUT} ESL and the output inductor (L_{OUT}). The square-wave component due to the ESL can be estimated as:

$$\Delta V_{OUT(SQ)} \approx V_{IN} \bullet \frac{ESL_{COUT}}{L1} \quad (7)$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value. For example, to obtain C_{OUT}=20 µF, a single 22 µF 0805 would produce twice the square wave ripple as two x 10 µF 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805s have lower ESL than 1206s. If low output ripple is a chief concern, some vendors produce 0508 or 0612 capacitors with ultra-low ESL. Placing additional small-value capacitors near the load also reduces the high-frequency ripple components.

Input Capacitor

The ceramic input capacitors should be placed as close as possible between the VIN pin and PGND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce under-damped ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective C_{IN} capacitance value decreases, as V_{IN} increases due to DC bias effects. This has no significant impact on regulator performance.

Thermal Considerations

Heat is removed from the IC through the solder bumps to the PCB copper. The junction-to-ambient thermal resistance (θ_{JA}) is largely a function of the PCB layout (size, copper weight, and trace width) and the temperature rise from junction to ambient (ΔT).

For the FAN53202UC, θ_{JA} is 38°C/W when mounted on its four-layer evaluation board in still air with two-ounce outer layer copper weight and one-ounce inner layers. Halving the copper thickness results in an increased θ_{JA} of 48°C/W.

For long-term reliable operation, the IC's junction temperature (T_J) should be maintained below 125°C.

To calculate maximum operating temperature ($\leq$125°C) for a specific application:

1. Use efficiency graphs to determine efficiency for the desired V_{IN}, V_{OUT}, and load conditions.
2. Calculate total power dissipation using:

$$P_T = V_{OUT} \times I_{LOAD} \times \left(\frac{1}{\eta} - 1\right) \tag{8}$$

where η is efficiency from Figure 3 and Figure 4.

Estimate inductor copper losses using:

$$P_L = I_{LOAD}{}^2 \times DCR_L \tag{9}$$

3. Determine IC losses by removing inductor losses (step 3) from total dissipation:

$$P_{IC} = P_T - P_L \tag{10}$$

4. Determine device operating temperature:

$$\Delta T = P_{IC} \times \Theta_{JA} \quad \text{and} \quad T_{IC} = T_A + \Delta T \tag{11}$$

It is important to note that the $R_{DS(ON)}$ of the IC's power MOSFETs increases linearly with temperature at about 1.21%/°C. This causes the efficiency (η) to degrade with increasing die temperature.

Recommended External Components

Table 8. Recommended Capacitors

Component	Quantity	Vendor	Vendor	C (µF)	Size	Rated
C_{OUT}	2 Pieces	C2012X5R0J226M	TDK	22	0805	6.3 V
C_{IN}	1 Piece	C2012X5R1A106M	TDK	10	0805	6.3 V

Table 9. Recommended Inductors

Manufacturer	Part#	L (nH)	DCR (mΩ)	I_{SAT} (4)	L	W	H
TOKO(4)	DFE201610E-R47M	470	16	6.3	2.0	1.6	1.0
TOKO	DFE252012F_R33M	330	14	8.5	2.5	2.0	1.2
TOKO	FDSD0412-H-R33M	330	16	10	4.0	4.0	1.2
Mag. Layers	MMD-04ABNR33M-M1-RU	330	12.5	7.5	4.5	4.1	1.2
CYNTEC	PIMB041B-R33MS	330	17	8.4	4.4	4.2	1.0
TDK	VLC5020T-R47M	470	15	5.4	5.0	5.0	2.0

Note:
4. This inductor is recommended for applications with I_{OUT} < 3 A.

Layout Recommendation

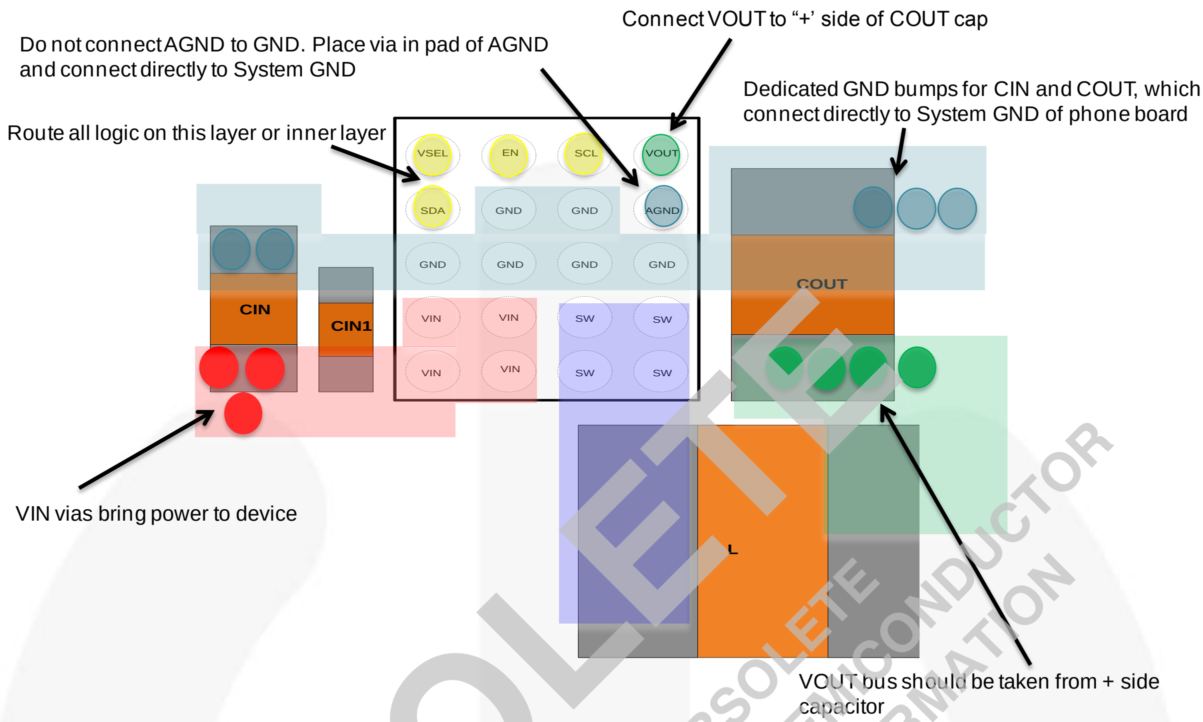


Figure 25. Guidance for Layer 1

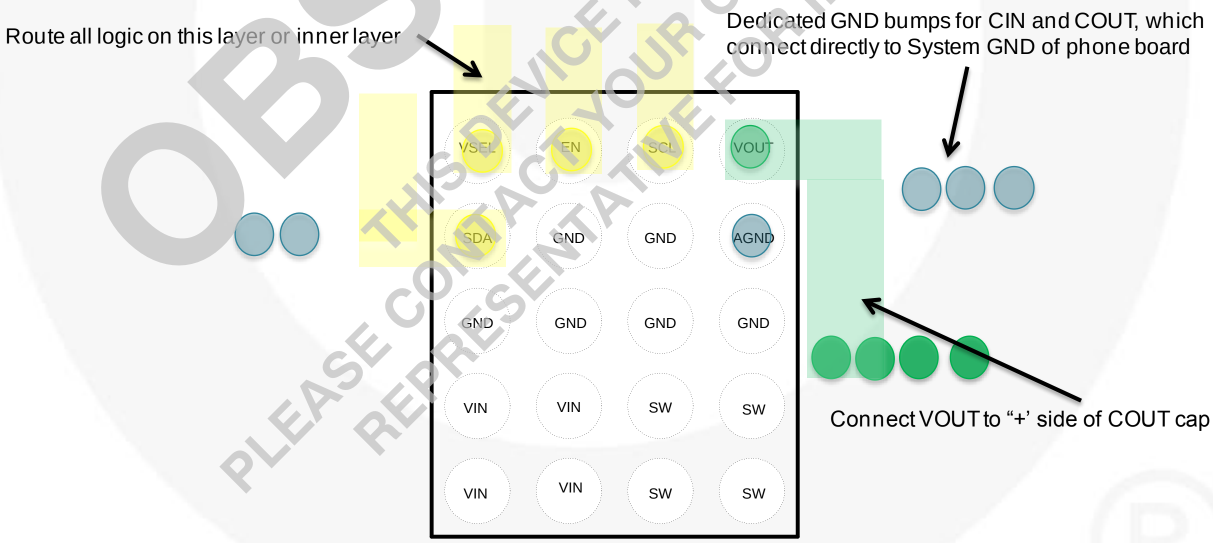


Figure 26. Guidance for Layer 2

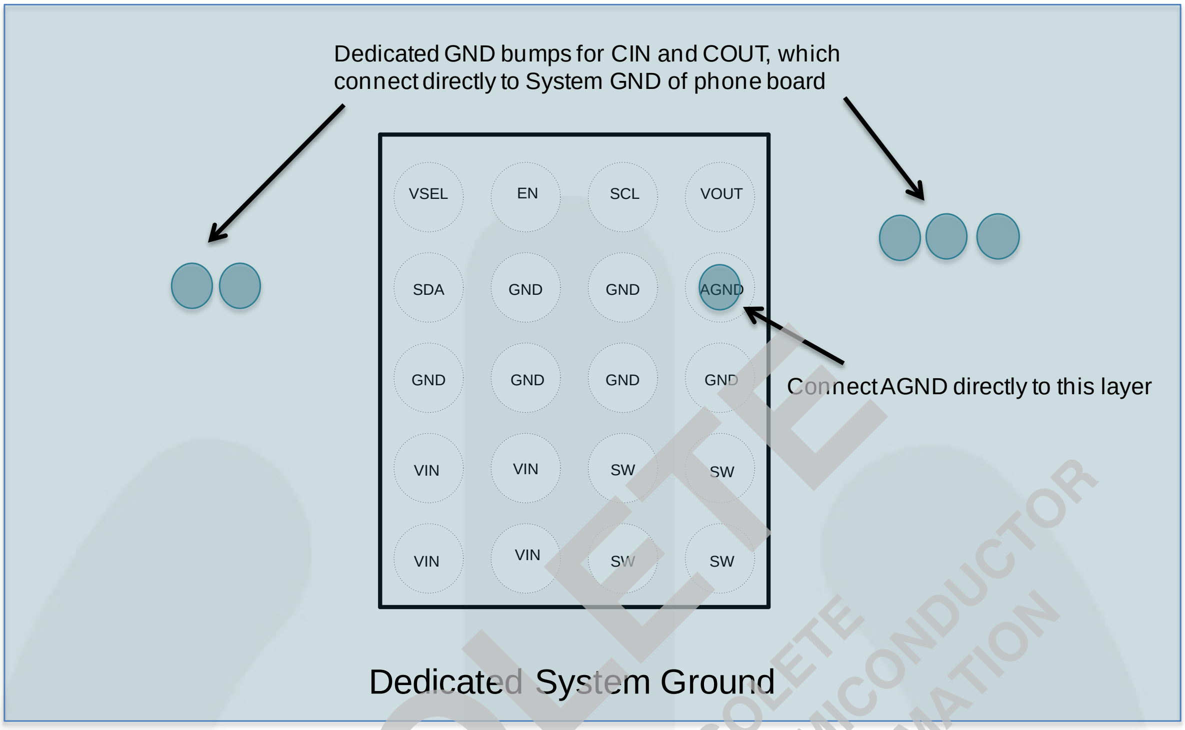
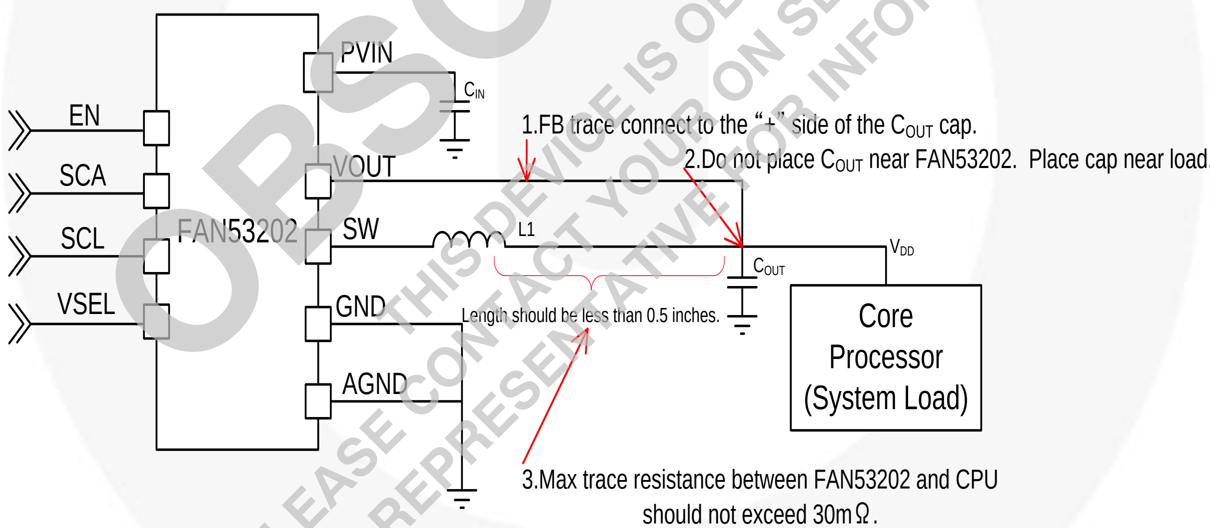


Figure 27. Guidance for Layer 3



The table provided for resistance for the given value of copper

Width (mils)	Length (mils)	Copper (Oz)	Resistance (mΩ)
25	5000	2	4.2
25	500	1.5	4.9
25	500	1	5.8
25	500	0.5	7.6

Figure 28. Remote Sensing Schematic

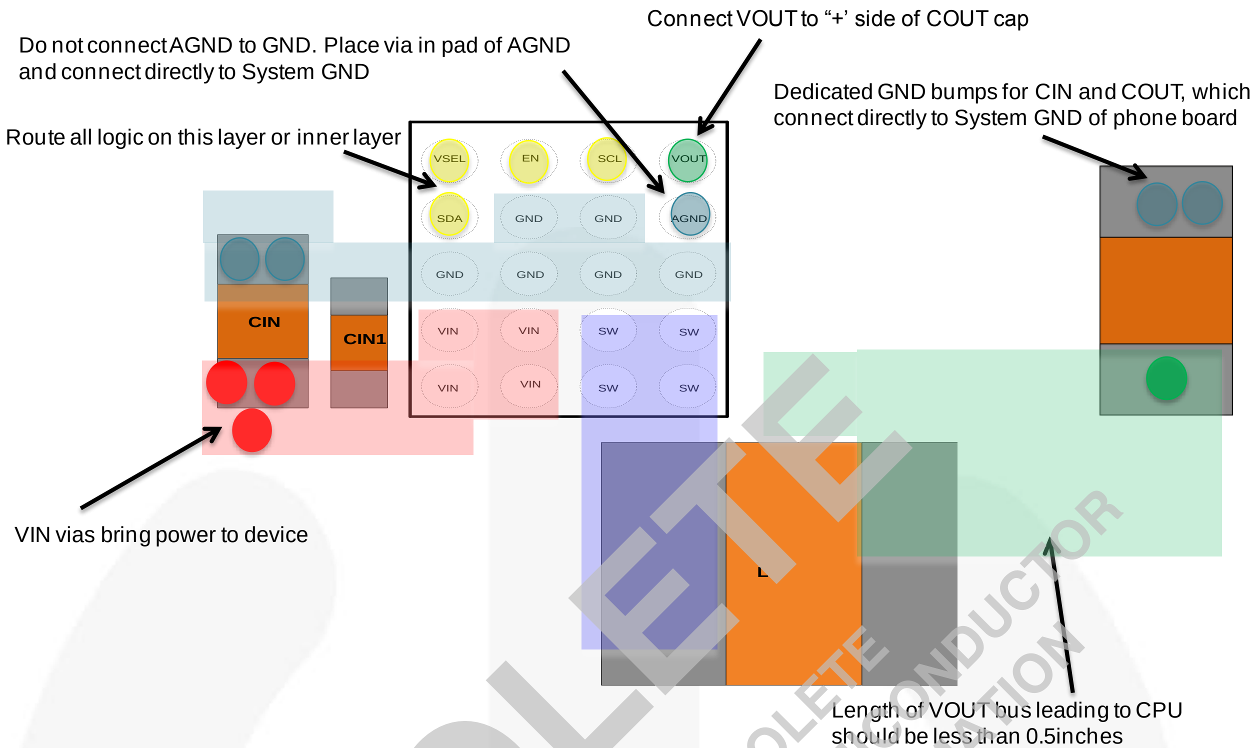
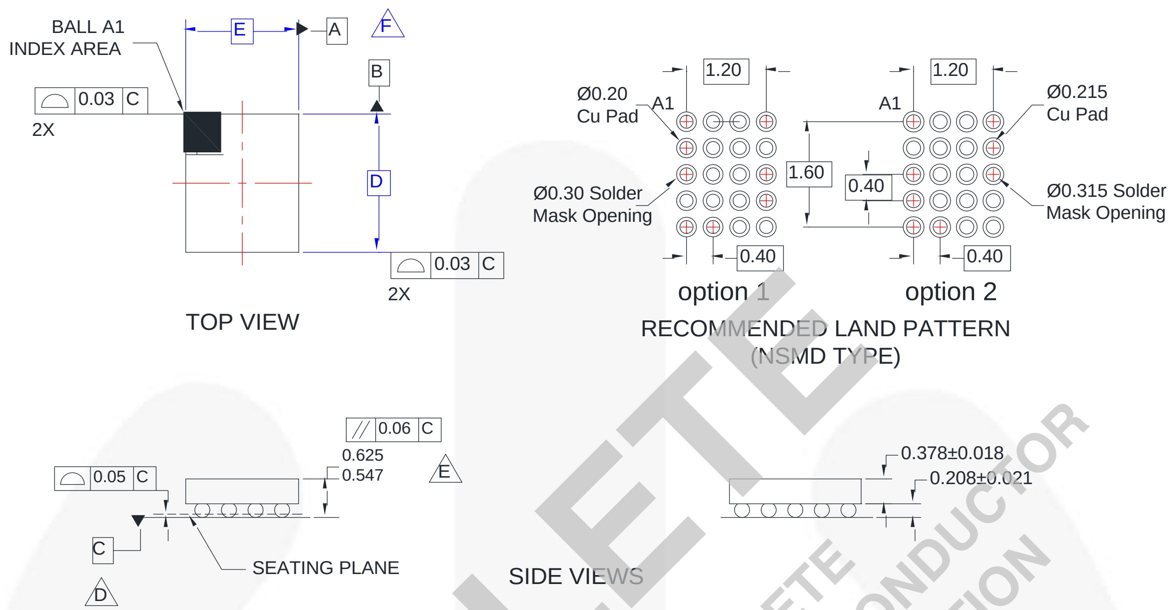
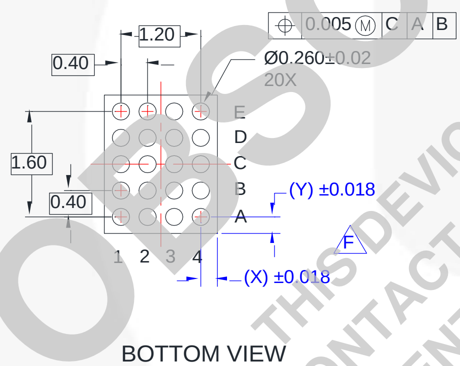


Figure 29. Remote Sensing Guidance, Top Layer

Physical Dimensions





NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC020AArev3.

Figure 30. 20-Ball, Wafer-Level Chip-Scale Package (WLCSP), 4x5 Array, 0.4 mm Pitch, 250 µm Ball

Product-Specific Dimensions

Product	D	E	X	Y
FAN53202UC23X	2.015 ±0.03	1.615 ±0.03	0.2075	0.2075

FAIRCHILD

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AttitudeEngine™
Awinda®
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™

F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
MotionGrid®
MTi®
MTx®
MVN®
mWSaver®
OptoHiT™
OPTOLOGIC®

OPTOPLANAR®
®
Power Supply WebDesigner™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™

SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
µ SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™
Xsens™
仙童™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT HTTP://WWW.FAIRCHILDSEMI.COM. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I74

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative