VSC7462

12-GbE + 2 × 10-GbE Port Carrier Ethernet Switch

Target Specification

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1 Introduction

This document consists of descriptions and specifications for both functional and physical aspects of the VSC7462 LynX-1 Carrier Access Switch. It is intended for system designers and software developers.

In addition to the datasheet, Vitesse maintains an extensive part-specific library of support and collateral materials that you may find useful in developing your own product. Depending upon the Vitesse device, this library may include:

- Application notes that provide detailed descriptions of the use of the particular Vitesse product to solve real-world problems
- White papers published by industry experts that provide ancillary and background information useful in developing products that take full advantage of Vitesse product designs and capabilities
- User guides that describe specific techniques for interfacing to the particular Vitesse products
- Reference designs showing the Vitesse device built in to applications in ways intended to exploit its relative strengths
- Software Development Kits with sample commands and scripts
- Presentations highlighting the operational features and specifications of the device to assist in developing your own product road map
- Input/Output Buffer Information specification (IBIS) models to help you create and support the interfaces available on the particular Vitesse product

Visit and register as a user on the Vitesse Web site to keep abreast of the latest innovations from research and development teams and the most current product and application documentation. The address of the Vitesse Web site is www.vitesse.com.

1.1 Standard References

This document uses the following industry references.

Table 1. Referenced Documents

Document	Title	Revision
IEEE		
802.3	Local and Metropolitan Area Networks - Specific requirements CSMA/CD access method and physical layer specifications	-2008
802.1D	Media Access Control (MAC) Bridges	-2004
802.1Q	Virtual Bridged Local Area Networks	-2005
802.1ad	802.1Q Amendment 4: Provider Bridges (PB)	-2005
P802.1ah	802.1Q Amendment 6: Provider Backbone Bridges (PBB)	-2008
P802.1ag	802.1Q Amendment 5: Connectivity Fault Management (CFM)	-2007

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Table 1. Referenced Documents *(continued)*

Document	Title	Revision
P802.1Qay	802.1Q Amendment: Provider Backbone Bridge Traffic Engineering (PBB-TE)	-2009
1588v2	Precision Clock Synchronization Protocol for Networked Measurement and Control Systems	-2008
MEF		
MEF-9	Abstract Test Suite for Ethernet Services at the UNI	10/2004
MEF-10.1	Ethernet Services Attributes Phase 2	11/2006
MEF-14	Abstract Test Suite for Traffic Management Phase 1	11/2005
MEF-16	Ethernet Local Management Interface (E-LMI)	1/ 2006
ITU-T		
Y.1731	OAM Functions and Mechanisms for Ethernet Based Networks	5/22/2006
G.8261	Timing and Synchronization Aspects in Packet Networks	12/14/2006
G.8262	Timing Characteristics of Synchronous Ethernet Equipment Slave Clock (EEC)	-2008
G.8263	Timing Characteristics of Packet-Based Equipment Clocks (PEC) and Packet-Based Service Clocks (PSC)	Evolving
IETF		
RFC-2863	The Interfaces Group MIB	6/2000
RFC-3635	Definitions of Managed Objects for Ethernet-like Interface Types	9/2003
RFC-2819	Remote Network Monitoring (RMON) MIB	5/2000
RFC-2236	Internet Group Management Protocol, Version 2 (IGMPv2)	11/1997
RFC-3376	Internet Group Management Protocol, Version 3 (IGMPv3)	10/2002
RFC-2710	Multicast Listener Discovery for IPv6 (MLDv1)	10/1999
RFC-3810	Multicast Listener Discovery Version 2 for IPv6 (MLDv2)	6/2004
RFC3031	MPLS Architecture	Jan 2001
RFC3270	MPLS Support of DiffServ	May 2002
RFC4090	RSVP-TE Fast Reroute	May 2005
RFC3985	PWE3 Architecture	March 2005
RFC4385	PWE3 Control Word for use over an MPLS PSN	Feb 2006
RFC4448	Encapsulation Methods for Transport of Ethernet over MPLS Networks	April 2006
RFC5085	Pseudowire Virtual Circuit Connectivity Verification (VCCV)	December 2007
RFC5586	MPLS Generic Associated Channel	June 2009
Other		
OIF-SPI4-02.1	OIF SPI4.2 Implementation Agreement	10/15/2003
SFP MSA	SFP MultiSource Agreement	9/14/2000
ENG-46158	Cisco Serial GMII (SGMII) Specification	1.9
JESD79	DDR2 SDRAM Specification	2B

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1.2 Terms and Abbreviations

The following terms and abbreviations are used throughout this document.

Table 2. Terms and Abbreviations

Term	Explanation
ASP	Vitesse Arrival Service Point (see SP).
Basic VLAN	The VLAN ID returned by the basic classification. A basic VLAN is assigned to every frame as a default classified VLAN if no more advanced VLAN classification is carried out on the frame.
B-VLAN	The classified VLAN of the B-Component when dual-domain processing is enabled. Also referred to as the classified B-VLAN.
Bridging	Forwarding is based on the principles of IEEE 802.1D using the MAC address. Optionally, bridging may include flooding and MAC address learning.
CFM	IEEE Connectivity Fault Management.
Classified VLAN	The final VLAN ID classification of a frame used in the forwarding process. The classified VLAN is the result of basic, service, and profile classification. With dual-domain processing enabled, the classified VLAN is the classified VLAN of the I-Component.
DEVICE	Common name for Device 1G, Device 2G5, and Device 10G.
DSP	Vitesse Departure Service Point (see SP).
E-LMI	MEF Ethernet Local Management Interface.
EoMPLS	IETF Ethernet over MPLS Pseudowire.
EPL, EVPL	MEF Ethernet Private Line, Ethernet Virtual Private Line service.
EP-LAN, EVP-LAN	MEF Ethernet Private LAN, Ethernet Virtual Private LAN service.
EP-TREE, EVP-TREE	MEF Ethernet Private TREE, Ethernet Virtual Private TREE service.
ESP	IEEE PBB-TE Ethernet Switched Path.
EVC	MEF Ethernet Virtual Connection.
Forwarding	The forwarding function performed by a switch and a MAC to obtain the set of destination ports for any given frame.
IQS	Vitesse Input Queue System.
LSP	IETF MPLS Label Switched Path.
MPLS	IETF Multi-Protocol Label Switching.
MPLS-TP	IETF/ITU-T MPLS Transport Profile.
NPI	The node processor interface (NPI) attaches to the VSC7462 device over SGMII and connects to the switch core as a dedicated GbE port. It is not an interface to the CPU device, but primarily a packet (frame) interface. The NPI cannot be used to directly access registers in the VSC7462 device.
OQS	Vitesse Output Queue System.
PAG	Vitesse Policy Access Group that is used to map many services to a shared security policy.
PB	IEEE 802.1AD Provider Bridging (also known as "Q-in-Q").
PBB	IEEE P802.1ah Provider Backbone Bridging (also known as "MAC-in-MAC").
PBB-TE	IEEE P802.1Qay Provider Backbone Bridging with Traffic Engineering (PBB with Traffic-Engineered Ethernet switched Paths).

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Table 2. Terms and Abbreviations *(continued)*

Term	Explanation
PCP	IEEE Priority Code Point interpretation of Ethernet Priority (also known as 802.1p) bits.
Profile VLAN	The VLAN ID returned by profile classification. If a valid Profile VLAN is assigned to a frame it takes precedence over service VLAN and Basic VLAN and always becomes the Classified VLAN.
PWE3	IETF Pseudowire Emulation Edge to Edge Technology.
QAG	Vitesse QoS Access Group, used to map many services to a shared QoS Policy.
Service VLAN	The VLAN ID returned by the service classification. A valid service VLAN takes precedence over basic VLAN.
SP	Vitesse Service Point. A reference point inside the CE Switch or MAC where service policy is applied. Service policy includes policing, statistics, tagging/encapsulation, QoS, and connectivity.
Switching	Forwarding is not based on the principles of 802.1D. Switching may forward based on service classification, VLAN tags, proprietary host interface header (HIH), and so on.
UNI and NNI	Any User/Network Interface and any Network/Network Interface
VAUI	Vitesse Attachment Unit Interface. Supports IEEE standard XAUI plus Vitesse-proprietary extensions.
VCAP	Vitesse Content Aware Processor, TCAM-based security.

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2 Overview

The VSC7462 LynX-1 is a Carrier Ethernet switch containing twelve 10/100/1000 Mbps Ethernet ports and two 10 Gbps XAUI Ethernet ports. LynX-1 provides a rich set of Carrier Ethernet services, Ethernet switching, and Ethernet transport features. Advanced TCAM-based QoS processing enables delivery of differentiated services with per-service SLA guarantees. Security is assured through separate processing using TCAM-based Vitesse Content Aware Processor (VCAP-II).

The VSC7462 provides comprehensive service and transport support for networks based on Provider Bridge (PB), Provider Backbone Bridge (PBB), Provider Backbone Bridge with Traffic Engineering (PBB-TE), and Multi-Protocol Label Switching (both MPLS and MPLS-TP).

A larger Carrier Ethernet Switch derivative is also available. The VSC7460 Jaguar-1 supports the exact same feature set as VSC7462 LynX-1, except that it contains twenty-four 10/100/1000 Mbps Ethernet ports and four 10 Gbps XAUI Ethernet ports.

Carrier Ethernet MAC devices, pin-compatible with Jaguar-1 (VSC7460) and LynX-1 (VSC7462), are available for aggregation applications requiring hierarchical traffic management with the advanced features of a Carrier Ethernet switch.

General Features

- 12 × 1 GbE ports, supporting
  – SGMII
  – 1000BASE-X SerDes
  – 100BASE-FX
  – 1000BASE-KX backplane
- 2 × 10 GbE VAUI (Vitesse XAUI) ports, supporting
  – Standard four-lane 10 Gbps XAUI
  – Two-lane 10 Gbps XAUI (two ports maximum)
  – Four one-lane 2.5 GbE per XAUI (eight ports maximum)
  – 10GBASE-CX4
  – 10GBASE-KX4 backplane
- 1 × 1 GbE node processing interface (NPI) port, supporting
  – SGMII for external frame inject/extract
- 32 Mbits of internal shared memory
  – 10056 byte jumbo frame support
  – Modified DWRR scheduler/shaper with mix of strict and weighted queues
  – Eight priorities and eight queues per port
- 4096 TCAM-based Service Classification entries
- 4096 TCAM-based service-specific egress tagging and QoS entries
- Integrated 416 MHz MIPS24K CPU
  – Up to 128 M × 16 DDR2 SDRAM program memory, 200 MHz
  – CPU operation: internal, external, or both

Layer 2 Switching Features

- 802.1Q VLAN switch
  – 32K MACs, 4K VLANs

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- Push/pop/translate up to two VLAN tags
  – on ingress and/or egress
- Policing with leaky bucket storm control and protection from broadcast, flooding, and multicast
- Rapid Spanning Tree Protocol (RSTP) support
- Multiple Spanning Tree Protocol (MSTP) support
- Independent VLAN Learning (IVL)
- Shared VLAN Learning (SVL)
- Hardware and software-based Learning
- 512 TCAM-based QoS, VLAN and Security Profile Classification entries
- 512 TCAM-based VCAP-II Security entries

Multicast Features

- 256 Layer 2 Multicast Groups
- 1K IPv4 (S, G) Multicast Groups
- 32K IPv4/IPv6 (G) Multicast Groups
- Internet Group Management Protocol version 2 (IGMPv2) support
- Internet Group Management Protocol version 3 (IGMPv3) support
- Multicast Listener Discovery (MLD) version 1 and version 2 support

Carrier Ethernet Features

- Provider Bridge (PB) switch
  – 32K MACs, 4K VLANs
- Provider Backbone Bridge (PBB) switch
  – 16K B-MACs, 4K B-VLANs
  – 16K C-MACs, 4K C-VLANs
  – 4K MAC-in-MAC encapsulations
- PBB-TE switch, includes all PBB features, plus
  – 4K Ethernet Switched Paths (ESPs)
  – 512 hardware-protected ESPs
- Ethernet over MPLS (EoMPLS) switch
  Includes all PB and PBB features, plus
  – 4K EoMPLS pseudowires and Label Switched Paths (LSPs)
  – 512 hardware-protected LSPs (tunnels)
- 4K MEF E-LAN, E-LINE, E-TREE service points
  – 4K dual leaky-bucket service policers with remarking per service point
  – Statistics and tagging options per service point
- 512 dual leaky-bucket tunnel policers with statistics per tunnel

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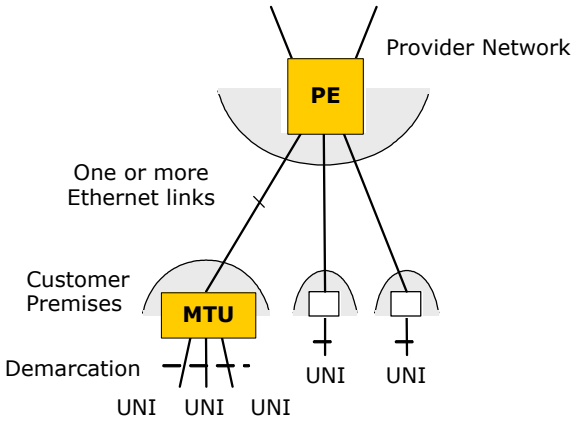
- OAM hardware for 4K service points, 512 paths, 32 ports
  – Software for OAM and protection switching
- Layer 1 (L1) Synchronous Ethernet
- Layer 2 (L2) IEEE 1588 timestamping hardware
- Enhanced Carrier Ethernet software API

2.1 Switch Applications

The following illustration shows the Customer Premise Equipment (CPE) and Provider Edge (PE) equipment placed in a network. LynX-1 can be used to implement the access and first-level aggregation functions in these boxes.

Figure 1. Switch Applications: Network Diagram



In these applications, LynX-1 form the demarcation between the customer network and the provider network, providing the full set of UNI features in a cost-effective manner:

- Map customer frame formats into provider frame formats
  – Classify frames and map to appropriate QoS profiles
  – Apply Provider Bridge (PB), Provider Backbone Bridge (PBB), Provider Backbone Bridge with Traffic Engineering (PBB-TE), or Ethernet over MPLS (EoMPLS) encapsulations
- Meter the customer traffic and ensure that the customer Service Level Agreement (SLA) is met
  – Police using MEF-defined dual leaky-bucket algorithm
  – Mark frames as Committed (Green) or Discard Eligible (Yellow)
  – Provide correct QoS treatment (traffic management)
  – Provide traffic statistics per customer in a manner consistent with the SLA
- Enable end-to-end Service OAM by the customer, if allowed
- Implement the service as defined by the SLA
  – E-LINE for point-point or backhaul services
  – E-LAN for multipoint/bridged services
  – E-TREE for video distribution or backhaul services

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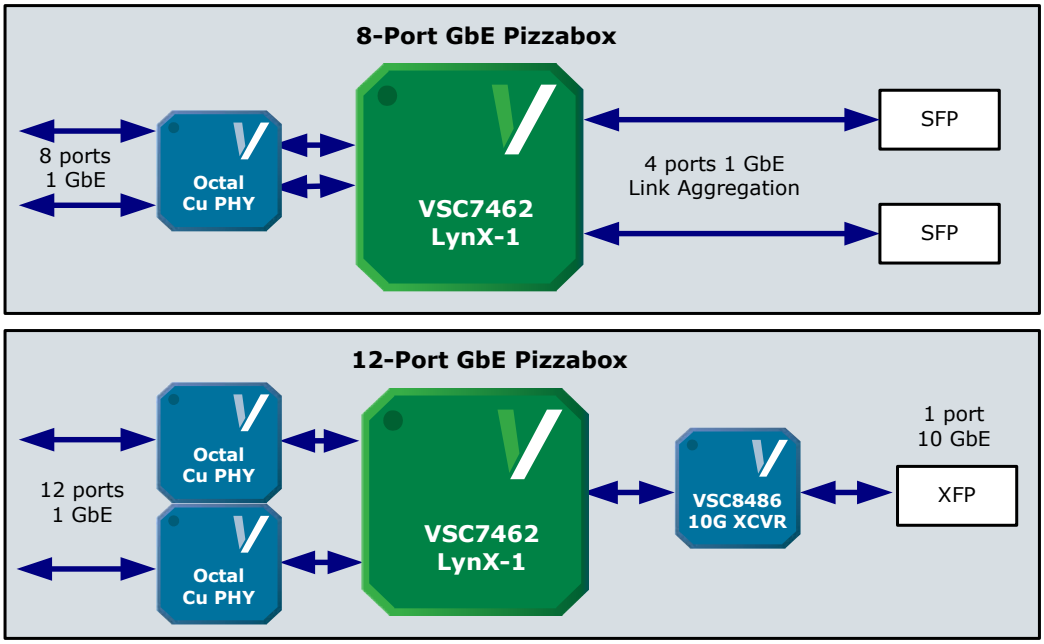
- Enable management and protection schemes as required by the provider
  – Link aggregation or other port protection schemes if used for access
  – OAM at the operator and service provider levels for remote management, fault diagnosis, and protection switching
- Support network timing and synchronization requirements as required
  – Synchronous Ethernet and IEEE 1588 functionality

At the first level of aggregation within the provider network, LynX-1 offers greater scale and additional capabilities such as:

- Traffic engineering and protection schemes are typically always applied here
- Ability to aggregate services already conditioned by other access gear while also offering new services directly
- Participation in Ethernet aggregation topologies such as meshes and rings

Using the LynX-1 device, pizzaboxes, or line cards of 10 Gbps to 40 Gbps can be implemented, as shown in the following illustration.

Figure 2. Switch Applications: Equipment Diagram



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2.2 Major Switch Configurations

This section describes major configurations and services that can be offered using the LynX-1 switch.

Table 3. Switch Configurations and Services

Major Switch Configurations	Services Available			
	IEEE VLAN Bridge	MEF E-LINE	MEF E-LAN	MEF E-TREE
PB or PBB Core Bridge (Service-unaware)	X			
Service-enabled PB or PBB Core Bridge	X	X	X	X
Service-enabled PBB/PBB-TE Edge Bridge	X	X	X	X
Service-enabled EoMPLS Edge Bridge	X	X	X	X

LynX-1 switch has the following major configurations:

- Provider Bridge (PB) or Provider Backbone (PBB) Core Bridge

  For standard PB operation, all frames on all ports use C-MAC addresses. These frames may be untagged or have combinations of C-tags and S-tags ("Q-in-Q" tagging).

  For standard PBB Core Bridge operation, all frames on all ports use B-MAC addresses ("MAC-in-MAC" encapsulation). These frames may be untagged or have up to two tags. It is also possible to operate where one set of VIDs uses C-MAC addresses and a different set of VIDs uses B-MAC addresses. Addressing must be consistent for each VID on all ports.

In these configurations, the switch supports 4K VLANs and 32K MAC addresses. Per-VLAN statistics are supported.

- Service-Enabled PB or PBB Core Bridge

  The switch operates as a PB or PBB Core Bridge with 4K VLANs and 32K MAC addresses.

  MEF E-LINE, E-LAN and E-TREE services can be overlaid on top of the standard bridging operation. Each service is configurable with its own policing, tagging, OAM and protection, control protocol tunneling, and statistics.

  It is possible to map all E-LINE services to one VLAN and still operate as a standard VLAN switch for the remaining VLANs.

- PBB/PBB-TE Edge Bridge

  For standard PBB operation, all frames on the backbone ports use B-MAC addresses while all frames on all other ports use C-MAC addresses. The switch supports 4K VLANs and 16K MAC addresses in the C-MAC domain (I components) and an additional 4K VLANs and 16K MAC addresses in the B-MAC domain (B component).

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The switch can perform standard PBB bridging among the I-components and the B-component. The switch provides the service mapping and applies the I-tag and MAC-in-MAC encapsulations. The association between I- and B-components must be learned by software or provisioned. Flooding into the B-component uses the reserved flood address per the PBB standard.

The switch can also implement PBB-TE between the I-components and the B-component. Ethernet Switched Paths (ESPs) are configured and used to connect over the backbone network to other PBB-TE Edge Bridges. Traffic Engineering and hardware-based protection can now be used to implement carrier-grade Ethernet. Forwarding into the B-component must be provisioned, or use the reserved flood address per the PBB standard. It is not possible to multicast a frame into multiple ESPs, other than for supported protection schemes.

MEF E-LINE, E-LAN, and E-TREE services are available in these configurations. It is possible to map all E-LINE services to one VLAN in each domain and still operate as a standard VLAN switch for the remaining VLANs.

It is also possible to operate where on the backbone ports one set of VIDs uses C-MAC addresses and a different set of VIDs uses B-MAC addresses. Addressing must be consistent for each VID on all ports. This capability enables the ability to incrementally add PBB/PBB-TE edge functionality over an existing PB network.

- EoMPLS Edge Bridge

  The switch operates as either:

  – A Provider Bridge or PBB Core Bridge as noted above with 4K VLANs and 32K MAC addresses

  – A PBB Edge Bridge as noted above with 4K VLANs and 16K MAC addresses each in the C-MAC domain (I component) and the B-MAC domain (B component), and full IB-BEB bridging functionality

  The switch can also map individual services over EoMPLS Pseudowires, and map multiple Pseudowires over MPLS Label Switched Paths (LSPs). Traffic Engineering and hardware-based protection can now be used to implement carrier-grade Ethernet. Forwarding over MPLS must be provisioned. It is not possible to multicast a frame onto multiple LSPs.

  MEF E-LINE, E-LAN, and E-TREE services are available in these configurations. It is possible to perform advanced tagging and MAC-in-MAC operations on the Ethernet frame and also transport it over MPLS.

2.3 Related Products

VSC8486 10 Gbps XAUI or XGMII to XFI LAN/WAN transceiver

The VSC8486 is a LAN/WAN XAUI or XGMII transceiver that converts four lanes of 3 Gbps XAUI data to a 10 Gbps XFI serial stream. At just 750 mW, the VSC8486 is ideal for applications requiring low power. The VSC8486 device is also equipped with an additional full-rate data port that can be used for bypass monitoring or channel monitoring applications. It meets all specifications for 10 Gigabit Ethernet (GbE) Layer-1 processing, as defined in IEEE 802.3-2005.

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VSC9138 (LOVCAT192™) 10 Gbps Multiservice High-Order/Low-Order Virtual Concatenation Mapper

The VersaCAT family adapts Ethernet technology to the WAN by efficiently provisioning Ethernet services across existing transport infrastructures while optimizing bandwidth utilization using hitless rate adaptation. It includes a suite of 2.5G and 10G mappers (HOVCAT, HOVCATe, LOVCAT) and multiprotocol WAN MACs (Meigs-IIE, Campbell-I, Barrington-I, Barrington-II, and eXEC1) that support Virtual Concatenation, fully integrated LCAS and GFP, as well as provides extensive Layer 2 aggregation, encapsulation and management features. More specifically this family is used for efficient provisioning of data services from Ethernet (10 Mbps) to 10 Gigabit Ethernet (10 Gbps) and various storage and video protocols over WAN transport infrastructure, while optimizing bandwidth utilization using hitless rate adaptation.

VSC7344-01 (Barrington-II™) 24 × 10/100/1000 and 2 × 10G Ethernet MAC with SPI-4.2 and XAUI host interfaces

The VSC7344-01 is an advanced Ethernet MAC containing twenty-four 10/100/1000 Ethernet ports with integrated SGMII and 100/1000 optical serializers/deserializers. The host interface can be configured as SPI-4.2, one XAUI, or two XAUI interfaces. Each SPI-4.2 and XAUI host interface uses a SPI-4.2 status channel for flow control. To support the high oversubscription factor, the VSC7344-01 has a set of advanced QoS features.

VSC7350-01 (eXEC1) Two-Port 10 GbE Aggregator VSC7350-01 is an advanced Ethernet aggregation device containing two 10 Gbps XAUI ports plus a SPI-4.2 host interface. It supports the conversion from XAUI to SPI-4.2 by transferring packets between each XAUI interface and up to 48 SPI-4.2 channels. This enables single platform development for seamless connectivity between Ethernet over SONET mappers, network processors, ASICs, and other Carrier Ethernet devices. The addition of VLAN-based aggregation in the MAC allows existing platforms to deliver all variations of EPL, EVPL, and E-LAN Metro Ethernet services over existing SONET/SDH networks.

The VSC7350-01 is software-compatible and pin-compatible with the existing Vitesse MAC product portfolio. The device also supports an enhancement to the standard XAUI interface in terms of channelization and granular flow-control.

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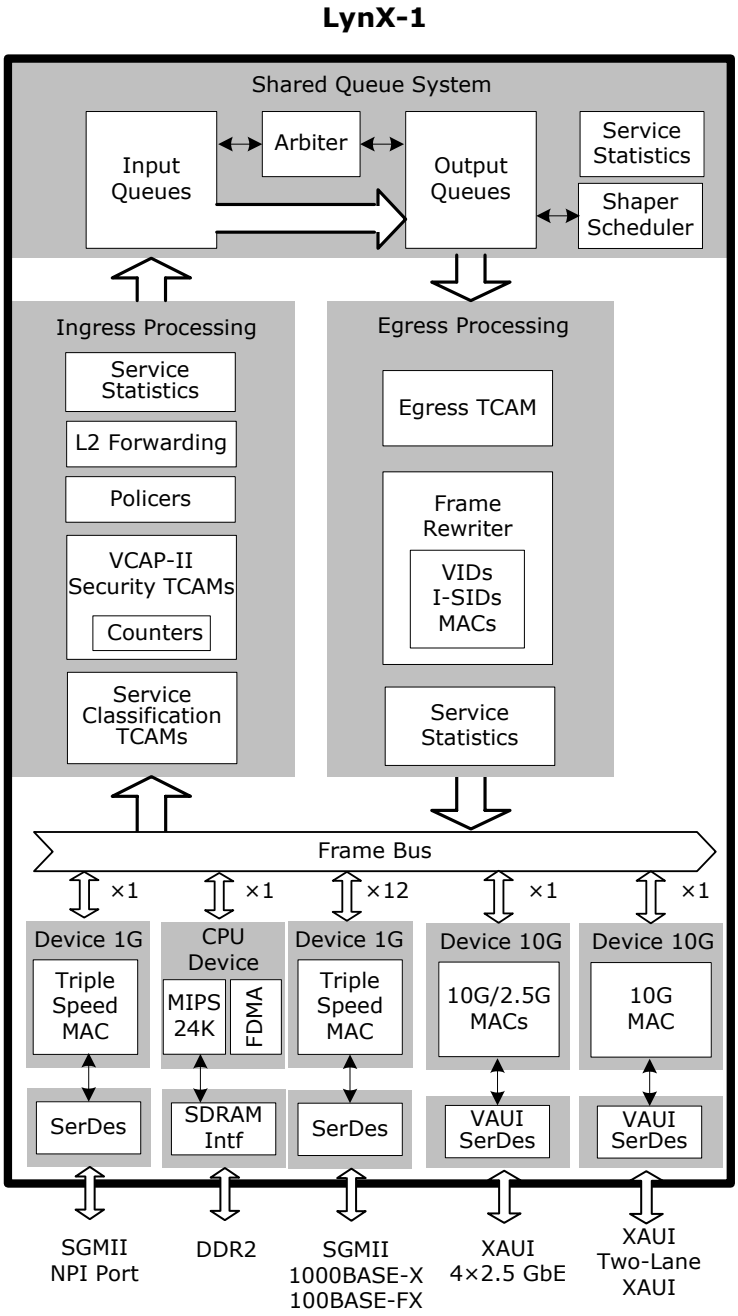
2.4 Frame Forwarding Walkthrough

Figure 3. Data Path Block Diagram



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2.4.1 Frame Arrival from Line Port

Both 10/100/1000 Mbps and 10 Gbps line ports are supported. The 10/100/1000 M ports use the DEVICE1G modules, and the 10G ports use the DEVICE10G modules.

DEVICE1G Line Ports

DEVICE1G line ports operate in one of the following modes:

- 10/100/1000 Mbps SGMII The SGMII interface connects to an external copper PHY device or a "copper SFP" optical module with SGMII interface. In this mode, autonegotiation is supported for link speed, duplex settings, pause settings, and remote fault signaling.

  Full-duplex is supported for all speeds, while half-duplex is supported for 10 Mbps and 100 Mbps. Full symmetric and asymmetric (unidirectional) pause flow control are both supported.

- 100BASE-FX The 100BASE-FX interface connects directly to 100BASE-FX SFP optical modules. Autonegotiation is not specified for 100BASE-FX and is not supported. Operation is always 100 Mbps and full duplex. Full symmetric and asymmetric (unidirectional) pause flow control are both supported.

- 1000BASE-X The 1000BASE-X interface connects directly to 1000BASE-X SFP optical modules. Autonegotiation is supported for pause settings and remote fault signaling. Operation is always 1000 Mbps and full duplex. Full symmetric and asymmetric (unidirectional) pause flow control are supported. 1G backplane Ethernet 1000BASE-KX is fully supported, including autonegotiation.

Each DEVICE1G contains a Media Access Controller (MAC) that performs a full suite of checks, such as VLAN Tag aware frame size checking, Frame Check Sequence (FCS) checking, and Pause frame identification.

DEVICE10G Line Ports

DEVICE10G line ports are standard 10 Gbps XAUI ports. The XAUI port connects directly to 10 GbE optical modules and to PHY devices with XAUI ports, as well as to switches and traffic management devices with XAUI ports.

Operation is always 10 Gbps and full duplex. Full symmetric and asymmetric (unidirectional) pause flow control are both supported. Remote fault signaling and local fault signaling are also supported.

When used with devices capable of WAN-PHY (10GBASE-W) operation, such as VSC8486, the DEVICE10G line ports support pacing mode as specified for 10GBASE-W operation.

Each DEVICE10G contains a Media Access Controller (MAC) that performs a full suite of checks, such as VLAN Tag aware frame size checking, Frame Check Sequence (FCS) checking, and Pause frame identification. Autonegotiation is supported for pause settings, remote fault signaling, and backplane Ethernet functions. 10GBASE-KX4 (four-lane backplane) and 10GBASE-CX4 (four-lane copper) are fully supported.

2.4.2 Ingress Frame Processing

This section discusses:

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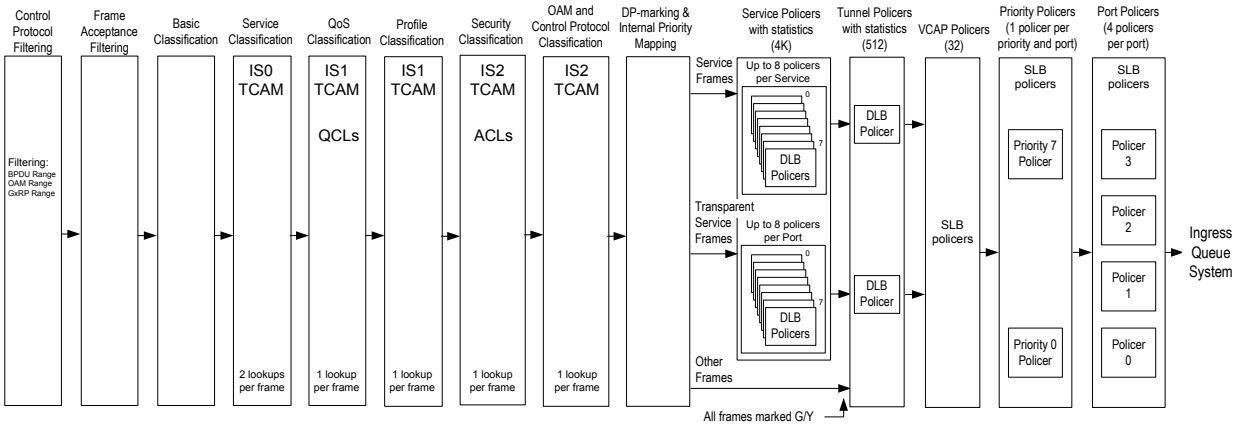
- Service and QoS Classification
- Profile Classification
- Security Classification
- OAM and Control Protocol Classification
- Drop precedence marking and Policing

The following illustration shows a generalized view of the ingress frame processing steps. Ingress frame processing is performed using a combination of configurable logic, TCAMs, and policing (metering) functions.

Figure 4. Ingress Frame Processing Flow



The following illustration shows how sophisticated QoS can be achieved using this flow.

Note terminology below

– Classified VLAN. The final internal VLAN used by all processing steps after classification including forwarding.

– Service VLAN. The VLAN returned by IS0 as part of a match. This may or may not become the Classified VLAN. The Service VLAN is only valid if IS0_VID_ENA is set.

– Basic VLAN. The VLAN returned by Basic Classification. This may or may not become the Classified VLAN. Note that a Basic VLAN is always assigned to every frame and becomes the Classified VLAN as the default processing option if no more-specific mapping is found.

– Profile VLAN. The VLAN returned by IS1 as part of a Profiling match. A valid Profile VLAN always becomes the Classified VLAN.

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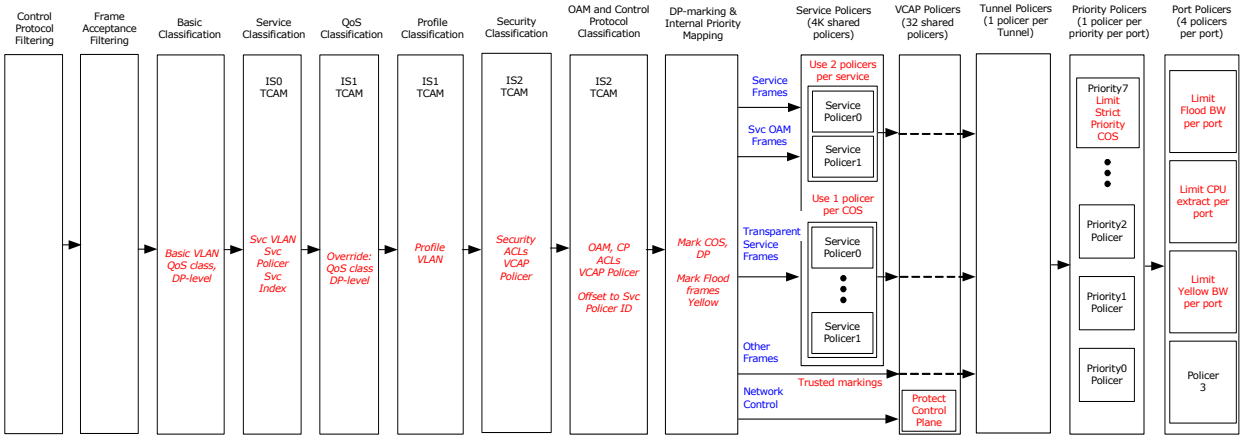
Figure 5. Example Configuration for Guaranteed SLA Delivery



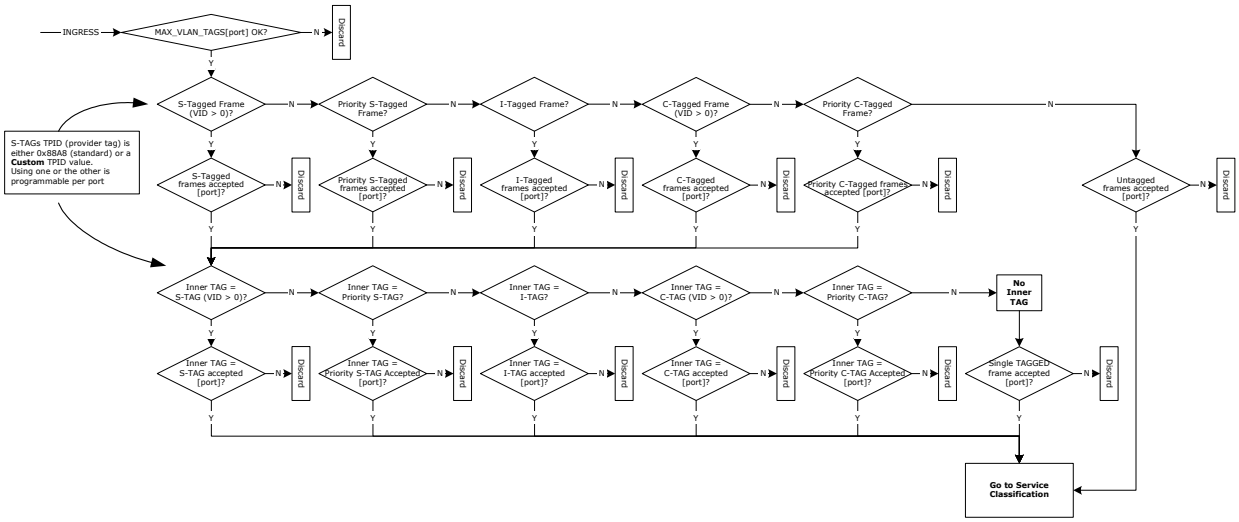
2.4.3 Control Protocol Filtering

To be added

2.4.4 Frame Acceptance VLAN Filtering

Basic VLAN filtering of acceptable frame types is shown in the following flow chart.

Figure 6. Acceptable Frame Types Filtering Flow Chart



2.4.5 Basic Classification

Every incoming frame is classified to a VLAN, QoS class, and drop precedence level (DP-level) in the Basic Classification after the frame has been accepted by the

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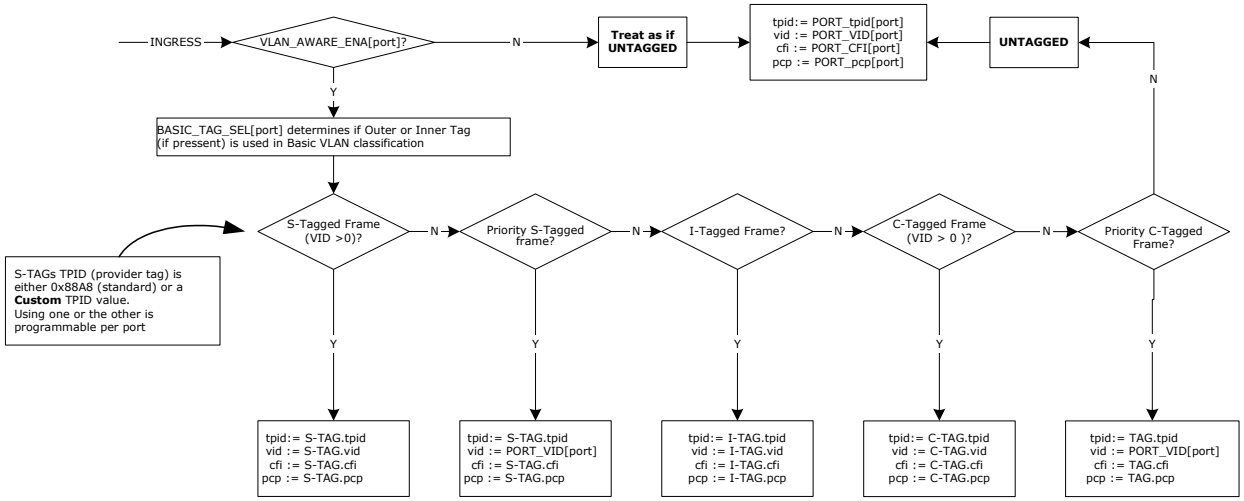
port-specific frame acceptance filtering. If a frame is untagged or otherwise not classified based on frame fields, a port default Basic VLAN, QoS class and DP-level is assigned to the frame. Basic Classification results may be overruled by more intelligent frame processing in the next step of the ingress service handling flow (IS0 and IS1).

Basic VLAN Classification

Basic VLAN Classification is shown in the following flow chart.

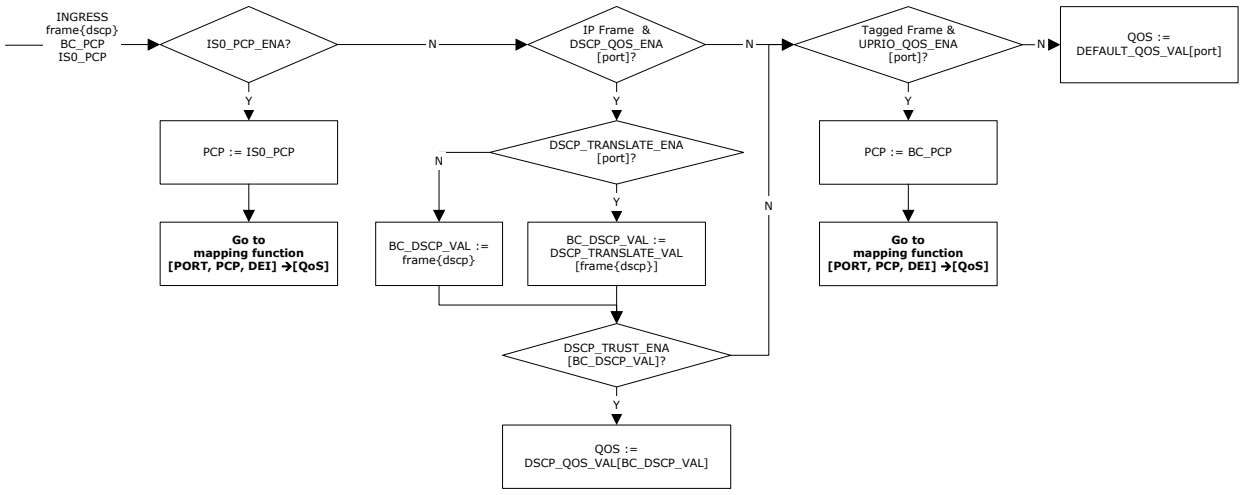
Figure 7. Basic VLAN Classification Flow Chart



Basic QoS Classification

Basic QoS Classification is shown in the following flow chart.

Figure 8. Basic QoS Classification Flow Chart



Basic DP-Level Classification

Basic drop precedence level classification is shown in the following flow chart.

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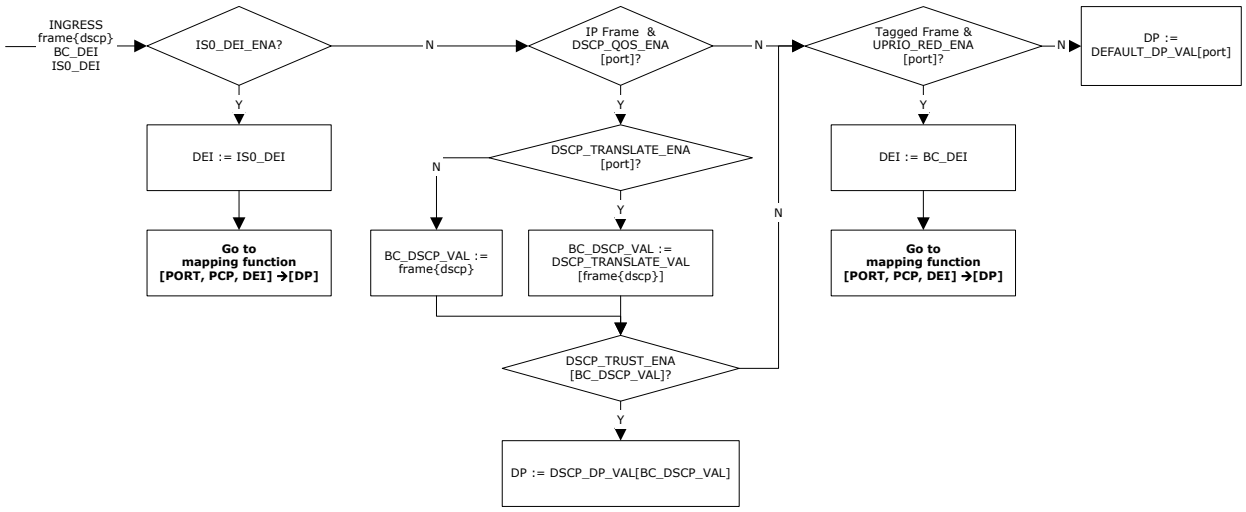
Figure 9. Basic Drop Precedence Classification Flow Chart



2.4.6 Service Classification

All incoming frames passes through the Service Classification TCAM (IS0 = Ingress Stage 0).

Preprocessing logic in front of the Service Classification TCAM determines if the frame must be matched against the content of IS0 or if the frame must bypass the Service Classification stage. The Service Classification preprocessing logic also generates the KEY used for the matching in IS0 if needed. The decision to use Service Classification or not depends on port specific configurations and frame specific parameters listed in the following:

If the arrival port of the frame is configured for host mode operation with host interface Header (HIH) enabled, certain parts of the IS0 KEY can be extracted from HIH fields. Four different modes of HIH operation exist for a port:

HM_CL_MODE = 00: A label switched mode where the logical port ID (LPID) field from the HIH is used directly to lookup the egress port(s) of the frame. The PCP and DE of the HIH are also used directly for QoS Classification. In this mode, Service Classification or L2 bridging is not performed. Port default values for Policy Association Group and ingress tag pop parameters are returned from the IS0 action RAM.

HM_CL_MODE = 01: A Service Classification mode where the HIH.LPID field from the HIH is used in the IS0 KEY generation as the arrival port information. Other parts of the KEY can be extracted from the frame itself (one or more VLAN tags).

HM_CL_MODE = 10: A Service Classification mode where the HIH.LPID, HIH.PCP, and HIH.DEI fields from the HIH are used in the IS0 KEY generation. Other parts of the KEY can be extracted from the frame itself (one or more VLAN tags).

HM_CL_MODE = 11: A mode where the host device has done the full Service Classification and provides a pointer to the Vitesse Service Classification database (IS0 action RAM) with all the attributes of the service. In this mode, the HIH.PCP and HIH.DEI values may be overwritten by the corresponding fields from the IS0 action

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database. In this mode, no Service Classification KEY is generated and no matching in the Service Classification TCAM is performed.

If the arrival port of the frame is not configured for host mode operation, the IS0 KEY can be generated from a variety of different frame fields as described in the following:

- Double VLAN-tagged frame and double tagged KEY generation is enabled for the port
- Single VLAN-tagged frame and single tagged KEY generation is enabled for the port
- Untagged frame
- MAC-in-MAC encapsulated frame and I-SID KEY generation is enabled for the port
- EoMPLS encapsulated frame KEY generation is enabled for the port
- Service Classification in the IS0 TCAM is enabled for the port (IS0_ENA). If disabled, port default values for Policy Association Group and ingress tag pop parameters are still returned from the IS0 action RAM.

The following flow chart illustrates Service Classification IS0 KEY generation hierarchy and Service Classification. Note that paths 0 through 2 bypass the IS0 Service Classification TCAM. Paths 1, 3, and 4 return service parameters from the IS0 service action RAM.

The result of Service Classification is mapping to an Arrival Service Point (ASP), which is indicated by an Ingress Service Index pointer (isdx_xxx_ptr).

For more information about the conceptual overview of services and service points, see "Service Concept," page 76.

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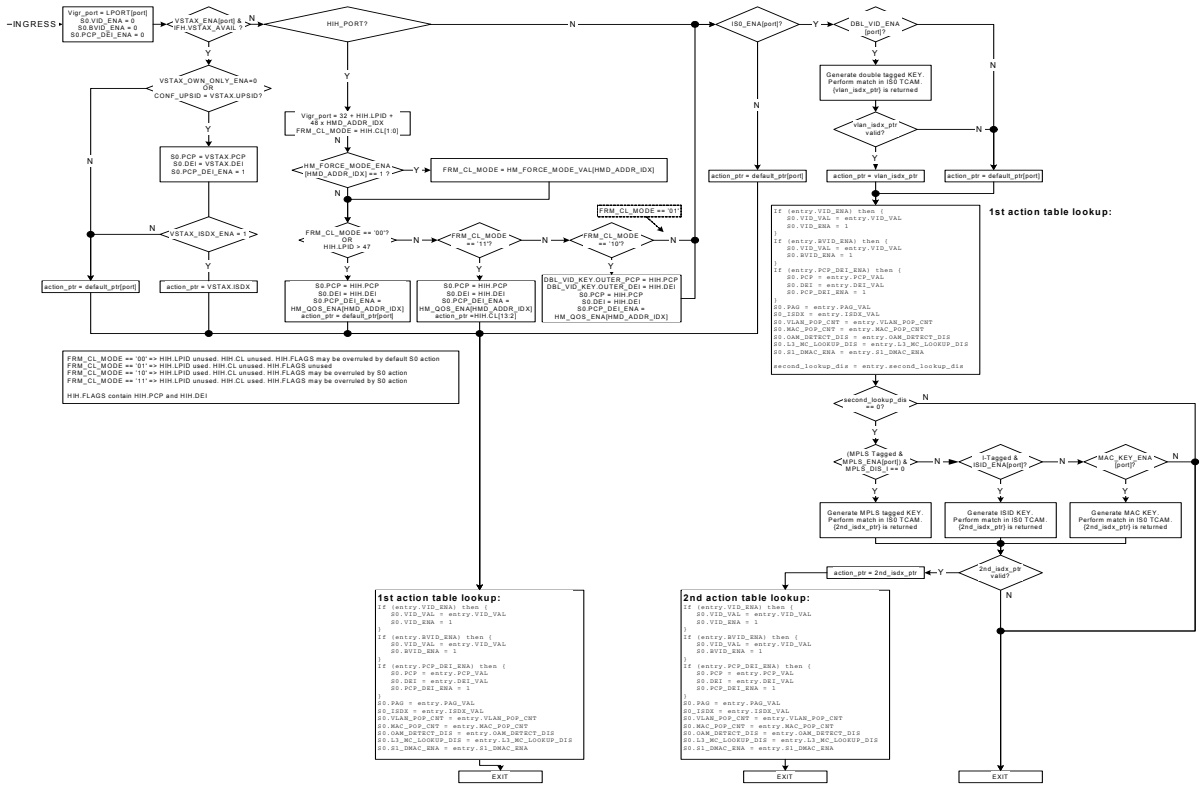
Figure 10. Service Classification Flow Chart



Service Classification by the Ingress Stage 0 (IS0) TCAM includes up to two matches. The first match is based on a set of frame fields [arrival port, outer VID, inner VID, PCP, DEI, DSCP] of the incoming frame. The second match is based on another set of frame fields [arrival port, I-SID, I-PCP, I-DEI] or [arrival port, Label1, EXP1, S1, Label2, EXP2, S2] of the incoming frame. I-SID is the frame's Provider Backbone Bridging (PBB) Backbone Service Instance Identifier of the I-Tag. I-PCP and I-DEI also come from the I-Tag. In the following, the first match in the IS0 TCAM is referred to as the "VLAN match" and the second match as the "I-SID match". For the I-SID match, the KEY can be alternatively configured per port to use the backbone VLAN QoS parameters as follows: [arrival port, I-SID, B-PCP, B-DEI].

Two different VLAN matches are possible for the VLAN match:

- If the incoming frame is double-tagged a double-tagged KEY is generated for the IS0 match.
- If the incoming frame is single-tagged or untagged a single-tagged KEY is generated for the IS0 match. If untagged the VID in the single tagged KEY is set to 0xFFF (don't care).

The VLAN match always returns a valid isdx_vlan_ptr. The IS0 TCAM includes a default rule per port for the VLAN match, which is always hit if none of the 4096 service rules are hit. The isdx_VLAN_ptr points to the frame's classified service of the VLAN match. The result of the VLAN match may be overruled by the I-SID match as explained below. The isdx_VLAN_ptr also points to the isid_lookup_dis parameter.

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If the frame is I-tagged, the I-SID match is enabled for the arrival port, the isid_lookup_dis parameter is false, and a valid isdx_isid_ptr is returned, the service of the frame becomes the service pointed to by the I-SID lookup. Otherwise the service is identified by the isdx_VLAN_ptr.

The purpose of the VLAN lookup gating function of the I-SID lookup (through the isid_lookup_dis parameter) is as follows:

Provider Bridging traffic, Provider Backbone Bridging traffic, and Provider Backbone Bridging - Traffic Engineering traffic may be mixed on network facing ports. PB/PBB traffic is kept isolated from PBB-TE traffic through the use of VIDs. That is, certain VIDs indicate only PB/PBB traffic whereas other VIDs indicate PBB-TE traffic. The VLAN match in the IS0 TCAM is used to determine if the frame belongs to a PBB/PBB-TE service VLAN. If so, the I-SID lookup is enabled and more service-specific classification of the frame is carried out.

The Service Classification result (either VLAN match or I-SID match) classifies the frame to one of the following three categories:

- A service frame. The service attributes are assigned to a service frame as a result of a service match in IS0.
- An L2 bridged frame (that may or may not require VLAN tag manipulations). Even though not being a service frame, an L2 bridged frame may still have a match in IS0. Reasons could be that VID push/pop/translate manipulations are needed or that the frame is part of a flow aggregate that is carried transparently through the CE switch. A flow aggregate can be supervised and upper bandwidth limited for network protection through assigning a set of statistics counters and a service policer to the flow aggregate.
- A frame that does not require per-service treatment, and that also does not require any VLAN tag translation. Frames belonging to this category get no Service Classification in IS0 (no match). These frames are forwarded as plain L2 bridge traffic based on classification results from Basic Classification and potentially Advanced QoS and Profile Classification (IS1).

Service Classification can also be used to assign VID translation, VLAN statistics, and VLAN policing capabilities for up to 4K VLANs of a provider network core bridge or provider backbone core bridge.

2.4.7 Shared TCAMs IS1 and IS2

Policy Association Group

An understanding of the Policy Association Group (PAG) is needed for the following sections. The PAG is the Policy Association Group to which each frame is classified. The PAG can be used to implement very efficient lists of rules in TCAM entries that are only relevant for frames that have been classified to a specific PAG value. PAG Classification is not constrained to “frames on a given port” or “frames on a given VLAN”, but is targeted at addressing all frames of a specific type requiring the same treatment and sharing a single (QOS, PROFILE, SECURITY, and/or OAM_CP) control list. Examples of frame types that can be grouped together using PAG values are VOIP and service OAM. The PAG value is used in the following TCAMs:

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- Default PAG Classification is done by the Service Classification (IS0).
  If the frame is not classified to a service, a default PAG value for the ingress port is returned from IS0.
- Advanced QoS Classification (IS1).
- Profile Classification (IS1). The PAG value can be modified by the Profile Classification for further specialized grouping of frames as input to Security and OAM_CP Classification in IS2.
- Security Classification (IS2)
- OAM and Control Protocol Classification (IS2)

IS1 and IS2 Lookups

The IS1 and IS2 TCAMs each allow for two lookups per frame. These four lookups are shared by different classification processes as follows:

- Advanced QoS Classification uses one lookup in the IS1 TCAM
- Profile Classification uses one lookup in the IS1 TCAM
- Security Classification uses one lookup in the IS2 TCAM
- OAM and Control Protocol Classification uses one lookup in the IS2 TCAM

Advanced QoS and Profile Classification TCAM (IS1)

The purpose of IS1 is exceptions handling where a variety of L2-L4 fields are used to provide Advanced QoS Classification and Profile Classification capabilities. A QoS, VLAN, DP, or DSCP value returned from IS1 in either of the lookups always becomes the final result for the frame.

Security and OAM_CP Classification TCAM (IS2)

IS2 allows line-speed frame inspection based on L2-L7 fields, including full bit mask and range capabilities. For Security Processing, the results of Profile Classification plus L2-L7 fields are used. For OAM and Control Protocol processing, typically L2-L4 fields are used to identify critical network control protocols and OAM frames.

2.4.8 QoS Class and DP-level Classification

Service Classification, Basic Classification, and Advanced QoS Classification all take part in the QoS and DP-level Classification, as shown in the following illustration.

Examples of the use of the Advanced QoS Classification are:

- QoS Classification based on specific DSCP values
- QoS Classification based on SMAC OUI or UDP port ranges to identify VOIP traffic needing preferential treatment

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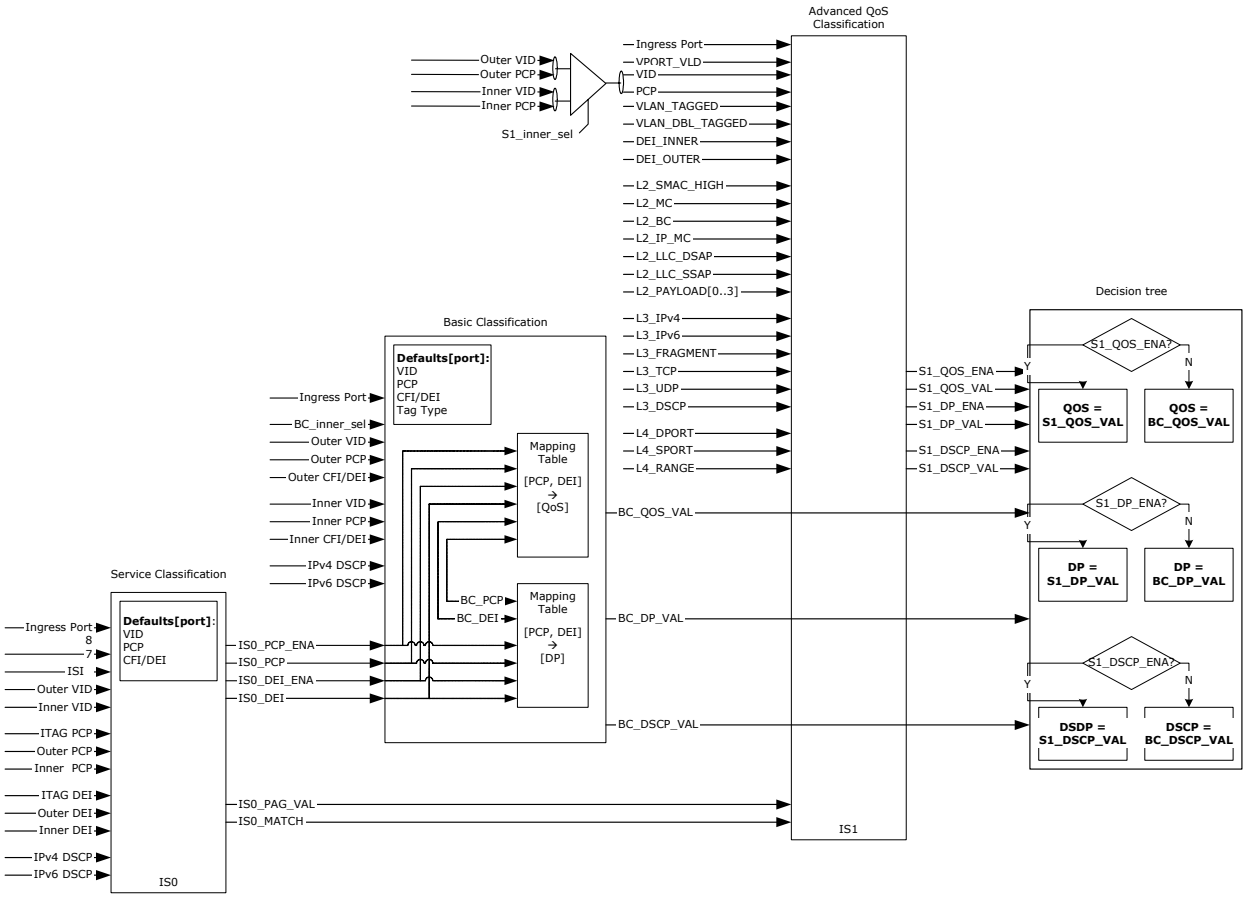
Figure 11. QoS Class and Drop Precedence Level Classification



IS0 may optionally return translated/normalized Priority Code Point (PCP) and Drop Eligibility Indication (DEI) values as a result of Service Classification. Normalized PCP, DEI values are needed on a per-port basis as input to Basic Classification for it to determine QoS class and DP-level values. QoS class and DP-level are the QoS parameters used globally within the device for queuing, arbitration, congestion handling, and scheduling.

Basic Classification performs plain L2 bridging/forwarding Classification of QoS and DP-level as described previously. If the service Classification returns valid PCP and/or DEI values, these are always used by Basic Classification for the mapping to QoS class and DP-level.

The Advanced QoS Classification performed in IS1 is targeted at handling exceptions from the general QoS and DP-level Classification model performed by Service Classification and Basic Classification. As shown in the previous illustration, many different L2-L4 fields of the frame are input to IS1. Together with the use of multiple QoS Control Entries (QCEs) in the IS1 TCAM, very advanced QoS Control Lists (QCLs) can be programmed. A valid QOS-class, DP-level, and/or a DSCP-value returned by the Advanced QoS Classification always becomes the final decision for the frame no matter the result of Service Classification and Basic Classification. The Advanced QoS Classification uses one lookup in IS1.

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Mapping [PCP, DEI] to [QoS class, DP-level]

PCP, DEI are frame field names of an S-tagged frame.

The IEEE802.1AD-2005 standard specifies how the drop_eligible parameter can be encoded in the PCP field of VLAN tagged frames with or without the use of the DEI bit. Both of these modes are supported by different configuration of per port classification tables from [PCP, DEI] to [QoS class, DP-level].

In the following classification tables, the internal priority is shown with the default mapping from QoS class to internal priority to justify the DP marking. Within each internal priority all four DP-levels are present to enable full four-level WRED within the Shared Queuing System (SQS).

The Basic Classification of DP-levels shown in the table is based on the assumption that DP-levels [00, 01] represent Green and DP-levels [10, 11] represent Yellow. Different encoding of Green and Yellow DP-levels requires a different mapping in the table.

The following table shows classification (decoding) of [PCP, DEI] to [QoS class, DP-level] for the {8P0D, Use_DEI = TRUE} mode in the IEEE802.1AD-2005 standard.

Table 4. PCP Encoding Example 1

PCP Bits (3 bits)	DEI (1 bit)	Internal QoS (3 bit)	Internal DP-level (2 bit)	Internal Priority (2-bit)
000	0	000	01	00
000	1	000	11	00
001	0	001	00	00
001	1	001	10	00
010	0	010	01	01
010	1	010	11	01
011	0	011	00	01
011	1	011	10	01
100	0	100	01	10
100	1	100	11	10
101	0	101	00	10
101	1	101	10	10
110	0	110	01	11
110	1	110	11	11
111	0	111	00	11
111	1	111	10	11

The following table shows classification (decoding) of [PCP, DEI] to [QoS class, DP-level] for the {6P2D, Use_DEI = FALSE} mode in the IEEE802.1AD-2005 standard.

Table 5. PCP Encoding Example 2

PCP bits (3 bits)	CFI (1 bit)	Internal QoS (3 bit)	Internal DP-level (2 bit)	Internal Priority (2 bit)
000	0	000	00	00
000	1	000	00	00

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Table 5. PCP Encoding Example 2 *(continued)*

PCP bits (3 bits)	CFI (1 bit)	Internal QoS (3 bit)	Internal DP-level (2 bit)	Internal Priority (2 bit)
001	0	001	00	00
001	1	001	00	00
010	0	010	10	01
010	1	010	10	01
011	0	010	00	01
011	1	010	00	01
100	0	100	10	10
100	1	100	10	10
101	0	100	00	10
101	1	100	00	10
110	0	110	00	11
110	1	110	00	11
111	0	111	00	11
111	1	111	00	11

[DSCP] to [QoS class, DP-level] Mapping

Basic mapping of DSCP values to QoS Class and DP-level is described in the Basic Classification section. The Advanced QoS Classification in IS1 takes the DSCP value as input and thereby provides enhanced DSCP-based QOS and DP-level Classification capabilities as shown earlier in this section.

2.4.9 VLAN Classification

TBD

2.4.10 Security Classification

The Vitesse Content Aware Processor (VCAP-II) is a TCAM-based processing engine enabling delivery of a rich set of security features. VCAP-II supports line-speed frame inspection based on L2-L7 fields, including full bit mask and range capabilities.

TBD: Examples of the use of the IS1 Profile Classification lookup:

- PAG Classification based on SMAC OUI or UDP port ranges for VOIP traffic
- Protocol-based VLANs
- SMAC-based VLANs
- DMAC-based VLANs.
- SIP-based VLANs

ISDX_ADD_ENA and ISDX_VAL are returned from IS1 Profile Classification.

IS2 TCAM processing includes:

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- Discard
- Redirect to CPU or other ports
- Copy to CPU (snooping)
- Ability to trigger a Global VCAP policer
- Mirroring
- Learning

Additionally, each S2 entry counts the number of times the entry was hit.

2.4.11 OAM and Control Protocol Classification

OAM and Control Protocol Classification uses one lookup in the S2 TCAM to identify the protocol and determine the correct treatment to apply. The lookup uses L2-L4 fields as well as intelligent pre-processing of Ethernet OAM. CCM OAM is identified in this step and mapped to the appropriate CCM checking hardware. See the OAM and Protection Switching Concept in the Features section for an overview.

IS2 TCAM processing actions include:

- Discard
- Redirect to CPU or other ports
- Copy to CPU (snooping)
- Ability to trigger a global VCAP policer
- Mirroring
- Learning
- Mapping of Ethernet CCM OAM to the correct CCM OAM checking hardware

Additionally, each S2 entry counts the number of times the entry is hit.

2.4.12 Drop Precedence Marking

The VSC7462 devices support four levels of drop precedence. A frame's drop precedence level is used as input to the Weighted Random Early Detection (WRED) mechanism implemented in the Shared Queuing System. WRED is an active queue management mechanism that provides preferential treatment of higher priority frames when traffic builds up within a queue. A higher drop precedence level assigned to a frame results in a higher probability that the frame is discarded during times of congestion. Note that the WRED mechanism operates within a priority (queue) and not between priorities.

A global chip configuration defines the drop precedence levels that are considered Green (in profile) and Yellow (Discard-Eligible), respectively. The default configuration is DP-levels = [0,1] are Green and DP-levels = [2,3] are Yellow.

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The Basic Classification assigns a DP-level to a frame based on frame fields such as DSCP-value, PCP bits, and DEI bit. Alternatively, a port default DP-level is assigned to each frame. As part of the Service Classification, a service-specific default DP-level can be assigned to service frames if previous color marking must be overruled.

A specific DP value (DP_ADD_YELLOW) is configured for each service policer. If a frame is Green on arrival to the service policer and must be marked as Yellow on departure, the DP_ADD_YELLOW value is added to the DP-level of the incoming frame to generate the outgoing DP-level of the frame. Default is DP_ADD_YELLOW = 2.

The VSC7462 provides the optional ability to mark flooded frames as Discard-Eligible. This capability can be used in combination with the policer functions described below and the color-aware mechanisms in the Shared Queuing System to guarantee SLA delivery in situations with otherwise heavy flooding.

Discard-Eligible marking of flood traffic is enabled/disabled per port. The DP-level added to flooded frames (DP_ADD_FLOOD) is configurable per port.

All DP marking calculations saturate at DP-level=3. It is possible to use only two DP-levels, where DP = 0 indicates Green (CIR compliant) and DP = 3 indicates Yellow (EIR compliant).

2.4.13 QoS Class to Internal Priority Mapping

Frames getting through the ingress policing stages are enqueued in the Input Queue System (IQS). The IQS has four internal priorities (queues) per ingress port. The mapping from QoS class to internal priority is configurable. The default mapping is shown in the following table.

Table 6. QoS to Priority Default Mapping

QoS Class	Internal Priority
000	00
001	00
010	01
011	01
100	10
101	10
110	11
111	11

This mapping table is common for all ports. However, the mapping from each port or service into the internal QoS class is configurable using QoS Classification techniques as described previously.

2.4.14 Policing

Each frame is subject to five different policing operations, in the following order:

1. Service policers
2. Global VCAP-II policers

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3. Tunnel policers
4. Priority policers
5. Port policers

Service Policing

Service policers are MEF-compliant dual bucket policers supporting both color-blind and color-aware operation (configurable per service policer). For color-aware operation, coupling mode is configurable for each service policer.

These policers are used to ensure Service Level Agreement (SLA) compliance. The outcome of this policing operation is to mark each accepted frame as in-profile (Green) or out-of-profile (Yellow). Yellow frames are treated as excess or Discard-Eligible, while Green frames are committed. Frames that exceed the Yellow/Excess limits are discarded (Red).

The ASP of a frame points to the service policer used for the service. The frame may however be redirected to another service policer by OAM and Control Protocol Classification, based on the frame protocol. It is possible to point to up to eight service policers from each ASP, however, any given frame is only subject to one service policer.

An example of using two service policers is to police service OAM traffic separately from other traffic within a service.

Service policers can also be assigned to protect the network when transparent services are carried through the Switch or MAC. That is, some traffic may already have been policed and color marked according to SLAs before entering the VSC7462 device. Such traffic may be carried transparently using dedicated VLANs on a given port. Service policers may be assigned to these VLANs (or aggregate of VLANs) to guarantee that failure of other equipment or misconfigurations do not impact other services or traffic.

Service policers can also be used to constrain non-service traffic within each port individually. For example, non-service traffic is plain L2 bridged traffic carried on specific VLANs on specific ports and must be constrained in order to not impact other service traffic. Note that this use of service policers does not require allocation of an ASP, but only a service policer index.

There are a total of 4K service policers.

Service policers provide service statistics according to each ASP, and not according to each policer.

Global VCAP-II Policing

Global VCAP-II policers are single bucket policers. An action of a match in the IS2 TCAM may be a pointer to the Global VCAP-II policer the frame must go through. Multiple entries in the IS2 TCAM may point to the same Global VCAP-II policer. Sharing of Global VCAP-II policers is controlled by the use of a portmask filter and Policy Access Group filter for each IS2 TCAM entry.

Whereas the service policers are targeted at per service policing and policing of traffic within each port individually, these Global VCAP-II policers are used to limit certain types of frames independent of arrival port, such as control frames sent to the local CPU system. The outcome of this policing operation is to pass or drop each frame.

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Each Global VCAP-II policer can be configured to only meter frames marked Discard-Eligible or all frames, regardless of marking.

There are 32 global VCAP-II policers. Global VCAP-II policers can operate in bits per second or frames per second.

Each frame is subject to only one global VCAP-II policer.

Tunnel Policing

Tunnel policers are MEF-compliant dual bucket policers supporting both color-blind and color-aware operation (configurable per tunnel policer). For color-aware operation, coupling mode is configurable for each tunnel policer.

These policers are used for traffic-engineered tunnels. The outcome of this policing operation is to mark each accepted frame as in-profile (Green) or out-of-profile (Yellow). Yellow frames are treated as excess or Discard-Eligible, while Green frames are committed. Frames that exceed the Yellow/Excess limits are discarded (Red).

The ASP of a frame points to the tunnel policer used for the service.

There are a total of 512 tunnel policers.

Tunnel policers provide tunnel statistics according to each tunnel, and not according to each ASP.

Ingress Queue Policing

Ingress queue policers are single bucket policers that are used to limit the frames going to each input queue. The outcome of this policing operation is to pass or drop each frame.

Ingress queue policers can be configured to only meter frames marked Discard-Eligible or all frames regardless of marking.

There are eight input queue policers dedicated to each port. Input queue policers can operate in bits per second or frames per second.

Each frame is subject to only one ingress queue policer.

Port Policing

Port policers are single-leaky bucket policers used to limit certain types of frames arriving from each port. The outcome of this policing operation is to pass or drop each frame.

Port policers can be configured to only meter frames marked Discard-Eligible or all frames regardless of marking. Each port policer can be configured to meter any of the following frame types:

- All traffic (but still modified by DE if that option is enabled)
- Unicast
- Multicast
- Broadcast
- Frames to be extracted to the local CPU system

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- Frames to be flooded

There are four port policers dedicated to each port. Port policers can operate in bits per second or frames per second.

Each frame is subject to all four port policers in parallel.

2.4.15 Layer 2 Forwarding (Bridging)

L2 forwarding determines the destination port set of each frame. Possible destinations for a frame include any of the 1 GbE ports, 10 GbE ports, the internal CPU, or the external CPU (SGMII CPU interface).

The destination port set is based on many pieces of information, such as:

- Service Classification Point-to-point services (E-LINEs) only have two member ports whereas point-to-multipoint services (E-TREE) and multipoint-to-multipoint services (E-LANs) may have many member ports. Also per service tunneling parameters of slow protocol frames etc. impacts the frame forwarding decision.
- VLAN Classification VLAN-based forward filtering options include source port filtering, destination port filtering, VLAN mirroring, asymmetric VLANs, and so on.
- Security Classification The security decision made by the VCAP-II may, for example, redirect the frame to the CPU based on some abnormality detection filters.
- OAM Classification Some OAM frames may be terminated in the device and are not forwarded, whereas other OAM frames may be forwarded as any other data frames.
- MAC Address and MAC-in-MAC Encapsulation B-SA, B-DA, C-SA, C-DA lookups in the MAC tables determine if a frame is a learn frame, a flood frame, a multicast frame, or a unicast frame.
- Learning Certain customer-facing ports can be configured with secure learning enabled, where an incoming frame with unknown source MAC address is classified as a "learn frame" and is redirected to the CPU. The CPU performs the learning decision and also decides whether the frame is forwarded.

  Network-facing ports can have hardware-based learning enabled, where MAC addresses are automatically learned in each MAC table, and each frame is forwarded entirely by the hardware without involving the CPU.

  Learning can also be disabled, in which case it does not matter if the source MAC address is in the MAC table.
- Link Aggregation A frame targeted at a link aggregate is further processed to determine on which of the link aggregate member ports the frame must be forwarded.
- Mirroring Mirror probes may be set up in different places in the forwarding path for monitoring purposes. As part of a mirror, a copy of the frame is sent either to the CPU or to another port.

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2.4.16 Frame Departure to Line Port

Frames are scheduled from the port output queues using a Modified Deficit Weighted Round Robin (M-DWRR) scheduler. This scheduler allows any of the queues to be given strict priority and the remaining queues to be given a weight. Each port can also be shaped.

The egress TCAM is used to determine the egress-specific rewriting instructions to apply to each frame. Egress rewriting operations are organized as per-Service (or VLAN), per-port. Frames use [Departure Port, Classified_VLAN] or [Departure Port, ASP] as the lookup key into the TCAM. The lookup key is selectable per Classified_VLAN.

The Rewriter now applies the ingress rewriting instructions and the egress rewriting instructions to the frame.

- Ingress rewriting instructions can pop up to two tags and push up to one tag. Egress rewriting instructions can push up to two tags. Tag swapping consists of a pop followed by a push.
- Ingress and egress rewriting instructions together also specify MAC-in-MAC push/pop operations. Note that a frame may require a MAC-in-MAC push or pop operation on one set of ports with no MAC-in-MAC operation on remaining ports.
- Egress rewriting instructions specify which I-SID to push along with any MAC-in-MAC push operation.
- Egress rewriting instructions also specify any frame remarking to apply. This may take the form of Priority Code Point (PCP, or 802.1p bits) in a VLAN tag, PCP bits in the MAC-in-MAC I-Tag, or Provider Bridges Discard Eligible (DE) bit.

Ports can be configured to drop in a QoS-aware manner or to flow-control. Half-duplex and full-duplex flow control are generated to the line port based on that port's input queue fill levels.

2.4.17 IP Multicast

TBD

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3 Functional Descriptions

This section provides the functional aspects of the VSC7462 LynX-1 Carrier Access Switch device. The main configurations supported are:

- 12 × 1 Gbps + 2 × 10 Gbps + NPI
- 12 × 1 Gbps + 4 × 2.5 Gbps + 1 × 10 Gbps + NPI
- 8 × 1 Gbps + 8 × 2.5 Gbps + NPI

3.1 Layer 1 Timing

The following table shows the configuration registers that are related to Layer 1 timing.

Table 7. Layer 1 Timing Configuration Register Overview

Register_group::Register.field	Description	Replication	Detail
MACRO_CTRL::SYNC_ETH_CFG	Configuration of recovered clock output pins	1	TBD
MACRO_CTRL::SERDES1G_ COMMON_CFG	Recovered clock selection 1G Macro	Per 1G Macro (21)	TBD
MACRO_CTRL::SERDES6G_ COMMON_CFG	Recovered clock selection 6G Macro	Per 6G Macro (16)	TBD

Two timing sources can be derived from the incoming data stream on any combination of two ports of the VSC7462 device, which are controlled by registers SERDES1G_COMMON_CFG.RECO_SEL_A, SERDES1G_COMMON_CFG.RECO_SEL_B, SERDES6G_COMMON_CFG.RECO_SEL_A, and SERDES6G_COMMON_CFG.RECO_SEL_B. These timing sources are provided to external timing circuitry on output pins RCVRD_CLK[1:0] for redundant timing implementations as configured by MACRO_CTRL::SYNC_ETH_CFG. If timing is compromised on either of the two sources, the appropriate clock output can be squelched to assist with fast timing switchover in the external clock synchronization circuitry. SERDES1G_COMMON_CFG.SE_AUTO_SQUELCH_A_ENA and SERDES1G_COMMON_CFG.SE_AUTO_SQUELCH_B_ENA control 1G macros squelching. Similar registers exist for 6G macros.

The clock frequency provided on the reference clock outputs can be divided down through registers MACRO_CTRL::SYNC_ETH_CFG.SEL_RECO_CLK_A and MACRO_CTRL::SYNC_ETH_CFG.SEL_RECO_CLK_B.

The following table shows the supported output clock frequencies.

Table 8. Recovered Clock Output Frequencies

Sourcing Macro/Data Rate	Recovered Clock Output Frequency
1G macro Data rate: 10/100/1000 Mbps	125 MHz, 31.25 MHz, or 25 MHz
6G macro Data rate: 10/100/1000 Mbps (one lane)	125 MHz, 31.25 MHz, or 25 MHz
6G macro Data rate: 10 Gbps (four lanes), 2.5 Gbps (one lane)	78.125 MHz or 62.5 MHz

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Table 8. Recovered Clock Output Frequencies *(continued)*

Sourcing Macro/Data Rate	Recovered Clock Output Frequency
6G macro Data rate: 12 Gbps (four lanes)	93.75 MHz or 75 MHz

3.2 Layer 2 Hardware Timestamping

Hardware timestamping provides nanosecond-accurate frame arrival and departure timestamps, which are used to obtain high precision timing synchronization and timing distribution, as well as much better accuracy in performance monitoring measurements than what is obtained from pure software implementations. For information about hardware timestamping as part of an IEEE 1588v2 implementation, see "IEEE 1588 Operation," page 95.

Arriving frames are Rx timestamped with a 32-bit timestamp value using a hardware timer (timestamper), which is implemented in the Media Access Control (MAC). The Rx timestamper provides high timestamp accuracy relative to actual arrival time of the first byte of the frame from the PHY device. Within the Analyzer block it is decided if the frame and associated Rx timestamp must be redirected or copied to CPU for processing. Otherwise the frame is forwarded as normal.

The Analyzer block also determines if a departure timestamp must be triggered for a frame and which of three Tx timestampers per destination port to use for storing the timestamp information. Tx timestampers are located at the transmit side of the MAC block as close to the PHY device as possible and provide high accuracy of timestamp relative to when the first byte of the frame is actually transmitted to the PHY.

3.2.1 Frame Classification

Frames requiring Rx or Tx timestamping are identified by IS2 TCAM ACEs and associated actions. The IS2 actions that triggers timestamping are OAM_RX_TIMESTAMP_ENA and OAM_TX_TIMESTAMP_SEL.

TBD: Must define how to present VCAP ACEs and actions!

IS2 TCAM ACEs can be configured to identify the following frame formats from the IEEE 1588v2 standard:

- Transport of PTP over User Datagram Protocol over Internet Protocol Version 4
- Transport of PTP over User Datagram Protocol over Internet Protocol Version 6
- Transport of PTP over IEEE 802.3/Ethernet

For more information about IEEE 1588 support, see "IEEE 1588 Operation," page 95.

Hardware timestamping can also be used as part of performance monitoring, such as those functions defined by the ITU-T Y.1731 standard. Two examples are delay measurements and delay variation measurements.

The frame formats defined by this standard are supported. Section YYY in Features chapter explains how OAM performance monitoring functions benefits from the hardware timestamping capabilities of the device.

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For information about the frame encapsulations supported within which PTP protocol frames and ITU-T Y.1731 protocol frames can be identified within the VSC7462 device, see XXX.

3.2.2 Master Timer

The Master Timer reflects the current time of day as determined by the IEEE 1588v2 protocol. It is loaded either externally or from software and regularly adjusted by software according to the IEEE_1588v2 algorithms.

The Master Timer generates the pulse that synchronizes all Rx and Tx timestampers together. The Master Timer is located in the CPU system block, and the timestampers are located in the MAC block of all ports.

The Master Timer block also provides synchronization pulse output and a reference clock output derived from the master timer. The master timer synchronization pulse can be controlled from an external pin.

The registers listed in the following table are used for controlling and monitoring the Master Timer.

Table 9. Master Timer Register Overview

Register_group::Register.field	Description	Replication	Detail
DEVCPU_GCB::PTP_MISC_CFG	GPIO configuration of hardware timer	1	TBD
DEVCPU_GCB::PTP_UPPER_LIMIT_CFG	Master counter configuration	1	TBD
DEVCPU_GCB::PTP_UPPER_LIMIT_1_TIME_ADJ_CFG	Master counter configuration	1	TBD
DEVCPU_GCB::GEN_EXT_CLK_HIGH_PERIOD_CFG	External clock output configuration	1	TBD
DEVCPU_GCB::GEN_EXT_CLK_LOW_PERIOD_CFG	External clock output configuration	1	TBD
DEVCPU_GCB::GEN_EXT_CLK_CFG	External clock output configuration	1	TBD
DEVCPU_GCB::CLK_ADJ_CFG	Master counter adjustment configuration	1	TBD
DEVCPU_GCB::PTP_SYNC_INTR_ENA_CFG	Interrupts control	1	TBD
DEVCPU_GCB::PTP_CURRENT_TIME_STAT	Master counter statistics. Current count value	1	TBD
DEVCPU_GCB::EXT_SYNC_CURRENT_TIME_STAT	Master counter statistics. Master counter value on last external synchronization pulse input	1	TBD
DEVCPU_GCB::PTP_EVT_STAT	Master timer event statistics	1	TBD

The following illustration shows the block diagram of the Master Timer.

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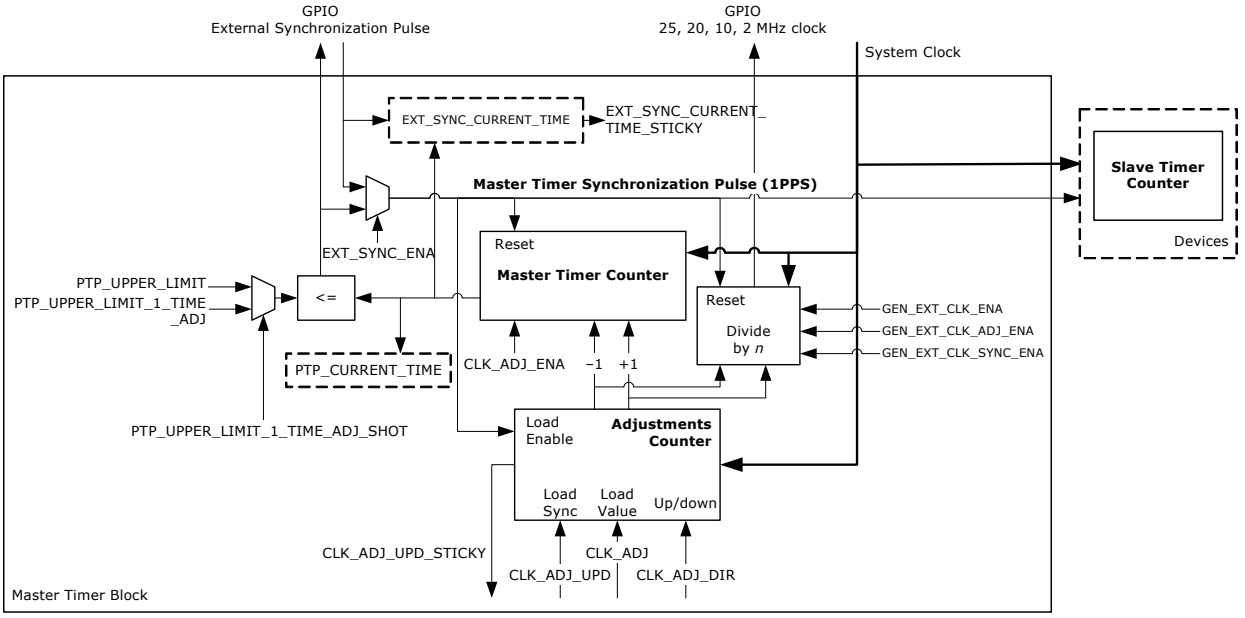
Figure 12. Master Timer Block Diagram



DEVCPU_GCB::PTP_MISC_CFG.PTP_ENA enables the Master Timer block and must be set for Master Timer Synchronization Pulse generation.

The master timer synchronization pulse is generated internally by default, with a frequency of one pulse per second (1 PPS). Other master timer synchronization pulse frequencies are obtained using register DEVCPU_GCB::PTP_UPPER_LIMIT_CFG. Every time a Master Timer Synchronization Pulse is generated towards the Slave Timers, a sticky bit is set (DEVCPU_GCB::PTP_EVT_STAT.SYNC_STAT) and an interrupt is generated if DEVCPU_GCB::PTP_SYNC_INTR_ENA_CFG.SYNC_STAT_ENA is enabled.

If a one-time correction to the master timer synchronization pulse is required, the correction time value must be written into register DEVCPU_GCB::PTP_UPPER_LIMIT_1_TIME_ADJ_CFG.PTP_UPPER_LIMIT_1_TIME_ADJ and one shot is enabled in register DEVCPU_GCB::PTP_UPPER_LIMIT_1_TIME_ADJ_CFG.PTP_UPPER_LIMIT_1_TIME_SDJ_SHOT.

Master Timer Counter Adjustments

Timing software running on internal or external CPU can control the master timer by issuing counter corrections to the Master Timer Counter. Master Timer Counter corrections are enabled in register DEVCPU_GCB::CLK_ADJ_CFG.CLK_ADJ_ENA.

Corrections to the Master Timer counter are controlled by the Adjustments Counter. The Adjustments Counter issues ±1 tick corrections to the Master Timer Counter, where one tick is equal to one system clock period. The time period between Master Timer corrections is determined by the load value of the Adjustments Counter. Time periods between corrections range from nanoseconds to one second.

The Adjustments Counter operates as follows: When the counter value of the Adjustments Counter equals the load value (DEVCPU_GCB::CLK_ADJ_CFG.CLK_ADJ), a one tick correction is generated. Up or down correction is determined by

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DEVCPU_GCB::CLK_ADJ_CFG.CLK_ADJ_DIR. It is determined through register DEVCPU_GCB::CLK_ADJ_CFG.CLK_ADJ_UPD whether a load value change takes immediate effect or whether it is synchronized to the next Master Timer Synchronization Pulse. When the load value change occurs, a sticky bit is set (DEVCPU_GCB::PTP_EVT_STAT.CLK_ADJ_UPD_STICKY). This sticky does not gate future updates to the load value; it is informative only. The Adjustment Counter is reset by loading all zeros.

External Synchronization Pulse Input

A Synchronization pulse can be provided as an input to the device. This is controlled through register DEVCPU_GCB::PTP_MISC_CFG. When this input is used to control the Master Timer Synchronization Pulse, the register DEVCPU_GCB::PTP_MISC_CFG.EXT_SYNC_ENA must be set. Also, if set the Master Timer Counter is reset by the External Synchronization Pulse.

Every time an external synchronization pulse arrives, the Master Timer counter value is captured in register DEVCPU_GCB::EXT_SYNC_CURRENT_TIME_STAT and DEVCPU_GCB::PTP_EVT_STAT.EXT_SYNC_CURRENT_TIME_STICKY is set. If DEVCPU_GCB::PTP_SYNC_INTR_ENA_CFG.EXT_SYNC_CURRENT_TIME_ENA is set, an interrupt is generated when an external synchronization pulse is received.

Because EXT_SYNC_CURRENT_TIME_STAT is updated, even when EXT_SYNC_ENA is cleared, a software function can be implemented that monitors the difference between internally controlled master clock and an external timing reference. That is, differences in counter values provided in register EXT_SYNC_CURRENT_TIME_STAT is an indication of the frequency difference between the master clock frequency and the clock frequency of the external synchronization pulse input.

Master Timer Synchronization Pulse Output

The Master Timer Synchronization Pulse can be provided as an output to the device. This is controlled through register DEVCPU_GCB::PTP_MISC_CFG.

Divide by *X* External Clock

A "divide by *X*" version of the Master Timer frequency can be provided as an output from the VSC7462 device. External clock frequencies up to 25 MHz are supported. The default clock frequency is 10 kHz.

The frequency and duty cycle of the external clock is controlled by registers DEVCPU_GCB::GEN_EXT_CLK_HIGH_PERIOD_CFG and DEVCPU_GCB::GEN_EXT_CLK_LOW_PERIOD_CFG. The "divide by *X*" counter implements a high period and a low period of the external clock based on these register values. The clock period of the external clock is calculated as (GEN_EXT_CLK_HIGH_PERIOD_CFG+GEN_EXT_CLK_LOW_PERIOD_CFG) × one core clock period.

The duty cycle of the external clock is 50%/50% only if GEN_EXT_CLK_HIGH_PERIOD_CFG and GEN_EXT_CLK_LOW_PERIOD_CFG are configured to the same value.

Register DEVCPU_GCB::GEN_EXT_CLK_CFG.GEN_EXT_CLK_SYNC_ENA controls whether the "divide by *X*" counter controlling the external clock shall be synchronized to the master timer synchronization pulse.

Register DEVCPU_GCB::GEN_EXT_CLK_CFG.GEN_EXT_CLK_ADJ_ENA controls whether the "divide by *X*" counter controlling the external clock is corrected by counter

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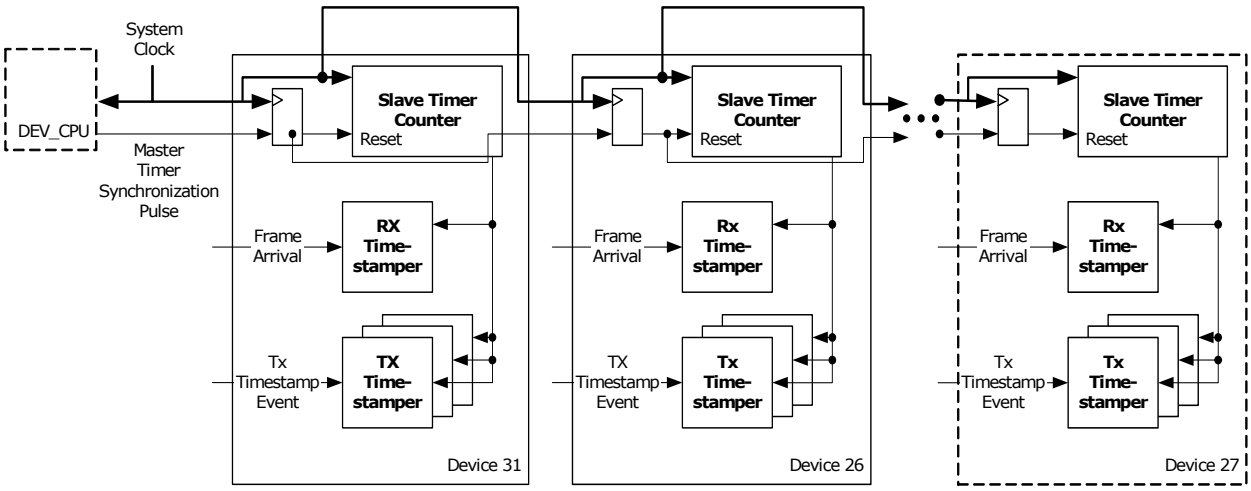
adjustments made to the Master Timer counter. If this register is enabled, the two counters are locked to each other. If this register is disabled, the counter is free-running of the system clock.

"Divide by *X*" counter adjustments show up directly on the external clock (unfiltered).

3.2.3 Slave Timer

A slave timer is located in each DEVICE1G and DEVICE10G. The slave timer provides the timing used for Rx and Tx timestamping and performs the actual timestamping of frames on arrival and departure. The following illustration shows pipelining being used to synchronize all slave timer to the master timer synchronization pulse.

Figure 13. Slave Timer



The following table shows the offset of a Slave Timer with a specific device, relative to the Master Timer. Offset is measured by the number of system clock ticks. For example, the Slave Timer in device 18 is twelve system-clock ticks off, relative to the Master Timer.

Table 10. Per Device Slave Timer Offset Relative To Master Timer

Device Number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Offset	*13*	*18*	*19*	*24*	*25*	*30*	*14*	*17*	*20*	*23*	*26*	*29*	*15*	*16*	*21*	*22*
Device Number	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Offset	*27*	*28*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*34*	*31*	*33*	*32*	*3*

The following table provides an overview of the Slave Timer Configuration registers.

Table 11. Slave Timer Configuration Registers

Register_group::Register.field	Description	Replication	Details
DEV[n]::DEV_PTP_CFG	Timestamping configuration	Per port	TBD

DEV[n]::DEV_PTP_CFG.PTP_ENA enables the slave timer and must be set to obtain Rx and/or Tx timestamping.

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Direct counter adjustments to a Slave Timer is not possible, therefore software must maintain a history of corrections made to the master timer from when the last Master Timer Synchronization Pulse was generated and compensate accordingly per slave timer to obtain highest accuracy timestamps.

Rx Timestamping

When the MAC block determines a new frame has arrived, the Rx timestamper generates a timestamp, which follows the frame all the way to the analyzer block. It is then determined if the frame and Rx timestamp must be copied or redirected to CPU. For more information, see "Frame Classification," page 51.

There are three frame format options for providing the Rx timestamp value inband with an Ethernet frame to the CPU:

- Overwriting the frame's FCS field with the Rx timestamp value. The frame length is unchanged. This frame format is proprietary and performing FCS checks on these frames will fail. This option must be used when copying the frame to CPU (with Rx timestamp written to frame's FCS field) while the original frame is forwarded as normal (with correct FCS). OAM_RX_TSTAMP_IN_FCS_ENA is enabled and OAM_RX_TSTAMP_FRM_EXTEND_ENA is disabled.
- Adding the timestamp value as a four-byte frame extension after the frame's FCS field. FCS is not recalculated. In this mode, the original frame content is unchanged. The frame format is proprietary. This mode can be used while redirecting timestamped frames to CPU. OAM_RX_TSTAMP_IN_FCS_ENA disabled and OAM_RX_TSTAMP_FRM_EXTEND_ENA enabled.
- Adding the timestamp value as a four-byte frame extension just in front of the frame's FCS field (last four bytes of frame payload). FCS is recalculated to include the timestamp value so the frame is changed from its original. The frame format is a standard Ethernet frame, but includes proprietary information. This mode can be used while redirecting timestamped frames to CPU. OAM_RX_TSTAMP_IN_FCS_ENA enabled and OAM_RX_TSTAMP_FRM_EXTEND_ENA enabled.

For the second and third options, the frame length of the Ethernet Frame on the wire when received must be less than 132 bytes to redirect/copy Rx Timestamp to the CPU. There is no frame size limit for the first option.

The registers in the following table select the frame format options.

Table 12. Rx Timestamp to CPU Configuration Registers

Register_group::Register.field	Description	Replication	Details
ANA_AC::MISC_CTRL.OAM_RX_TSTAMP_IN_FCS_ENA	Rx timestamp is written in location of FCS in original frame	1	TBD
ANA_AC::MISC_CTRL.OAM_RX_TSTAMP_FRM_EXTEND_ENA	Extend frame with 4 bytes to allow Rx Timestamp to be added without overwriting FCS	1	TBD

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The following table summarizes the frame formats supported to provide Rx timestamps to the CPU.

Table 13. Supported Frame Formats for Including Rx Timestamps

Feature	Timestamp Overwrites FCS	Timestamp Appended After FCS	Timestamp Inserted Before FCS
COPY to eternal CPU	Yes	No	No
REDIRECT to external CPU	Yes	Yes	Yes
COPY to internal CPU	Yes	No	No
REDIRECT to internal CPU	Yes	Yes	Yes
Arrival frame size limit	None	132 bytes	132 bytes
Extracted frame size	Same as arrival frame	Increased by 4 bytes	Increased by 4 bytes
FCS coverage	No FCS on frame; No FCS on timestamps	Original FCS on frame; No FCS on timestamp	FCS updated to cover frame and timestamp

Tx Timestamping

The analyzer determines which frames are Tx timestamped and which timestamper is used. For more information, see "Frame Classification," page 51.

The DEVICEs registers listed in the following table relate to Tx timestamping capabilities.

Table 14. Tx Timestamp Register Overview

Register_group::Register.field	Description	Replication	Details
DEV[n]::DEV_PTP_TX_STICKY	Tx timestamp events	3 per port	TBD
DEV[n]::DEV_PTP_TX_TSTAMP	Tx timestamp values	3 per port	TBD
DEV[n]::DEV_PTP_TX_ID	Tx timestamp identifications	3 per port	TBD
DEV[n]::DEV1G_INTR_CFG. PTP_UPDATE_INTR_ENA	Timestamping interrupt mask	Per port	TBD
DEV[n]::DEV1G_INTR. PTP_UPDATE_INTR_STICKY	Timestamping interrupt sticky bit	Per port	TBD
DEV[n]::DEV1G_INTR_IDENT. PTP_UPDATE_INTR_IDENT	Timestamping interrupt status	Per port	TBD

When Tx timestamping is performed the timestamp value is stored in register DEV_PTP_TX_TSTAMP and a sticky bit is set in DEV_PTP_TX_STICKY for the Tx timestamper being used. A Tx timestamper cannot be reused for timestamping later frames until the associated sticky bit has been cleared by software. A unique timestamp_ID for the frame is stored together with the timestamp in register DEV_PTP_TX_ID. The timestamp_ID is used by software to associate a timestamp with correct frame. The Tx timestamper functionality simplifies two-step clock applications where software must generate a follow-up message for Tx timestamp events.

An interrupt is triggered towards internal or external CPU when a sticky bit is set and if PTP_UPDATE_INTR_ENA is set. PTP_UPDATE_INTR_IDENT is the interrupt status signal.

Tx Timestamp Interrupt Control

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The registers listed in the following table control whether the Tx timestamp event triggers an interrupt towards the internal or the external CPU.

Table 15. Tx Timestamp Register Overview

Register_group::Register.field	Description	Replication	Details
ICPU_CFG::PTP_SYNC_INTR_CONFIG	Interrupt control	1	TBD

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4 Features

This section provides a feature-oriented description of how the VSC7462 device operates.

4.1 Device Configuration

This section describes the basic configuration of the VSC7462 device, identifies the interface types supported, and introduces fundamental forwarding capabilities of the device.

In this document, IEEE802.1 and Metro Ethernet Forum standards are used as a reference for the terminology and modeling, however, full compliance with precise definitions by these standards are not guaranteed. For more information about the standards for which the VSC7462 device claims compliance, see "Standard References," page 20.

Metro Ethernet Forum's Services and the service concept functions supported by the VSC7462 are described in following sections and can be seen as capabilities layered on top of the basic Layer 2 functionality discussed in this section. That is, the fundamental Switch functionality presented here is a prerequisite for what is presented in later sections.

4.1.1 Provider Bridge and Customer Bridge

VLAN-Unaware Bridge

VLAN-unaware Customer Bridge, as defined in IEEE802.1Q (*Virtual Bridged Local Area Networks*), is the most fundamental mode of the VSC7462 device. All traffic on arrival, whether VLAN-tagged, priority-tagged, or untagged, is treated as untagged within the device. All frames on arrival are classified to a port-based C-VLAN on which they are forwarded. By default all ports are members of all VLANs, so a port specific port-based C-VLAN can be configured for all ports without losing connectivity across the bridge. Tag manipulation is not performed on any frame in this mode.

VLAN-Aware Bridge

A VLAN-aware Customer Bridge, as defined in IEEE802.1Q, is also supported. Frames are bridged within a single customer network using C-VLANs for traffic separation. In this mode, VLAN-unaware equipment attached to the bridge is assigned a port-based C-VLAN on which the traffic is forwarded. Priority-tagged frames are also assigned the port-based C-VLAN. For VLAN-aware ports on the bridge the C-VLAN of arrival frames is used directly for forwarding. C-VLAN tags may be pushed and popped in this mode controlled on a per-port basis.

Provider Edge Bridge

Two types of provider bridges are defined in IEEE802.1ad (*Provider Bridges*): S-VLAN Bridge/Provider Bridge (PB) and Provider Edge Bridge (PEB). Both the Provider Bridge and the Provider Edge Bridge are supported by the VSC7462. The functionality of the Provider Edge Bridge is a superset of the S-VLAN bridge, because it supports customer-edge port interfaces.

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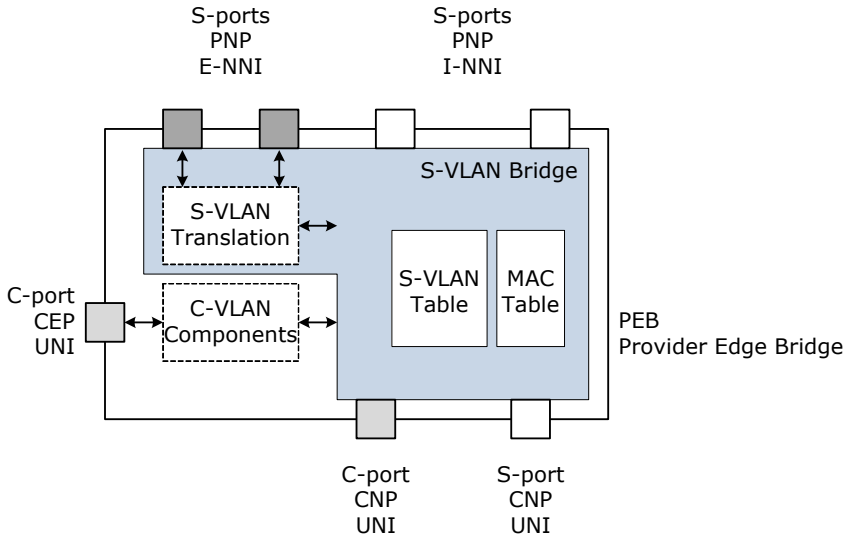
The following illustration depicts a model of the five interface types supported by a Provider Edge Bridge implemented using the VSC7462.

Figure 14. Simple Model of Provider Edge Bridge



- S-port I-NNI Provider Network Port (PNP) Interface. Ports configured as S-port I-NNI PNPs carry S-VLAN tagged traffic and are directly connected to the S-VLAN Bridge inside the Provider Edge Bridge. These ports connect directly to other equipment within the Service Provider's own network. The two outer most VLAN tags can be used by the VSC7462 in VLAN classification.

- S-port E-NNI Provider Network Port (PNP) Interface. Ports configured as S-port E-NNI PNPs carry S-VLAN tagged traffic and connect to the S-VLAN Bridge through a S-VLAN translation table. These ports connect equipment from another service provider. As shown in Figure 15, page 61, Provider A is peering with Provider C and S-VLAN translation may be required. Also, on another port, Provider A is a customer of Provider B where S-VLAN translation is normally not required. In both cases, the ports on PEB 1 are PNPs as they connect to another provider's network. The two outermost VLAN tags can be used in VLAN classification. The S-VLAN translation table performs 1:1 S-VLAN translations between the two providers VLAN spaces.

  The VSC7462 supports up to 4K S-VLAN to S-VLAN translations.

- S-port UNI Customer Network Port (CNP) Interface. Ports configured as S-port UNI CNPs carry S-VLAN tagged traffic. These ports connect to equipment from another service provider's network. As shown in Figure 15, page 61, Provider A is a customer of Network Provider B so Provider B's port facing Provider A is a UNI. Incoming frames are classified to Provider B's own VLAN space, a corresponding S-VLAN tag is pushed and used for forwarding within Provider B's network. The two outermost VLAN tags can be used in VLAN classification. In most cases, the S-VLAN tags of Provider A's network is carried as an inner tag through the provider network. Optionally, Provider A's tags can be removed while carried through Provider B's network. On egress, Provider B's own S-VLAN tag is removed again.

  The VSC7462 supports up to 4K S-VLAN classifications.

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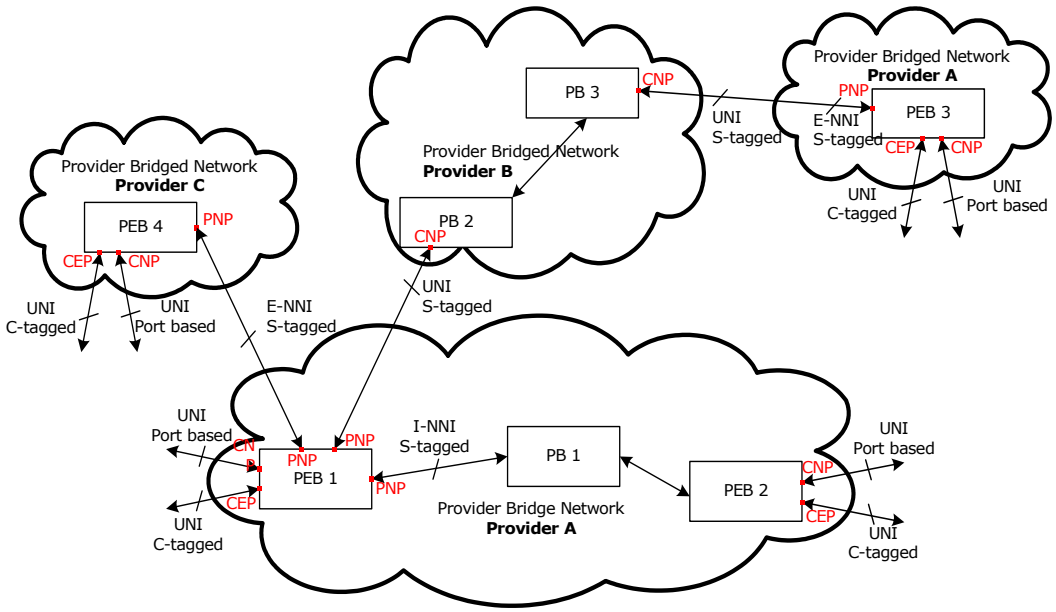
- C-port UNI Customer Network Port (CNP) Interface. A port-based service is provided to ports configured as UNI CNPs, and all customer traffic is classified to a port-based S-VLAN on which the traffic is forwarded within the S-VLAN bridge.
- C-port UNI Customer Edge Port (CEP) Interface. Ports configured as customer edge ports carry C-VLAN tagged, priority tagged, or untagged traffic and are connected to a C-VLAN component. The C-VLAN component classifies incoming traffic to an S-VLAN on which the traffic is forwarded within the S-VLAN bridge. The S-VLAN classification within the C-VLAN component can use the C-VID (if available) as part of S-VID selection. Within this S-VLAN classification, it is also decided if the C-VLAN is kept or removed from the frame before transmission through the provider bridge network. Each customer edge port is attached to its own C-VLAN component, providing independent S-VLAN classification. That is, two C-ports each receiving C-VLAN = 1 tagged frames may be classified to different S-VLANs for transmission through the provider network.

  The VSC7462 supports up to 4K S-VLAN classifications.

The following illustration demonstrates where each of these interfaces are located in a Provider Bridge Network. In this depiction, the connection between PEB 1 and PB 2 is a client-server relationship, where one carrier (Provider A) tunnels through another carrier (Provider B). At the UNI S-port on PB 2's CNP, a specific S-Tag for transmission through Provider B's network, is pushed/popped on top of Provider A S-Tags. The connection between PEB 1 and PB 1 is a peering relationship where both ends of the connection (I-NNI S-port PNPs) use the same S-VLAN IDs for all VLANs (no S-Tag translation). The connection between PEB 1 and PEB 4 is a peering relationship where the E-NNI S-port PNPs translate S-Tags.

Figure 15. Provider Bridge Network



The S-VLAN Bridge inside the Provider Edge Bridge includes a S-VLAN table and a MAC address table. The MAC address table contains Customer MAC addresses as well as Provider Network MAC addresses. All frames are forwarded within the Provider Edge Bridge based on classified S-VLAN. No traffic within a Provider Edge Bridge is forwarded

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based on C-VLAN tags. Even in the case where two ports of a Provider Edge Bridge are connected to equipment from the same customer the traffic between the two customer sites are forwarded within the Provider Edge Bridge using a S-VLAN of the provider network.
The VSC7462 supports 4K S-VLANs.

It is possible to push and/or pop any combination of up to two outermost C-VLAN tags or S-VLAN tags per frame within the Provider Edge Bridge. That is, the number of VLANs popped is an arrival port decision, whereas the number of VLANs pushed is decided independently for each departure port of the frame.

Note Supporting all three interface types described above on the same VSC7462 device and the ability to multicast / flood between them requires per egress port VLAN manipulation capabilities.

Up to 4K specific ingress VLAN and arrival port pop actions, and up to 4K specific egress VLAN and departure port push actions are supported.

Note The VLAN classification, and the VLAN push/pop functionality of the VSC7462 operates on the two outermost VLAN tags only. Frames with more than two VLAN tags are also supported; however, the third VLAN tag and below are not processed by the VSC7462.

In summary, the following interfaces are supported by a Provider Edge Bridge using:

- Port-based service
- C-Tagged service
- S-Tagged service

4.1.2 Provider Backbone Edge Bridge (B-BEB)

The following illustration shows a simplified model of a Provider Backbone Edge Bridge with a B-component (B-BEB) as supported by the VSC7462.

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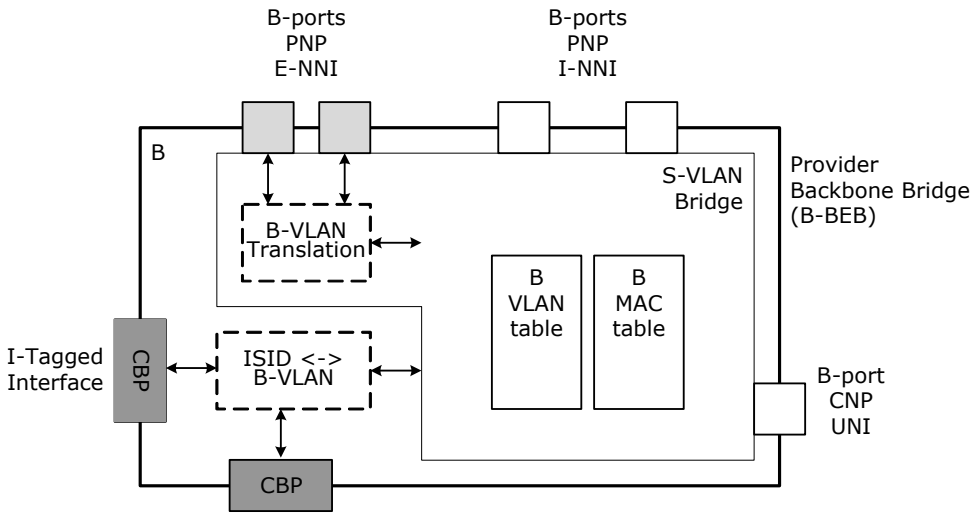
Figure 16. Simple Model of Provider Backbone Edge Bridge (B-BEB)



I-Tagged Interface

Four interface types are supported:

- **B-Port I-NNI Interfaces** Provider Network Ports (B-ports) directly attached to other equipment operating within the same provider backbone network as the bridge of concern. These ports provide connectivity to the other bridges within and attached to the backbone network. Such B-ports are directly attached to the S-VLAN bridge inside of the B-BEB.

- **B-port E-NNI Provider Network Port Interfaces** Provider Network Ports attached to equipment from another backbone service provider's network. B-VID translation may be required to peer a service with another provider. Separation of backbone MAC address between service providers over this interface is not supported. This interface type can be used to interface Provider Bridging equipment and carry Provider Bridging traffic over the same network infrastructure as Provider Backbone Bridging traffic separated by VLANs.

  This interface type is not part of IEEE802.1ah (Provider Backbone Bridges). According to IEEE802.1ad (Provider Bridges), it is optional for an S-VLAN bridge to support a VID translation.

  Up to 4K VLAN translations are supported.

- **B-port UNI Customer Network Port Interfaces** Provider Network Ports attached to equipment being part of another backbone service provider's network. This interface type can be used by a provider to deliver a service to another backbone provider. Separation of backbone MAC address between service providers is not supported over this interface.

  This interface type is not part of IEEE802.1ah (Provider Backbone Bridges).

- **I-Tagged Interfaces (E-NNI)** Frames exchanged over an I-tagged interface are untagged MAC-in-MAC frames (no B-VLAN) with an I-TAG. Generally, the B-DA of I-Tagged frames is the address of the destination edge bridge at the other end of

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the backbone network (the address of the egress BEB's PIP). The CBP discards frames with an I-SID value that has not been configured for the CBP. A B-VLAN is assigned to the frame and, within the backbone network, the frame is forwarded as any other frame based on B-VLAN and B-DA. The B-VLAN is stripped from traffic that reaches a customer backbone port from the backbone network.

Up to 32 customer backbone ports (I-Tagged interfaces) are supported by the VSC7462.

I-Tagged Interface

The I-Tagged interface can connect to a customer backbone port on another backbone Network Provider's equipment (B-Component) or to a customer's Provider Instance Port (I-Component).

The following optional capabilities from IEEE802.1ah are supported on an I-Tagged interface of the Carrier Ethernet Switch:

- B-VLAN lookup (ELINEs, ELANs and ETREEs). For traffic going towards the backbone network, the ISID can be used to determine the B-VLAN.

  Up to 4K ISID to B-VLAN lookups are supported.

- B-DA substitution (ELINEs). An example of this use is a unicast frame (unicast C-DA) received over the I-Tagged interface using the default B-DA (flooding) as the customer equipment attached to the I-Tagged interface do not know the C-DA location. If the provider backbone bridge has better knowledge of the network the backbone bridge substitutes the default destination address with the unicast B-DA of the far end destination (or another group address) before transmission into the network. Thereby the distribution of the frame is limited within the B-VLAN of the backbone network. The reverse address substitution is performed at the backbone network's egress CBP.

- I-SID substitution (ELINEs). On an E-NNI interface, it may not be possible to exchange unique I-SID values between backbone network providers. 1:1 mapping of I-SIDs on either side of the E-NNI is therefore advantageous.

  Up to 4K I-SID to I-SID translations are supported.

- B-SA substitution (ELINEs). By substituting the backbone source MAC address, it is possible to hide the address of the customer equipment within the core network.

By only looking at the Tag Protocol ID (TPID) of the outer VLAN tag, it is not possible to distinguish a Provider Bridge Ethernet frame from a Provider Backbone Bridge Ethernet frame. As a result, the fundamental operation of a B-BEB is to forward both PB and PBB traffic concurrently. The VSC7462 can, however, be configured to allow only Provider Backbone Bridge Ethernet traffic by also looking for the I-TAG TPID of incoming frames. This filtering is controlled per arrival port using the frame acceptance filter. For more information about filtering, see "Frame Acceptance VLAN Filtering," page 34.

A B-BEB contains a single bridging domain (a single MAC table and a single VLAN table) In addition to supporting the I-Tagged interface, it operates similar to a Provider Edge bridge. The MAC table and VLAN table is shared if both PB traffic and PBB traffic is bridged by the B-BEB. Traffic separation between PB and PBB is obtained using VLANs.

For more information about Provider Bridge and Customer Bridge operation, see"Provider Bridge and Customer Bridge," page 59.

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In summary, the following service interfaces are supported by a B-BEB using the VSC7462 device:

- Port-based service
- S-Tagged service
- I-Tagged service

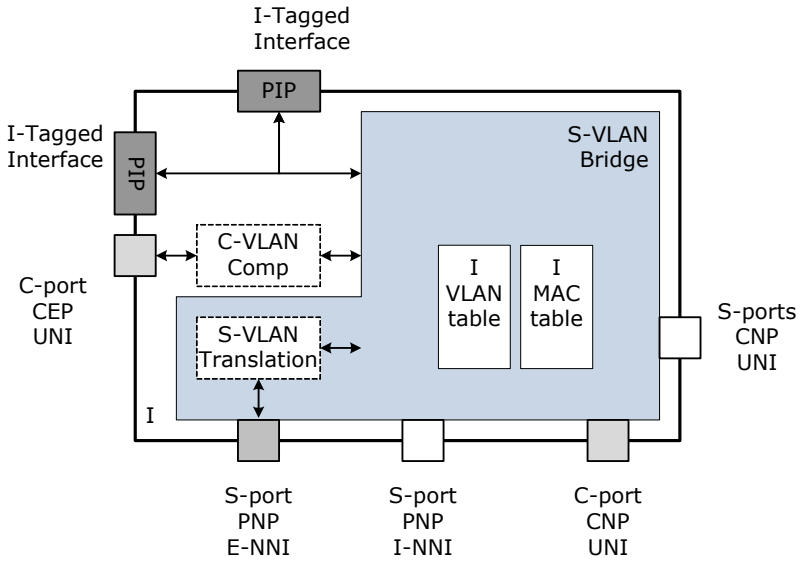
Backbone Core Bridge (BCB)

The Backbone Core Bridge is identical to B-BEB, except it does not support the I-Tagged interface. All forwarding within the BCB is standard Layer 2 and based on backbone MAC addresses.

4.1.3 Provider Backbone Edge Bridge (I-BEB)

The following illustration shows a simplified model of a Provider Backbone Edge Bridge with an I-Component (I-BEB) as supported by the VSC7462 device.

Figure 17. Simple Model of Provider Backbone Edge Bridge (I-BEB)



Six interface types are supported on the I-BEB. Five of these are identical to the interfaces on the Provider Edge Bridge. The sixth interface is the I-Tagged interface. For more information about the interface types supported, see "Provider Bridge and Customer Bridge," page 59 and "Provider Backbone Edge Bridge (B-BEB)," page 62. Within the I-Component, the I-Tagged interface is connected to a Provider Instance Port (PIP).

A backbone MAC address is associated with the PIP. This MAC address is the source MAC address (B-SA) of all traffic entering the Backbone Network through this PIP. Within the PBBN, PIP MAC addresses are used as destination MAC addresses and are learned by Provider Backbone Core Bridges.

In summary, the following interfaces are supported on an I-BEB using the VSC7462:

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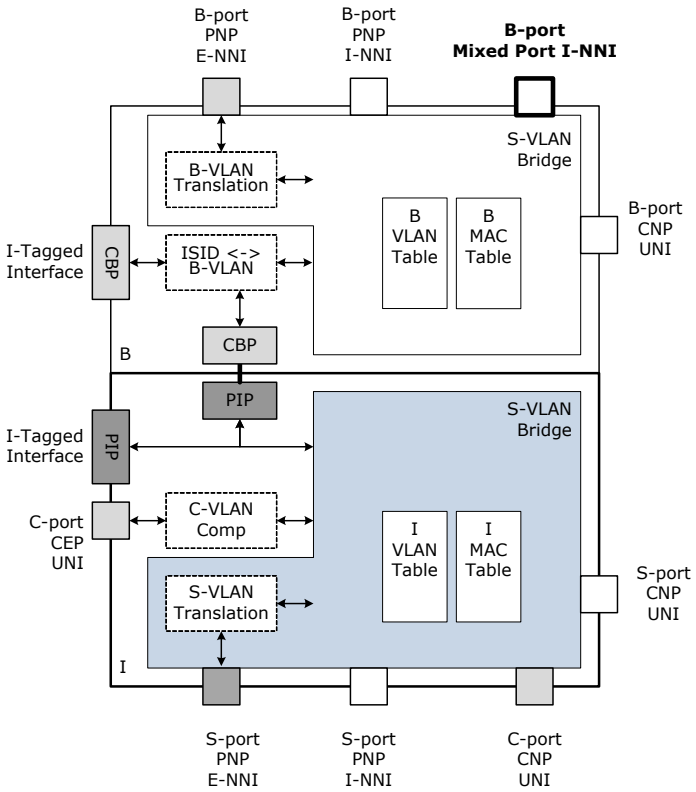
- Port-based service
- S-Tagged service
  - One-to-one
  - Bundled many-to-one
  - Bundled all-to-one
- I-Tagged service
- C-Tagged service

4.1.4 Provider Backbone Edge Bridge (IB-BEB)

The following illustration shows a simple model of an IB-BEB. The IB-BEB contains both an I-Component and a B-Component. The interfaces supported are the sum of interfaces supported by the I-BEB and the B-BEB, plus the proprietary B-port Mixed Port I-NNI interface, as highlighted in the illustration.

Figure 18. Simple Model of Provider Backbone Edge Bridge (IB-BEB)



Compared to the standard model of a Provider Backbone Edge Bridge, with both a B-Component and an I-Component (IB-BEB), the IB-BEB (IB*-BEB) supported by the VSC7462 has four enhanced capabilities. The standard referenced is IEEE802.1ah (Provider Backbone Bridges):

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- E-NNI support within the B-Component. For more information, see "Provider Backbone Edge Bridge (B-BEB)," page 62.
- ISID to B-VLAN lookup within the B-Component. For more information, see "Provider Backbone Edge Bridge (B-BEB)," page 62. Within IEEE802.1ah this is an optional capability.
- Provider Edge Bridge support within the I-Component. A Provider Edge Bridge, as defined by IEEE802.1ad (Provider Bridges), allows for direct attachment of customer equipment to the IB-BEB. In summary the I-Component supports the following interfaces from the standards:
  - Port-based service interface
  - C-Tagged service interface
  - S-Tagged service interface
  - I-Tagged service interface
- Mixed port support. For more information, see "Mixed Port," page 71.

The B-Component of the IB*-BEB supports the UNI, I-NNI, E-NNI, and I-Tagged interface. For more information, see "Provider Backbone Edge Bridge (B-BEB)," page 62.

The I-Component of the IB*-BEB supports the UNI, I-NNI, E-NNI, and I-Tagged interface. For more information, see "Provider Backbone Edge Bridge (I-BEB)," page 65.

Supporting all these I- and B-Component interfaces within the same VSC7462 provides huge flexibility and advanced frame encapsulation capabilities. An example is encapsulation of a customer's C-Tagged frame into a MAC-in-MAC frame with S-Tag bundling. In this case, an S-VLAN TAG, I-TAG, B-SA, B-DA, and a B-VLAN TAG is pushed and popped per frame by the VSC7462 device.

As shown, an IB-BEB contains one bridge in the I-Component and one bridge in the B-Component. These bridges are totally independent and have dedicated VLAN and MAC tables. Before adding services on top of an IB-BEB, it operates as two unconnected bridges. The B-Component operates as a B-BEB and can operate as a Provider Backbone Core Bridge. The I-Component operates as an I-BEB and can operate as a Provider Bridge or Provider Edge Bridge. No traffic is exchanged between the I-Component and the B-Component without adding the service layer on top of basic Layer 2 forwarding. For more information about this service concept, see "Service Concept," page 76.

For more information about B-Component operating as a B-BEB, see "Provider Backbone Edge Bridge (B-BEB)," page 62. For more information about I-Component operating as an I-BEB, see "PBB with Traffic Engineering," page 70.

The arrival port of a frame determines within which of the components the frame is forwarded. For example, if a non-service frame enters on an I-Component port, it is only forwarded within the I-Component. The internal CPU can inject frames directly into either of the components and frames can be extracted to internal CPU from any of the components.

The independent Layer-2 forwarding of I-Component and B-Component also includes multicasting and flooding. That is, a non-service frame being flooded or multicasted is constrained to the single domain where the frame arrived. The same multicast DMAC address can be configured in the MAC tables of both domains.

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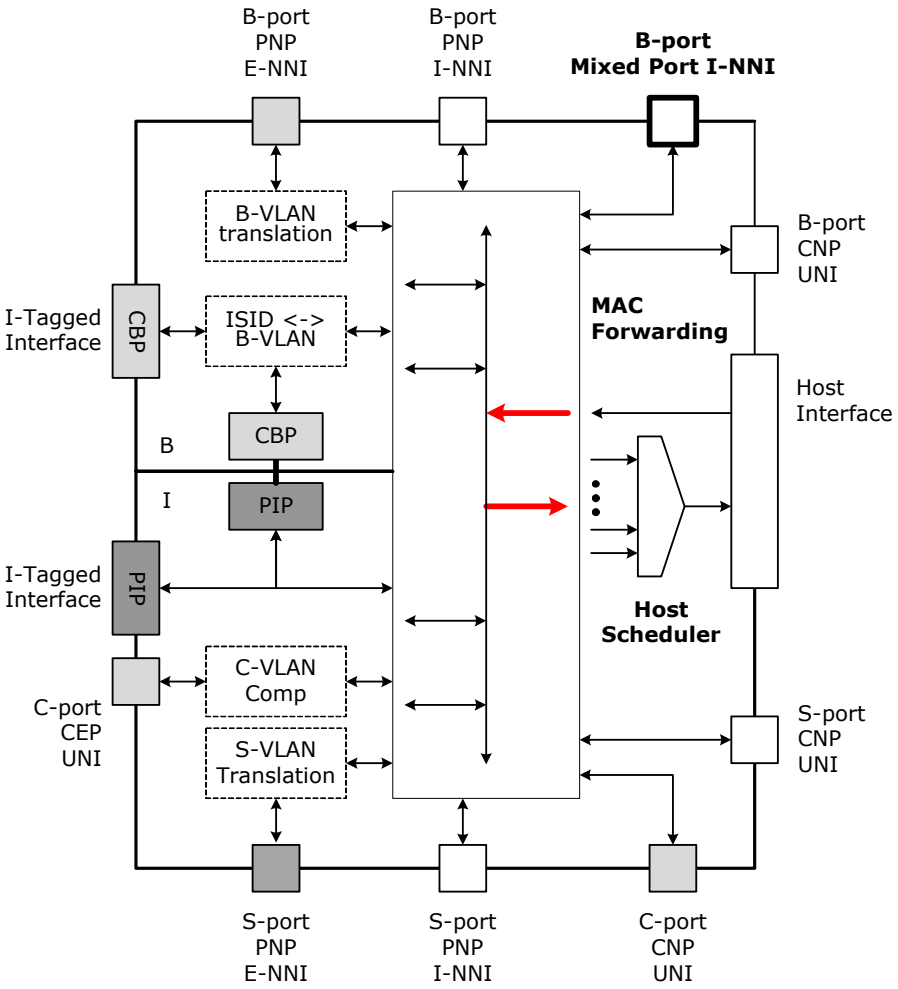
4K B-Component VLANs and 4K I-Component VLANs are supported by the VSC7462 device.

The following illustration shows frame forwarding within the VSC7462 device while implementing the Provider Backbone Edge Bridge.

Figure 19. Simple Model of MAC Provider Backbone Edge Bridge (IB-BEB)



Forwarding within the IB-BEB MAC is static and identical to the forwarding within the Provider Bridge MAC. For more information, see "Provider Bridge and Customer Bridge," page 59.

As depicted, the host interface is accessible from both the I-Component and B-Component. Any line port and interface has direct access to all host ports and host queues on the host interface, however, only push/pop of MACinMAC headers to frames (going between the I-Component and B-Component) is possible if the service layer is enabled. For more information about the service concept, see "Service Concept," page 76. Frame classification within the VSC7462 determines if service-based forwarding is required or if MAC forwarding within a single component (B-Component or

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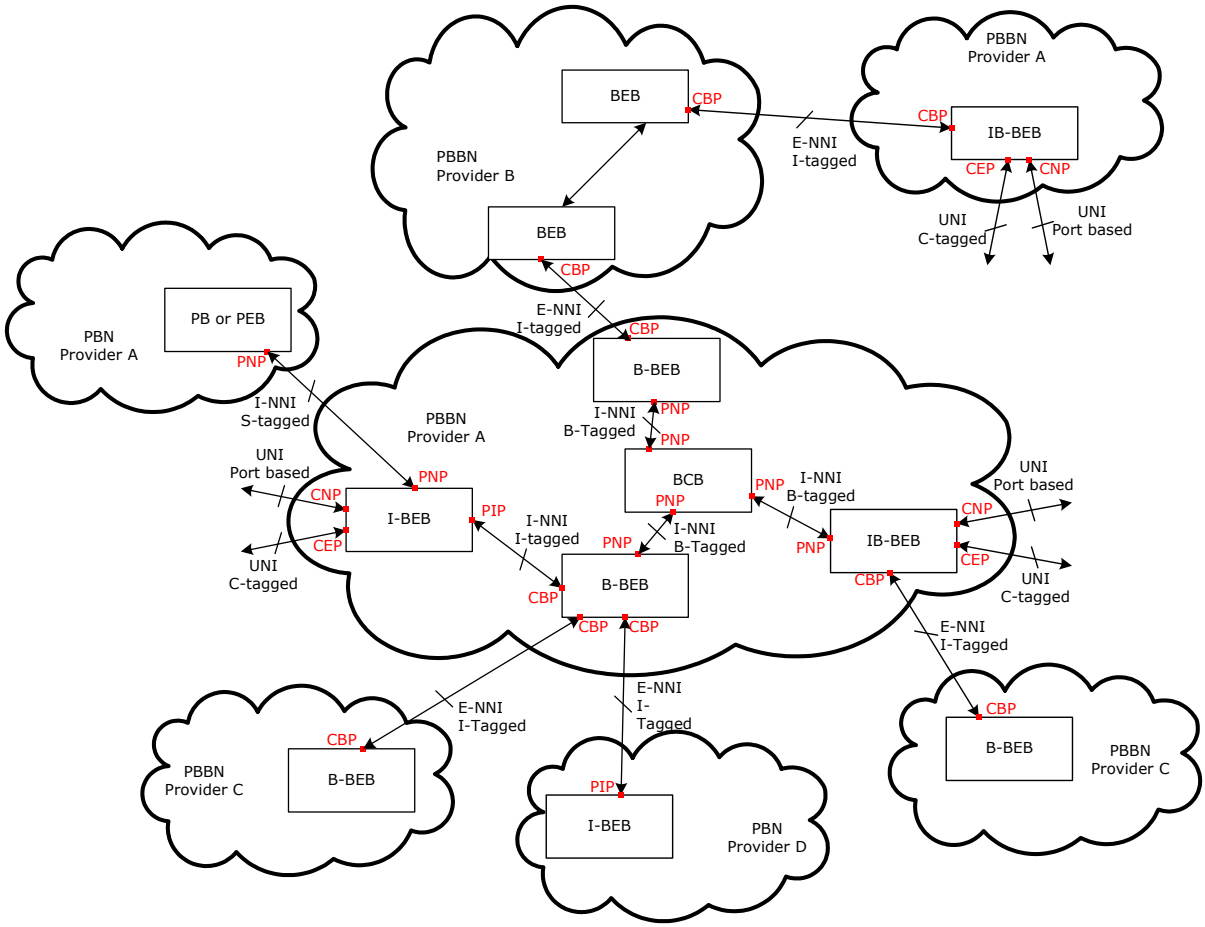
I-Component) is sufficient. The following constraints apply for MAC forwarding (as for the Provider Edge Bridge MAC):

- Forwarding between line ports is unconstrained and both unicast, multicast (flood) is supported
- Forwarding from host Interface to line ports is unconstrained and both unicast, multicast (flood) is supported
- Any forwarding to the host interface can only address a single host queue on a single host port

Forwarding to a mix of line ports and the host interface is not supported.

The following illustration shows most of the interfaces that are supported by B-BEBs, I-BEBs, and IB-BEBs, as described above, and how customer equipment can be attached to a PBBN.

Figure 20. Provider Backbone Bridge Network



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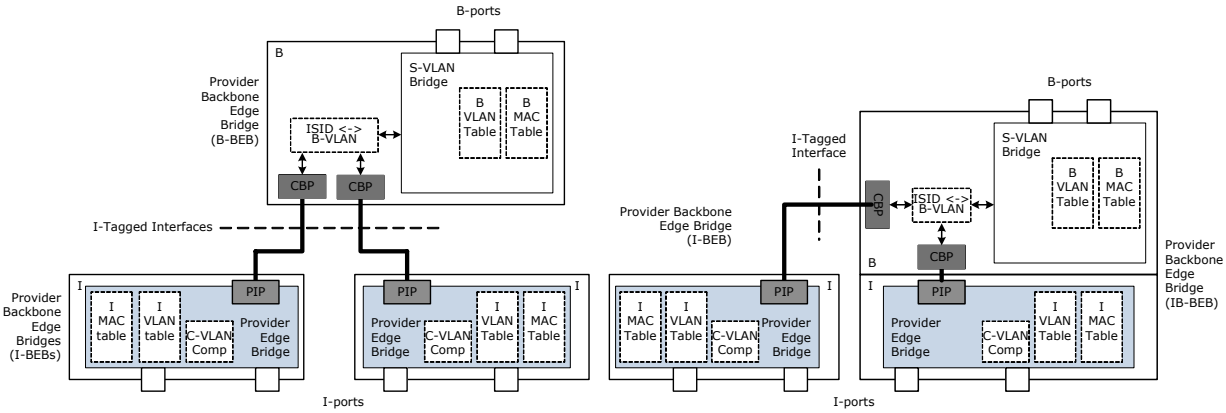
4.1.5 Backbone Edge Bridge Applications

A Backbone Edge Bridge with an I-Component only (I-BEB) can be connected to a B-BEB or IB-BEB using an I-Tagged service interface to increase service density beyond the 4K services of Provider Network Edge equipment.

In the following illustration, the left side shows two I-BEBs connected to a B-BEB. On the right side, an I-BEB connected to an IB-BEB. The term "I-port" is an I-Component port, which can be either an S-port or a C-port as defined previously.

Highest integration is obtained by the right side application showing only two devices. However, three devices provides more memory per service, which may be advantageous for certain applications. In both setups, a total of 8K services are supported. The B-Component's ISID to B-VLAN mapping table contain a total of 4K entries so many-to-one mapping of ISIDs to B-VLAN is therefore required to scale services to 8K. More I-BEBs can be added to the applications scaling services even further.

Figure 21. I-BEB Applications



4.1.6 PBB with Traffic Engineering

Provider Backbone Bridging Traffic Engineering (PBB-TE), as defined in the IEEE802.1Qay (Provider Backbone Bridge Traffic Engineering) specification, defines a set of constraints for the ubiquitous connectivity obtained by provider backbone bridging that enable provisioned connection oriented paths. These paths, called Ethernet Switch Paths (ESPs), have the following properties:

- Within a single PBB-TE network, an ESP provides a unidirectional end-to-end path between Backbone Edge bridges. The path is identified as a 3-tuple (Backbone Destination Address, Backbone Source Address, B-VLAN ID). Up to 32K ESPs are supported by the VSC7462.
- An ESP is point-to-point or point-to-multipoint.
- PBB-TE ESPs are separated from other PBB traffic by using dedicated B-VLAN IDs for which xSTP has been disabled. That is, PBB-TE B-VLAN IDs are mapped to a special Spanning Tree instance (TE-MSTID).

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- Learning of MAC addresses is disabled within the TE-MSTID (all PBB-TE B-VLANs). The Backbone MAC addresses of ESP endpoint equipment (BEBs) must be installed in all network equipment along the path.
- Frames with unknown destination backbone MAC address are discarded for the TE-MSTID (all PBB-TE B-VLANs).

1:1 protection between ESPs. Within the VSC7462, both normal 1:1 protection and 1:1 protection with load sharing are supported. 512 hardware protected path groups are supported by the device. A path group establishes a connection between a pair of ESPs used in 1:1 protection. Software can protect more ESPs up to the 32K limit. Protection within PBB-TE is the subject of section "PBB-TE Ethernet Switched Path Protection," page 87

Bidirectional connectivity is also supported within PBB-TE by configuration of co-routed but reverse ordered ESPs. For point-to-point connections co-routed paths are defined as a unidirectional path from point A to point B and a unidirectional path from point B to point A, where all links and nodes are the same and traversed in the exact same but reversed order. Co-routed paths are supported for both point-to-point connections (requiring two co-routed paths) and point-to-multipoint connections (requiring one point-to-multipoint ESP and N point-to-point ESPs with N+1 points in a connection).

As defined in IEEE802.1Qay, all Backbone Edge Bridges used in PBB-TE must be IB-BEBs. Backbone Core Bridges are standard L2 bridges. An important property of PBB-TE is that only backbone edge devices are actively involved in determining the frame forwarding of PBB-TE traffic into ESPs. When the MAC tables of Backbone Core Bridges have been statically populated with the provisioned backbone MAC addresses and PBB-TE B-VLANs the ESP is fully defined and the standard L2 forwarding within BCBs is PBB-TE unaware. In fact, the 60-bits "label" composed of the B-DA (48-bits) and B-VLAN (12-bits) defines the exact path of the ESP taken from ingress BEB to egress BEB within the PBBN. With this approach each BEB can be reached from up to 2^{12} different paths selected by the PBB-TE B-VLAN. Also, the number of PBBN B-VLANs that must be allocated to Traffic Engineering is determined by the maximum number of ESPs required to reach any given BEB (Backbone MAC address). As all PBB-TE MAC addresses are provisioned, this firm requirement on allocation of B-VLANs to PBB-TE can be alleviated by allowing more than one Backbone MAC address per BEB (supporting multiple PIPs and CBPs within the IB-BEB). The VSC7462 supports 32 Source Backbone MAC addresses.

4.1.7 Mixed Port

A mixed port is a physical port on the VSC7462 device that carries both PBB/PBB-TE traffic and PB traffic (S-tagged) and/or customer traffic (C-tagged). On the Carrier Ethernet IB-BEB Bridge (VSC7462), a mixed port is a B-Component port that is also capable of carrying non MACinMAC encapsulated traffic. On the Carrier Ethernet MAC (), a mixed port can be any port that is not configured as a host interface. As explained in "Provider Bridge and Customer Bridge," page 59 and "Provider Backbone Edge Bridge (I-BEB)," page 65, frame-specific encapsulation is supported by the device's host interface and is determined by service properties. This is a native host interface functionality and, by definition, is not a mixed port functionality.

Mixed port functionality simplifies the introduction of Provider Backbone Bridging and Provider Backbone Bridging Traffic Engineering technologies in existing Provider Bridged Networks. Initially, PB, PBB, and PBB-TE can go hand in hand within a unified network and the backbone network can grow as needed or be separated out at a later

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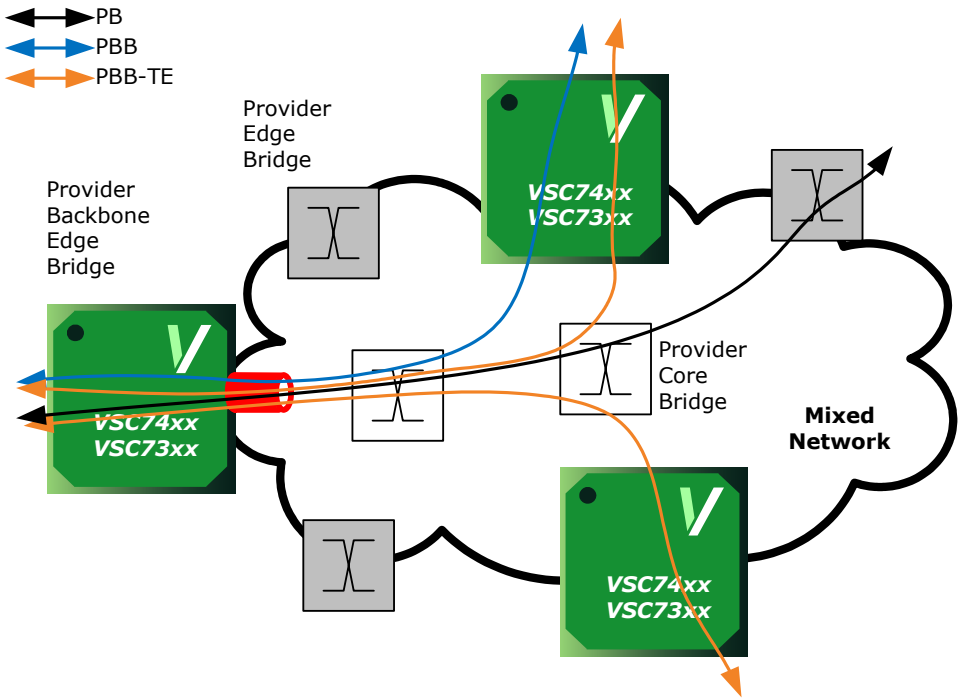
stage, as shown in the following illustration. In the depiction, the port on the left-most BEB facing the mixed network is a mixed port. The advantage of mixed port functionality is that any encapsulation is carried over a single physical interface into the network providing simpler edge connectivity requiring only a single port on already installed Provider Core Bridge. As an example, a 10 GbE port of the VSC7462 could be configured for mixed port operation.

Figure 22. Mixed Port



Provider Backbone Edge devices supporting PB, PBB, and PBB-TE are attached to an already existing Provider Bridge Network. Within the PB Network the different technologies are separated by VLANs. Provider Core Bridges are unaware of the different technologies and bridges all traffic as standard Provider Bridged Traffic. Only PB traffic is initiated and terminated by Provider Edge Bridges. The Provider Backbone Edge Bridges can initiate and terminate any of the technologies.

A network that mixes Provider Bridging and Provider Backbone Bridging technologies has certain properties that are not standards compliant:

- Only a single 4K VLAN space exists within the mixed network. The VLAN space of the original Provider Bridged Network must be shared between PB, PBB, and PBB-TE within the mixed network.

Provider Core Bridge MAC tables may be populated with both Customer MAC addresses (PB) and Operator MAC addresses (PBB/PBB-TE). This can eventually be avoided if PBB/PBB-TE VLANs in the mixed network are all point-to-point with learning disabled (flooding VLANs).

The single VLAN space within a mixed network dictates constraints to the IB-BEB model inside the Provider Backbone Edge Bridge. That is, the mixed port is a B-Component Port and is associated with the B-VLAN table, however, because the mixed port is

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attached to a PB network, it is required that the B-VLAN table and I-VLAN table operate as one common table for PB VLANs on the mixed port. This is obtained within the VSC7462 by requiring that B-VLAN ID = I-VLAN ID for PB traffic going across the mixed port.

On a Provider Backbone Edge Bridge (IB-BEB) the NPI port of the VSC7462 device may be configured as a mixed port. By configuring the NPI port as a mixed port it is possible to obtain direct Layer 2 access to both the B-Component bridge and I-Component bridge without pre-configuring services. Any frame type (PB, PBB, PBB-TE) can be directly injected and extracted from/to external CPU if the NPI port is a mixed port.

4.1.8 MPLS-TP Operation

MPLS-TP operations are supported. For more information, see the MPLS-TP FPGA specification.

4.1.9 Stacking

TBD

4.2 MEF Services

The Metro Ethernet Forum (MEF) specifies the following Ethernet Virtual Connection (EVC) types, which can be implemented using the service concept:

- **E-LINE EVC: Point-point Service** Ethernet Private Line (EPL) allows only one EVC per UNI port, while Ethernet Virtual Private Line (EVPL) allows multiple EVCs per UNI port.
- **E-LAN EVC: Multipoint Service** Ethernet Private LAN (EP-LAN) allows only one EVC per UNI port, while Ethernet Virtual Private LAN (EVP-LAN) allows multiple EVCs per UNI port. This is a bridged service.
- **E-TREE EVC: Rooted Multipoint Service** Ethernet Private Tree (EP-TREE) allows only one EVC per UNI port, while Ethernet Virtual Private Tree (EVP-TREE) allows multiple EVCs per UNI port. This is a bridged service where the allowed connectivity can be configured per ASP.

4.3 MEF Bandwidth Profiles

The MEF standards specify a dual-bucket policing scheme to regulate the amount of data arriving at each UNI port. This bandwidth profile (BWP) can be applied in the following ways.

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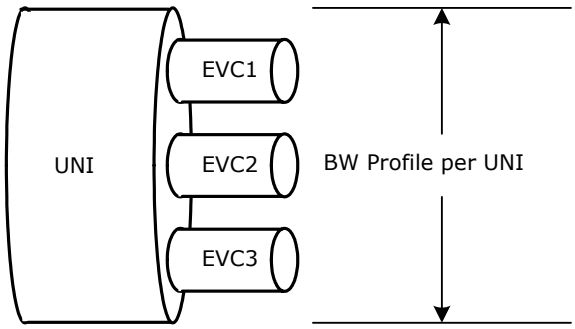
4.3.1 Bandwidth Profile per Port

The following example shows that three EVCs share one BWP for the port. Each EVC requires its own ASP, but all three ASPs will indicate the same service policer. Statistics are still kept separately for each EVC. Each EVC can have multiple Classes of Service, however, these are not metered or counted separately.

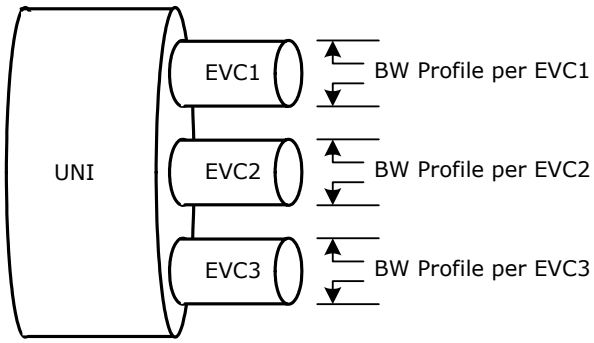
Figure 23. Bandwidth Profile per Port



4.3.2 Bandwidth Profile per EVC

The following example shows three EVCs, each having its own BWP. Each EVC requires its own ASP, and each ASP maps to its own service policer. Statistics are kept separately for each EVC. Each EVC can have multiple Classes of Service, however, these are not metered or counted separately.

Figure 24. Bandwidth Profile per EVC



4.3.3 Bandwidth Profile Per COS Indicator Per EVC

The following example shows two EVCs, each having multiple Classes of Service, which are reduced to three COS Indicators. Each COS Indicator on each EVC requires its own ASP, and each ASP maps to its own Service policer. Statistics are kept separately for each COS Indicator on each EVC.

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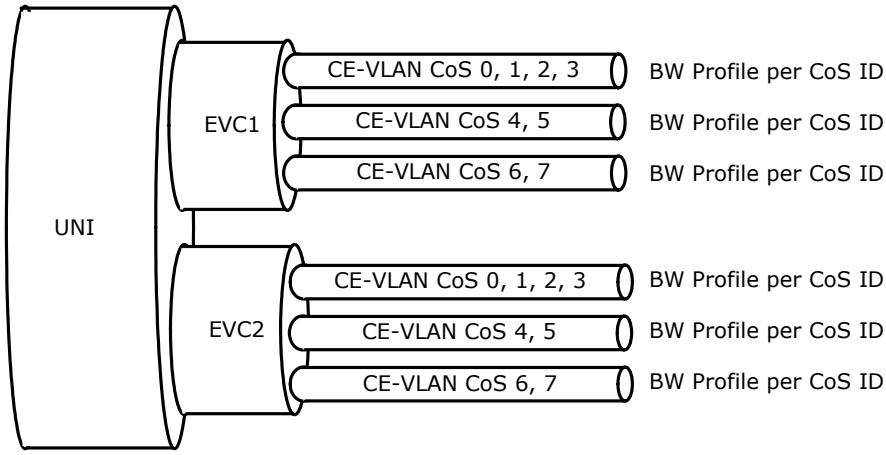
Figure 25. Bandwidth Profile per COS per EVC



4.3.4 MEF Service Attributes

The MEF standards specify a set of service attributes for each UNI and for each EVC per UNI. The following table summarizes the service attributes and associated granularity supported by the VSC7462 device.

Note that the supported service attributes are independent of the port type (C-port, S-Port, or B-port).

Table 16. Supported Service Attributes

Service Attribute	Granularity
CE-VLAN ID / EVC MAP untag / prio tag	Per UNI
CE-VLAN ID / EVC MAP	Per EVC and UNI Up to 4K CE-VLAN IDs per UNI can be individually mapped to an EVC.
CE-VLAN ID Preservation	Per EVC Configurable per EVC whether CE-VLAN IDs shall be preserved, removed, or translated
CE-VLAN CoS Preservation	Per EVC Configurable per EVC whether CE-VLAN CoS shall be preserved or translated
Service multiplex	Per UNI
Bundling	Per UNI
All-to-one bundling	Per UNI
Ingress BW profile	Per UNI Per (EVC, UNI) Per (CoS, EVC, UNI) Per EVC across all UNIs - Proprietary Per (CoS, EVC) across all UNIs - Proprietary
Unicast Service Frame Delivery	Per UNI Per EVC

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Table 16. Supported Service Attributes *(continued)*

Service Attribute	Granularity
Multicast Service Frame Delivery	Per UNI Per EVC
Broadcast Service Frame Delivery	Per UNI Per EVC
MTU Size	Per UNI
L2 Control Protocol Processing	Per UNI

4.4 Service Concept

The following illustration provides an overview of how services are delivered from the VSC7462 device. This depiction only includes the service layer.

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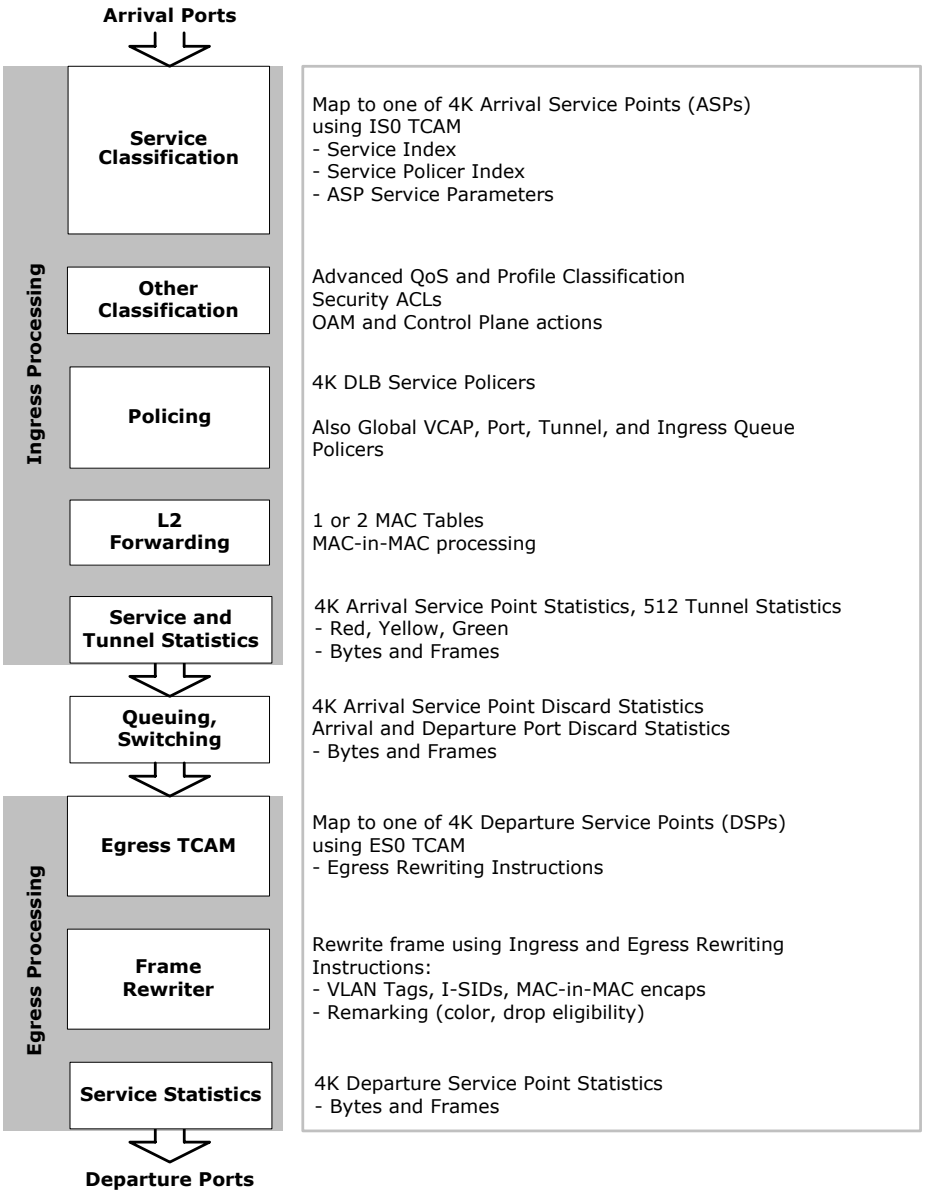
Figure 26. Carrier Ethernet Service Concept



The service layer defines the treatment that each frame receives with the VSC7462 device. At ingress each service frame is mapped to an Arrival Service Point (ASP), and at egress each service frame is mapped to one or more Departure Service Points (DSP).

Note All frames need not be mapped to a service.

- Management and Control Protocols such as Link OAM, E-LMI, LACP, and Pause frames would normally not be mapped to a service. There are a variety of configuration options related to this.

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- Certain VLANs may optionally be forwarded with limited per-VLAN treatment. For example, VLANs that have no customer UNI ports on the device can be forwarded without consuming Service resources.

Service Definitions

A "Service" consists of at least one ASP and one DSP and is primarily defined by the configured parameters of those service points.

A service may be unidirectional or bidirectional. It may be point-point, point-multipoint, multipoint-point, or multipoint-multipoint.

An Arrival or Departure "Service Point" is an abstract reference point within the chip where a service policy is applied. Service Points are always unidirectional. The VSC7462 device described by this document support 4K ASPs and 4K DSPs, which can be used to implement up to 4K Services.

The number in the following table relate to unprotected services.

Table 17. Service Point Consumption per Services

Service Type	Number of Arrival Service Points Consumed	Number of Departure Service Points Consumed	Number of Forwarding VLAN IDs Consumed
Unidirectional E-LINE	1	1	1 shared by all E-LINEs
Bidirectional E-LINE	2	2	1 shared by all E-LINEs
E-LAN with N port members. Per departure port egress statistics. (Independent of Arrival port)	N	N	1
E-LAN with N port members. Per departure port and arrival port egress statistics	N	N × (N – 1)	1
E-TREE with N port members. Per departure port egress statistics. (Independent of Arrival port)	N	N	1

ASP Service Parameters

Each ASP provides the following parameters:

- Ingress Service Index. Identifies the ASP.
- Service Policer Index. The Service Policer provides SLA enforcement. Multiple ASPs may map to the same Service Policer, however, any given frame is measured only against one service policer.
- Tunnel Policer Index. The tunnel policer provides for traffic engineering. Multiple ASPs may map to the same tunnel policer; however, any given frame is only measured against one tunnel policer.
- Arrival statistics
- Service VLAN

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- Portmap of all ports that can be reached from this ASP. This provides a way to limit forwarding on a per-ASP basis for implementing multipoint services such as E-TREE using only a single classified VLAN. This is also the mechanism that allows all point-point services to share one classified VLAN.
- Classified S-VLAN service classification can overrule the basic VLAN classification. This can be used in combination with the ASP-specific portmap to classify many services (such as E-LINEs) to a common VLAN without providing connectivity between the services.
- Classified B-VLAN. Service frames arriving on a B-port may need forwarding in both the B-Component and I-Component. Service specific B-VLAN classification also enables E-NNI interface support.
- Policy Association Group (PAG). Each service is associated with a policy that can be used as part of efficient and advanced filtering with respect to QoS, profiling, security, or OAM_CP.
- Arrival tagging/encapsulation instructions. Frame format is independent for each ASP of a service. This also dictates the encapsulation of the service if going out on a network-facing port. That is, whether the service is a PB, PBB, or PBB-TE service.
- Service OAM handling. Independent for each ASP of a service. Includes, ability to map CCM OAM to a hardware OAM checker, and ability to police all service OAM independently of other service frames.
- QoS parameters. QoS markings are independent for each ASP of a service. These can be further modified by the Advanced QoS Classification TCAM.
- Path group identifier. Used in PBB-TE path protection to identify both the active and backup path for the service.

The ASP is identified through the Service Classification TCAM (IS0) using the following fields:

- Arrival port
- Arrival virtual port on HIH_Port
- Arrival virtual port on HMD_Port
- Outer VLAN tag, inner VLAN tag, PBB I-SID, MPLS/MPLS-TP labels
- Ethernet PCP, DEI; IP DSCP; MPLS/MPLS-TP EXP

DSP Service Parameters

Each DSP provides the following parameters:

- Departure tagging/encapsulation instructions: frame format is independent for each DSP of a service.
- QoS marking or re-marking: QoS markings are independent for each DSP of a service. Frames can also be re-marked based on the results of policing.
- Per-DSP Departure Statistics

The DSP is identified through the egress service encapsulation and tagging TCAM (egress stage 0) using the following fields:

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- Departure port
- Departure virtual port on HIH_Port
- Departure virtual port on HMD_Port
- ASP or classified VLAN (selectable for each classified VLAN)

4.5 Service Examples

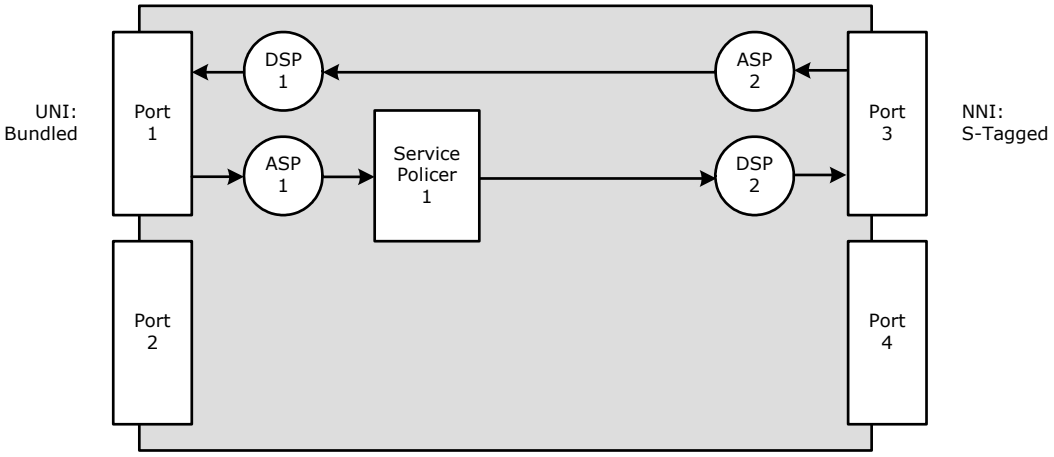
4.5.1 Provider Bridge E-LINE Service Example

The following illustration shows a bidirectional Provider Bridge E-LINE service.

- Port 1 is a bundled UNI. All frames on this port are mapped to this E-LINE service, tagged or untagged. Any customer tag is preserved.
- Port 3 is an NNI port, connecting into a provider network. This port may have many services mapped to it, each distinguished by a different S-tag.
- Frames belonging to this E-LINE are always classified to an S-tag. Frames are forwarded on the classified S-tag.
  – S-Tag is pushed before departure and popped upon arrival.
  – Frames belonging to this E-LINE may have a C-tag.

Kristian: Need to add tunnel policer (like Caracal) to the graphic below.

Figure 27. Provider Bridge E-LINE



This service consumes the following resources:

- Two of the 4K ASPs and two of the 4K DSPs
- One of the 4K service policers
- One of the 4K provider VLANs (S-TAGs) (all E-LINEs can share one VLAN)

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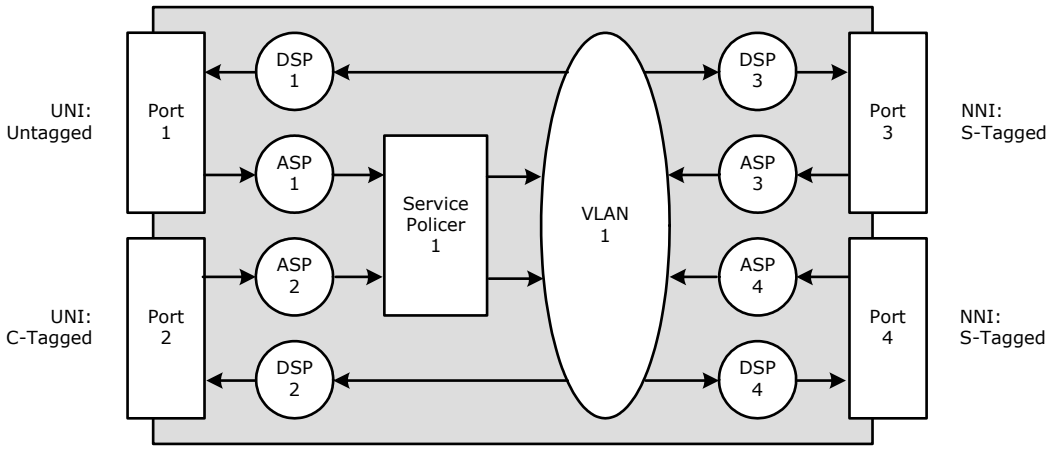
4.5.2 Provider Bridge E-LAN Service Example

The following illustration shows a Provider Bridge E-LAN providing service to four ports.

- Port 1 is an untagged UNI. All frames on this port are classified to provider VLAN 1. Tagged frames are discarded. (Alternatively, tagged frames may also be classified to provider VLAN 1)
  – All service frames arriving and departing on Port 1 are untagged.
- Port 2 is a C-tagged UNI (Virtual UNI). All frames with a specific C-tag are classified to provider VLAN 1. Other frames are discarded or mapped to other services.
  – The C-tag is pushed before departure and popped on arrival. Alternatively, it is also possible to preserve the C tag.
- Ports 3 and 4 are NNI ports, connecting into a provider network. These ports likely have many services mapped to them, each distinguished by a different S-tag. RSTP or MSTP can be used for port protection.
  – The S-Tag is pushed before departure and popped on arrival.

Figure 28. Provider Bridge E-LAN



Connectivity is determined by a combination of ASP and VLAN portmasks, and the MAC destination address of the frame.

In this example, a single service policer is shared by both port 1 and port 2. It is also possible to police services individually per arrival port including NNI ports (not shown).

This service consumes the following resources:

- Four of the 4K ASPs and four of the 4K DSPs
- One of the 4K service policier
- One of the 4K provider VLANs

Using a separate ASP and DSP on each port for this service allows:

- Separate arrival and departure statistics per-port, per-service
- Flexible tagging and policing options

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- OAM tunneling behaviors per-port, per-service
- The possibility of limiting connectivity based on arrival port (that is, disable switching from UNI to UNI).
- NNI-to-NNI connectivity if the two network interfaces connect to different Provider Networks

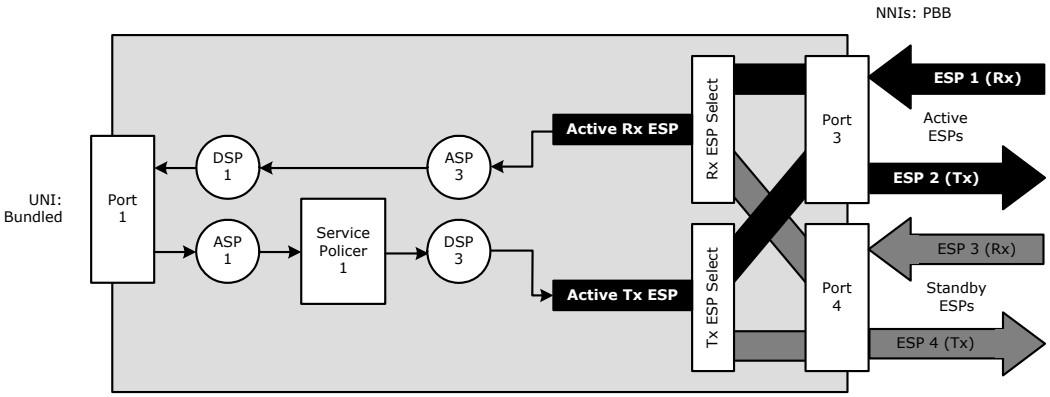
4.5.3 PBB-TE E-LINE Service Example with 1:1 Path Protection

The following illustration shows a bidirectional E-LINE service transported over 1:1 protected PBB-TE Ethernet Switched Paths (ESPs).

- Port 1 is a bundled UNI. All frames on this port are mapped to this E-LINE service, tagged or untagged. Any customer tag is preserved.
- Port 3 and port 4 are NNI ports, connecting into a provider network. These ports may have many services mapped to them, including a mix of PB and PBB.

  In this example, each NNI port has a pair of unidirectional PBB-TE ESPs provisioned. These ESPs provide a path layer, and can carry many services. The ESPs are 1:1 protected using hardware mechanisms.
  – Each ESP has a MAC-in-MAC encapsulation (B-DA, B-SA, B-VID).
  – Each service mapped to an ESP uses a service-specific I-SID. The I-SID remains the same on Active and Standby ESPs.

Figure 29. PBB-TE E-LINE



This service consumes these resources:

- Two of the 4K ASPs and two of the 4K DSPs
- One of the 4K service policer
- One of the 4K I-SID
- One of the 4K I-component VLANs (all E-LINEs share one VLAN)

The ESPs consume these resources:

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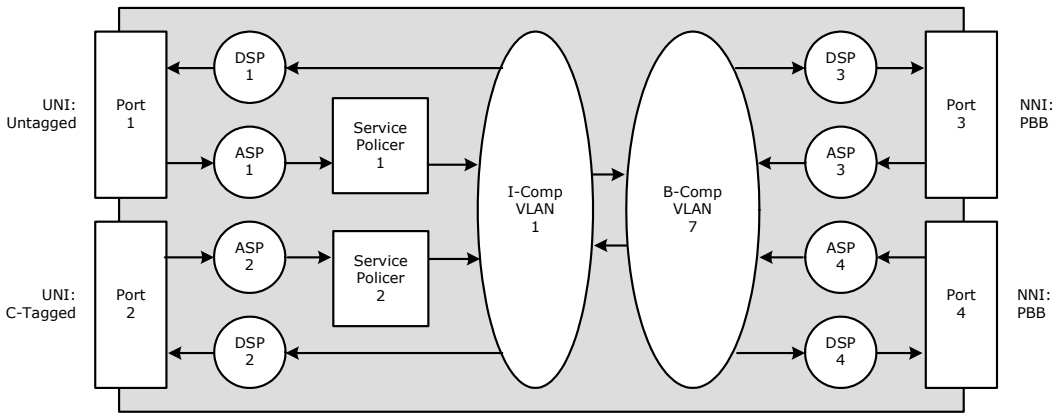
- At least two of the 512 protected ESP encapsulations
  – One per direction if the only difference between working/protect is B-VID
- At least two of the 4K B-component VLANs
  – One for working, one for protect
  – A subset of all 4K B-component VLANs is allocated for PBB-TE

4.5.4 PBB E-LAN Service Example

The following illustration shows a Provider Backbone Bridge E-LAN service for four ports.

- Port 1 is an untagged UNI. All frames on this port are classified to VLAN 1. Tagged frames are discarded.
  – All service frames arriving and departing on port 1 are untagged.
- Port 2 is a C-tagged UNI. All frames with a specific C-tag are classified to VLAN 1. Other frames are discarded or mapped to other services.
  – The C-tag is pushed before departure and popped upon arrival. Alternatively it is also possible to preserve the C tag.
- Port 3 and port 4 are NNI ports, connecting into a provider network. These ports may have many services mapped to them, including a mix of PB and PBB.
  – In this example, one B-VLAN is shown connected to the two ports.
  – B-VLAN 7 carries one customer's service, I-VLAN 1. Many services may map to B-VLAN 7. Each service has its own I-SID and possibly B-MAC.
  – PBB frames may be switched between NNI ports, or PBB may be terminated and the frame switched to the I-component. The MAC-in-MAC encapsulation is pushed on arrival from the I-component, and popped on departure to the I-Component.

Figure 30. PBB E-LAN



Connectivity in the I-component is determined by ASP, I-VLAN, and C-MAC address. Connectivity in the B-component is determined by ASP, B-VLAN, and B-MAC address. Port 1 and Port 2 each has its own Service Policer.

This service consumes these resources:

- Four of the 4K ASPs and four of the 4K DSPs

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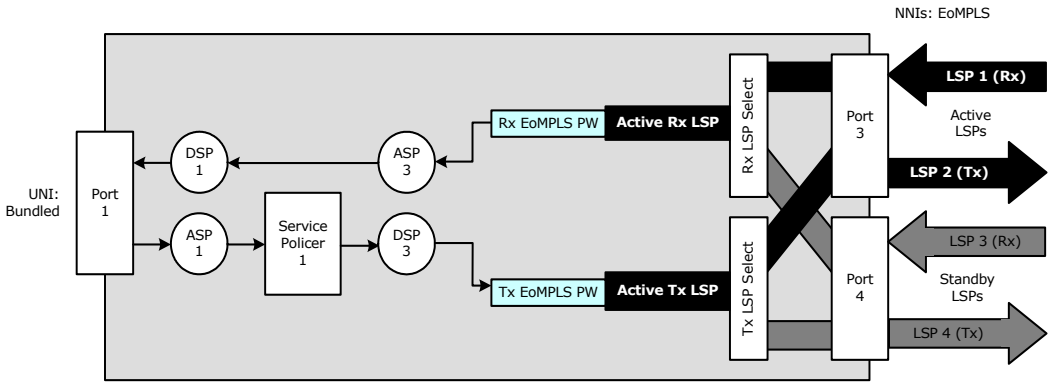
- Two of the 4K Service Policers
- One of the 4K I-SIDs
- One of the 4K I-VLANs and one of the 4K B-VLANs

4.5.5 MPLS E-LINE Service Example with 1:1 Path Protection

The following illustration shows a bidirectional E-LINE service transported over 1:1 protected MPLS Label Switched Paths (LSPs). The E-LINE is an EoMPLS Pseudowire.

- Port 1 is a bundled UNI port. All frames on this port are mapped to this E-LINE service, tagged or untagged. Any customer tag is preserved.
- Ports 3 and 4 are NNI ports, connecting into a provider network. These ports may have many services mapped to them, including a mix of PB and PBB.
  - In this example, each NNI port has a pair of unidirectional MPLS LSP Tunnels provisioned. These LSPs provide a path layer, and can carry many services. The LSPs are 1:1 protected.
  - Each LSP has its own encapsulation: Link MAC (DA, SA) and MPLS Tunnel Label.
  - Each service mapped to an LSP uses a service-specific Pseudowire encapsulation: PW Label and optional control word.

Figure 31. MPLS E-LINE



This service consumes these resources:

- Two of the 4K MPLS PW ASPs and two of the 4K MPLS PW DSPs
- One of the 4K Service Policer
- One of the 4K VLAN (all E-LINEs share one VLAN)

The Tunnel LSPs consumes one 512 protected LSP encapsulation.

4.6 OAM and Protection Switching

The VSC7462 device provides the following hardware mechanisms to support OAM:

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- Ability to classify OAM frames formatted according to:
  – IEEE P802.1ag (CFM)
  – IEEE 802.3 (EFM)
  – ITU-T Y.1731 (ETH-OAM)
  – MEF-16 (E-LMI)
- Classification of OAM for working and protect port, path, and service entities
- Programmable forwarding and processing behavior for all supported OAM types, including extraction of specified OAM to internal or external CPU
- Processing based on the maintenance level
- Insertion of OAM from internal or external CPU
- CCM generation using hardware Frame DMA engine and MIPS24K CPU
- CCM hardware checkers which interrupt the MIPS24K CPU with a vector correlating the event to the protected entity
- Generation and checking of:
  – 4K Service CCM flows
  – 512 Path CCM flows
  – 32 Port CCM flows
- Individual OAM flow policing or aggregate OAM policing for each port

The following illustration shows the conceptual approach to OAM and protection switching. All switchovers are activated by updating a small number of table entries or register bits per direction. The hardware mechanisms that support protection switching are:

- Link aggregation: Update Rx and Tx portmasks
- Port protection (Linear): Update Rx and Tx port protect group table entry
- PBB-TE ESP path protection (Linear): Update Rx and Tx path group table entry
- E-LINE service protection: Update arrival and departure service point entry
- Rapid Spanning Tree Protocol: Update RSTP port states and portmasks
- Multiple Spanning Tree Protocol: Update MSTP port/VLAN states and portmasks

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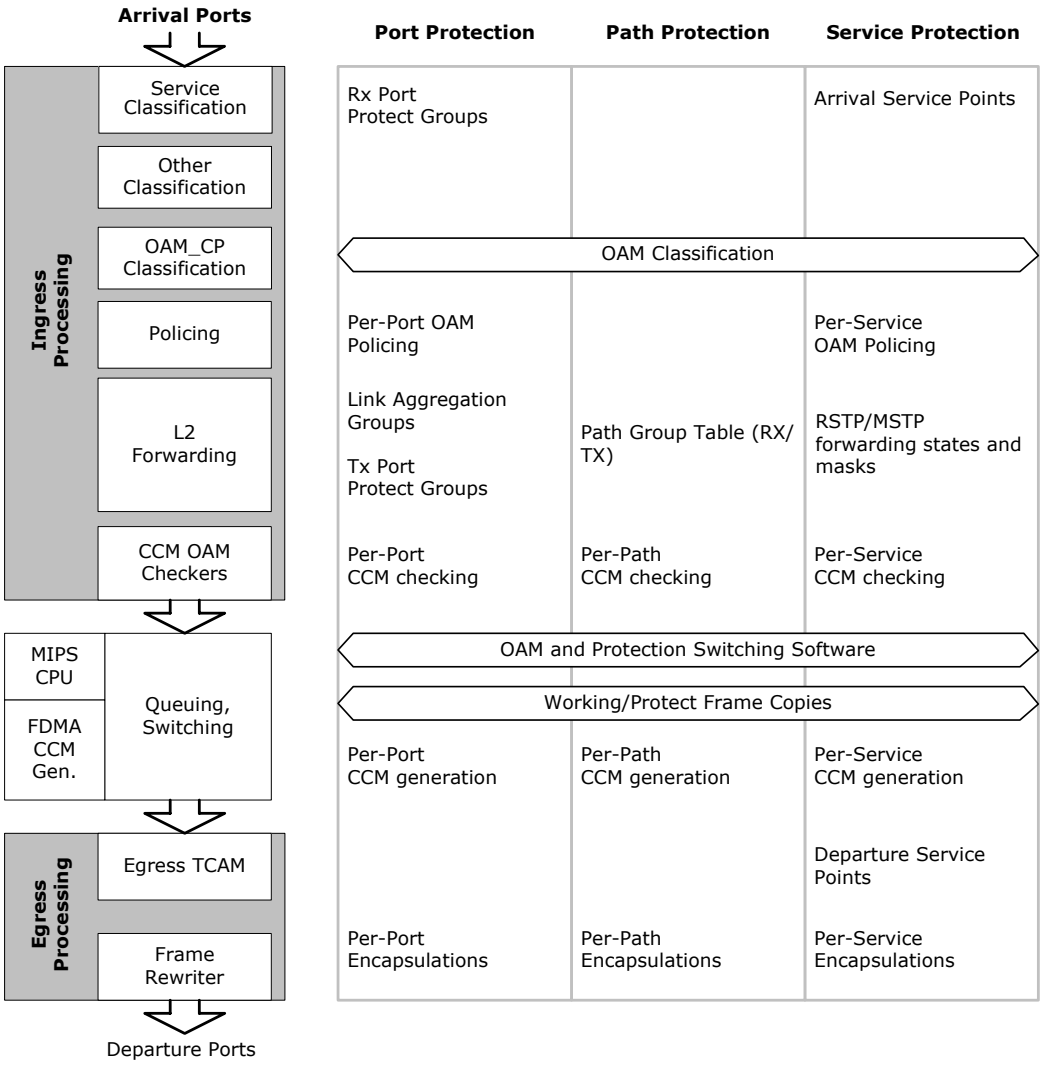
Figure 32. OAM and Protection Switching Concept



4.6.1 Port Protection

The following illustration shows the port protection schemes supported on VSC7462 device. Unique copies of OAM and control plane frames can be sent and received over each port independently. The hardware-based CCM features can be used in the selection of the active port and failover process.

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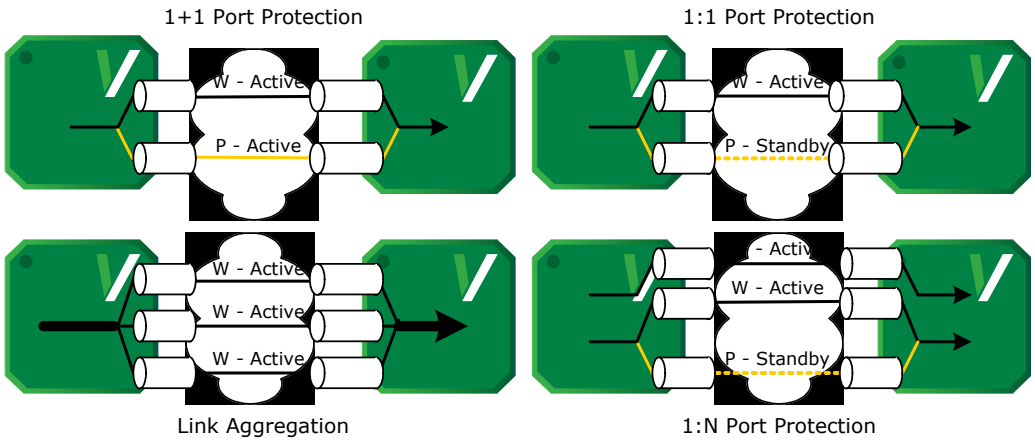
Figure 33. Port Protection



1+1 Port Protection

Identical service frames are sent over both ports by the transmitter. The receiver selects which port to use for service frames. Both ports are pre-provisioned, enabling a fast failover by the receiver.

1:N and 1:1 Port Protection

One port protects N active ports, and one copy of each frame is sent by the transmitter. Both ends must select the active port, but all ports are pre-provisioned, enabling a fast failover.

Note 1:1 protection is a subset of 1:N protection where N = 1.

Frame formats (MAC-in-MAC, VLAN tags, I-SIDs, or MPLS labels) may be independent on working and protect ports, although this consumes two Service Points. If identical frame formats are used on working and protect ports, only a single Service Point is consumed.

Link Aggregation

Up to eight ports are active simultaneously in one Link Aggregation Group (LAG). The transmitter identifies flows and distributes the flows among the ports. Failover consists of redistributing all flows over the remaining active ports. One copy of each service frame is sent by the transmitter.

Link Aggregation Control Protocol (LACP) is used to determine the working ports within each LAG. Because the LAG is treated as a single logical interface, service frame format does not vary based on the physical port that is used to transmit the frame.

4.6.2 PBB-TE Ethernet Switched Path Protection

The following illustration shows the PBB-TE ESP protection schemes supported on the VSC7462 device. Unique copies of OAM frames can be sent and received over each ESP independently. The -based CCM features can be used in the selection of the active ESP and failover process.

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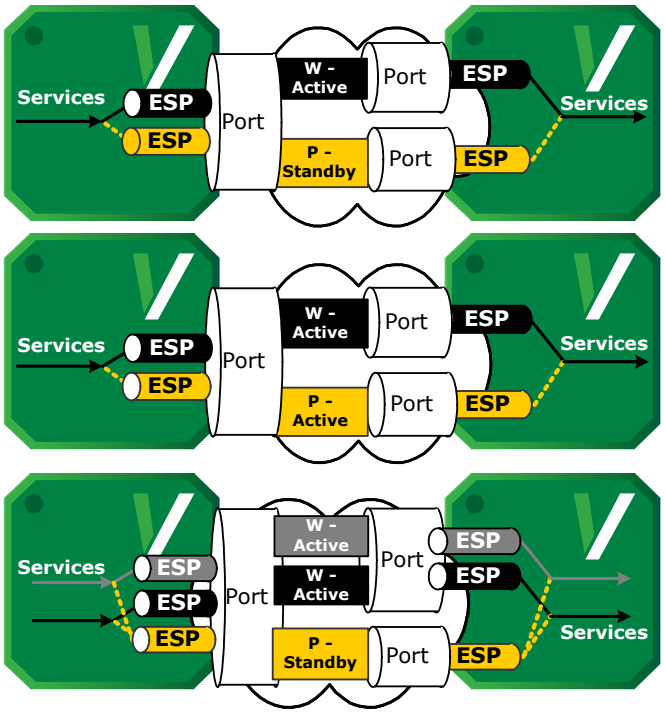
Figure 34. PBB-TE ESP Protection



1:1 and 1:N ESP Protection

One ESP protects N ESPs, and one copy of each frame is sent by the transmitter. Both ends must select the active port, but all ESPs are pre-provisioned, enabling a fast failover.

Note 1:1 protection is a subset of 1:N protection where N=1.

B-DA and B-VID are independent on each ESP, but I-SIDs and VLAN tags are identical on working and protect. Independent formatting is possible with service protection.

1:1 ESP Protection with Load Sharing

Two active ESPs are used by a number of services, where each service can designate one of the ESPs as working and the other as protect. If one of the ESPs fails, all services end up on the remaining ESP. This failover is accomplished with the same fast failover mechanism as 1:1 ESP protection, and uses the hardware-based CCM features.

4.6.3 MPLS Label Switched Path Protection

The following illustration shows the MPLS label switched path (LSP) protection schemes supported by the VSC7462 device. Unique copies of OAM and control plane frames can be sent and received over each LSP independently. The hardware-based Ethernet CCM features can be used in the selection of the active LSP and failover process.

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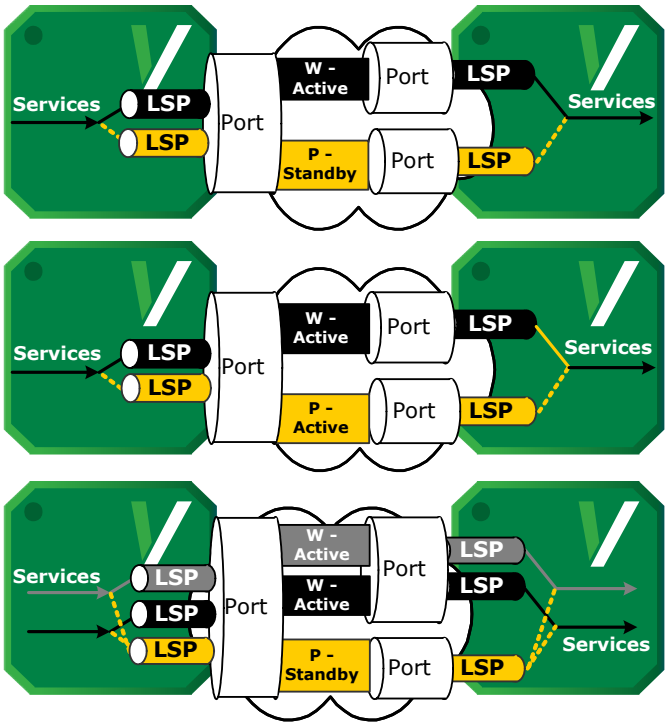
Figure 35. MPLS LSP Protection



1:1 and 1:N LSP Protection

One LSP protects N LSPs, and one copy of each frame is sent by the transmitter. Both ends must select the active port, but all LSPs are pre-provisioned, enabling a fast failover.

Note 1:1 protection is a subset of 1:N protection where N=1.

1:1 LSP Protection with Load Sharing

Two active LSPs are used by a number of EoMPLS Pseudowires, where each pseudowire can designate one of the LSPs as working and the other as protect. If one of the LSPs fails, all pseudowires end up on the remaining LSP. This failover is accomplished with the same fast failover mechanism as 1:1 LSP protection.

4.6.4 E-LINE Service Protection

The following illustration shows the E-LINE service protection scheme supported on the VSC7462 device. Unique copies of OAM frames can be sent and received over each service independently. The hardware-based CCM features can be used in the selection of the active service and failover process.

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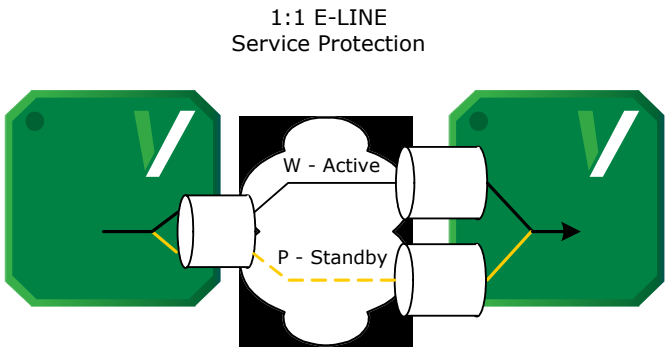
Figure 36. E-LINE Service Protection



1:1 E-LINE Service Protection

Two E-LINE EVCs are provisioned in protect group pairs, with one working and the other protect. One copy of each frame is sent by the transmitter. Both ends must select the active EVC, but all EVCs are pre-provisioned, enabling a fast failover. The EVCs may span different ports or paths, and multiple layers of protection can apply.

Frame formats (B-DA, B-VID, I-SID, C-VIDs, S-VIDs, or MPLS labels) may be programmed completely independently on the working and protect EVCs.

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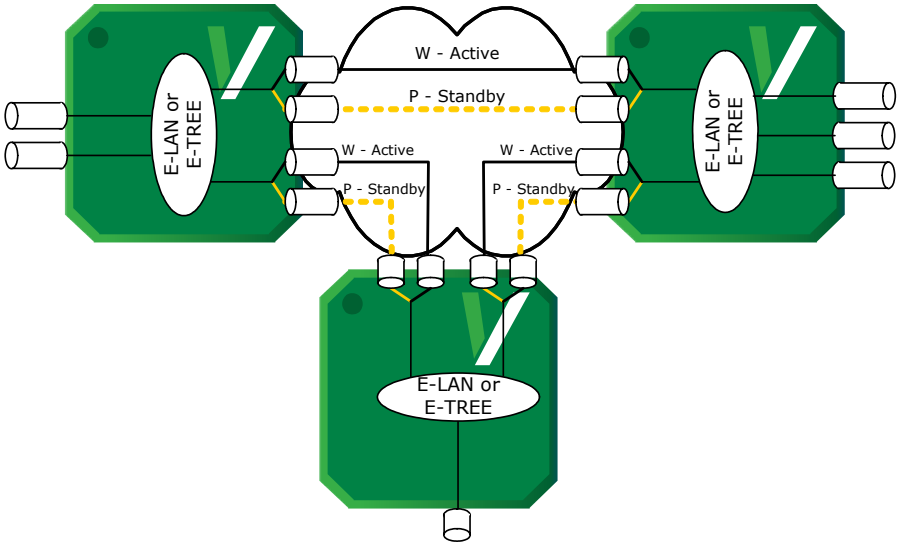
4.6.5 E-LAN and E-TREE Service Protection

The following illustration shows the E-LAN and E-TREE protection schemes supported by the Vitesse Carrier Ethernet Switch. Unique copies of OAM frames can be sent and received over each port, PBB-TE ESP, or MPLS LSP independently. The hardware-based Ethernet CCM features can be used in the selection of the active port/ESP/LSP and failover process.

Figure 37. E-LAN and E-TREE Service Protection



Split Horizon E-LAN and E-TREE Protection

Protected pairs of ports/ESPs/LSPs are established in a full mesh between all switching nodes. One Service Point from each service is attached to a pair of ports/ESPs/LSPs: the service is unaware that this protection is applied. Protection exists only at the port/ESP/LSP level and performs. For more information, see "PBB-TE Ethernet Switched Path Protection," page 87.

Spanning Tree E-LAN and E-TREE Protection

Spanning Tree protection works in partially or fully meshed topologies, with RSTP or MSTP selecting the best port for forwarding and eliminating looping.

While the service itself is unaware of the protection applied, it has one Service Point configured for each attached port. Frame formats (B-DA, B-VID, I-SID, C-VIDs, S-VIDs, or MPLS labels) can be programmed independently on each port.

4.6.6 PBB-TE Ring with Drop and Continue Protection

The following illustration shows how the Vitesse Carrier Ethernet Switch can use the Traffic Engineering and Path Protection capabilities of PBB-TE in a ring. One ESP is sent around the ring from headend to each node in a clockwise direction, while a second ESP is sent around the ring from headend to each node in a counter-clockwise direction. At each node, a "drop and continue" connection is made.

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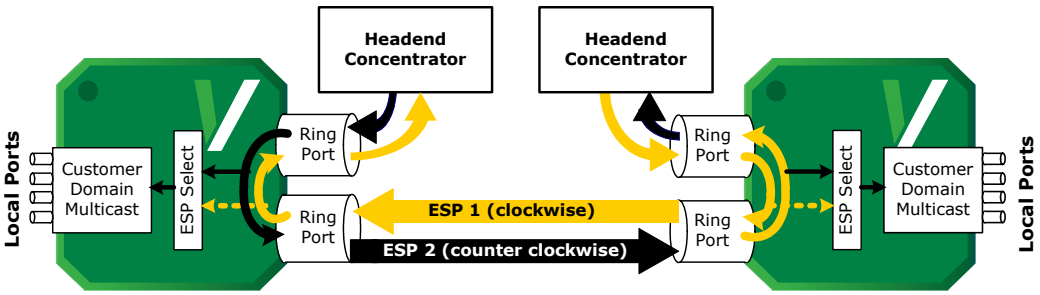
Figure 38. Ring with PBB-TE ESP Drop and Continue Protection



Drop and continue allows each node to drop a copy of any services needed, and continue the service around the ring to the next node. This is modeled after SDH SubNetwork Connection (SNC) protection, and is especially useful for redundant multicast distribution.

In this implementation, the ESP is multicast at each node into the I-domain and also to the next ring port. Within the I-domain, IGMP-based multicasting can be used to distribute service out to each subscribing customer. The CCM OAM hardware generator/checkers and protection switching can be used at the ESP level to protect the service feeds.

4.6.7 G.8032 Ethernet Ring with Shared Protection (E-SPRing)

The following illustration shows how the Vitesse Carrier Ethernet Switch can be used in the implementation of G.8032 E-SPRing.

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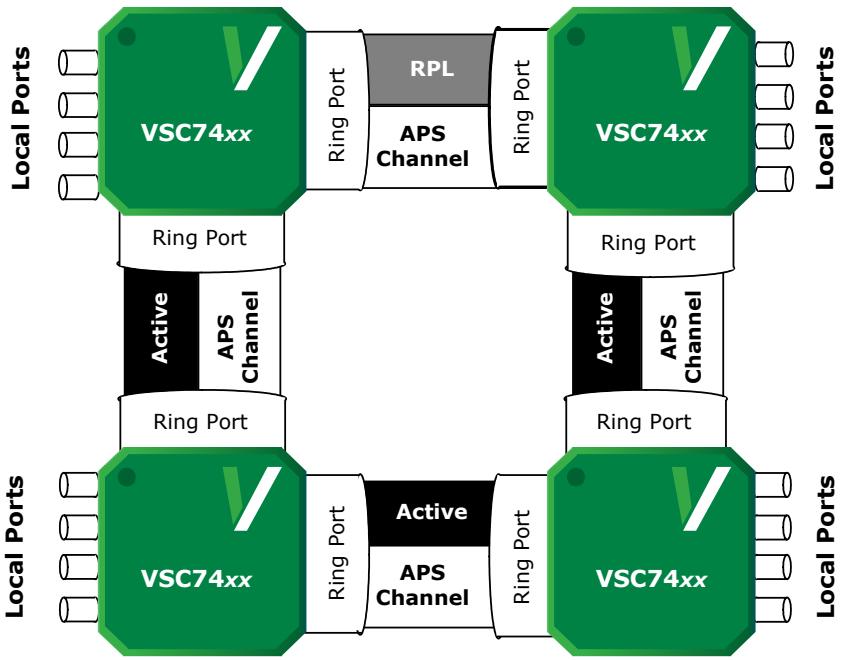
Figure 39. G.8032 E-SPRing Protection



E-SPRing nodes are connected in a ring topology, where one link is designated as the Ring Protection Link (RPL), and used only for redundancy. Each link reserves a VLAN to be used for OAM (APS Channel). CCM OAM is used over each APS Channel to assess the health of the link. The hardware-based CCM generator-checkers and protection switching mechanisms may be used here to provide fast failure detection and switchover. APS OAM is used by the software for coordination.

E-SPRing also takes advantage of the per-service, per-port tagging capabilities, since the tagging on the active port may be different from the tagging on the standby port.

4.7 Synchronous Ethernet Operation

Synchronous Ethernet as defined by ITU-T G.8261 allows for the transfer of quality network timing from a traceable reference to all network elements. Because this is a physical layer process, the timing quality does not vary with the network load.

The following illustration shows how Vitesse Carrier Ethernet Switch, MAC, and PHY devices can be used to implement Synchronous Ethernet.

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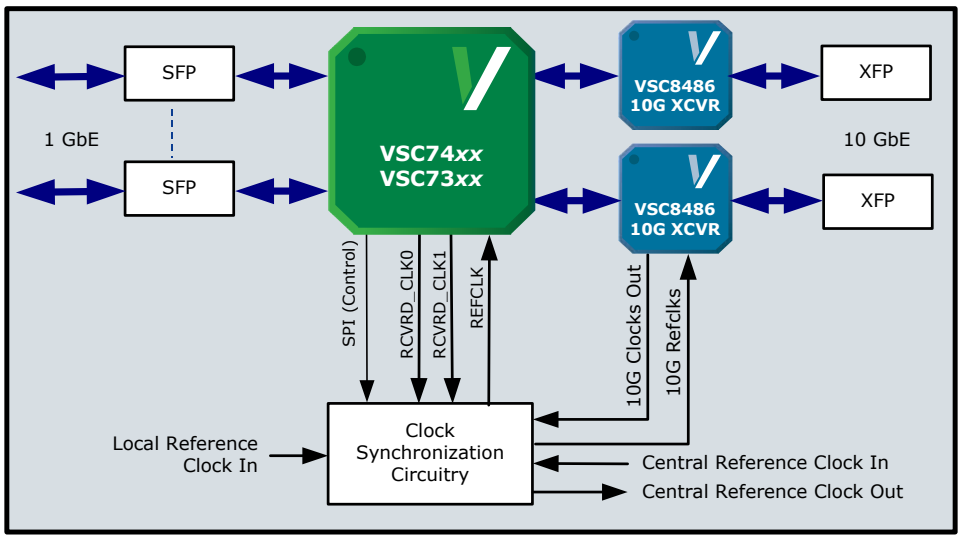
Figure 40. Synchronous Ethernet Application



The PHY devices recover the network timing from each line port and output the port recovered timing. The VSC7462 provides two clock outputs for redundancy and allows each output to select recovered timing from all possible line ports. If timing is compromised, the appropriate clock output can be squelched to assist with fast timing switchover in the clock synchronization circuitry.

Transmit timing is common for all ports and derived from the REFCLK, which is also used to clock the core logic. This is not an issue, because this clock is always available and tightly controlled by the clock synchronization circuitry during a timing failover.

The external clock synchronization circuitry is available from multiple third parties. This circuitry receives clocks from many possible sources and generates a set of stable output reference clocks to be used for transmit timing.

Reference clock input frequencies supported are 25 MHz, 125 MHz, or 156.25 MHz. The supported frequencies can be configured by using the RefClk_Sel[2:0] input pins.

For information about supported reference clock output frequencies, see Table 8, page 50.

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4.8 IEEE 1588 Operation

The Precision Time Protocol (PTP) is defined by IEEE 1588. The use of PTP allows for the network-wide synchronization of precise time of day. It is also possible to derive network timing. IEEE 1588 is a packet-based Layer 2 to Layer 4 process, depending on the PTP protocol frame formats used, and the timing quality therefore varies with the network size, topology and load. Network time accuracy based on IEEE 1588 improves with fewer hops from master to slave, and by having 1588-aware network elements. Synchronous Ethernet may also improve the network time accuracy due to the quality of the local clocks used throughout the network.

As compared to Synchronous Ethernet, the packet nature of IEEE 1588 enables carrying timing information across network islands that do not understand timing or do not take part in timing distribution. IEEE 1588-aware network elements (PTP devices) are however important for fast timing recovery in the event of a network failure and topology change. In this case, it is possible to pre-compute the effect of the topology change and instantly correct for it. The volume of protocol information exchanges with the master clock during topology changes is also reduced by having IEEE 1588 aware network elements.

The IEEE 1588 standard defines the following basic PTP devices, all of which can be supported by the VSC7462 device:

- Ordinary clock (master)
- Ordinary clock (slave)
- End-to-end transparent clock
- Peer-to-peer transparent clock
- Boundary clock

IEEE 1588 defines two different mechanisms for synchronizing clocks using PTP: delay request-response mechanism and peer delay mechanism. The following table summarizes the major differences between the two mechanisms.

Table 18. Delay Request-Response vs. Peer Delay Synchronization

	Delay Request-Response Mechanism	Peer Delay Mechanism
PTP messages used	Sync, Follow_Up, Delay_Req, and Delay_Resp	Sync, Follow_Up, Pdelay_Req, Pdelay_Resp, and Pdelay_Resp_Follow_Up
Master clock load	Master generates Sync and Follow_Up messages. Master responds with a Delay_Resp to Delay_Req messages from all slaves. With many slave clocks this may become a significant burden on the master clock.	Master generates Sync and Follow_Up messages. Master responds with Pdealy_Resp (and potentially Pdelay_Resp_Follow_Up) to Pdelay_Req messages from all peers (directly attached link partner devices)
Slave clock load	Slave clock is responsible for end-to-end delay measurement (slave-to-master direction only)	Slave clocks is responsible for link delay measurement. (Both sides of a link maintains own link delay measurements)

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Table 18. Delay Request-Response vs. Peer Delay Synchronization *(continued)*

	Delay Request-Response Mechanism	Peer Delay Mechanism
Transparent clock	End-to-end. End-to-end transparent clocks responds to traversing Sync, Follow_Up, Delay_Req, and Delay_Resp. End-to-end transparent clocks never initiates a PTP frame except as a response.	Peer-to-peer. Peer-to-peer transparent clocks responds to traversing Sync and Follow_Up messages but also actively participates in peer-to-peer link delay measurements - including PTP frame generation.
Delay measurements	End-to-end delay measurement that must following the path of Sync and Follow_Up messages Bi-directional paths between master and all slaves are required	Link Delay measurements on all links carrying Sync and Follow_Up messages and also alternative links. Bi-directional paths between master and slaves not required.
Network topology changes where Sync and Follow_Up is carried over new path	Timing recovery time depends on re-calculating End-to-end delay based on new technology.	Sync and Follow_Up messages over new path implicitly carry delay information for new path so no timing recovery is needed

4.8.1 Delay Request-Response Mechanism

The Precision Time Protocol works by sending Sync messages from one or more 1588 masters through a number of network elements, which may or may not be 1588-aware, to 1588 slaves. The Sync message contains a timestamp with the time of day. PTP can operate with:

- One-step clock: the timestamp within the Sync message is accurate.
- Two-step clock: the timestamp within the Sync message is approximate. The PTP device accurately records when the Sync message departs, and issues/updates a Follow_Up message with a correction time. The combination of Sync+Follow_Up timestamps is accurate.

VSC7462 support both one-step and two-step models, however, one-step accuracy is reduced as it requires timing approximation and software processing. In this document, the two-step clock model is used. For more information about one-step clock support, see "Boundary Clock," page 100.

Slave clock devices in the delay request-response model measures the end-to-end delay (round-trip) from slave to master. The slave clock sends out a delay_Req message and the master responds with a delay_Resp.

Network wide timing synchronization is possible by knowing local timestamps and the timing information included in the Sync, Follow_Up, Delay_Req, and Delay_Resp messages.

The following illustration shows the timing related PTP messaging within a timing domain using the delay request-response mechanism. Sync and Follow_Up messaging flow are shown on the left side of the figure and Delay_Req and Delay_Resp on the right. Sync messaging is shown as a Multicast flow but also Unicast to each individual slave in the network can be used. Only the Delay_Req and Delay_Resp flow for a single slave clock device is shown. All devices shown are IEEE 1588 aware.

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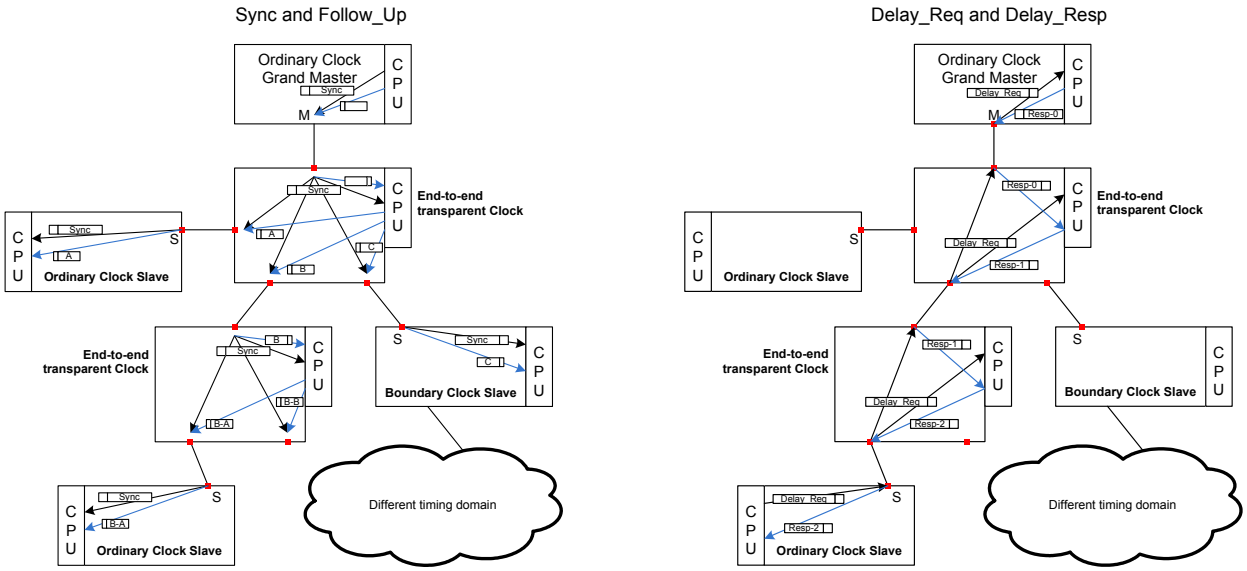
Figure 41. Delay Request-Response Messaging



All PTP devices shown can be implemented using the VSC7462The message handling is shown using the IEEE 1588 capabilities of the VSC7462, meaning:

- Red dots illustrate the points where hardware timestamping is performed. For more information about the hardware timestamping capabilities of the VSC7462 device, see "Layer 2 Hardware Timestamping," page 51.
- Within end-to-end transparent clocks Follow_Up messages are generated with specific timing information for each port being a member of the Sync distribution towards all slaves. Illustrated by indexing Follow_Up frames with A, B, C, B-A, and B-B.
- The CPU device can be either the internal CPU or an external CPU connected to the NPI port of the VSC7462 PTP software runs on the CPU device.
- End-to-end delay measurements using two step clock model requires transparent clocks to remember the Tx timestamp of outstanding Delay_Req messages (towards master) for inclusion in the Delay_Resp message (towards slaves). This book-keeping is required for each slave which timing path to the master goes through the transparent clock and is supported by the VSC7462 device using a combination of hardware and software capabilities.

The following table summarizes the protocol frames actions for the Delay request-response mechanism for PTP devices implemented using the capabilities of the VSC7462 device.

Table 19. PTP Protocol Frame Handling for Delay Request-Response Mechanism

	Sync	Follow_Up	Delay_Req	Delay_Resp
Ordinary clock master	Generation	Generation	Termination	Generation
Ordinary clock slave	Termination	Termination	Generation	Termination

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Table 19. PTP Protocol Frame Handling for Delay Request-Response Mechanism

	Sync	Follow_Up	Delay_Req	Delay_Resp
End-to-end transparent clock	Copy to CPU and forward. Measure Residence Time	Redirect to CPU. Update message to include residence time of associated sync message. Reinject message	Copy to CPU and forward. Measure residence time	Redirect to CPU. Update message to include residence time of associated Delay_Req Message. Reinject message

4.8.2 Peer Delay Mechanism

Peer delay Sync and Follow_Up message protocol handling is similar to Delay request-response. The only difference is that Sync messages or Follow_Up messages (when necessary) in the peer delay mechanism includes timestamp corrections for both Residence time and link delay.

The following illustration shows the timing related PTP messaging within a timing domain using the peer delay mechanism. Sync and Follow_Up messaging flow are shown on the left side of the figure and Pdelay_Req, Pdelay_Resp, Pdelay_Resp_Follow_Up on the right. Sync messaging is shown as a multicast flow but also Unicast to each individual slave in the network can be used.

1588 Slaves and 1588-aware network elements all implement a link delay request/response/response-follow-up handshake in order to measure the propagation delay between network elements. Pdelay_Resp_Follow_Up must be used for the VSC7462 device. Link delays can be measured on all links in the network topology to have link delays pre-computed in the event of network failure. Link delay measurements are illustrated between:

- Slave clock and transparent clock
- Two transparent clocks
- Master clock and transparent clock. (A master clock needs not initiating a link delay measurement, which is why the figure only have one way arrows on this link.)

It should be noted that PTP devices on both sides of a link performs their own link delay measurement. All devices shown in the following illustration are IEEE 1588 aware.

For the peer delay mechanism network wide timing synchronization is obtained from local timestamps and the timing information included in the Sync and Follow_Up messages.

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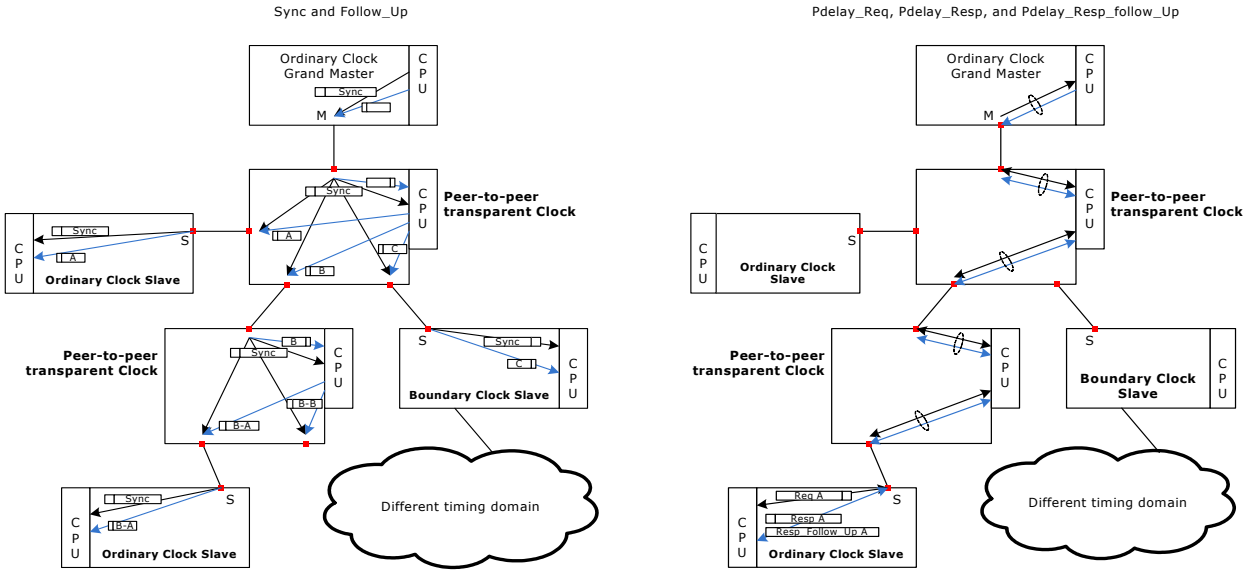
Figure 42. Peer Delay Messaging



All PTP devices shown can be implemented using the VSC7462.The message handling is shown using the IEEE 1588 capabilities of the VSC7462, meaning:

- Two-step clock model.
- Red dots illustrate the points where hardware timestamping is performed. For information about the hardware timestamping capabilities of the VSC7462, see "Layer 2 Hardware Timestamping," page 51.
- Within peer-to-peer transparent clocks Follow_Up messages are generated with specific timing information for each port being a member of the Sync distribution towards all slaves. Illustrated by indexing Follow_Up frames with A, B, C, B-A, and B-B.
- The CPU device can be either the internal CPU or an external CPU connected to the NPI port of the VSC7462 device PTP software runs on the CPU device.

The following table lists the protocol frames actions for the Peer delay mechanism for PTP devices implemented using the capabilities of the VSC7462.

Table 20. PTP Protocol Frame Handling for Peer Delay Mechanism

	Sync	Follow_Up	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_Follow_Up
Ordinary clock master	Generation	Generation	Termination	Generation	Generation
Ordinary clock slave	Termination	Termination	Generation Termination	Generation Termination	Generation Termination

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Table 20. PTP Protocol Frame Handling for Peer Delay Mechanism *(continued)*

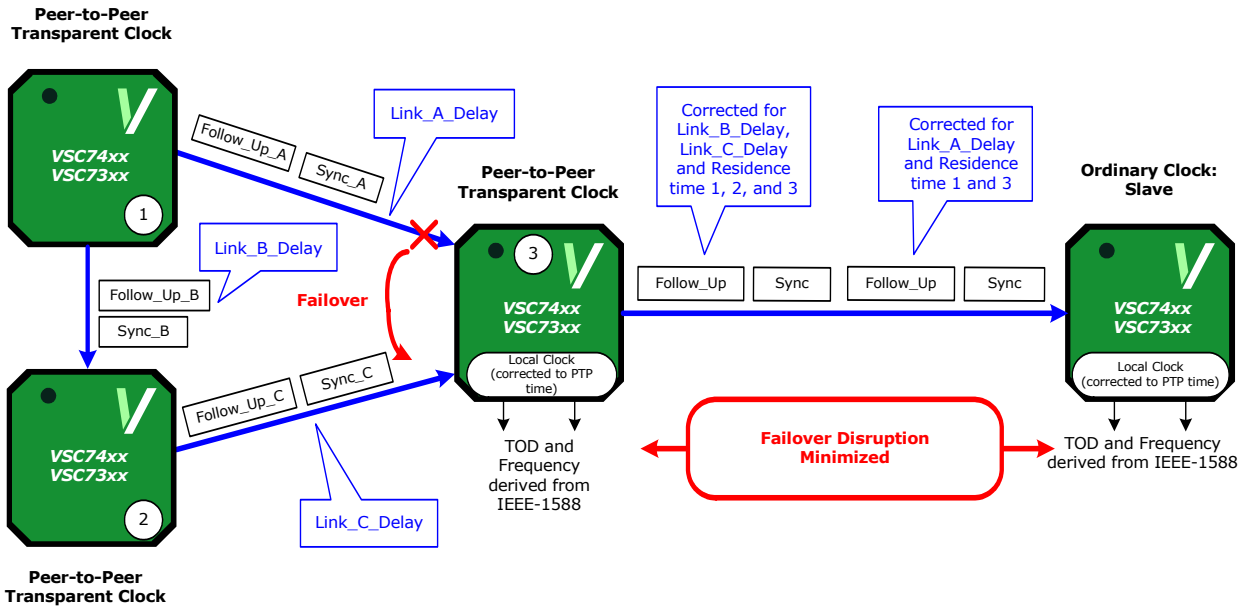
	Sync	Follow_Up	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_Follow_Up
Peer-to-peer transparent clock	Copy to CPU and forward. Measure Residence Time	Redirect to CPU.(1) Update message to include residence time and link delay of associated Sync Message. Reinject message	Termination Generation	Termination Generation	Termination Generation

1. If this transparent clock device is the first device on the path from master towards slave(s) that do not support one-step clock, it must generate a Follow_Up message including the residence time of associated Sync Message.

Implicit Timing Redundancy Using Peer Delay Mechanism

The following illustration shows how the peer delay mechanism implicitly includes delay changes (both residence time changes and link delay changes) in Follow_Up messages when traffic is re-routed so that disruption due to failovers are minimized. This capability requires that link delays between transparent clocks 1 and 2 and between 2 and 3 are pre-computed using the Pdelay_Req, Pdelay_Resp, and Pdelay_Resp_Follow_Up messaging (not shown).

Figure 43. Failover Disruption Using Peer Delay Mechanism



4.8.3 Boundary Clock

The primary purpose of boundary clocks is to interface different timing domains. Boundary clocks are also used to interconnect timing domains where one domain uses peer delay mechanism and another the delay request-response mechanism. For such applications it may be required that a bridge in the network that is also a boundary

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clock supports both timing mechanisms concurrently. That is, link delay measurements must be performed on some set of ports of the bridge device whereas also end-to-end delay measurements must be processed correctly. Boundary clock functionality is also supported by the VSC7462.

4.8.4 One-Step Clock Operation

One-step clock operation is also supported by the VSC7462. One-step clocks prime advantage over two-step is that all timing information is included directly in the Sync message so that a Follow_Up message can be avoided.

One-step clock is supported using a combination of hardware accurate arrival timestamps (Rx timestamps) and software generated departure timestamps (Tx). The precision of approximated departure timestamps is considerably improved by the following two capabilities of the VSC7462 device:

- If the one-step PTP software is running on the internal CPU the super priority frame injection mechanism can be used to minimize the uncertainty in delay from the Sync frame is ready for departure in the CPU until it is seen on the wire of the departure port. Super priority injection provides an unbuffered path from the CPU Device directly to a departure ports and totally bypasses the normal L2 forwarding flow. See section XXX for a description of the super priority frame inject mechanism.

Hardware delay measurements using the precise Tx timestamping capability can be performed in advance of timing distribution. A delay measurement test is set up by the CPU device running the one-step PTP software:
External CPU The VSC7462 is configured to both Rx and Tx timestamp the delay test frames. An average delay is calculated from this timestamp information and is included in all timing updates within the PTP messages. Note that the reference clock of the external CPU can be frequency locked to the reference clock of the VSC7462 device using reference clock inputs or outputs.

Internal CPU The VSC7462 is configured to Tx timestamp the delay test frames. Software measures the departure timestamp when the frame is injected to the switch core on its own. An average delay is calculated and included in all timing updates within the PTP messages.

4.8.5 Redundant Masters and Multiple Timing Domains

The following illustration shows a provider network that is synchronized using IEEE 1588. Cell towers are connected to this provider network, and different wireless operators have their antennas connected to the cell towers. Different models exists on how to distribute timing to the cell towers and to the equipment from each wireless operator.

- Wireless operator 3 is the same as the operator of the provider network and the timing needs of the wireless equipment for this operator is fulfilled by extending the provider network timing to include cell towers.

- Wireless operator 2 provides own timing to his/her wireless equipment in the cell towers. This timing information is carried through the provider network as a high priority data service with sufficiently low transmission delay variation as needed by the timing accuracy requirements of the wireless operator.

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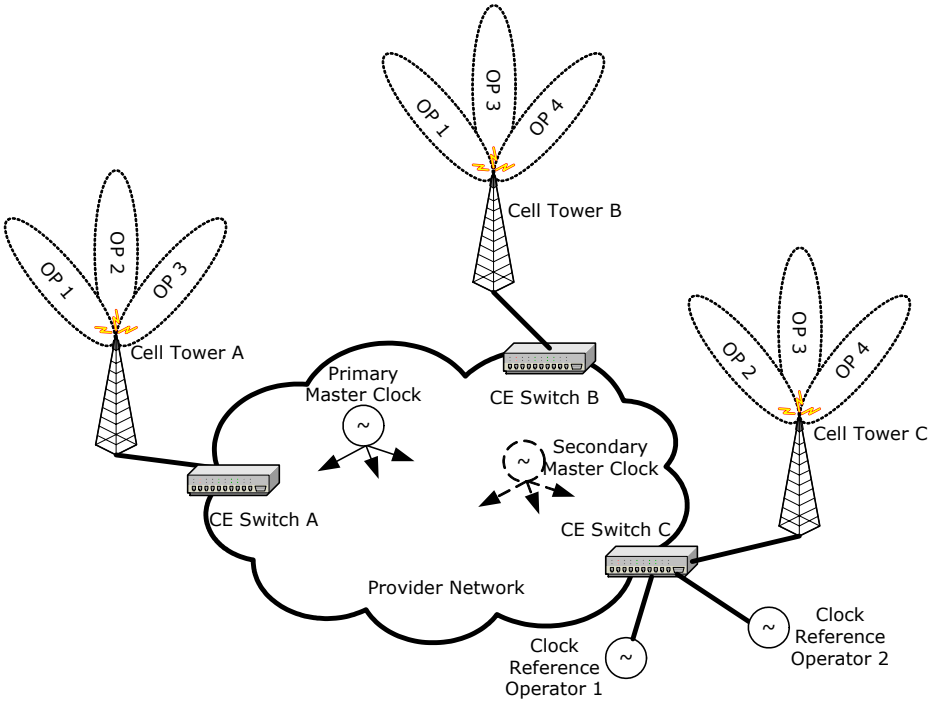
- Wireless operator 1 has bought a timing service from the network provider. That is, the Provider network takes active part in distributing timing to operator 1's wireless equipment in the cell towers. The Provider network equipment operates as transparent clocks within operator 1's timing topology.
- Wireless operator 4 obtains his timing by means not involving the Provider network at all.

The following illustration shows that many timing domains can exist concurrently in a network. As a result, IEEE 1588 aware equipment must be able to do very specific filtering of PTP messages. If, for example, the clock references of operator 1 and 2 arrives on the same port of CE Switch C, frame filtering must make sure to map operator 2's PTP frames to a data service whereas operator 1's PTP frames must be processed. Filtering per timing domain and port is supported on the VSC7462 by use of VCAP S2 ACEs.

Figure 44. Cell Tower Timing



4.8.6 IEEE 1588 Two-Step Clock Processing Flow

The VSC7462 device can accurately implement two-step clocks as needed by implementing 1588-aware network elements (Peer-to-peer and end-to-end transparent clock) in various switches and routers. It can also be used to implement cost-effective IEEE 1588 master and slave devices (ordinary clock). The following illustration shows the approach.

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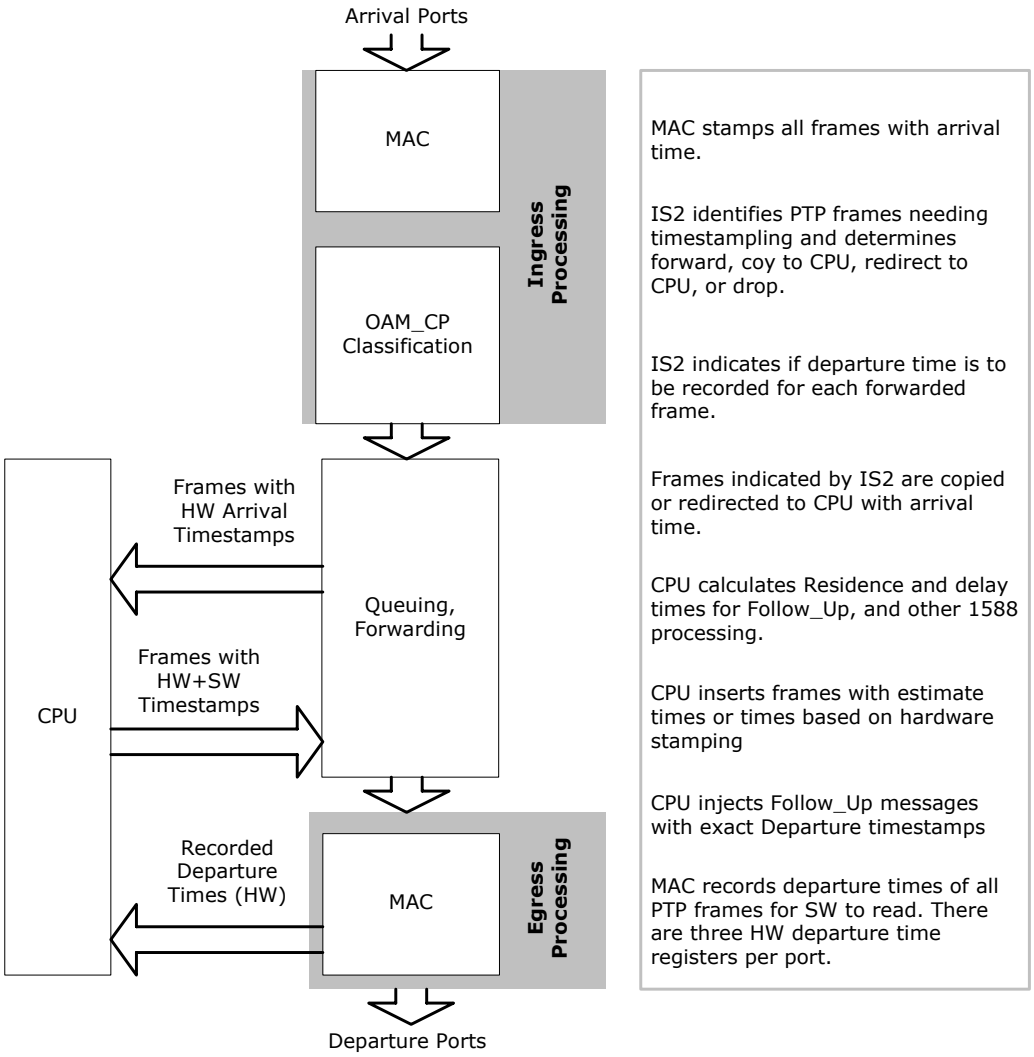
Figure 45. IEEE 1588 Processing Concept



All frames are timestamped upon arrival using a hardware timer in the MAC, providing 20 nS accuracy and a resolution equal to the system clock period. PTP frames of interest may be forwarded as normal, forwarded as normal plus copied to the CPU, redirected only to the CPU, or dropped.

The time of departure for PTP frames of interest is recorded by the MAC with 20 nS accuracy and a resolution equal to the system clock period. A separate departure time is maintained for each port for hardware-forwarded and software-forwarded PTP frames of interest.

The CPU now receives PTP frames with the timestamp when they were sent, along with an accurate timestamp when they were received in the VSC7462. The CPU is also provided an accurate departure time for when PTP frames depart from the VSC7462 device.

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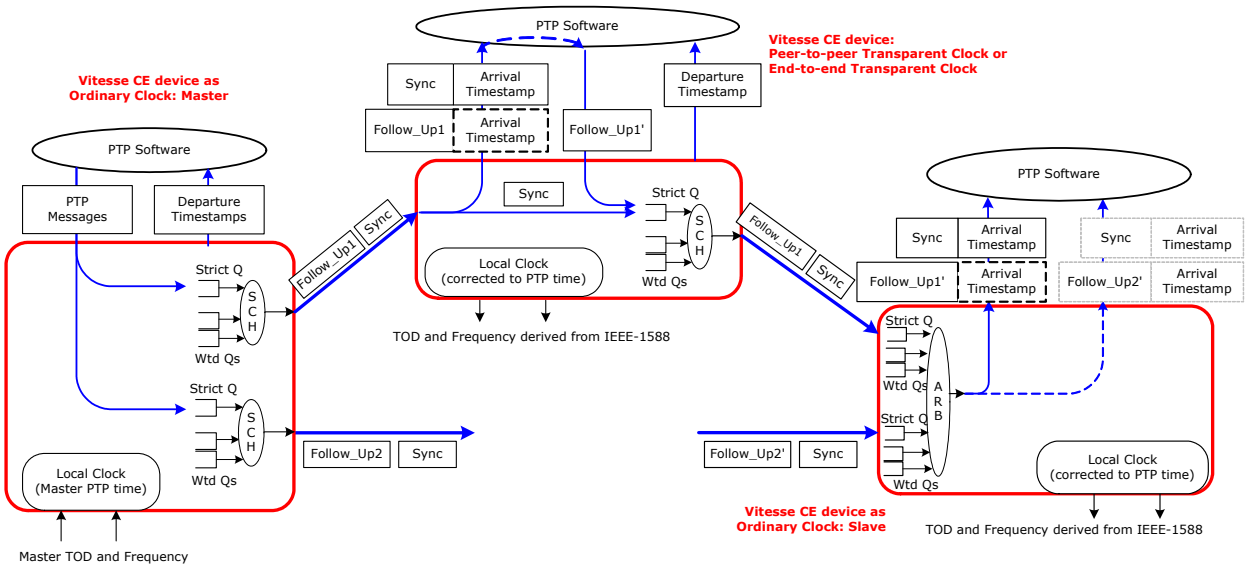
To calculate Residence time, the CPU gets a copy of the frame upon arrival with the arrival timestamp and also gets the departure time. To implement two-step clocks, the CPU sends the Sync message with a timestamp based on the internal timer and an estimated insertion delay, monitors the departure time, and then sends a Follow_Up message with a completely accurate timestamp.

4.8.7 IEEE 1588 Two-Step Clock

The following illustration shows PTP device examples implemented using the VSC7462 and associated software. In all PTP devices, the PTP frames are QoS classified to the strictest highest priority for both ingress and egress to assure delivery and obtaining low latency. PTP frame injection from software is done using the super priority inject mechanism where frames are sent directly out the egress link with no internal queuing within the switch core. Only Sync and Follow_Up messaging is shown here, but delay measurement messages are treated the same.

Figure 46. PTP Device Examples



Sync messages are copied to CPU with arrival timestamp and forwarded through hardware for low latency. Departure timestamp is captured for the CPU to read.

Follow_Up messages are redirected to CPU, updated with residence time, and injected again to follow Sync messages. The arrival timestamp of Follow_Up messages can be provided to CPU, however, is not used by PTP software.

The ordinary clock slave receives timing information from two timing sources. Only the PTP frames from the primary master is forwarded to CPU. PTP frames from secondary master can be monitored through statistics counters but are otherwise discarded by the hardware of the VSC7462. Fast switch over to secondary master is provided through only a few configuration register accesses. Alternatively, the slave can be set up to forward PTP frames from both masters to PTP software and allow the primary versus secondary source selection be done at SW level.

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IEEE1588 over MPLS is supported using the MPLS Co-Processor FPGA providing EoMPLS.

4.8.8 VCAP S2 PTP Message Handling

TBD

4.8.9 Quality of Service (QoS) Delivery

The VSC7462 is designed with a powerful set of QoS features to guarantee SLA delivery for each service, as well as for each Class of Service. The device uses per-service QoS overlaid on top of class-based QoS.

The following illustration shows the approach.

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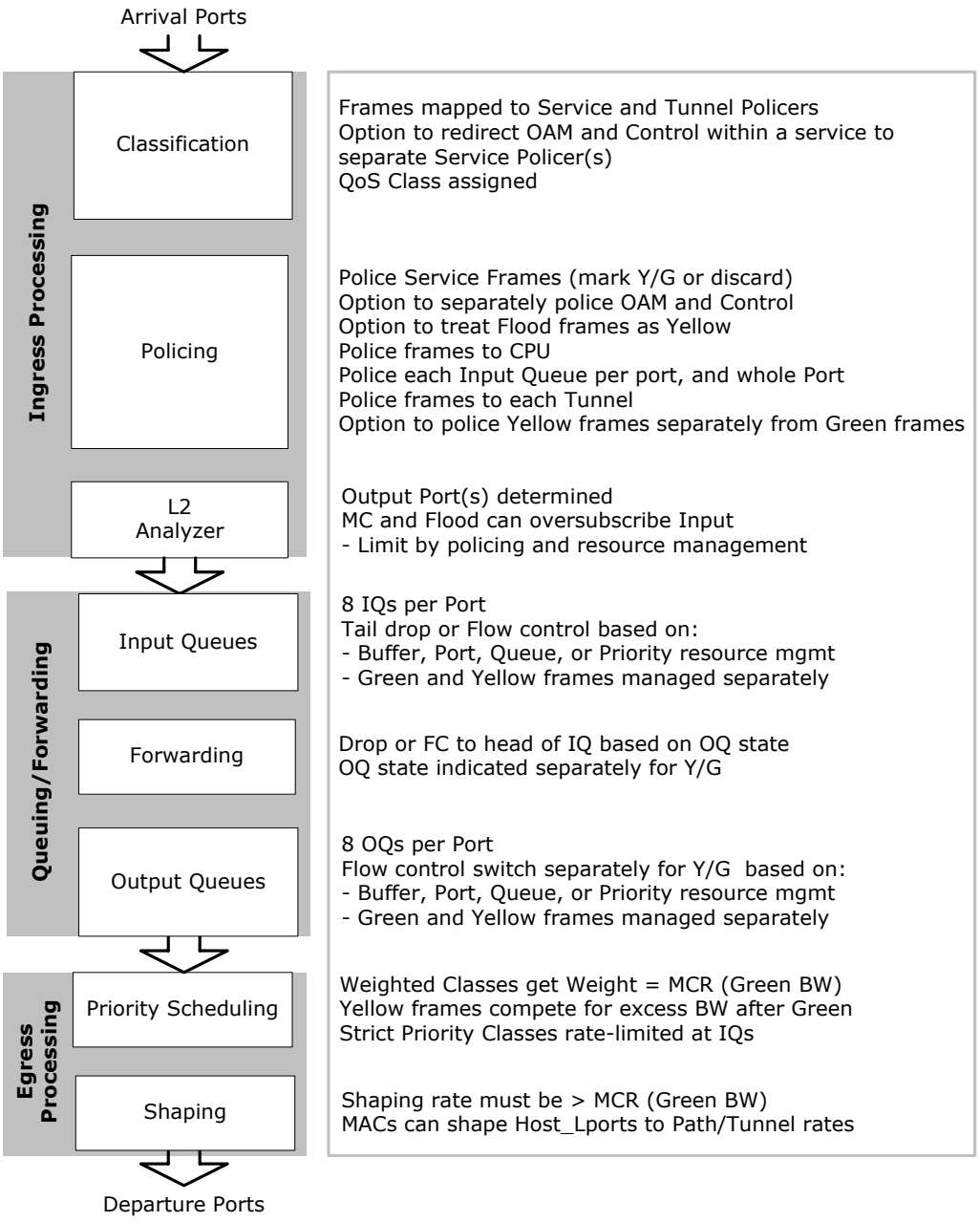
Figure 47. Carrier Ethernet Switch QoS Service Concept



In this approach, all frames are mapped to a Class of Service, and all frames are marked whether they are Committed (Green) or Discard Eligible (Yellow). Frames may be metered (policed) in the VSC7462, or they may have been metered in other locations of the network and must be correctly interpreted by the VSC7462.

Delivery of Green frames is guaranteed by controlling the amount of Green data admitted into the switch, allocating sufficient buffers for Green data, and scheduling enough bandwidth from each port to deliver all Green data.

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These mechanisms help manage other frames not to impact delivery of Green frames:

- Policing at Service, Tunnel, Port, Priority, and Global levels
- Protecting the integrity of control and management planes by policing OAM and other control/management protocols
- Treating Flood frames as Yellow, and policing Flood and Yellow frames
- Rate-limiting classes, which are given strict priority
- Discarding Yellow/Flood frames at the head of the Input Queues if there are insufficient Yellow buffers at the Output Queues
- Limiting buffer use at the Queue, Port, Priority, and Buffer levels within the pool of shared buffers
- Scheduling output queues in a bandwidth-aware manner, with the ability to deliver excess bandwidth as available

Performance properties (bandwidth, delay, delay variation) of each service class can be established due to the class-based queuing, scheduling, and buffer management.

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5 VCore-III System and CPU Interfaces

This section provides the functional description of blocks and interfaces related to the VCore-III on-chip microprocessor system.

The VSC7462 device contains an embedded CPU. This is a powerful, MIPS24KEc-compatible microprocessor system that includes a high-bandwidth DMA engine. The VCore-III system is capable of controlling the device independently or it can support an external CPU, relieving the external CPU of the otherwise time-consuming tasks of transferring frames, maintaining the switch core, and handling networking protocols. When enabled, the VCore-III CPU boots from either the parallel interface (PI) or from the serial interface (SI).

An external CPU can be connected through either the parallel interface (PI) or the serial interface (SI). Both interfaces are available for external CPU access when the VCore-III is disabled. If the VCore-III is enabled, the VCore-III boot interface cannot be used by an external CPU.

Both the VCore-III CPU and the external CPUs have access to internal chip registers for configuring, monitoring, and collecting statistics.

The VCore-III microprocessor system includes a number of functional blocks and registers that are tightly coupled to the VCore-III CPU. The external CPU can also access these through an indirect addressing scheme. They are available both when the VCore-III is enabled and when it is disabled.

The following illustration shows how the serial and the parallel controllers can operate in either master or slave mode. When the VCore-III CPU is enabled, it takes ownership of the boot-interface. When the serial or parallel controller is in slave mode, it accesses the chip registers, via these registers the CPU Memory Domain (all blocks and directly attached VCore-III registers) are accessible via indirect access.

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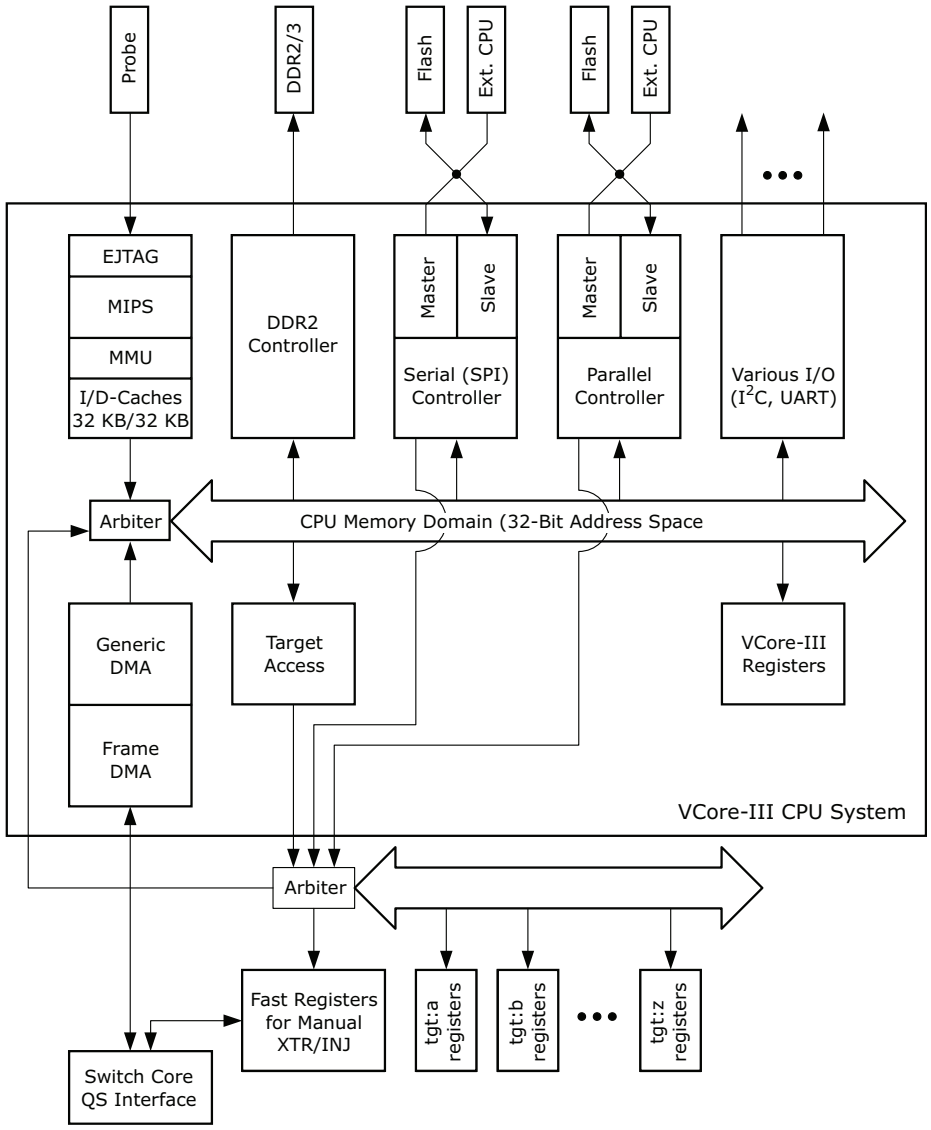
Figure 48. VCore-III System Block Diagram



VCore-III is enabled by pulling the VCore_Cfg[1] strapping pin low, which causes VCore-III to take ownership of its boot interface. By default, the VCore-III CPU boots from the SI interface, but it can be configured to boot from the PI instead by pulling the VCore_Cfg[0] strapping pin low. It is not possible to attach an external CPU to the interface that the VCore-III CPU uses for booting. If the VCore_Cfg[1] strapping pin is pulled high the VCore-III is disabled. The following table summarizes the VCore-III, SI and PI configurations.

Table 21. VCore-III Configurations

Level of Strapping Pins		Behavior		
VCore_Cfg[1]	VCore_Cfg[0]	VCore-III	SI owned by:	PI owned by:

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Table 21. VCore-III Configurations *(continued)*

Level of Strapping Pins		Behavior		
0	0	Enabled and boots from PI	External CPU(1)	VCore-III
0	1	Enabled and boots from SI	VCore-III	External CPU(1)
1	X	Disabled	External CPU	External CPU

1. The VCore-III can take ownership of the non-boot interface though register configuration. <REFERENCE>

The VCore_Cfg[0] configuration must not be changed after the device has been released from reset. While VCore_Cfg[1] is set high, it causes hard-reset of the VCore-III microprocessor. For more information, see "VCore-III Clocking and Reset," page 111.

By default, the MIPS24KEc microprocessor operates in little endian mode, however by using the VCore_BE_en configuration input, it is possible to reconfigure the MIPS24KEc to operate in big endian mode. In big endian mode, the VCore-III and chip registers must be byte-swapped when reading and writing, see the API documentation for more information <TBA add reference to API documentation>.

The description of the VCore-III system is done with a little endian system in mind..

5.1 VCore-III CPU

The VCore-III CPU is a MIPS24KEc-compatible microprocessor featuring a Memory Management Unit and separate 32-kilobyte instruction and 32-kilobyte data caches.

The boot-vector of the VCore-III CPU points to the beginning of keseg1 in the virtual address space, which maps to physical address 0x00000000.

The VCore-III system interrupt inputs are mapped to VCore-III CPU interrupt inputs 0 and 1, respectively.

For more information, see the MIPS documentation.

5.1.1 JTAG Control

When the Test_Mode pin is pulled high, the JTAG interface is attached to the VCore-III JTAG. When the VCore_ICE_nEn pin is pulled low, the JTAG interface is attached to the MIPS24KEc EJTAG debug controller. When pulled high, it is attached to the JTAG boundary scan controller.

5.2 DMA Engine

The DMA Engine has a dedicated connection to the switch core and can move frames between system memory and switch core without loading the VCore-III or external CPU.

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For more information about how to use the DMA Engine, see "Frame DMA (FDMA) Engine," page 113.

5.3 External CPU Access

TBD

5.4 VCore-III Clocking and Reset

The VCore-III CPU always operates at twice the frequency of the VCore-III system. The frequency of the VCore-III system (with the VCore-III CPU) can be changed from the <ADD REF TO HSIO REG>, this can be done "on the fly" while the VCore-III CPU is running. Some devices (UART, two-wire serial, and DDR2 SDRAM controller) require a constant clock frequency during normal operation, so software should change the clock frequency during boot operation only. For information about the available frequencies, see <ADD REF TO HSIO REG DESCRIPTION>.

The DDR frequency is the same as the VCore-III system frequency, so the frequency of the VCore-III system should not exceed the speed of the available DDR2 SDRAMs. For example, if DDR533 is used, the clock for a DDR533 SDRAM must not exceed 266 MHz. In this example, the maximum VCore-III system frequency, when equipped with DDR533 SDRAM, is then 250 MHz.

The VCore-III system can be soft-reset by using RESET.CORE_RST_FORCE. By default this will reset the complete VCore-III system and the VCore-III CPU. It is possible to protect the VCore-III system from reset by configuring RESET.CORE_RST_CPU_ONLY, in this case a soft-reset will only affect the VCore-III CPU. When soft-resetting the VCore-III system, the Frame DMA must be disabled.

A hard reset of the chip will always cause the VCore-III system and VCore-III CPU to be reset. By default, a soft reset of the chip will cause the VCore-III system and VCore-III CPU to be reset, however it is possible to protect both the VCore-III system and VCore-III CPU from chip-level soft reset by configuring RESET.CORE_RST_PROTECT.

The VCore-III system contains a watchdog timer, a reset caused by the watchdog timer works in the same way as a soft reset (set via RESET.CORE_RST_FORCE) so the configuration that protects the VCore-III system from soft-reset also protects it from watchdog reset (again, the VCore-III CPU is always reset by soft and watchdog resets).

When the VCore-III CPU is disabled by using the VCore_Cfg[1] configuration input, it is possible to release the VCore-III CPU via RESET.CPU_RELEASE. After this field is set, the VCore_Cfg[1] no longer has any effect (a hard reset of the chip will bring everything back to the initial state).

5.5 VCore-III Shared Bus

The VCore-III shared bus is a 32-bit address and 32-bit data bus with dedicated master and slave interfaces. The VCore-III CPU, the Frame DMA, and an external CPU are masters on the shared bus, and only they can start accesses on the bus.

The shared bus uses byte addresses, and transfers of 8, 16, or 32 bits can be made. For 16-bit and 32-bit accesses, the addresses must be aligned to 16-bit and 32-bit

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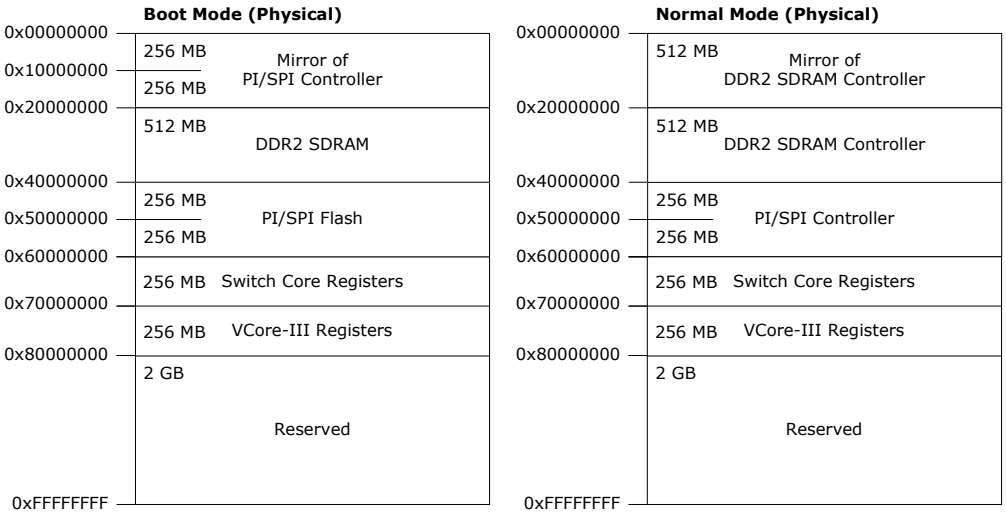
addresses, respectively. To increase performance, bursting of multiple 32-bit words on the shared bus can be performed.

5.5.1 Shared Bus Memory Map

All slaves are mapped into the VCore-III system's 32-bit address space and can be accessed directly from the VCore-III CPU, Frame DMA, or External Interface. There are two possible mappings of VCore-III shared bus slaves:

- Boot Mode. This mode is active after power-up and reset of the VCore-III system. In this mode, the PI and SPI controller is mirrored into the lowest address region.
- Normal Mode. In normal mode, the DDR2 SDRAM controller is mirrored into the lowest address region.

Figure 49. VCore-III Shared Bus Memory Map



Changing from boot mode into normal mode (GENERAL_CTRL.BOOT_MODE_ENA) interchanges PI/SPI for DDR2 SDRAM memory space.

The VCore_Cfg[0] strapping pin configures whether the VCore-III microprocessor boots from either PI or SPI interface. The PI/SPI controller always places the boot-interface in the lower 256 Mbyte of the 512 Mbyte space used by the controller. For information about strapping, see <TBA: Reference to the table in "CPU System and CPU Interfaces" showing the strapping map>.

By default, the VCore-III cannot access the interface that it did not boot from; that interface is in slave mode, so an external CPU can use it for accessing the chip. However, by using GENERAL_CTRL.IF_MASTER_ENA it is possible to force the non-boot interface into master mode (that is, owned by the VCore-III). When controlled by the VCore-III, the non-boot interface is accessible through the upper half of the PI/SPI controller's 512 Mbyte region.

In boot mode, the PI/SPI controller's memory is mirrored into the lowest region of the memory map. In Normal Mode, the DDR2 SDRAM controller's memory is mirrored into the lowest region of the memory map. If the contents of the PI/SPI memory and DDR2

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SDRAM memory are the same, it is possible for software to execute from the mirrored region when swapping from boot mode to normal mode. Otherwise, software has to execute from the PI/SPI controller's memory when changing from boot mode to normal mode.

The registers for the arbiter, two-wire serial interface controller, UART controller, timers, and Watchdog timer are all mapped into the "VCore-III Registers region". For information about addresses, see "Overview of Registers," page 123.

5.6 Frame DMA (FDMA) Engine

The Frame DMA (FDMA) engine is a modified general-purpose DMA engine. In addition to standard DMA operations, the FDMA extracts and injects frames directly from/to the Queuing system. It can also inject frames directly to ports using dedicated high-priority injection paths.

The FDMA engine has access to the entire memory map of the CPU system. Although DDR2 SDRAM memory is the most obvious working area for FDMA, it is possible to transfer data across the parallel interface or from the SPI interface.

The FDMA engine features eight individual channels that can be configured for general purpose data transfers, frame injection, or frame extraction. A single channel can only operate in one of these modes.

The three major capabilities of the FDMA engine are:

- General-purpose transfers
- Frame injection
- Frame extraction

While it is possible to manually instruct the FDMA engine to move arbitrary blocks of memory, most of the time it is desirable to organize blocks of memory into containers that hold information about length, offsets, destinations, and so forth. The FDMA engine supports this functionality through the use of DMA Control block structures (DCBs). DCBs are structures that can be linked together to form lists of multiple DCBs, where each DCB has one corresponding data area.

The following illustration shows the general layout of a DCB.

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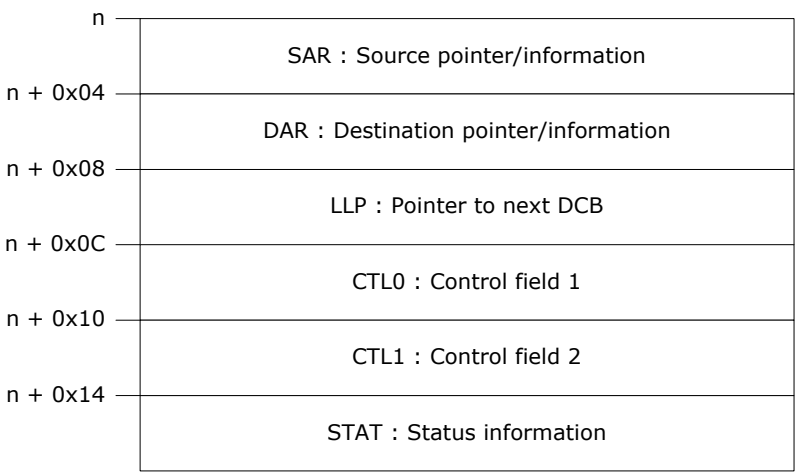
Figure 50. DCB General Layout



Injection and Extraction One Ethernet frame can be contained within the data-area of a single DCB or it can be split across multiple data areas of consecutive DCBs. The data-area of one DCB can never contain more than a single Ethernet frame.

DCBs and the corresponding data-area must be aligned to 32-bit addresses. The encoding of specific DCB-fields differs when used for general-purpose data transfers, injection, or extraction. The sections dealing with each transfer type will also explain how to configure the specific fields of the DCBs.

The LLP field in the DCB is always used for linking DCBs together in a chain. The FDMA engine interprets the LLP field as a 32-bit pointer, when chaining DCBs together the LLP of one DCB must point to the SAR field of the next DCB. The last DCB in a chain must always have the LLP field set to NULL (0x00000000).

The following illustration shows two examples of DCB chains with corresponding data areas and illustrate that chains of DCBs and the corresponding data-areas can be placed in any order inside the memory and that the data areas can be of different sizes. For the general purpose DCBs, both SAR and DAR fields points to memory areas. For Injection and Extraction, either SAR or DAR points to a memory area.

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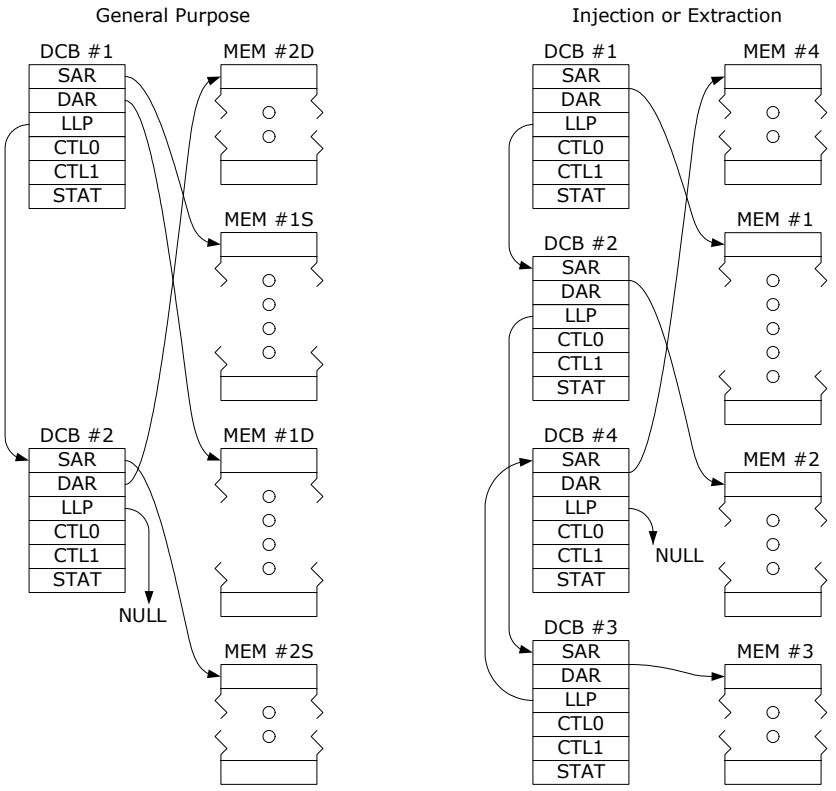
Figure 51. DCB Chain Examples



It is desirable to get interrupts when the FDMA engine finishes processing DCBs for injection or extraction. Injection interrupts are generated after one complete frame (which may take up multiple DCBs) has been injected. Extraction interrupts are generated for each DCB that the FDMA engine extracts (for frames that span multiple DCBs there will be more than one extraction interrupt).

The interrupt that must be used is called BLOCK; it can be configured on a per-channel basis by using the <TBA:DMAC-'PATH'>.MASK_BLOCK register. The per-frame injection interrupt is handled by disabling interrupts for each DCB that does not contain end-of-frame. When Extracting, software must manually check each DCB for an end-of-frame indication (because the length of a frame is not normally known before it is received).

The FDMA engine autonomously processes chains of DCBs, so adding DCBs to an active chain requires care. Chains of new DCBs must be built separately from the active chain. When the new chain is completed, it must be added to the end of the active chain. Then the status of the channel must be checked <TBA:DMAC-'PATH'>.CH_EN_REG.CH_EN, if the channel is disabled - the pointer to the first DCB that has not yet been processed by the FDMA engine must be written to the <TBA:DMAC-'PATH'>.LLP register of the corresponding channel and then the channel must be re-enabled. By looking at the DCB.STAT field it is possible to determine if the DCB has been processed by the FDMA engine.

Note Channels must have been configured for general purpose, injection, or extraction before adding chains of DCBs. For more information, see "Initialization of FDMA Channel for Injection," page 119.

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The switch stores local information about each frame in the Internal Frame Header (IFH). When extracting a frame from the Queuing System, the IFH is prepended to the frame data (it is located before the actual Ethernet frame). When injecting a frame into the Queuing System or to an Ethernet port via Super priority injection, a suitable IFH must be generated and prepended to the frame data (before the actual Ethernet frame). For information about interpreting and generating IFH, see <TBA add reference to IFH info section>.

The FDMA engine always interprets frame data in big endian format. This means that the CPU (no matter which "endianness" it uses) must access extracted frame data in line-order by doing byte-accesses on incrementing byte-addresses. The first byte received by the switch is put on the lowest address, and subsequent bytes are put on incrementing byte-addresses.

When constructing frames for transmission, the CPU must also put frame data on incrementing byte-addresses. The first byte that the switch transmits is put on the lowest byte-address, and subsequent bytes are put on incrementing byte-addresses.

Note Generally, when the CPU is in big endian mode, it is able to directly access fields in the frames that are wider than 1 byte. When the CPU is in little endian mode, software may swap bytes when accessing fields wider than 1 byte.

5.6.1 General-Purpose Data Transfers

TBD

5.6.2 Injection

Frames can be injected to the Queuing system or directly to Ethernet ports. The Queuing System has two complete queues available for injection from the CPU system. The priority of the frame must be encoded into the IFH (Internal Frame Header) prior to injecting the frame, see <TBA reference to IFH info section>.

The CPU System selects a destination by injecting to one of several injection groups. Each group maps to either one of the Queuing System queues, or one of the port injection groups. Each frame has one (and only one) injection group destination encoded directly into the DAR field of the DCB. If the frame is split across multiple DCBs, all DCBs must be configured with the same destination injection group.

Table 22. FDMA Injection Groups

Injection Group	Description
0	CPU Queue 0 of the Queuing System
1	CPU Queue 1 of the Queuing System
2	<TBA: Which port?>
3	<TBA: Which port?>
4	<TBA: Which port?>

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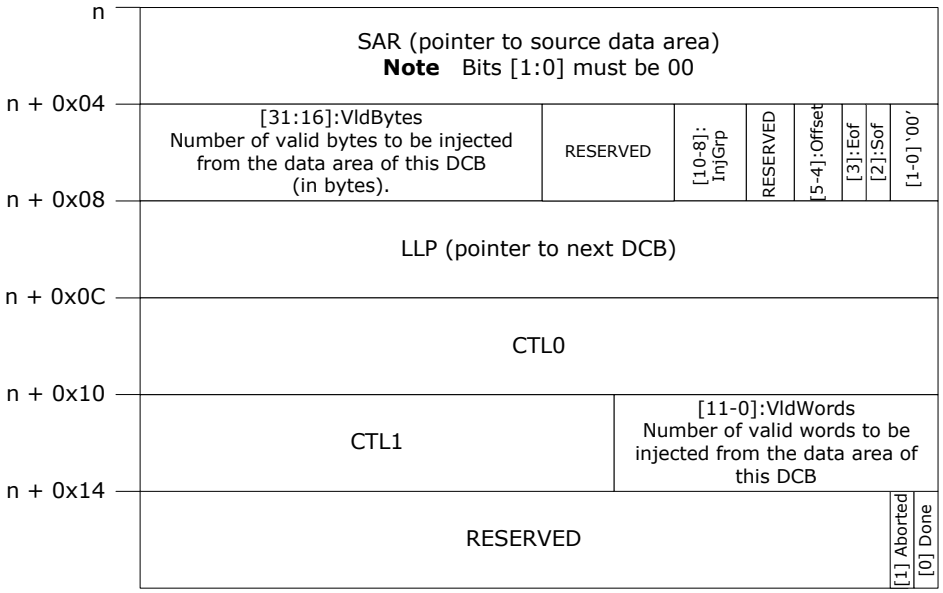
5.6.3 Initialization of Injection DCBs

This section contains information about configuration of DCB fields for injection of frames to the Queuing System or directly to front ports.

The following illustration shows the detailed layout of an injection DCB. Each field is described in the following sections, except LLP, which was described previously.

Figure 52. Injection DCB Layout



5.6.4 SAR Field Encoding for Injection

For injection DCBs, the SAR must contain a pointer to the first 32-bit word of frame data. While the SAR must point to a 32-bit data word, all bytes in that word do not have to be valid. The Offset field in the DAR specifies the number of valid bytes. The following table shows the encoding of the Offset field depending on the number of bytes that are valid in the first 32-bit word to which the SAR points.

Table 23. DAR Offset Field Encoding

Valid Byte-Addresses Inside the First 32-bit Data-Word	DAR: Offset
All byte-addresses (0,1,2, and 3) are valid(1)	0
Byte-addresses 1,2, and 3 are valid(1)	1
Byte-addresses 2 and 3 are valid(1)	2
Only byte-address 3 is valid	3

1. It is possible to still use data-offset, even when all the frame data of the DCB is contained inside the first word of the data-area. For example, if only byte-address 2 is valid, data-offset is still 2 (and valid-bytes is 1).

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5.6.5 DAR Field Encoding for Injection

When injecting frames the DAR field holds destination information. The destination group (InjGrp) field and the data-offset (Offset) have been described earlier. In addition to these fields; the injection DCB DAR field contains start-of-frame (Sof) indication, end-of-frame (Eof) indication, and data-length information (VldBytes).

The Sof field must be set in each DCB containing the first byte of data from the IFH of an Ethernet frame. When an Ethernet frame and IFH are contained in multiple DCBs, only the first DCB may have Sof set. The Eof field must be set in each DCB that contains the last byte of data from an Ethernet frame. When an Ethernet frame and IFH are contained in multiple DCBs only the last DCB may have Eof set. Note that if an entire Ethernet frame and IFH are contained in the data-area of a single DCB, then that DCB must have both Sof and Eof set.

All injection DCBs must have the VldBytes field set. The value in that field reflects how many bytes of data that is valid in the data-area of that DCB. The smallest allowed value is 1, and the largest allowed value is the maximum allowed frame size (i.e. MTU) plus the length of the IFH. This means that it is possible to store anything from 1 byte to a complete frame in the data-area of one DCB.

It is important to stress that the VldBytes field only reflects the number valid bytes in the data-area of the specific DCB. That is, when an Ethernet frame and IFH is contained in multiple DCBs, the VldBytes field in each individual DCB only indicates the number of valid bytes in the data-area of that particular DCB.

Note VldBytes do not have to be a multiple of 4 bytes, because the FDMA engine takes care of appropriate realigning and buffering of frame data. It is even possible to specify a count of only one. However, keep in mind that there is a fixed overhead for processing each DCB, so there is a performance impact when frames are scattered across many DCBs.

5.6.6 CTL0 and CTL1 Field Encoding for Injection

The CTL fields are loaded into the corresponding FDMA registers when processing injection DCBs. The following values achieve optimal performance for injection.

- CTL0: Must be set to 0x1890D924 + DAR:Eof

  The least significant bit of CTL0 is the interrupt enable field, for injection this field must only be set for DCBs that contains Eof.

- CTL1: Use the following algorithm to calculate the required value of this field: ((DAR:VldBytes + DAR:Offset + 3) >> 2) and 0x00000FFF

  This algorithm adds three to the sum of the VldBytes and Offset fields from the DAR, then applies a modulus 4 operation (by right-shifting). Only the low 12 bits of CTL1 can be set.

5.6.7 STAT Field Encoding for Injection

When a DCB has been processed by the FDMA engine, STAT is updated with information about injection status. Done is set when STAT has been updated and valid. Aborted is set when the contents of this DCB have been aborted by the user (through <TBA: Add

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register field+name for abort field in FDMA>). If an Ethernet frame and IFH spans multiple DCBs, this field will be set for the current DCB (the active DCB at the time the user aborted the frame) and for the remainder of the DCBs that contains the aborted Ethernet frame and IFH. That is, the last of the DCBs for a particular frame (the DCB that has DAR:Eof set) always indicates if a frame was aborted.

The STAT field must be set to 0x00000000 when initializing the DCB.

5.6.8 Initialization of FDMA Channel for Injection

Any of the FDMA channels can be configured for frame Injection. After an FDMA channel is configured for Injection, it can only be used for that purpose. That is, it can no longer be used for Extraction or general-purpose transfers.

One FDMA channel can inject to multiple injection groups, but one injection group can never receive frames from more than one FDMA channel. This means that one FDMA channel will be enough to handle all injection groups; however, backpressure on any injection group will cause backpressure on the corresponding FDMA channel. For increased performance, it may be desirable to separate high-priority and low-priority groups by using different FDMA channels.

<TBA: Update from TCL func: fdma_ffl_inj_ch_cfg>A number of steps are required for initializing an FDMA channel for injection.

1. For each of the injection groups (which is handled by the channel), enable backpressure to the channel (fields INJ_GRP_BP_ENA and INJ_GRP_BP_MAP in CFG.FDMA_INJ_CFG).

2. Initialize specific FDMA channel registers:
   CTL0=
   CFG0=, CFG1=
   DSTATAR=0x00000000

3. Configure FDMA engine for injection and enable the channel (fields USAGE and CH_ENA in CFG.FDMA_CH_CFG).

All other registers related to the channel and the injection groups should be kept at the default values.

Software follows the progress of injection either by polling the status of the FDMA engine or through interrupts. The FDMA engine generates an interrupt when a complete chain of DCBs is injected (when a NULL pointer is reached) or after injection of each individual DCB. When operating in interrupt mode, the FDMA channel must be re-enabled by software after each interrupt.

Injection of Frames

After an FDMA channel is initialized for injection of frames, providing the FDMA channel with a DCB or a chain of DCBs starts frame injection. The destination injection groups are specified in the DCB, and software must ensure that the channel only injects to the groups that have already been associated with the channel (done during initialization of the channel).

To start frame injection from a single DCB or a list of DCBs, perform the following steps:

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1. Write the pointer to the first DCB into the LLP register.
2. Enable the channel by using CH_EN_REG.

The FDMA engine will now inject frames until it reaches a DCB with the LLP field set to NULL. When that happens, the FDMA engine can be configured to generate an interrupt so that the VCore-III processor can provide the FDMA engine with more DCBs.

Concurrent FDMA Injection from External CPU

Injection groups that are not targeted by FDMA injection can be used by an external CPU that access DEVCPU injection registers directly. A typical scenario is to use one QS group for FDMA injection and the other for external CPU injection.

Note It is not possible for the FDMA engine and the external CPU to share injection groups (by handshaking ownership, i.e. semaphores). After the FDMA engine is enabled and a channel is allocated to the FDMA engine, irreversible changes or optimizations are done to that particular injection group.

It is possible to configure priorities between injection groups in the DEVCPU (by using DEVCPU.INJ_GRP_CFG.GRP_PRIO). Injection groups that are used by the external CPU must be assigned a higher than default priority, simplifying the protocol for external CPU injection.

For more information about how to inject directly from external CPU, see <TBA: add reference to section on "injection via DEVCPU">.

5.6.9 Extraction

The FDMA engine can receive frames from the Queuing System and Ethernet ports (super priority frames). The possible frame sources are four priorities per CPU Queue in the Queuing System (there are two CPU Queues) and two super priority channels.

Each of the two CPU Queues observes internal priorities when frames are selected for extraction; higher priority frames are extracted before lower priority frames. Frames from the two CPU Queues and the two front port channels are extracted in a round robin fashion.

Each of the frame sources are mapped directly to an extraction group. One extraction group can handle all of the frame sources, however, performance may be improved by separating high priority sources from low priority sources (by mapping to more than one extraction group).

Each of the frame sources must be mapped to one of four possible extraction groups <TBA: Need reference to DEVCPU regs>. It is possible to configure priorities for each of the frame sources <TBA: Regs for priority encoding between xtr. channels>. The FDMA engine reads directly from the extraction groups, which are hard coded to specific DMA channels.

Table 24. FDMA Extraction Groups

Extraction Group	Corresponding DMA Channel
0	0
1	1
2	2

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Table 24. FDMA Extraction Groups *(continued)*

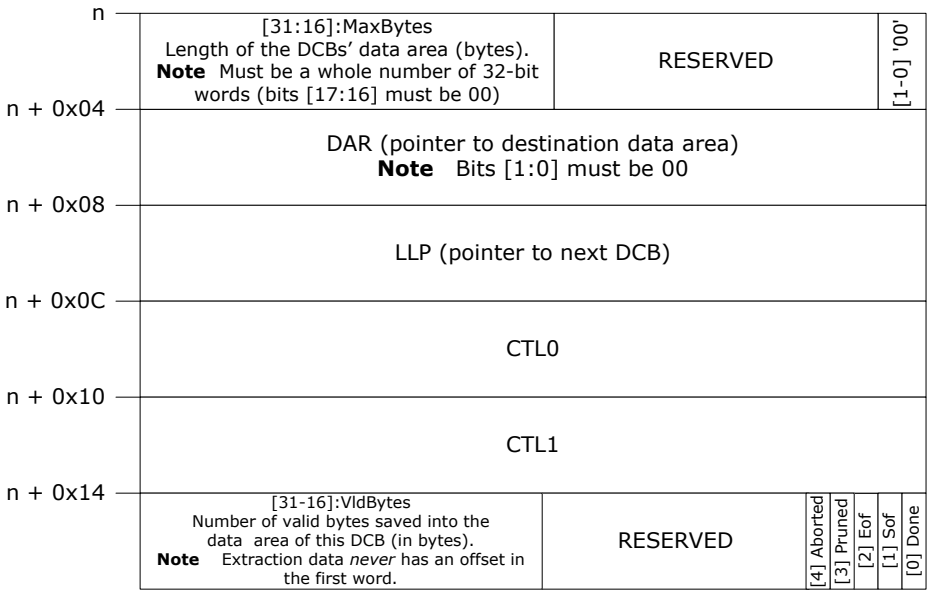
Extraction Group	Corresponding DMA Channel
3	3

Because the FDMA engine is optimized for bursting extraction data, there is a minimum size requirement for the data-area corresponding to each extraction DCB. The minimum size is 68 bytes (17 × 32-bit words).

Initialization of Extraction DCBs

This section contains information about the configuration of DCB fields for extraction of frames from any of the extraction groups. The following illustration shows the detailed layout of an extraction DCB:

Figure 53. Extraction DCB Layout



Each field is described in the following sections.

5.6.10 SAR Field Encoding for Extraction

The extraction DCB SAR field contains information about the byte-length of the data-area corresponding to the DCB. Data-areas must be aligned to 32-bit boundaries; because of this the two least significant bits in the data-area-length field will be zero.

<TBA: Figure showing the SAR field for extraction>

Note Because the DMA extraction channels are hardcoded to extraction groups, there is no encoding of particular extraction groups in the SAR field. In other words, a properly initialized extraction DCB can be used with any of the extraction groups.

DAR Field Encoding for Extraction

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For extraction DCBs, the destination address field must contain a pointer to the first 32-bit word of the data area corresponding to the DCB.

<TBA: Figure showing the DAR field for extraction>

5.6.11 CTL0 and CTL1 Field Encoding for Extraction

The CTL fields are loaded into the corresponding DMA registers when processing extraction DCBs. The following values achieve optimal performance for injection.

- CTL0: Must be set to 0x1A40DC25
- CTL1: Must be set to 0x00000000

5.6.12 STAT Field Encoding for Extraction

When a DCB has been processed by the DMA engine, the status field is updated with information about extraction status. When bit 0 of this field is set, the field has been updated and it is valid. <TBA: Go through the XTR-STAT indications one by one>

<TBA: Figure that shows STAT field for extraction>

The STAT field must be set to 0x00000000 when initializing the DCB.

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6 Registers

This section contains information about the software interface. The purpose of this section is to provide information about the programming interface, register maps, register descriptions, and register tables.

6.1 Overview of Registers

This section provides an overview of the registers in the VSC7462 device.

6.2 Origin in CPU Device

6.2.1 Origin Registers

Table 25. ORG

Address	Short Description	Register Name
0x00	Target Module ID is Unknown	ERR_ACCESS_DROP
0x02	Target Module is Busy	ERR_TGT
0x03	Error Counters	ERR_CNTS
0x07	Configuration and Status Register	CFG_STATUS

6.3 Arbiter

6.3.1 Various configuration and status registers

Table 26. CFG_STATUS

Address	Short Description	Register Name
0x00	Configuration of settings affecting all ports	PORT_ARB_CFG
0x01 - 0x23	Configuration of ingress shaper bandwidth	INGR_SHAPER_CFG
0x24 - 0x2B	Configuration of leaky buckets (LB) for priority bandwidth control	PRIO_ARB_CFG
0x2C - 0x31	Configuration of priority DWRR	PRIO_COST_CFG
0x32	Enable DWRR control of priority 0 to 5	DWRR_CFG
0x33 - 0x3A	CMI operation control	CM_CFG_VEC0
0x3B - 0x42	CMI operation control	CM_CFG_VEC1
0x43	CMI access control	CM_ACCESS
0x44	CMI data	CM_DATA

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Table 26. CFG_STATUS *(continued)*

Address	Short Description	Register Name
0x45	CMI disable updates	CM_IGNORE_UPDATE
0x46	Stack operation control	STACK_CFG
0x47 - 0x4E	Configure the priority of GCPU frames. One value per extraction CPU port	GCPU_PRIO_CFG
0x4F - 0x51	Mirror probe operation control	MIRROR_CFG
0x52	Host mode operation control	HM_CFG
0x54	Congestion handling configuration	CH_CFG
0x55	Flush control	FLUSH_CTRL
0x56	Configuration of beating pattern protection mechanism	RND_GEN_CFG

6.3.2 Registers controlling the Drop modes in ARB

Table 27. DROP_MODE_CFG

Address	Short Description	Register Name
0x57 - 0x5E	Configuration of drop mode per outbound ethernet port	OUTB_ETH_DROP_MODE_CFG
0x5F - 0x66	Configuration of drop mode per outbound CPU port	OUTB_CPU_DROP_MODE_CFG
0x67 - 0x6E	Configuration of drop mode per outbound virtual device port	OUTB_VD_DROP_MODE_CFG
0x6F	Configuration of multicast drop mode	MC_DROP_MODE_CFG

6.3.3 Configuration of aging

Table 28. AGING_CFG

Address	Short Description	Register Name
0x70	Configuration of era generation	ERA_CTRL
0x71	Configuration of era prescaling	ERA_PRESCALER
0x72	Configuration of aging per port.	PORT_AGING_ENA_VEC0
0x73	Configuration of aging per port.	PORT_AGING_ENA_VEC1

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6.3.4 Sticky bit status

Table 29. STICKY

Address	Short Description	Register Name
0x74 - 0x7B	Queue overflow sticky	REQ_QU_OFLW_VEC0
0x7C - 0x83	Queue overflow sticky	REQ_QU_OFLW_VEC1
0x84	Queue empty sticky	REQ_QU_EMPTY
0x85	Queue not empty sticky	REQ_QU_NON_EMPTY
0x86 - 0x8D	OQS Flow Control Status	OQS_ETH_QU_FC_STATUS
0x8E - 0x95	OQS Flow Control Status	OQS_VD_QU_FC_STATUS
0x96 - 0x9D	OQS Flow Control Status	OQS_CPU_QU_FC_STATUS
0x9E	OQS Flow Control Status	OQS_ETH_PORT_FC_STATUS
0x9F	OQS Flow Control Status	OQS_VD_PORT_FC_STATUS
0xA0	OQS Flow Control Status	OQS_CPU_PORT_FC_STATUS
0xA1	OQS Flow Control Status	OQS_PRIO_FC_STATUS
0xA2	OQS Flow Control Status	OQS_BUF_FC_STATUS

6.4 Assembler

Table 30. DEV_STATISTICS (28 instances)

Address	Short Description	Register Name
0x00	Rx Byte Counter	RX_IN_BYTES_CNT
0x01	Rx Symbol Carrier Error Counter	RX_SYMBOL_ERR_CNT
0x02	Rx Pause Frame Counter	RX_PAUSE_CNT
0x03	Rx Control Frame Counter	RX_UNSUP_OPCODE_CNT
0x04	Rx OK Byte Counter	RX_OK_BYTES_CNT
0x05	Rx Bad Byte Counter	RX_BAD_BYTES_CNT
0x06	Rx Unicast Frame Counter	RX_UC_CNT
0x07	Rx Multicast Frame Counter	RX_MC_CNT
0x08	Rx Broadcast Frame Counter	RX_BC_CNT
0x09	Rx CRC Error Counter	RX_CRC_ERR_CNT
0x0A	Rx Undersize Counter (valid frame format)	RX_UNDERSIZE_CNT
0x0B	Rx Undersize Counter (CRC error)	RX_FRAGMENTS_CNT
0x0C	Rx In-range Length Error Counter	RX_IN_RANGE_LEN_ERR_CNT
0x0D	Rx Out-Of-Range Length Error Counter	RX_OUT_OF_RANGE_LEN_ERR_CNT
0x0E	Rx Oversize Counter (valid frame format)	RX_OVERSIZE_CNT
0x0F	Rx Jabbers Counter	RX_JABBERS_CNT
0x10	Rx 64 Byte Frame Counter	RX_SIZE64_CNT

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Table 30. DEV_STATISTICS (28 instances) *(continued)*

Address	Short Description	Register Name
0x11	Rx 65-127 Byte Frame Counter	RX_SIZE65TO127_CNT
0x12	Rx 128-255 Byte Frame Counter	RX_SIZE128TO255_CNT
0x13	Rx 256-511 Byte Frame Counter	RX_SIZE256TO511_CNT
0x14	Rx 512-1023 Byte Frame Counter	RX_SIZE512TO1023_CNT
0x15	Rx 1024-1518 Byte Frame Counter	RX_SIZE1024TO1518_CNT
0x16	Rx 1519 To Max. Length Byte Frame Counter	RX_SIZE1519TOMAX_CNT
0x17	Rx Inter Packet Gap Shrink Counter	RX_IPG_SHRINK_CNT
0x18	Tx Byte Counter	TX_OUT_BYTES_CNT
0x19	Tx Pause Frame Counter	TX_PAUSE_CNT
0x1A	Tx OK Byte Counter	TX_OK_BYTES_CNT
0x1B	Tx Unicast Frame Counter	TX_UC_CNT
0x1C	Tx Multicast Frame Counter	TX_MC_CNT
0x1D	Tx Broadcast Frame Counter	TX_BC_CNT
0x1E	Tx 64 Byte Frame Counter	TX_SIZE64_CNT
0x1F	Tx 65-127 Byte Frame Counter	TX_SIZE65TO127_CNT
0x20	Tx 128-255 Byte Frame Counter	TX_SIZE128TO255_CNT
0x21	Tx 256-511 Byte Frame Counter	TX_SIZE256TO511_CNT
0x22	Tx 512-1023 Byte Frame Counter	TX_SIZE512TO1023_CNT
0x23	Tx 1024-1518 Byte Frame Counter	TX_SIZE1024TO1518_CNT
0x24	Tx 1519 To Max. Length Byte Frame Counter	TX_SIZE1519TOMAX_CNT
0x25	Tx Multi Collision Counter	TX_MULTI_COLL_CNT
0x26	Tx Late Collision Counter	TX_LATE_COLL_CNT
0x27	Tx Excessive Collision Counter	TX_XCOLL_CNT
0x28	Tx First Defer Counter	TX_DEFER_CNT
0x29	Tx Excessive Defer Counter	TX_XDEFER_CNT
0x2A	Tx 1 Backoff Counter	TX_BACKOFF1_CNT
0x2B	Tx Carrier Sense Error Counter	TX_CSENSE_CNT
0x2C	MSB of RX in byte Counter	RX_IN_BYTES_MSB_CNT
0x2D	MSB of RX ok byte Counter	RX_OK_BYTES_MSB_CNT
0x2E	MSB of RX bad byte Counter	RX_BAD_BYTES_MSB_CNT
0x2F	MSB of Tx out byte Counter	TX_OUT_BYTES_MSB_CNT
0x30	MSB of Tx ok byte Counter	TX_OK_BYTES_MSB_CNT

6.4.1 Assembler Configuration Registers

Table 31. CFG

Address	Short Description	Register Name
0x700	Statistics counter configuration	STAT_CFG
0x701 - 0x800	Cell bus calendar configuration	CBC_CFG

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Table 31. CFG *(continued)*

Address	Short Description	Register Name
0x801	Cell bus calendar configuration	CBC_LEN_CFG
0x802 - 0x821	MAC Address Configuration Register (MSB)	MAC_ADDR_HIGH_CFG
0x822 - 0x841	MAC Address Configuration Register (LSB)	MAC_ADDR_LOW_CFG
0x842 - 0x861	Ethernet port configuration	ETH_CFG
0x862 - 0x863	This register holds CPU specific configuration	CPU_CFG
0x864	Holds DEVCPU specific Flow Control configuration signals	CPU_FC_CFG
0x865 - 0x884	Holds configuration related to Pause frame detection.	PAUSE_CFG

6.4.2 VStax2 Congestion Management configuration registers

Table 32. CM_CFG

Address	Short Description	Register Name
0x8B1 - 0x8B7	Enable reception of CMEFs	CMEF_RX_CFG

6.4.3 VStax2 Congestion Management status and sticky bit registers

Table 33. CM_STATUS

Address	Short Description	Register Name
0x8B8 - 0x8B9	CMEF counter	CMEF_CNT
0x8BA	CMEF discard sticky bits	CMEF_DISCARD_STICKY

6.4.4 Configuration registers for Super-Priority

Table 34. SP_CFG

Address	Short Description	Register Name
0x8BB - 0x8C1	Super-Priority reception configuration Register	SP_RX_CFG
0x8C2	Configuration register for own UPSID	SP_UPSID_CFG
0x8C3	Configuration register for SP TTL check	SP_KEEP_TTL_CFG

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6.4.5 Super-Priority status and sticky bit registers

Table 35. SP_STATUS

Address	Short Description	Register Name
0x8C4	Super-Priority sticky registers	SP_STICKY

6.5 Classifier sub block of the Analyzer

6.5.1 Data delay fifo integrety information

Table 36. INTEGRETY_IDENT

Address	Short Description	Register Name
0x8C0	Data delay fifo integrety information	INTEGRETY_IDENT

6.5.2 Contains the counter inside of the virtual queue

Table 37. VQ_COUNTER

Address	Short Description	Register Name
0x8C1	Drop counter inside of the virtual device	DROP_CNT

6.5.3 Contains port based configuration

Table 38. PORT (35 instances)

Address	Short Description	Register Name
0x00	Filter Configuration	FILTER_CTRL
0x01	Stacking configuration	STACKING_CTRL
0x02	PVID	VLAN_CTRL
0x03	Port ID Data	PORT_ID_CFG
0x04 - 0x13	Configuration per cfi, user priority	UPRIO_MAP_CFG
0x14	QOS configuration	QOS_CFG
0x15	CPU Forward Control	CAPTURE_CFG
0x16	BPDU and GXRP Bridge Management Group Address Control	CAPTURE_8021D_CFG_BPDU_AG
0x17	GXRP redirection control	CAPTURE_8021D_CFG_GXRP

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Table 38. PORT (35 instances) *(continued)*

Address	Short Description	Register Name
0x18	BPDU redirection control	CAPTURE_8021D_CFG_BPDU
0x19	Advanced classification configuration registers	ADV_CL_CFG
0x1A - 0x29	DP configurations	DP_CONFIG
0x2A	Contains the PBB configuration bits	PBB_CFG
0x2B	Contains the I-TAG and MPLS settings	TAG_CTRL

6.5.4 Common configuration for all ports

Table 39. COMMON

Address	Short Description	Register Name
0x8C2	Configure UPSID when stacking	UPSID_CFG
0x8C3	Common port control	COMMON_CTRL
0x8C4 - 0x903	Various configuration per DSCP	DSCP_CFG
0x904 - 0x90B	Configuration per QOS class	QOS_MAP_CFG
0x90C	Aggregation Calculation	AGGR_CFG
0x90D	Ethertype used for identifying service tagged frames	VLAN_STAG_CFG
0x90E - 0x91D	CPU queue configuration	CPU_BPDU_QU_CFG
0x91E	CPU queue configuration	CPU_PROTO_QU_CFG
0x91F - 0x926	Configuration of TCP range generation	ADV_RNG_CTRL
0x927 - 0x92E	Configuration of matcher range generation	ADV_RNG_VALUE_CFG
0x92F	Configuration of TCP range generation	ADV_RNG_OFFSET_CFG
0x930	Configuration for the virtual queue	VQ_CFG
0x931	Contains the one shot bitgroups for the VQ	VQ_ONE_SHOT
0x932	VStaX configruations	IFH_CFG
0x933 - 0x934	STAG type ctrl	CUSTOM_STAG_ETYPE_CTRL
0x935 - 0x938	HMD port configurations	HM_CFG
0x939 - 0x948	BPDU/BPDU_AG/GARP QOS configuration	BPDU_AG_GARP_QOS
0x949 - 0x94A	Configuration of the IFH chksum checker	IFH_CHKSUM_CFG

6.5.5 Sticky event registers

Table 40. STICKY

Address	Short Description	Register Name
0x94B	Sticky bits register	FILTER_STICKY
0x94C	Sticky bits register	CLASS_STICKY
0x94D	Sticky bits register	CAT_STICKY

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Table 40. STICKY *(continued)*

Address	Short Description	Register Name
0x94E	Sticky bits register	IP_HDR_CHK_STICKY
0x94F	Sticky bits register	VQ_STICKY_REG
0x950	Sticky bits register	MISC_CONF_STICKY

6.5.6 Sticky event counter mask

Table 41. STICKY_MASK (4 instances)

Address	Short Description	Register Name
0x951	Sticky counter mask register	FILTER_STICKY_MASK
0x952	Sticky counter mask register	CLASS_STICKY_MASK
0x953	Sticky counter mask register	CAT_STICKY_MASK
0x954	Sticky counter mask register	IP_HDR_CHK_STICKY_MASK

6.6 Layer 3 sub block of the Analyzer

6.6.1 MSTP table configuration (B-Domain)

Table 42. BMSTP (66 instances)

Address	Short Description	Register Name
0x4E00	MSTP Learning Control	BMSTP_LRN_CFG
0x4E01	MSTP Forwarding Control in B-Domain	BMSTP_FWD_CFG

6.6.2 Integrity error identification

Table 43. INTEGRITY_IDENT

Address	Short Description	Register Name
0x4E84	RAM integrity errors	INTEGRITY_IDENT

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6.6.3 Enable per concurrent counter for each sticky bit

Table 44. L3_STICKY_MASK (4 instances)

Address	Short Description	Register Name
0x4E85	Enable per concurrent counter for each sticky bit	RLEG_STICKY_MASK
0x4E86	Enable per concurrent counter for each sticky bit	ROUT_STICKY_MASK
0x4E87	Enable per concurrent counter for each sticky bit	SECUR_STICKY_MASK
0x4E88	Enable per concurrent counter for each sticky bit	VLAN_MSTP_STICKY_MASK

6.6.4 Basic registers

Table 45. COMMON

Address	Short Description	Register Name
0x4E95	BVLAN Filter Control	BVLAN_FILTER_CTRL
0x4E96	Clear ONE SHOT bits	ONE_SHOT_CLR_REG
0x4E97	VLAN Control	VLAN_CTRL
0x4E98	Unicast routing control configuration	L3_UC_ENA
0x4E99	Common table control	TABLE_CTRL
0x4E9A	Multicast routing control Configuration	L3_MC_ENA
0x4E9B	Forwarding Control	PORT_FWD_CTRL
0x4E9C	Learning Control	PORT_LRN_CTRL
0x4E9D	VLAN Filter Control	VLAN_FILTER_CTRL
0x4E9E	Switch Mode	ROUTING_CFG
0x4E9F	VLAN isolated port mask	VLAN_ISOLATED_CFG
0x4EA0	Router Leg base MAC address	RLEG_CFG_0
0x4EA1	Router Leg base MAC address	RLEG_CFG_1
0x4EA2	VLAN Community port mask	VLAN_COMMUNITY_CFG
0x4EA3	CPU Queue	CPU_QU_CFG
0x4EA4	Virtual Router Leg Protocol Configuration	VRRP_CFG_0
0x4EA5	Source based SMAC compare enable	SIP_SECURE_ENA
0x4EA6	Destination based DMAC compare enable	DIP_SECURE_ENA
0x4EA7	Virtual Router Leg Protocol Configuration	VRRP_CFG_1
0x4EA8	Mask containing I-component ports	VLAN_PORT_TYPE_MASK_CFG

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6.6.5 VLAN table configuration

Table 46. VLAN (4096 instances)

Address	Short Description	Register Name
0x00	VLAN Configuration for B-component	BVLAN_CFG
0x01	VLAN mapping configuration	VMID_CFG
0x02	VLAN Configuration	VLAN_CFG
0x03	VLAN Port Mask Configuration	VLAN_MASK_CFG

6.6.6 MSTP table configuration (C-Domain)

Table 47. MSTP (66 instances)

Address	Short Description	Register Name
0x4EA9	MSTP Forwarding Control	MSTP_FWD_CFG
0x4EAA	MSTP Learning Control	MSTP_LRN_CFG

6.6.7 Router Leg (RLEG=VMID) table configuration

Table 48. VMID (128 instances)

Address	Short Description	Register Name
0x4C00	Router Interface control	RLEG_CTRL
0x4C01 - 0x4C02	Virtual Router Leg configuration	VRRP_CFG

6.6.8 Control of Longest Prefix Matching TCAM

Table 49. LPM

Address	Short Description	Register Name
0x4F2D	LPM and REMAP Access control	ACCESS_CTRL
0x4F2E	Configuration for Move Access Operations	ACCESS_MV_CFG
0x4F2F - 0x4F32	Longest Prefix DATA configuration	LPM_DATA_CFG
0x4F33 - 0x4F36	Longest Prefix MASK configuration	LPM_MASK_CFG
0x4F37 - 0x4F3A	IP Prefix usage configuration	LPM_USAGE_CFG

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6.6.9 Remapping table configuration

Table 50. REMAP

Address	Short Description	Register Name
0x4F3B	ARP/L3MC table addressing	REMAP_CFG

6.6.10 ARP table used for unicast and security lookup result

Table 51. ARP (1024 instances)

Address	Short Description	Register Name
0x4000	ARP Data	ARP_CFG_0
0x4001	ARP Data 1	ARP_CFG_1

6.6.11 IP miltcast spread pattern table configuration

Table 52. L3MC (128 instances)

Address	Short Description	Register Name
0x4800 - 0x4803	Multicast VLAN replication mask	EVMID_MASK_CFG
0x4804	L3 multicast control register	L3MC_CTRL

6.6.12 Diagnostic Registers

Table 53. LPM_REMAP_STICKY

Address	Short Description	Register Name
0x4F3C	Router Leg Diagnostic	L3_LPM_REMAP_STICKY

6.6.13 Diagnostic Registers

Table 54. VLAN_ARP_L3MC_STICKY

Address	Short Description	Register Name
0x4F3D	VLAN Diagnostic	VLAN_STICKY

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Table 54. VLAN_ARP_L3MC_STICKY *(continued)*

Address	Short Description	Register Name
0x4F3E	ARP and L3MC table related diagnostic registers	L3_ARP_IPMC_STICKY

6.6.14 Build in test for TCAM

Table 55. TCAM_BIST

Address	Short Description	Register Name
0x4F3F	Control of the TCAM	TCAM_CTRL
0x4F42	Status for the TCAM	TCAM_STAT

6.7 Layer 2 sub block of the Analyzer

6.7.1 Configuration and status registers

Table 56. COMMON

Address	Short Description	Register Name
0x4400	CCM options	CCM_CFG
0x4401	Jaguar as a MAC configuration	HM_CFG
0x4402	Forwarding options	FWD_CFG
0x4403	Table initializations	TABLE_CLR_CFG
0x4404	Learn options	LRN_CFG
0x4405	Remote filter configuration to be used by autoage and CPU scan	FILTER_OTHER_CTRL
0x4406	Port filter configuration to be used by autoage and CPU scan	FILTER_LOCAL_CTRL
0x4407	Learn options for B-domain	BLRN_CFG
0x4408	Auto learn configuration	AUTO_LRN_CFG
0x4409	Secure learn configuration	LRN_SECUR_CFG
0x440A	Secure learn configuration for locked entries	LRN_SECUR_LOCKED_CFG
0x440B	Learn copy configuration	LRN_COPY_CFG
0x440C	Auto learn configuration for BMAC table	AUTO_BLRN_CFG
0x440D	Secure learn configuration for BMAC table	BLRN_SECUR_CFG
0x440E	Learn copy configuration for BMAC table	BLRN_COPY_CFG
0x440F - 0x442E	Port default service DLB indexes	PORT_DLB_CFG
0x442F - 0x444E	Port CCM control	PORT_CCM_CTRL

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Table 56. COMMON *(continued)*

Address	Short Description	Register Name
0x444F	Port Move Logger	MOVELOG_STICKY
0x4450	VSTAX learning and forwarding control	VSTAX_CTRL
0x4451 - 0x4470	Controls auto learn limits	LRN_CNT_CTRL
0x4471	ANA_L2 event sticky	INTR
0x4472	ANA_L2 interrupt enable mask	INTR_ENA
0x4473	ANA_L2 interrupt status	INTR_IDENT
0x4474	RAM integrity errors	RAM_INTGR_ERR_IDENT

6.7.2 Pathgroup table configuration

Table 57. PATHGRP (512 instances)

Address	Short Description	Register Name
0x4000 - 0x4001	Configuration of path group connections. index 0 is primary	CONID_CFG

6.7.3 Ingress service configuration

Table 58. ISDX (4096 instances)

Address	Short Description	Register Name
0x00	Ingress service port mask configuration	PORT_MASK_CFG
0x01	Ingress service forwarding control	SERVICE_CTRL
0x02	Ingress service CCM control	CCM_CTRL
0x03	Ingress service dual leaky bucket configuration	DLB_CFG

6.7.4 Sticky diagnostic

Table 59. STICKY

Address	Short Description	Register Name
0x4475	CCM diagnostic	CCM_STICKY
0x4476	Layer 2 Diagnostic	STICKY

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6.7.5 Counter mask registers

Table 60. STICKY_MASK (4 instances)

Address	Short Description	Register Name
0x4477	CCM Diagnostic counter mask	CCM_STICKY_MASK
0x4478	Layer 2 Diagnostic counter mask	STICKY_MASK

6.8 Learn block

6.8.1 Common status and configuration registers

Table 61. COMMON

Address	Short Description	Register Name
0x00	MAC Table Control	COMMON_ACCESS_CTRL
0x01	MAC entry Data 0	MAC_ACCESS_CFG_0
0x02	MAC entry Data 1	MAC_ACCESS_CFG_1
0x03	MAC entry Data 2	MAC_ACCESS_CFG_2
0x04	MAC entry Data 3	MAC_ACCESS_CFG_3
0x05	MAC entry Data 4	MAC_ACCESS_CFG_4
0x06	Age Filter	SCAN_NEXT_CFG
0x07	Age Filter	SCAN_NEXT_CFG_1
0x09	Age Filter	SCAN_NEXT_CNT
0x0A	Auto age configuration	AUTOAGE_CFG
0x0B	Auto age configuration	AUTOAGE_CFG_1
0x0C	Auto Learn Options	AUTO_LRN_CFG
0x0D	CCM scan configuration	CCM_CTRL
0x0E - 0x10	Configuration of CCM types	CCM_TYPE_CFG
0x11	CCM SCAN row status	CCM_STATUS
0x12	Layer 2 Diagnostic	EVENT_STICKY
0x13	Learn Diagnostic	LATEST_POS_STATUS
0x14	RAM integrity errors	RAM_INTGR_ERR_IDENT

6.9 Access Control sub block of the Analyzer

Controls mask handling etc.

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6.9.1 Common configuration and status registers

Table 62. PS_COMMON

Address	Short Description	Register Name
0x1BA63	Miscellaneously Control	MISC_CTRL
0x1BA64 - 0x1BA67	Configuration of host mode operation	HM_CFG
0x1BA68	Common general control	PS_COMMON_CFG
0x1BA69	Initialize port selector tables	PS_TABLE_CLR_CFG
0x1BA6A	Configuration of sFlow	SFLOW_CFG
0x1BA6B	Configuration of sFLOW reset	SFLOW_RESET_CTRL
0x1BA6C - 0x1BA8B	sFLOW sample control	SFLOW_CTRL
0x1BA8C - 0x1BAAB	sFLOW status counts	SFLOW_CNT
0x1BAAC	Physical source port aggregation control	PHYS_SRC_AGGR_CFG
0x1BAAD	Stack port mask configuration	STACK_CFG
0x1BAAE	Stack direction A mask configuration	STACK_A_CFG
0x1BAAF	Common stack configuration	COMMON_VSTAX_CFG
0x1BAB0	Common stack configuration	COMMON_EQUAL_STACK_LINK_TTL_CFG
0x1BAB1 - 0x1BAD0	Per port stack mode configuration	VSTAX_CTRL
0x1BAD1	Gmirror destination configuration	VSTAX_GMIRROR_CFG
0x1BAD2 - 0x1BAD9	Traffic class profile configuration	TRAFFIC_CLASS_CFG
0x1BADA	CPU handling configuration	CPU_CFG
0x1BADE	RAM integrity errors	RAM_INTGR_ERR_IDENT

6.9.2 Mirror probe control per probe index

Table 63. MIRROR_PROBE (3 instances)

Address	Short Description	Register Name
0x1BADF	Mirror Probe Configuration	PROBE_CFG
0x1BAE0	Mirror Probe Port Configuration	PROBE_PORT_CFG

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6.9.3 Aggregation control per aggregation code

Table 64. AGGR (16 instances)

Address	Short Description	Register Name
0x1BAF7	Aggregation port mask configuration	AGGR_CFG

6.9.4 Source port filtering per physical frontport number

Table 65. SRC (35 instances)

Address	Short Description	Register Name
0x1BA40	Local source port mask configuration	SRC_CFG

6.9.5 Stack unit configuration per upsid

Table 66. UPSID (32 instances)

Address	Short Description	Register Name
0x1BB07	Equal cost UPSID destination configuration	STACK_LINK_EQUAL_COST_CFG
0x1BB08	UPSID destination configuration	UPSID_CFG

6.9.6 Global Link Aggregation filtering per GLAG id

Table 67. GLAG (32 instances)

Address	Short Description	Register Name
0x1BB47	Global link aggregation source port mask configuration	GLAG_CFG
0x1BB48	Global link aggregation member count configuration	MBR_CNT_CFG

6.9.7 Port group ID destination configuration per pgid index

Table 68. PGID (1312 instances)

Address	Short Description	Register Name
0x1B000	PGID port mask / destination configuration	PGID_CFG_0

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Table 68. PGID (1312 instances) *(continued)*

Address	Short Description	Register Name
0x1B001	PGID mask handling configuration	PGID_CFG_1

6.9.8 Sticky diagnostic

Table 69. PS_STICKY

Address	Short Description	Register Name
0x1BB87	Port Selector diagnostics	STICKY

6.9.9 Counter mask registers

Table 70. PS_STICKY_MASK (4 instances)

Address	Short Description	Register Name
0x1BB88	Port Selector diagnostic counter masks	STICKY_MASK

6.9.10 Various policer controls

Table 71. POL_ALL_CFG

Address	Short Description	Register Name
0x1D630 - 0x1D64F	Configuration of ACL policer rates	POL_ACL_RATE_CFG
0x1D650 - 0x1D66F	Configuration of ACL policer thresholds	POL_ACL_THRES_CFG
0x1D670 - 0x1D68F	Configuration of ACL policers	POL_ACL_CTRL
0x1D690 - 0x1D6B0	Configuration of port policer flow control	POL_PORT_FC_CFG
0x1D6B1	Global configuration of policers	POL_ALL_CFG
0x1D6B2	Policer Diagnostics	POL_STICKY
0x1D6B3	RAM integrity errors	POL_RAM_INTGR_ERR_IDENT

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6.9.11 Port policer controls

Table 72. POL_PORT_CFG

Address	Short Description	Register Name
0x1BC00 - 0x1BC83	Configuration of policer upper threshold	POL_PORT_THRES_CFG_0
0x1BD00 - 0x1BD83	Configuration of policer lower threshold	POL_PORT_THRES_CFG_1
0x1BE00 - 0x1BE83	Configuration of policer rate	POL_PORT_RATE_CFG

6.9.12 Port policer controls indexed per port

Table 73. POL_PORT_CTRL (33 instances)

Address	Short Description	Register Name
0x1DC00	Configuration of policer gap which is common for all port policers within a port	POL_PORT_GAP
0x1DC01 - 0x1DC04	Configuration of the port policers	POL_PORT_CFG

6.9.13 Priority policer controls

Table 74. POL_PRIO_CFG

Address	Short Description	Register Name
0x1D000 - 0x1D107	Configuration of priority policer rates	POL_PRIO_RATE_CFG
0x1D200 - 0x1D307	Configuration of priority policer thresholds	POL_PRIO_THRES_CFG

6.9.14 Priority policer controls indexed per queue.

Table 75. POL_PRIO_CTRL (264 instances)

Address	Short Description	Register Name
0x1D800	Configuration of priority policer gap value	POL_PRIO_GAP
0x1D801	Configures the behavior of priority policers	POL_PRIO_CFG

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6.9.15 Global configuration.

Table 76. STAT_GLOBAL_CFG_PORT

Address	Short Description	Register Name
0x1BBC8 - 0x1BBCB	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x1BBCC	Reset all statistic counter.	STAT_RESET

6.9.16 Individual configuration.

Table 77. STAT_CNT_CFG_PORT (35 instances)

Address	Short Description	Register Name
0x1D400	Sticky bits for events.	STAT_EVENTS_STICKY
0x1D401 - 0x1D404	Event handling configuration.	STAT_CFG
0x1D405 - 0x1D408	Least significant 32 bits.	STAT_LSB_CNT
0x1D409 - 0x1D40C	Most significant 8 bits.	STAT_MSB_CNT

6.9.17 Global configuration.

Table 78. STAT_GLOBAL_CFG_ISDX

Address	Short Description	Register Name
0x1BBCD - 0x1BBD2	Global configuration register	STAT_GLOBAL_CFG
0x1BBD3 - 0x1BBD8	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x1BBD9	Reset all statistic counter.	STAT_RESET

6.9.18 Individual configuration.

Table 79. STAT_CNT_CFG_ISDX (4096 instances)

Address	Short Description	Register Name
0x00 - 0x05	Least significant 32 bits.	STAT_LSB_CNT
0x06 - 0x08	Most significant 8 bits.	STAT_MSB_CNT

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6.9.19 Global configuration.

Table 80. STAT_GLOBAL_CFG_TUNNEL

Address	Short Description	Register Name
0x1BBDA - 0x1BBDF	Global configuration register	STAT_GLOBAL_CFG
0x1BBE0 - 0x1BBE5	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x1BBE6	Reset all statistic counter.	STAT_RESET

6.9.20 Individual configuration.

Table 81. STAT_CNT_CFG_TUNNEL (512 instances)

Address	Short Description	Register Name
0x18000 - 0x18005	Least significant 32 bits.	STAT_LSB_CNT
0x18006 - 0x18008	Most significant 8 bits.	STAT_MSB_CNT

6.9.21 Global configuration.

Table 82. STAT_GLOBAL_CFG_IRLEG

Address	Short Description	Register Name
0x1BBE7 - 0x1BBEC	Global configuration register	STAT_GLOBAL_CFG
0x1BBED - 0x1BBF2	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x1BBF3	Reset all statistic counter.	STAT_RESET

6.9.22 Individual configuration.

Table 83. STAT_CNT_CFG_IRLEG (128 instances)

Address	Short Description	Register Name
0x1C000 - 0x1C005	Least significant 32 bits.	STAT_LSB_CNT
0x1C006 - 0x1C00B	Most significant 8 bits.	STAT_MSB_CNT

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6.9.23 Global configuration.

Table 84. STAT_GLOBAL_CFG_ERLEG

Address	Short Description	Register Name
0x1D6B4 - 0x1D6B9	Global configuration register	STAT_GLOBAL_CFG
0x1D6BA - 0x1D6BF	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x1D6C0	Reset all statistic counter.	STAT_RESET

6.9.24 Individual configuration.

Table 85. STAT_CNT_CFG_ERLEG (128 instances)

Address	Short Description	Register Name
0x1C800 - 0x1C805	Least significant 32 bits.	STAT_LSB_CNT
0x1C806 - 0x1C80B	Most significant 8 bits.	STAT_MSB_CNT

6.9.25 Common DLB configuration and status registers

Table 86. common_sdlb

Address	Short Description	Register Name
0x1BBF4	Configuration of common dual leaky bucket handling	DLB_CTRL
0x1BBF5	DLB policer diagnostic	DLB_STICKY

6.9.26 Dual leaky buckets

Table 87. sdlb (4096 instances)

Address	Short Description	Register Name
0x10000	Configuration of DLB policer	DLB_CFG
0x10001 - 0x10002	Configuration of leaky buckets	LB_CFG

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6.9.27 Common DLB configuration and status registers

Table 88. common_tdlb

Address	Short Description	Register Name
0x1BBF6	Configuration of common dual leaky bucket handling	DLB_CTRL
0x1BBF7	DLB policer diagnostic	DLB_STICKY

6.9.28 Dual leaky buckets

Table 89. tdlb (512 instances)

Address	Short Description	Register Name
0x1A000	Configuration of DLB policer	DLB_CFG
0x1A001 - 0x1A002	Configuration of leaky buckets	LB_CFG

6.10 VCAP S0

Ingress Service classification block.

6.10.1 Miscellaneous Configuration Registers for VCAP

Table 90. VCAP

Address	Short Description	Register Name
0x00	Miscellaneous VCAP Configuration	ACL_CFG
0x01	Entry and Action Control	ACE_UPDATE_CTRL
0x02	Advanced Move/Copy Operations	ACE_MV_CFG
0x03	Entry/Action Cache Status	ACE_STATUS
0x04	Status Sticky Bits	ACE_STICKY

6.10.2 Entry Pattern Cache Configuration Register

Table 91. ENTRY_DATA

Address	Short Description	Register Name
0x05 - 0x14	Indirect Entry Pattern Cache Access	ACE_ENTRY_DATA

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6.10.3 Entry Mask Cache Configuration Register

Table 92. ENTRY_MASK

Address	Short Description	Register Name
0x15 - 0x24	Indirect Entry Mask Cache Access	ACE_ENTRY_MASK

6.10.4 Action Cache Configuration Register

Table 93. ACTION_DATA

Address	Short Description	Register Name
0x25 - 0x28	Indirect Action Cache Access	ACE_ACTION_DATA

6.10.5 Build in test for TCAM

Table 94. TCAM_BIST

Address	Short Description	Register Name
0x29	Control of the TCAM	TCAM_CTRL
0x2C	Status for the TCAM	TCAM_STAT

6.11 VCAP S1

Ingress QoS and Profile classification block.

6.11.1 Miscellaneous Configuration Registers for VCAP

Table 95. VCAP

Address	Short Description	Register Name
0x00	Miscellaneous VCAP Configuration	ACL_CFG
0x01	Entry and Action Control	ACE_UPDATE_CTRL
0x02	Advanced Move/Copy Operations	ACE_MV_CFG
0x03	Entry/Action Cache Status	ACE_STATUS
0x04	Status Sticky Bits	ACE_STICKY

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6.11.2 Entry Pattern Cache Configuration Register

Table 96. ENTRY_DATA

Address	Short Description	Register Name
0x05 - 0x24	Indirect Entry Pattern Cache Access	ACE_ENTRY_DATA

6.11.3 Entry Mask Cache Configuration Register

Table 97. ENTRY_MASK

Address	Short Description	Register Name
0x25 - 0x44	Indirect Entry Mask Cache Access	ACE_ENTRY_MASK

6.11.4 Action Cache Configuration Register

Table 98. ACTION_DATA

Address	Short Description	Register Name
0x45 - 0x54	Indirect Action Cache Access	ACE_ACTION_DATA

6.11.5 Build in test for TCAM

Table 99. TCAM_BIST

Address	Short Description	Register Name
0x55	Control of the TCAM	TCAM_CTRL
0x58	Status for the TCAM	TCAM_STAT

6.12 VCAP S2

Ingress Security, OAM, and Control protocol classification block.

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6.12.1 Miscellaneous Configuration Registers for VCAP

Table 100. VCAP

Address	Short Description	Register Name
0x00	Miscellaneous VCAP Configuration	ACL_CFG
0x01 - 0x23	Ingress Port to PAG Mapping	PAG_CFG
0x24	Entry and Action Control	ACE_UPDATE_CTRL
0x25	Advanced Move/Copy Operations	ACE_MV_CFG
0x26	Entry/Action Cache Status	ACE_STATUS
0x27	Status Sticky Bits	ACE_STICKY

6.12.2 Entry Pattern Cache Configuration Register

Table 101. ENTRY_DATA

Address	Short Description	Register Name
0x28 - 0x127	Indirect Entry Pattern Cache Access	ACE_ENTRY_DATA

6.12.3 Entry Mask Cache Configuration Register

Table 102. ENTRY_MASK

Address	Short Description	Register Name
0x128 - 0x227	Indirect Entry Mask Cache Access	ACE_ENTRY_MASK

6.12.4 Action Cache Configuration Register

Table 103. ACTION_DATA

Address	Short Description	Register Name
0x228 - 0x22B	Indirect Action Cache Access	ACE_ACTION_DATA

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6.12.5 Build in test for TCAM

Table 104. TCAM_BIST

Address	Short Description	Register Name
0x22C	Control of the TCAM	TCAM_CTRL
0x22F	Status for the TCAM	TCAM_STAT

6.13 VCAP ES0

Egress per Service or VLAN frame manipulations block.

6.13.1 Miscellaneous Configuration Registers for VCAP

Table 105. VCAP

Address	Short Description	Register Name
0x00	Miscellaneous VCAP Configuration	ACL_CFG
0x01	Entry and Action Control	ACE_UPDATE_CTRL
0x02	Advanced Move/Copy Operations	ACE_MV_CFG
0x03	Entry/Action Cache Status	ACE_STATUS
0x04	Status Sticky Bits	ACE_STICKY

6.13.2 Entry Pattern Cache Configuration Register

Table 106. ENTRY_DATA

Address	Short Description	Register Name
0x05 - 0x08	Indirect Entry Pattern Cache Access	ACE_ENTRY_DATA

6.13.3 Entry Mask Cache Configuration Register

Table 107. ENTRY_MASK

Address	Short Description	Register Name
0x09 - 0x0C	Indirect Entry Mask Cache Access	ACE_ENTRY_MASK

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6.13.4 Action Cache Configuration Register

Table 108. ACTION_DATA

Address	Short Description	Register Name
0x0D - 0x1C	Indirect Action Cache Access	ACE_ACTION_DATA

6.13.5 Build in test for TCAM

Table 109. TCAM_BIST

Address	Short Description	Register Name
0x1D	Control of the TCAM	TCAM_CTRL
0x20	Status for the TCAM	TCAM_STAT

6.14 Inbound Queue System

6.14.1 Congestion handling as flow-control vs. dropping

Table 110. CONG_CTRL

Address	Short Description	Register Name
0x5300	Congestion handling configuration	CH_CFG

6.14.2 Configuration and mapping of preallocated frame size

Table 111. MTU

Address	Short Description	Register Name
0x5301 - 0x5304	Pre-allocated frame size	MTU_FRM_SIZE_CFG

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6.14.3 Combined configuration bitgroups located in one RAM

Table 112. QU_RAM_CFG

Address	Short Description	Register Name
0x6000 - 0x6117	Resource control configuration on queue level	QU_RC_CFG
0x6200 - 0x6317	High and low watermarks for queues	QU_RC_HLWM_CFG
0x6400 - 0x6517	ATOP and SWM for queue configuration	QU_RC_ATOP_SWM_CFG
0x6600 - 0x6717	Mapping of MTUs to queues	MTU_QU_MAP_CFG
0x6800 - 0x6917	Configuration bits for Minth and MaxTh for RED and ECN	RED_ECN_MINTH_MAXTH_CFG
0x6A00 - 0x6B17	Miscellaneous configuration bits for RED and ECN	RED_ECN_MISC_CFG
0x6C00 - 0x6D17	Cut-through mode configuration	CTHRU_CFG

6.14.4 Combined configuration bitgroups located in one RAM

Table 113. PORT_RAM_CFG

Address	Short Description	Register Name
0x5200 - 0x5222	Resource control configuration on port level	PORT_RC_CFG
0x5240 - 0x5262	High and low watermark for ports	PORT_RC_HLWM_CFG
0x5280 - 0x52A2	ATOP and SWM for port configuration	PORT_RC_ATOP_SWM_CFG
0x52C0 - 0x52E2	GWM for port configuration	PORT_RC_GWM_CFG

6.14.5 Resource control configuration

Table 114. RESOURCE_CTRL_CFG

Address	Short Description	Register Name
0x5305	Resource control configuration on buffer level	BUF_RC_CFG
0x5306	High and low watermarks for buffers	BUF_PORT_RC_HLWM_CFG
0x5307	Resource control configuration on priority related buffer level	BUF_PRIO_RC_CFG

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Table 114. RESOURCE_CTRL_CFG *(continued)*

Address	Short Description	Register Name
0x5308	High and low watermarks for buffers	BUF_PRIO_RC_HLWM_CFG
0x5309 - 0x5310	Resource control configuration on priority level	PRIO_RC_CFG
0x5311 - 0x5318	High and low watermarks for priorities	PRIO_RC_HLWM_CFG
0x5319 - 0x5320	ATOP and SWM for priority configuration	PRIO_RC_ATOP_SWM_CFG

6.14.6 Combined configuration bitgroups located in one RAM

Table 115. QU_MEM_RAM_STATUS

Address	Short Description	Register Name
0x5400 - 0x5517	Fill level for a queue	QU_MEM_ALLOC_STATUS
0x5600 - 0x5717	Additional features concerning memory allocation per queue	QU_MEM_STATUS

6.14.7 Combined configuration bitgroups located in one RAM

Table 116. RED_RAM

Address	Short Description	Register Name
0x5800 - 0x5917	Average fill level for a queue fractional part	QU_MEM_AVG_ALLOC_FRAC_STATUS
0x5A00 - 0x5B17	Average fill level for a queue	QU_MEM_AVG_ALLOC_STATUS
0x5C00 - 0x5D17	Configuration register for Wq	RED_ECN_WQ_CFG

6.14.8 Combined configuration bitgroups located in one RAM

Table 117. PORT_MEM_RAM_STATUS

Address	Short Description	Register Name
0x5180 - 0x51A2	Fill level for queues of a port	PORT_MEM_ALLOC_STATUS
0x51C0 - 0x51E2	Fill level for queues of a port for green traffic only	PORT_GMEM_ALLOC_STATUS

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6.14.9 Status of different data memories

Table 118. RESOURCE_CTRL_STATUS

Address	Short Description	Register Name
0x5321	Fill level for queues of a buffer	BUF_MEM_QU_PORT_ALLOC_STATUS
0x5322 - 0x5329	Fill level for queues of one priority	PRIO_MEM_ALLOC_STATUS
0x532A	Fill level for priorities of a buffer	BUF_MEM_PRIO_ALLOC_STATUS

6.14.10 Combined QS configuration fields

Table 119. MAIN

Address	Short Description	Register Name
0x532B	Basic QS configurations	MAIN_CFG
0x532C	Basic status information	MAIN_STATUS
0x532D	Reinitialization of ABMs, Q-Descriptors and counters	MAIN_REINIT_1SHOT
0x532E	Status of main data flow functions	MAIN_STICKY
0x532F	Flag for errors during RAM integrity check	RAM_INTEGRITY_ERR_STICKY

6.14.11 Reinitialization and status of allocation bitmaps

Table 120. ABM_DBG

Address	Short Description	Register Name
0x5338	Threshold for ABMs	ABM_CFG
0x5339	Reinitialization of allocation bitmaps	ABM_DBG_REINIT_1SHOT
0x533A	Flag for a full ABM	ABM_FULL_STATUS
0x533B	Status of allocation bitmap	ABM_EMPTY_STICKY

6.14.12 RX counter global configuration registers

Table 121. STAT_GLOBAL_CFG_RX

Address	Short Description	Register Name
0x5354 - 0x5357	Event mask for counter.	STAT_GLOBAL_EVENT_MASK

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Table 121. STAT_GLOBAL_CFG_RX *(continued)*

Address	Short Description	Register Name
0x5358	Reset all statistic counter.	STAT_RESET

6.14.13 RX counter per queue configuration and status registers

Table 122. STAT_CNT_CFG_RX (280 instances)

Address	Short Description	Register Name
0x4000	Sticky bits for events.	STAT_EVENTS_STICKY
0x4001 - 0x4004	Event handling configuration.	STAT_CFG
0x4005 - 0x4008	Least significant 32 bits.	STAT_LSB_CNT
0x4009 - 0x400C	Most significant 8 bits.	STAT_MSB_CNT

6.14.14 TX counter global configuration registers

Table 123. STAT_GLOBAL_CFG_TX

Address	Short Description	Register Name
0x5359 - 0x535A	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x535B	Reset all statistic counter.	STAT_RESET

6.14.15 TX counter per queue configuration and status registers

Table 124. STAT_CNT_CFG_TX (280 instances)

Address	Short Description	Register Name
0x7000	Sticky bits for events.	STAT_EVENTS_STICKY
0x7001 - 0x7002	Event handling configuration.	STAT_CFG
0x7003 - 0x7004	Least significant 32 bits.	STAT_LSB_CNT
0x7005 - 0x7006	Most significant 8 bits.	STAT_MSB_CNT

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6.14.16 ISDX counter global configuration registers

Table 125. STAT_GLOBAL_CFG_ISDX

Address	Short Description	Register Name
0x535C - 0x535D	Global configuration register	STAT_GLOBAL_CFG
0x535E - 0x535F	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x5360	Reset all statistic counter.	STAT_RESET

6.14.17 ISDX counter per service configuration and status registers

Table 126. STAT_CNT_CFG_ISDX (4096 instances)

Address	Short Description	Register Name
0x00 - 0x01	Least significant 32 bits.	STAT_LSB_CNT
0x02	Most significant 8 bits.	STAT_MSB_CNT

6.15 Outbound Queue System

6.15.1 Congestion handling as flow-control vs. dropping

Table 127. CONG_CTRL

Address	Short Description	Register Name
0x5E00	Congestion handling configuration	CH_CFG

6.15.2 Configuration and mapping of preallocated frame size

Table 128. MTU

Address	Short Description	Register Name
0x5E01 - 0x5E04	Pre-allocated frame size	MTU_FRM_SIZE_CFG

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6.15.3 Combined configuration bitgroups located in one RAM

Table 129. QU_RAM_CFG

Address	Short Description	Register Name
0x6000 - 0x61CF	Resource control configuration on queue level	QU_RC_CFG
0x6200 - 0x63CF	High and low watermarks for queues	QU_RC_HLWM_CFG
0x6400 - 0x65CF	ATOP and SWM for queue configuration	QU_RC_ATOP_SWM_CFG
0x6600 - 0x67CF	Mapping of MTUs to queues	MTU_QU_MAP_CFG
0x6A00 - 0x6BCF	Configuration bits for Minth and MaxTh for RED and ECN	RED_ECN_MINTH_MAXTH_CFG
0x6C00 - 0x6DCF	Miscellaneous configuration bits for RED and ECN	RED_ECN_MISC_CFG

6.15.4 Combined configuration bitgroups located in one RAM

Table 130. PORT_RAM_CFG

Address	Short Description	Register Name
0x8800 - 0x8858	Resource control configuration on port level	PORT_RC_CFG
0x8880 - 0x88D8	High and low watermark for ports	PORT_RC_HLWM_CFG
0x8900 - 0x8958	ATOP and SWM for port configuration	PORT_RC_ATOP_SWM_CFG
0x8980 - 0x89D8	Congestion Management Port Watermark	CM_PORT_WM
0x8A00 - 0x8A58	GWM for port configuration	PORT_RC_GWM_CFG

6.15.5 Resource control configuration

Table 131. RESOURCE_CTRL_CFG

Address	Short Description	Register Name
0x5E05	Resource control configuration on buffer level	BUF_RC_CFG
0x5E06	High and low watermarks for buffers	BUF_PORT_RC_HLWM_CFG
0x5E07	Resource control configuration on priority related buffer level	BUF_PRIO_RC_CFG

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Table 131. RESOURCE_CTRL_CFG *(continued)*

Address	Short Description	Register Name
0x5E08	High and low watermarks for buffers	BUF_PRIO_RC_HLWM_CFG
0x5E09 - 0x5E10	Resource control configuration on priority level	PRIO_RC_CFG
0x5E11 - 0x5E18	High and low watermarks for priorities	PRIO_RC_HLWM_CFG
0x5E19 - 0x5E20	ATOP and SWM for priority configuration	PRIO_RC_ATOP_SWM_CFG

6.15.6 Combined configuration bitgroups located in one RAM

Table 132. QU_MEM_RAM_STATUS

Address	Short Description	Register Name
0x8C00 - 0x8DCF	Fill level for a queue	QU_MEM_ALLOC_STATUS
0x8E00 - 0x8FCF	Additional features concerning memory allocation per queue	QU_MEM_STATUS

6.15.7 Combined configuration bitgroups located in one RAM

Table 133. RED_RAM

Address	Short Description	Register Name
0x8000 - 0x81CF	Average fill level for a queue fractional part	QU_MEM_AVG_ALLOC_FRAC_STATUS
0x8200 - 0x83CF	Average fill level for a queue	QU_MEM_AVG_ALLOC_STATUS
0x8400 - 0x85CF	Configuration register for Wq	RED_ECN_WQ_CFG

6.15.8 Combined configuration bitgroups located in one RAM

Table 134. PORT_MEM_RAM_STATUS

Address	Short Description	Register Name
0x5D00 - 0x5D58	Fill level for queues of a port	PORT_MEM_ALLOC_STATUS
0x5D80 - 0x5DD8	Fill level for queues of a port for green traffic only	PORT_GMEM_ALLOC_STATUS

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6.15.9 Status of different data memories

Table 135. RESOURCE_CTRL_STATUS

Address	Short Description	Register Name
0x5E21	Fill level for queues of a buffer	BUF_MEM_QU_PORT_ALLOC_STATUS
0x5E22 - 0x5E29	Fill level for queues of one priority	PRIO_MEM_ALLOC_STATUS
0x5E2A	Fill level for priorities of a buffer	BUF_MEM_PRIO_ALLOC_STATUS

6.15.10 Combined QS configuration fields

Table 136. MAIN

Address	Short Description	Register Name
0x5E2B	Basic QS configurations	MAIN_CFG
0x5E2C	Basic status information	MAIN_STATUS
0x5E2D	Reinitialization of ABMs, Q-Descriptors and counters	MAIN_REINIT_1SHOT
0x5E2E	Status of main data flow functions	MAIN_STICKY
0x5E2F - 0x5E36	Flag for BIP8 errors in the IFH	IFH_BIP8_ERR_STICKY
0x5E37	Flag for errors during RAM integrity check	RAM_INTEGRITY_ERR_STICKY

6.15.11 Reinitialization and status of allocation bitmaps

Table 137. ABM_DBG

Address	Short Description	Register Name
0x5E40	Threshold for ABMs	ABM_CFG
0x5E41	Reinitialization of allocation bitmaps	ABM_DBG_REINIT_1SHOT
0x5E42	Flag for a full ABM	ABM_FULL_STATUS
0x5E43	Status of allocation bitmap	ABM_EMPTY_STICKY

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6.15.12 Register group for Host Mode configuration

Table 138. CE_HOST_MODE_CFG

Address	Short Description	Register Name
0x5E67	Host Mode VStaX2 congestion management configuration	HOST_MODE_CM_CFG
0x5E68	Configuration register for Host mode backpressure to ARB	HOST_PORT_RESRC_CTL_CFG

6.15.13 VStax2 CM Buffer Watermark

Table 139. CM_BUF_WM

Address	Short Description	Register Name
0x5E69	VStax2 CM Buffer Watermark	CM_BUF_WM

6.15.14 Prune mode configuration

Table 140. CPU_CFG

Address	Short Description	Register Name
0x5E6A	Number of extra copies to a CPU port	COPIES_TO_CPU_PORTS_CFG
0x5E6B	Enable for prune mode and each CPU queue to receive prune data	OQS_PRUNE_MODE_CFG

6.15.15 RX counter global configuration registers

Table 141. STAT_GLOBAL_CFG_RX

Address	Short Description	Register Name
0x5E6D - 0x5E70	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x5E71	Reset all statistic counter.	STAT_RESET

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6.15.16 RX counter per queue configuration and status registers

Table 142. STAT_CNT_CFG_RX (464 instances)

Address	Short Description	Register Name
0x4000	Sticky bits for events.	STAT_EVENTS_STICKY
0x4001 - 0x4004	Event handling configuration.	STAT_CFG
0x4005 - 0x4008	Least significant 32 bits.	STAT_LSB_CNT
0x4009 - 0x400C	Most significant 8 bits.	STAT_MSB_CNT

6.15.17 TX counter global configuration registers

Table 143. STAT_GLOBAL_CFG_TX

Address	Short Description	Register Name
0x5E72 - 0x5E73	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x5E74	Reset all statistic counter.	STAT_RESET

6.15.18 TX counter per queue configuration and status registers

Table 144. STAT_CNT_CFG_TX (464 instances)

Address	Short Description	Register Name
0x7000	Sticky bits for events.	STAT_EVENTS_STICKY
0x7001 - 0x7002	Event handling configuration.	STAT_CFG
0x7003 - 0x7004	Least significant 32 bits.	STAT_LSB_CNT
0x7005 - 0x7006	Most significant 8 bits.	STAT_MSB_CNT

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6.15.19 ISDX counter global configuration registers

Table 145. STAT_GLOBAL_CFG_ISDX

Address	Short Description	Register Name
0x5E75 - 0x5E76	Global configuration register	STAT_GLOBAL_CFG
0x5E77 - 0x5E78	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0x5E79	Reset all statistic counter.	STAT_RESET

6.15.20 ISDX counter per service configuration and status registers

Table 146. STAT_CNT_CFG_ISDX (4096 instances)

Address	Short Description	Register Name
0x00 - 0x01	Least significant 32 bits.	STAT_LSB_CNT
0x02	Most significant 8 bits.	STAT_MSB_CNT

6.16 Register definition for FreeFlight Scheduler

6.16.1 QSIF SCH registers

Table 147. QSIF

Address	Short Description	Register Name
0xA1C	Flush Control	QSIF_FLUSH_CTRL
0xA1D	Various QSIF control information.	QSIF_CTRL
0xA1E	Various Host Mode control	QSIF_HM_CTRL
0xA1F - 0xA24	Enable queue-level flow control for Host Mode device A (HMDA)	QSIF_HMDA_QU_FC_ENA
0xA25 - 0xA2A	Enable queue-level flow control for Host Mode device B (HMDB)	QSIF_HMDB_QU_FC_ENA
0xA2B - 0xA2C	Enable VP-level flow control for Host Mode device A (HMDA)	QSIF_HMDA_VP_FC_ENA
0xA2D - 0xA2E	Enable VP-level flow control for Host Mode device B (HMDB)	QSIF_HMDB_VP_FC_ENA
0xA2F - 0xA4E	QSIF device control for Ethernet devices	QSIF_ETH_DEV_CTRL
0xA4F	QSIF device control for Virtual device(s)	QSIF_VD_DEV_CTRL
0xA50 - 0xA51	QSIF device control for Host Mode devices	QSIF_HM_DEV_CTRL

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Table 147. QSIF *(continued)*

Address	Short Description	Register Name
0xA52	QSIF device control for CPU devices	QSIF_CPU_DEV_CTRL
0xA53 - 0xA72	QSIF Port Control for Ethernet ports	QSIF_ETH_PORT_CTRL
0xA73	QSIF Port Control for Virtual Device ports	QSIF_VD_PORT_CTRL
0xA74 - 0xB33	QSIF Port Control for HM ports	QSIF_HM_PORT_CTRL
0xB34 - 0xB3B	QSIF Port Control for CPU ports	QSIF_CPU_PORT_CTRL

6.16.2 Registers related to HM Scheduler

Table 148. HM

Address	Short Description	Register Name
0xB4B - 0xC0A	DWRR cost configuration	HM_DWRR_COST
0xC0B - 0xC3A	Additional configuration parameters for virtual ports	HM_DWRR_AND_LB
0xC3B - 0xCCA	Additional configuration parameters for virtual ports	HM_LB_CFG
0xCCB	Overall HM scheduler control.	HM_SCH_CTRL

6.16.3 Configuration of leaky buckets for shaping virtual ports.

Table 149. HM_LB

Address	Short Description	Register Name
0x800 - 0x88F	HM Leaky bucket threshold	HM_LB_THRES
0x900 - 0x98F	HM Leaky bucket rate	HM_LB_RATE

6.16.4 ETH SCH registers

Table 150. ETH

Address	Short Description	Register Name
0xCCC	Ethernet device scheduler control register	ETH_CTRL
0xCCD	ETH warnings	ETH_WARN
0xCD6 - 0xCF6	ETH port pause frame mode	ETH_PORT_PAUSE_FRM_MODE
0xCF7	ETH port pause frame priority mask	ETH_PORT_PAUSE_FRM_PRIO_MASK
0xCF8	ETH Leaky bucket frame adjustment	ETH_LB_DWRR_FRM_ADJ
0xCF9 - 0xD19	ETH Leaky bucked frame adjustment	ETH_LB_DWRR_CFG

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Table 150. ETH *(continued)*

Address	Short Description	Register Name
0xD1A - 0xD3A	Ethernet device scheduler deficit weighted round robin control register	ETH_DWRR_CFG
0xD3B	ETH deficit weighted round robin queuing control	ETH_DWRR_CTRL
0xD3C - 0xD5C	Ethernet device scheduler shaping control register	ETH_SHAPING_CTRL
0xD5D	ETH leaky bucket control	ETH_LB_CTRL

6.16.5 ETH leaky bucket SCH registers

Table 151. ETH_LB

Address	Short Description	Register Name
0x00 - 0x128	Ethernet leaky bucket threshold	ETH_LB_THRES
0x200 - 0x328	Ethernet leaky bucket rate	ETH_LB_RATE

6.16.6 Registers related to CPU Scheduler

Table 152. CPU

Address	Short Description	Register Name
0xD60	CPU cell request counter	CPU_CELL_CNT
0xD61	Cell request counter per-port enable	CPU_CELL_CNT_PORT_VEC0
0xD62	Cell request counter per-type enable	CPU_CELL_CNT_PRIO_TYPE

6.16.7 CBC SCH registers

Table 153. CBC

Address	Short Description	Register Name
0xD64	CBC Length Configuration	CBC_LEN_CFG

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6.16.8 Configuration of Device IDs in Cell Bus Calendar

Table 154. CBC_DEV_ID_CFG

Address	Short Description	Register Name
0x400 - 0x7FF	Configuration of Device IDs in Cell Bus Calendar	CBC_DEV_ID

6.16.9 Miscellaneous SCH registers

Table 155. MISC

Address	Short Description	Register Name
0xD65	Era Generator Control Register	ERA_CTRL
0xD66	Era Generator Prescaler Register	ERA_PRESCALER
0xD67	RAM integrity errors register.	RAM_INTEGRITY_ERR_STICKY

6.17 Rewriter

6.17.1 Common configuration and status for all rewriter ports

Table 156. COMMON

Address	Short Description	Register Name
0xB900	Common Control configuration	COMMON_CTRL
0xB901	Various configuration of service handling in rewriter module	SERVICE_CTRL
0xB902 - 0xB904	Configure mirror probes	MIRROR_PROBE_CFG
0xB905 - 0xB944	Remap table of DSCP values.	DSCP_REMAP
0xB945	Rewriter router leg configuration.	RLEG_CFG_0
0xB946	Rewriter router leg configuration.	RLEG_CFG_1
0xB947 - 0xB966	Mac addresses for MacInMac encapsulation.	ITAG_SMAC_HI
0xB967 - 0xB986	Mac addresses for MacInMac encapsulation.	ITAG_SMAC_LO
0xB987	Control register for counter events	CNT_CTRL
0xB988	Controls the common sticky event counter.	STICKY_EVENT_COUNT
0xB989	Mask for the STICKY_EVENT_COUNT	STICKY_EVENT_CNT_MASK_CFG
0xB98A	Rewriter sticky bit register	STICKY_EVENT

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Table 156. COMMON *(continued)*

Address	Short Description	Register Name
0xB98B	Ram integrity errors	RAM_INTEGRITY_ERR_STICKY
0xB98C	Global design for test configuration	DFT_TIMESTAMP_CFG
0xB98D	VSTAX global CPU configuration	VSTAX_GCPU_CFG
0xB98E - 0xB98F	VSTAX Configuration per logical Stacking port	VSTAX_PORT_GRP_CFG
0xB990	Various Host Mode control	HM_CTRL
0xB991 - 0xB994	Various Host Mode control	HIH_CTRL
0xB995 - 0xB998	Default values for transmitted HIHS	HIH_DEF_CFG

6.17.2 Port based configuration and status for rewriter

Table 157. PORT (224 instances)

Address	Short Description	Register Name
0x8000	Configures per port costum values for TAGs	PORT_TAG_DEFAULT
0x8001	Map drop precedence to drop eligible value	PORT_DP_MAP
0x8002 - 0x8009	Map internal priority to tagged priority.	PCP_MAP_DE0
0x800A - 0x8011	Map internal priority to tagged priority.	PCP_MAP_DE1
0x8012 - 0x8019	Map internal priority to tag value.	DEI_MAP_DE0
0x801A - 0x8021	Map internal priority to tag value.	DEI_MAP_DE1
0x8022	Configure PORT tagging	TAG_CTRL
0x8023	Enable DSCP updates on the port.	DSCP_MAP

6.17.3 Port based configuration and status for rewriter

Table 158. PHYSPORT (32 instances)

Address	Short Description	Register Name
0xB999	Controls stacking operation on port	VSTAX_CTRL
0xB99A	Controls frame drop of frames with invalid IFH checksum	PORT_CTRL

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6.17.4 Egress Mapped VLAN (EVMID) configuration

Table 159. VMID (256 instances)

Address	Short Description	Register Name
0xB800	Rewriter router leg control	RLEG_CTRL

6.17.5 Global configuration.

Table 160. STAT_GLOBAL_CFG_ESDX

Address	Short Description	Register Name
0xB9D9 - 0xB9DC	Global configuration register	STAT_GLOBAL_CFG
0xB9DD - 0xB9E0	Event mask for counter.	STAT_GLOBAL_EVENT_MASK
0xB9E1	Reset all statistic counter.	STAT_RESET

6.17.6 Individual configuration.

Table 161. STAT_CNT_CFG_ESDX (4096 instances)

Address	Short Description	Register Name
0x00 - 0x03	Least significant 32 bits.	STAT_LSB_CNT
0x04 - 0x05	Most significant 8 bits.	STAT_MSB_CNT

6.18 Disassembler

6.18.1 Configuration registers

Table 162. CFG

Address	Short Description	Register Name
0x298	Enables port protect feature.	PORT_PROTECT_ENA
0x299 - 0x2B8	Configuration of buffer space.	BUF_CFG
0x2B9 - 0x2D8	Rate control of dataflow to devices	RATE_CTRL
0x2D9	Rate control watemark of dataflow to devices	RATE_CTRL_WM
0x2DA - 0x2E2	Rate control watemark of dataflow to device2G5s	RATE_CTRL_WM_DEV2G5

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Table 162. CFG *(continued)*

Address	Short Description	Register Name
0x2E3 - 0x2E6	Rate control watemark of dataflow to device10Gs	RATE_CTRL_WM_DEV10G
0x2E7	Configuration register for IPG shrink mode	IPG_SHRINK_CFG
0x2E8	Configuration register for the stacking port calendar	STACK_PORT_CAL_CFG
0x2E9 - 0x2EA	Clear a single buffer in the DSM.	CLR_BUF
0x2EB - 0x30A	SCH stop fill level	SCH_STOP_WM_CFG
0x30B - 0x32A	Pause frame handling in RX direction	RX_PAUSE_CFG
0x32B - 0x34A	FC configuration for Ethernet ports.	ETH_FC_GEN
0x34B - 0x36A	MAC Configuration Register.	MAC_CFG
0x36B - 0x38A	MAC Address Base Configuration Register - bits 47-24.	MAC_ADDR_BASE_HIGH_CFG
0x38B - 0x3AA	MAC Address Base Configuration Register - bits 23-0.	MAC_ADDR_BASE_LOW_CFG
0x3AB	Debug control	DBG_CTRL

6.18.2 Status registers

Table 163. STATUS

Address	Short Description	Register Name
0x5E0 - 0x600	Counts number of aged frames.	AGED_FRMS
0x601	Sticky bits for the DSM cell bus interface.	CELL_BUS_STICKY
0x602	Buffer Overflow	BUF_OFLW_STICKY
0x603	Buffer Underrun	BUF_UFLW_STICKY
0x604	Pause Frame pre-counter overflow sticky register	PRE_CNT_OFLW_STICKY
0x605	Contains sticky bits for IQS global status.	IQS_GLOBAL_STATUS
0x606 - 0x628	Contains sticky bits for IQS port status.	IQS_PORT_STATUS
0x629 - 0x64B	Contains sticky bits for IQS queue status.	IQS_QU_STATUS
0x64C	Current HWM status.	IQS_HWM_PORT_STATUS
0x64D	Current SWM port status	IQS_SWM_PORT_STATUS
0x64E	Read and write the extended reach FC value.	XAUI_EXT_REACH_PORT_STATUS

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6.18.3 VStax2 Congestion Management configuration registers

Table 164. CM_CFG

Address	Short Description	Register Name
0x3B5	CMEF relay buffer flush	CMEF_RELAY_BUF_FLUSH_SHOT
0x3B6	Mask for generating CMM info	CMM_MASK_CFG
0x3B7 - 0x3BE	Mask for generating CMM info on queue level	CMM_QU_MASK_CFG
0x3BF - 0x3C4	Mask for generating CMM info for host queues	CMM_HOST_QU_MASK_CFG
0x3C5 - 0x3C6	Mask for generating CMM info for logical host ports	CMM_HOST_LPORT_MASK_CFG
0x3C7	Configuration register for Host mode backpressure to ARB	HOST_PORT_RESRC_CTL_CFG
0x3C8	Register to control forward of CMMs to ARB	CMM_TO_ARB_CFG
0x3C9	Register to config max and min interval for CMEF generation.	CMEF_RATE_CFG
0x3CA - 0x3D0	CMEF generation config register	CMEF_GEN_CFG
0x3D1	CMEF MAC address lower 24 bits	CMEF_MAC_ADDR_LOW_CFG
0x3D2	CMEF MAC address upper 24 bits	CMEF_MAC_ADDR_HIGH_CFG
0x3D3	Register to hold the own UPSID	CMEF_OWN_UPSID_CFG
0x3D4	Register to define active UPSIDs	CMEF_UPSID_ACTIVE_CFG
0x3D5 - 0x3F4	Logical port number mapping registers	LPORT_NUM_CFG
0x3F5	Shot register for Logical port number mapping table initialization	LPORT_NUM_INIT

6.18.4 VStax2 Congestion Management status and sticky bit registers

Table 165. CM_STATUS

Address	Short Description	Register Name
0x64F	Relay buffer overflow sticky register	CMEF_RELAY_BUF_OFLW_STICKY
0x650 - 0x651	Counter for extracted CMMs.	CMM_XTRCT_CNT
0x652	Sticky bit register for CMMs failed verify	CMM_XTRCT_STICKY
0x653 - 0x654	Sticky bit register for dropped CMEFs	CMEF_DROP_STICKY
0x655 - 0x656	This counter holds the number of relayed CMEFs from this port	CMEF_RELAYED_STATUS
0x657 - 0x658	This counter holds the number of generated CMEFs from this port	CMEF_GENERATED_STATUS
0x659 - 0x667	Curren CM status.	CURRENT_CM_STATUS
0x668 - 0x669	Curren CM status for LPorts.	CURRENT_LPORT_CM_STATUS
0x66A - 0x678	Curren CM status.	CM_STICKY

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Table 165. CM_STATUS *(continued)*

Address	Short Description	Register Name
0x679 - 0x67A	Curren CM Lport status.	CM_LPORT_STICKY

6.18.5 Super-Priority configuration registers

Table 166. SP_CFG

Address	Short Description	Register Name
0x67B	Super-Priority buffer flush	SP_BUF_FLUSH_SHOT
0x67C	Configuration register for disable of TTL decrementation	SP_KEEP_TTL_CFG
0x67D - 0x683	Super-Priority transmit configuration register	SP_TX_CFG
0x684	Super-Priority extract configuration register	SP_XTRCT_CFG
0x685	Configuration register for injection on front ports	SP_FRONT_PORT_INJ_CFG
0x686	Super-Priority frame counter source select configuration register	SP_FRM_CNT_SRC_SEL_CFG
0x687	Configuration Register for Super-Priority Injection FC watermark	SP_INJ_CFG

6.18.6 Super-Priority status and sticky bit registers

Table 167. SP_STATUS

Address	Short Description	Register Name
0x3F6	Super-Priority overflow sticky register	SP_BUF_OFLW_STICKY
0x3F7	Super-Priority Front Port Injection Status register	SP_FRONT_PORT_INJ_STAT
0x3F8 - 0x3FE	Super-Priority frame counter	SP_FRAME_CNT

6.18.7 Configuration registers for rate limit modes

Table 168. RATE_LIMIT_CFG

Address	Short Description	Register Name
0x688 - 0x6A7	Configuration register for rate limit modes	TX_RATE_LIMIT_MODE
0x6A8 - 0x6C7	Configuration register for txFineIpgStretchRatio	TX_IPG_STRETCH_RATIO_CFG
0x6C8 - 0x6E7	configuration register for txFrameRateStart	TX_FRAME_RATE_START_CFG

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Table 168. RATE_LIMIT_CFG *(continued)*

Address	Short Description	Register Name
0x6E8	Header size configuration register for txRateLimitPayloadRate mode	TX_RATE_LIMIT_HDR_CFG

6.18.8 Status registers for rate limit modes

Table 169. RATE_LIMIT_STATUS

Address	Short Description	Register Name
0x3FF	Sticky bit register for rate limit modes	TX_RATE_LIMIT_STICKY

6.18.9 Registers required for Host Interface configuration

Table 170. HOST_IF_CFG

Address	Short Description	Register Name
0x6E9 - 0x6EC	Host Interface Header configuration register	HIH_CFG
0x6ED	Configutarion register for ITAG - TPID field	HIH_ITAG_TPID_CFG

6.18.10 Host Interface Inbound Status Configuration Registers

Table 171. HOST_IF_IBS_CFG

Address	Short Description	Register Name
0x6EE - 0x6EF	Host Interface Inbound Status Configuration Register	XAUI_IBS_CFG
0x6F0 - 0x6F1	Host Interface Inbound Status Diagnostic Register	XAUI_IBS_DIAG

6.18.11 RAM integrity errors

Table 172. RAM_INTEGRITY

Address	Short Description	Register Name
0x6F2	RAM integrity errors sticky register	RAM_INTEGRITY_ERR_STICKY

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6.18.12 Host Interface Inbound Status Combined Configuration and Status Registers per Status channel

Table 173. HOST_IF_CONF_IBS_CAL (320 instances)

Address	Short Description	Register Name
0x00 - 0x01	Host Interface Inbound Status Calendar Table	XAUI_IBS_CAL

6.18.13 Host Interface Inbound Status Common Configuration Registers

Table 174. HOST_IF_IBS_COMMON_CFG

Address	Short Description	Register Name
0x6F3 - 0x6FC	Register holds the upsid to capture status from.	CAPTURE_UPSID_CFG
0x6FD	Host Interface Inbound Status Source Select	XAUI_IBS_SRC_SEL

6.18.14 Host Interface Outbound Status Configuration Registers

Table 175. HOST_IF_OBS_CFG

Address	Short Description	Register Name
0x6FE - 0x6FF	Host Interface Outbound Status Configuration Register	XAUI_OBS_CFG
0x700 - 0x701	Host Interface Outbound Status Diagnostic Register	XAUI_OBS_DIAG_CFG
0x702 - 0x703	Host Interface Outbound Link Status Configuration Register	XAUI_OBS_LNK_CFG

6.18.15 Configuration Registers for OBS Calendar Table

Table 176. HOST_IF_CONF_OBS_CAL (240 instances)

Address	Short Description	Register Name
0x400 - 0x401	Host Interface Outbound Status Port Calendar Table	XAUI_OBS_CAL

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6.18.16 Host Interface Outbound Status Status Registers

Table 177. HOST_IF_OBS_STATUS

Address	Short Description	Register Name
0x704 - 0x705	Host Interface Outbound DIP-2 Error Counter	XAUI_OBS_DIP2_ERR_CNT
0x706 - 0x707	Host Interface Outbound Status Event Register	XAUI_OBS_STICKY
0x708 - 0x709	Host Interface Status General Status Register	XAUI_OBS_STATUS

6.19 Device 1G

The device operates as an interface between the TAXI bus and SGMII macro supporting data rates of 10M, 100M, and 1000Mbps. The device includes PCS, MAC and rate adaption logic.

6.19.1 Dev1g Configuration and Status Registers

Table 178. DEV_CFG_STATUS

Address	Short Description	Register Name
0x00	DEV_RST_CTRL register	DEV_RST_CTRL
0x02	Loopback Configuration Register	DEV_LB_CFG
0x03	Device Debug Config	DEV_DBG_CFG
0x04	Configuration for the port protectio feature	DEV_PORT_PROTECT
0x05	Precision Time Protocol Configuration	DEV_PTP_CFG
0x06	PTP Time Stamp Sticky Register	DEV_PTP_TX_STICKY
0x07 - 0x09	PTP Time Stamp Register	DEV_PTP_TX_TSTAMP
0x0A - 0x0C	PTP Identification Register	DEV_PTP_TX_ID

6.19.2 MAC1G Configuration and Status Registers

Table 179. MAC_CFG_STATUS

Address	Short Description	Register Name
0x0D	Mode Configuration Register	MAC_ENA_CFG
0x0E	Mode Configuration Register	MAC_MODE_CFG
0x0F	Max Length Configuration Register	MAC_MAXLEN_CFG
0x10	VLAN / Service tag configuration register	MAC_TAGS_CFG
0x11	Advanced Check Feature Configuration Register	MAC_ADV_CHK_CFG
0x12	Inter Frame Gap Configuration Register	MAC_IFG_CFG

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Table 179. MAC_CFG_STATUS *(continued)*

Address	Short Description	Register Name
0x13	Half Duplex Configuration Register	MAC_HDX_CFG
0x14	Sticky Bit Register	MAC_STICKY

6.19.3 PCS 1G Configuration Status Registers

Table 180. PCS1G_CFG_STATUS

Address	Short Description	Register Name
0x15	PCS1G Configuration	PCS1G_CFG
0x16	PCS1G Mode Configuration	PCS1G_MODE_CFG
0x17	PCS1G SignalDetect Configuration	PCS1G_SD_CFG
0x18	PCS1G Aneg Configuration	PCS1G_ANEG_CFG
0x19	PCS1G Aneg Nextpage Configuration	PCS1G_ANEG_NP_CFG
0x1A	PCS1G Loopback Configuration	PCS1G_LB_CFG
0x1B	PCS1G Debug Configuration	PCS1G_DBG_CFG
0x1C	PCS1G comma detection Configuration	PCS1G_CDET_CFG
0x1D	PCS1G ANEG Status Register	PCS1G_ANEG_STATUS
0x1E	PCS1G Aneg Next Page Status Register	PCS1G_ANEG_NP_STATUS
0x1F	PCS1G link status	PCS1G_LINK_STATUS
0x20	PCS1G link down counter	PCS1G_LINK_DOWN_CNT
0x21	PCS1G sticky register	PCS1G_STICKY
0x22	PCS1G debug status	PCS1G_DEBUG_STATUS
0x23	PCS1G Low Power Idle Configuration	PCS1G_LPI_CFG
0x24	PCS1G Low Power Idle Status	PCS1G_LPI_STATUS

6.19.4 PCS1G Testpattern Configuration and Status Registers

Table 181. PCS1G_TSTPAT_CFG_STATUS

Address	Short Description	Register Name
0x25	PCS1G TSTPAT MODE CFG	PCS1G_TSTPAT_MODE_CFG
0x26	PCS1G TSTPAT STATUS	PCS1G_TSTPAT_STATUS

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6.19.5 PCS FX100 Configuration Registers

Table 182. PCS_FX100_CONFIGURATION

Address	Short Description	Register Name
0x27	PCS 100Base FX Configuration	PCS_FX100_CFG

6.19.6 PCS FX100 Status Registers

Table 183. PCS_FX100_STATUS

Address	Short Description	Register Name
0x28	PCS 100Base FX Status	PCS_FX100_STATUS

6.19.7 Device 1G Interrupt Configuration and Status Registers

Table 184. DEV1G_INTR_CFG_STATUS

Address	Short Description	Register Name
0x29	Dev1g Intr Configuration	DEV1G_INTR_CFG
0x2A	Dev1g Interrupt Reg	DEV1G_INTR
0x2B	Dev1g Interrupt Ident	DEV1G_INTR_IDENT

6.20 Device 2G5

The device operates as an interface between the TAXI bus and SGMII macro supporting data rates of 10M, 100M, 1000Mbps, and 2.5 Gbps. The device includes PCS, MAC and rate adaption logic.

6.20.1 Dev1g Configuration and Status Registers

Table 185. DEV_CFG_STATUS

Address	Short Description	Register Name
0x00	DEV_RST_CTRL register	DEV_RST_CTRL
0x02	Loopback Configuration Register	DEV_LB_CFG
0x03	Device Debug Config	DEV_DBG_CFG
0x04	Configuration for the port protectio feature	DEV_PORT_PROTECT
0x05	Precision Time Protocol Configuration	DEV_PTP_CFG

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Table 185. DEV_CFG_STATUS *(continued)*

Address	Short Description	Register Name
0x06	PTP Time Stamp Sticky Register	DEV_PTP_TX_STICKY
0x07 - 0x09	PTP Time Stamp Register	DEV_PTP_TX_TSTAMP
0x0A - 0x0C	PTP Identification Register	DEV_PTP_TX_ID

6.20.2 MAC1G Configuration and Status Registers

Table 186. MAC_CFG_STATUS

Address	Short Description	Register Name
0x0D	Mode Configuration Register	MAC_ENA_CFG
0x0E	Mode Configuration Register	MAC_MODE_CFG
0x0F	Max Length Configuration Register	MAC_MAXLEN_CFG
0x10	VLAN / Service tag configuration register	MAC_TAGS_CFG
0x11	Advanced Check Feature Configuration Register	MAC_ADV_CHK_CFG
0x12	Inter Frame Gap Configuration Register	MAC_IFG_CFG
0x13	Half Duplex Configuration Register	MAC_HDX_CFG
0x14	Sticky Bit Register	MAC_STICKY

6.20.3 PCS 1G Configuration Status Registers

Table 187. PCS1G_CFG_STATUS

Address	Short Description	Register Name
0x15	PCS1G Configuration	PCS1G_CFG
0x16	PCS1G Mode Configuration	PCS1G_MODE_CFG
0x17	PCS1G SignalDetect Configuration	PCS1G_SD_CFG
0x18	PCS1G Aneg Configuration	PCS1G_ANEG_CFG
0x19	PCS1G Aneg Nextpage Configuration	PCS1G_ANEG_NP_CFG
0x1A	PCS1G Loopback Configuration	PCS1G_LB_CFG
0x1B	PCS1G Debug Configuration	PCS1G_DBG_CFG
0x1C	PCS1G comma detection Configuration	PCS1G_CDET_CFG
0x1D	PCS1G ANEG Status Register	PCS1G_ANEG_STATUS
0x1E	PCS1G Aneg Next Page Status Register	PCS1G_ANEG_NP_STATUS
0x1F	PCS1G link status	PCS1G_LINK_STATUS
0x20	PCS1G link down counter	PCS1G_LINK_DOWN_CNT
0x21	PCS1G sticky register	PCS1G_STICKY
0x22	PCS1G debug status	PCS1G_DEBUG_STATUS
0x23	PCS1G Low Power Idle Configuration	PCS1G_LPI_CFG

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Table 187. PCS1G_CFG_STATUS *(continued)*

Address	Short Description	Register Name
0x24	PCS1G Low Power Idle Status	PCS1G_LPI_STATUS

6.20.4 PCS1G Testpattern Configuration and Status Registers

Table 188. PCS1G_TSTPAT_CFG_STATUS

Address	Short Description	Register Name
0x25	PCS1G TSTPAT MODE CFG	PCS1G_TSTPAT_MODE_CFG
0x26	PCS1G TSTPAT STATUS	PCS1G_TSTPAT_STATUS

6.20.5 PCS FX100 Configuration Registers

Table 189. PCS_FX100_CONFIGURATION

Address	Short Description	Register Name
0x27	PCS 100Base FX Configuration	PCS_FX100_CFG

6.20.6 PCS FX100 Status Registers

Table 190. PCS_FX100_STATUS

Address	Short Description	Register Name
0x28	PCS 100Base FX Status	PCS_FX100_STATUS

6.20.7 Device 1G Interrupt Configuration and Status Registers

Table 191. DEV1G_INTR_CFG_STATUS

Address	Short Description	Register Name
0x29	Dev1g Intr Configuration	DEV1G_INTR_CFG
0x2A	Dev1g Interrupt Reg	DEV1G_INTR
0x2B	Dev1g Interrupt Ident	DEV1G_INTR_IDENT

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6.21 Device NPI

The packet interface towards an external node processor. The device operates as an interface between the TAXI bus and SGMII macro supporting data rates of 10M, 100M, and 1000Mbps. The device includes PCS, MAC and rate adaption logic.

6.21.1 Dev1g Configuration and Status Registers

Table 192. DEV_CFG_STATUS

Address	Short Description	Register Name
0x00	DEV_RST_CTRL register	DEV_RST_CTRL
0x02	Loopback Configuration Register	DEV_LB_CFG
0x03	Device Debug Config	DEV_DBG_CFG
0x04	Configuration for the port protectio feature	DEV_PORT_PROTECT
0x05	Precision Time Protocol Configuration	DEV_PTP_CFG
0x06	PTP Time Stamp Sticky Register	DEV_PTP_TX_STICKY
0x07 - 0x09	PTP Time Stamp Register	DEV_PTP_TX_TSTAMP
0x0A - 0x0C	PTP Identification Register	DEV_PTP_TX_ID

6.21.2 MAC1G Configuration and Status Registers

Table 193. MAC_CFG_STATUS

Address	Short Description	Register Name
0x0D	Mode Configuration Register	MAC_ENA_CFG
0x0E	Mode Configuration Register	MAC_MODE_CFG
0x0F	Max Length Configuration Register	MAC_MAXLEN_CFG
0x10	VLAN / Service tag configuration register	MAC_TAGS_CFG
0x11	Advanced Check Feature Configuration Register	MAC_ADV_CHK_CFG
0x12	Inter Frame Gap Configuration Register	MAC_IFG_CFG
0x13	Half Duplex Configuration Register	MAC_HDX_CFG
0x14	Sticky Bit Register	MAC_STICKY

6.21.3 PCS 1G Configuration Status Registers

Table 194. PCS1G_CFG_STATUS

Address	Short Description	Register Name
0x15	PCS1G Configuration	PCS1G_CFG

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Table 194. PCS1G_CFG_STATUS *(continued)*

Address	Short Description	Register Name
0x16	PCS1G Mode Configuration	PCS1G_MODE_CFG
0x17	PCS1G SignalDetect Configuration	PCS1G_SD_CFG
0x18	PCS1G Aneg Configuration	PCS1G_ANEG_CFG
0x19	PCS1G Aneg Nextpage Configuration	PCS1G_ANEG_NP_CFG
0x1A	PCS1G Loopback Configuration	PCS1G_LB_CFG
0x1B	PCS1G Debug Configuration	PCS1G_DBG_CFG
0x1C	PCS1G comma detection Configuration	PCS1G_CDET_CFG
0x1D	PCS1G ANEG Status Register	PCS1G_ANEG_STATUS
0x1E	PCS1G Aneg Next Page Status Register	PCS1G_ANEG_NP_STATUS
0x1F	PCS1G link status	PCS1G_LINK_STATUS
0x20	PCS1G link down counter	PCS1G_LINK_DOWN_CNT
0x21	PCS1G sticky register	PCS1G_STICKY
0x22	PCS1G debug status	PCS1G_DEBUG_STATUS
0x23	PCS1G Low Power Idle Configuration	PCS1G_LPI_CFG
0x24	PCS1G Low Power Idle Status	PCS1G_LPI_STATUS

6.21.4 PCS1G Testpattern Configuration and Status Registers

Table 195. PCS1G_TSTPAT_CFG_STATUS

Address	Short Description	Register Name
0x25	PCS1G TSTPAT MODE CFG	PCS1G_TSTPAT_MODE_CFG
0x26	PCS1G TSTPAT STATUS	PCS1G_TSTPAT_STATUS

6.21.5 PCS FX100 Configuration Registers

Table 196. PCS_FX100_CONFIGURATION

Address	Short Description	Register Name
0x27	PCS 100Base FX Configuration	PCS_FX100_CFG

6.21.6 PCS FX100 Status Registers

Table 197. PCS_FX100_STATUS

Address	Short Description	Register Name
0x28	PCS 100Base FX Status	PCS_FX100_STATUS

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6.21.7 Device 1G Interrupt Configuration and Status Registers

Table 198. DEV1G_INTR_CFG_STATUS

Address	Short Description	Register Name
0x29	Dev1g Intr Configuration	DEV1G_INTR_CFG
0x2A	Dev1g Interrupt Reg	DEV1G_INTR
0x2B	Dev1g Interrupt Ident	DEV1G_INTR_IDENT

6.22 Device 10G(VAUI @ 12Gbps 2 lanes, XAUII @ 10 Gbps, XAUII @ 12 Gbps, VAUI @ 10Gbps 2 lanes and SGMII @ 10/100/1000/2500 Mbps)

6.22.1 PCS 1G Configuration Status Registers

Table 199. PCS1G_CFG_STATUS

Address	Short Description	Register Name
0x00	PCS1G Configuration	PCS1G_CFG
0x01	PCS1G Mode Configuration	PCS1G_MODE_CFG
0x02	PCS1G SignalDetect Configuration	PCS1G_SD_CFG
0x03	PCS1G Aneg Configuration	PCS1G_ANEG_CFG
0x04	PCS1G Aneg Nextpage Configuration	PCS1G_ANEG_NP_CFG
0x05	PCS1G Loopback Configuration	PCS1G_LB_CFG
0x06	PCS1G Debug Configuration	PCS1G_DBG_CFG
0x07	PCS1G comma detection Configuration	PCS1G_CDET_CFG
0x08	PCS1G ANEG Status Register	PCS1G_ANEG_STATUS
0x09	PCS1G Aneg Next Page Status Register	PCS1G_ANEG_NP_STATUS
0x0A	PCS1G link status	PCS1G_LINK_STATUS
0x0B	PCS1G link down counter	PCS1G_LINK_DOWN_CNT
0x0C	PCS1G sticky register	PCS1G_STICKY
0x0D	PCS1G debug status	PCS1G_DEBUG_STATUS
0x0E	PCS1G Low Power Idle Configuration	PCS1G_LPI_CFG
0x0F	PCS1G Low Power Idle Status	PCS1G_LPI_STATUS

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6.22.2 PCS1G Testpattern Configuration and Status Registers

Table 200. PCS1G_TSTPAT_CFG_STATUS

Address	Short Description	Register Name
0x10	PCS1G TSTPAT MODE CFG	PCS1G_TSTPAT_MODE_CFG
0x11	PCS1G TSTPAT STATUS	PCS1G_TSTPAT_STATUS

6.22.3 MAC10G Configuration and Status Registers

Table 201. MAC_CFG_STATUS

Address	Short Description	Register Name
0x12	Mode Configuration Register	MAC_ENA_CFG
0x13	Mode Configuration Register	MAC_MODE_CFG
0x14	Max Length Configuration Register	MAC_MAXLEN_CFG
0x15	VLAN / Service tag configuration register	MAC_TAGS_CFG
0x16	Advanced Check Feature Configuration Register	MAC_ADV_CHK_CFG
0x17	Link Fault Signaling Register	MAC_LFS_CFG
0x18	Miscellaneous Configuration Register	MAC_LB_CFG
0x1C	Sticky Bit Register	MAC_STICKY

6.22.4 Device Statistics Registers

Table 202. DEV_STATISTICS_32BIT

Address	Short Description	Register Name
0x1D	Rx Symbol Carrier Error Counter	RX_SYMBOL_ERR_CNT
0x1E	Rx Pause Frame Counter	RX_PAUSE_CNT
0x1F	Rx Control Frame Counter	RX_UNSUP_OPCODE_CNT
0x20	Rx Unicast Frame Counter	RX_UC_CNT
0x21	Rx Multicast Frame Counter	RX_MC_CNT
0x22	Rx Broadcast Frame Counter	RX_BC_CNT
0x23	Rx CRC Error Counter	RX_CRC_ERR_CNT
0x24	Rx Undersize Counter (valid frame format)	RX_UNDERSIZE_CNT
0x25	Rx Undersize Counter (CRC error)	RX_FRAGMENTS_CNT
0x26	Rx In-range Length Error Counter	RX_IN_RANGE_LEN_ERR_CNT
0x27	Rx Out-Of-Range Length Error Counter	RX_OUT_OF_RANGE_LEN_ERR_CNT
0x28	Rx Oversize Counter (valid frame format)	RX_OVERSIZE_CNT

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Table 202. DEV_STATISTICS_32BIT *(continued)*

Address	Short Description	Register Name
0x29	Rx Jabbers Counter	RX_JABBERS_CNT
0x2A	Rx 64 Byte Frame Counter	RX_SIZE64_CNT
0x2B	Rx 65-127 Byte Frame Counter	RX_SIZE65TO127_CNT
0x2C	Rx 128-255 Byte Frame Counter	RX_SIZE128TO255_CNT
0x2D	Rx 256-511 Byte Frame Counter	RX_SIZE256TO511_CNT
0x2E	Rx 512-1023 Byte Frame Counter	RX_SIZE512TO1023_CNT
0x2F	Rx 1024-1518 Byte Frame Counter	RX_SIZE1024TO1518_CNT
0x30	Rx 1519 To Max. Length Byte Frame Counter	RX_SIZE1519TOMAX_CNT
0x31	Rx Inter Packet Gap Shrink Counter	RX_IPG_SHRINK_CNT
0x32	Tx Pause Frame Counter	TX_PAUSE_CNT
0x33	Tx Unicast Frame Counter	TX_UC_CNT
0x34	Tx Multicast Frame Counter	TX_MC_CNT
0x35	Tx Broadcast Frame Counter	TX_BC_CNT
0x36	Tx 64 Byte Frame Counter	TX_SIZE64_CNT
0x37	Tx 65-127 Byte Frame Counter	TX_SIZE65TO127_CNT
0x38	Tx 128-255 Byte Frame Counter	TX_SIZE128TO255_CNT
0x39	Tx 256-511 Byte Frame Counter	TX_SIZE256TO511_CNT
0x3A	Tx 512-1023 Byte Frame Counter	TX_SIZE512TO1023_CNT
0x3B	Tx 1024-1518 Byte Frame Counter	TX_SIZE1024TO1518_CNT
0x3C	Tx 1519 To Max. Length Byte Frame Counter	TX_SIZE1519TOMAX_CNT
0x3D	Rx HiH Checksum Error Counter	RX_HIH_CKSM_ERR_CNT
0x3E	Rx XGMII Protocol Error Counter	RX_XGMII_PROT_ERR_CNT

6.22.5 Device Statistics Registers

Table 203. DEV_STATISTICS_40BIT

Address	Short Description	Register Name
0x3F	Rx Byte Counter	RX_IN_BYTES_CNT
0x40	Rx In Bytes Counter - MSB part	RX_IN_BYTES_MSB_CNT
0x41	Rx OK Byte Counter	RX_OK_BYTES_CNT
0x42	Rx Ok Bytes Counter - MSB part	RX_OK_BYTES_MSB_CNT
0x43	Rx Bad Byte Counter	RX_BAD_BYTES_CNT
0x44	Rx Bad Bytes Counter - MSB part	RX_BAD_BYTES_MSB_CNT
0x45	Tx Byte Counter	TX_OUT_BYTES_CNT
0x46	Tx Out Bytes Counter - MSB part	TX_OUT_BYTES_MSB_CNT
0x47	Tx OK Byte Counter	TX_OK_BYTES_CNT
0x48	Tx OK Bytes Counter - MSB part Tx OK Bytes Counter - MSB	TX_OK_BYTES_MSB_CNT

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6.22.6 PCS XAUI Configuration Registers

Table 204. PCS_XAUI_CONFIGURATION

Address	Short Description	Register Name
0x49	PCS XAUI Configuration	PCS_XAUI_CFG
0x4A	PCS XAUI Extended Configuration	PCS_XAUI_EXT_CFG
0x4B	PCS XAUI SignalDetect Configuration	PCS_XAUI_SD_CFG
0x4C	PCS Transmitter Sequence Configuration Register	PCS_XAUI_TX_SEQ_CFG
0x4D	PCS XAUI Receiver Error Counter Configuration	PCS_XAUI_RX_ERR_CNT_CFG
0x4E	PCS Interleave Mode Configuration	PCS_XAUI_INTERLEAVE_MODE_CFG
0x4F	PCS Low Power Idle Configuration	PCS_XAUI_LPI_CFG

6.22.7 PCS XAUI Status Registers

Table 205. PCS_XAUI_STATUS

Address	Short Description	Register Name
0x50	PCS Receiver Status Register	PCS_XAUI_RX_STATUS
0x51	PCS Receiver Lane Error Status	PCS_XAUI_RX_ERROR_STATUS
0x52	PCS Receiver Sequence Result Register	PCS_XAUI_RX_SEQ_REC_STATUS
0x53	PCS RX Fifo Overflow Error and Lane 0 Error Counter	PCS_XAUI_RX_FIFO_OF_ERR_L0_CNT_STATUS
0x54	PCS RX Fifo Underflow Error and Lane 1 Error Counter	PCS_XAUI_RX_FIFO_UF_ERR_L1_CNT_STATUS
0x55	PCS RX 10b8b Disparity Error and Lane 2 Error Counter	PCS_XAUI_RX_FIFO_D_ERR_L2_CNT_STATUS
0x56	PCS RX 10b8b Codegroup Error and Lane 3 Error Counter	PCS_XAUI_RX_FIFO_CG_ERR_L3_CNT_STATUS
0x57	PCS Low Power Idle Status	PCS_XAUI_LPI_STATUS

6.22.8 PCS XAUI Testpattern Configuration Registers

Table 206. PCS_XAUI_TSTPAT_CONFIGURATION

Address	Short Description	Register Name
0x58	PCS XAUI Test Pattern Configuration	PCS_XAUI_TSTPAT_CFG

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6.22.9 PCS XAUI Testpattern Status Registers

Table 207. PCS_XAUI_TSTPAT_STATUS

Address	Short Description	Register Name
0x59	Test Pattern Receive Sequence Counter	PCS_XAUI_TSTPAT_RX_SEQ_CNT_STATUS
0x5A	Test Pattern Transmit Sequence Counter	PCS_XAUI_TSTPAT_TX_SEQ_CNT_STATUS

6.22.10 PCS2x6G Configuration Registers

Table 208. PCS2X6G_CONFIGURATION

Address	Short Description	Register Name
0x5B	PCS2x6G Configuration	PCS2X6G_CFG

6.22.11 PCS2x6G Status Registers

Table 209. PCS2X6G_STATUS

Address	Short Description	Register Name
0x5C	PCS2x6G Status	PCS2X6G_STATUS
0x5D	PCS2x6G Error Status	PCS2X6G_ERR_STATUS
0x5E	PCS2x6G Error Counter	PCS2X6G_ERR_CNT_STAT

6.22.12 PCS2x6G Extended Configuration Registers

Table 210. PCS2X6G_EXT_CONFIGURATION

Address	Short Description	Register Name
0x5F	PCS2x6G Extended Configuration	PCS2X6G_EXT_CFG

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6.22.13 Device 10G Configuration and Status Registers

Table 211. DEV_CFG_STATUS

Address	Short Description	Register Name
0x60	Clock/Reset Control Register	DEV_RST_CTRL
0x61	Port Proetection Configuration Register	DEV_PORT_PROTECT
0x65	Interrupt Source Register	INTR
0x66	Interrupt Enable Register	INTR_ENA
0x67	Interrupt Status Register	INTR_IDENT
0x68	Ingress (receive) Path Status Register	DEV_RX_STATUS
0x69	Egress (transmit) Path Status Register	DEV_TX_STATUS
0x6A	Precision Time Protocol - Configuration Register	DEV_PTP_CFG
0x6B	IEEE 1588 TX Sticky Bit Register	DEV_PTP_TX_STICKY
0x6C - 0x6E	Precision Time Protocol - TX Time Stamp Register	DEV_PTP_TX_TSTAMP
0x6F - 0x71	Precision Time Protocol -Frame ID Register	DEV_PTP_TX_ID

6.23 Macro Control Register Collection

Register Collection for Control of Macros (SERDES1G, SERDES6G, LCPLL)

6.23.1 PLL5G Configuration Registers

Table 212. PLL5G_CFG

Address	Short Description	Register Name
0x00	PLL5G Configuration 0	PLL5G_CFG0
0x01	PLL5G Configuration 1	PLL5G_CFG1
0x03	PLL5G Configuration 3	PLL5G_CFG3
0x04	PLL5G Configuration 4	PLL5G_CFG4
0x05	PLL5G Configuration 5	PLL5G_CFG5

6.23.2 PLL5G Status Registers

Table 213. PLL5G_STATUS

Address	Short Description	Register Name
0x06	PLL5G Status 0	PLL5G_STATUS0

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6.23.3 RCOMP Status Registers

Table 214. RCOMP_STATUS

Address	Short Description	Register Name
0x09	RCOMP Status	RCOMP_STATUS

6.23.4 SYNC_ETH Configuration Registers

Table 215. SYNC_ETH_CFG

Address	Short Description	Register Name
0x0A	SYNC ETH Configuration 0	SYNC_ETH_CFG

6.23.5 SERDES1G Analog Configuration Registers

Table 216. SERDES1G_ANA_CFG

Address	Short Description	Register Name
0x0B	SERDES1G Deserializer Cfg	SERDES1G_DES_CFG
0x0C	SERDES1G Input Buffer Cfg	SERDES1G_IB_CFG
0x0D	SERDES1G Output Buffer Cfg	SERDES1G_OB_CFG
0x0E	SERDES1G Serializer Cfg	SERDES1G_SER_CFG
0x0F	SERDES1G Common Cfg	SERDES1G_COMMON_CFG
0x10	SERDES1G Pll Cfg	SERDES1G_PLL_CFG

6.23.6 SERDES1G Analog Status Register

Table 217. SERDES1G_ANA_STATUS

Address	Short Description	Register Name
0x11	SERDES1G Pll Status	SERDES1G_PLL_STATUS

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6.23.7 SERDES1G Digital Configuration Register

Table 218. SERDES1G_DIG_CFG

Address	Short Description	Register Name
0x12	SERDES1G DFT Configuration register 0	SERDES1G_DFT_CFG0
0x13	SERDES1G DFT Configuration register 1	SERDES1G_DFT_CFG1
0x14	SERDES1G DFT Configuration register 2	SERDES1G_DFT_CFG2
0x15	SERDES1G Test Pattern Configuration	SERDES1G_TP_CFG
0x16	SERDES1G Misc Configuration	SERDES1G_MISC_CFG

6.23.8 MCB SERDES1G Configuration Register

Table 219. MCB_SERDES1G_CFG

Address	Short Description	Register Name
0x18	MCB SERDES1G Address Cfg	MCB_SERDES1G_ADDR_CFG

6.23.9 SERDES6G Analog Configuration Registers

Table 220. SERDES6G_ANA_CFG

Address	Short Description	Register Name
0x19	SERDES6G Deserializer Cfg	SERDES6G_DES_CFG
0x1A	SERDES6G Input Buffer Cfg	SERDES6G_IB_CFG
0x1B	SERDES6G Input Buffer Cfg1	SERDES6G_IB_CFG1
0x1C	SERDES6G Output Buffer Cfg	SERDES6G_OB_CFG
0x1D	SERDES6G Output Buffer Cfg1	SERDES6G_OB_CFG1
0x1E	SERDES6G Serializer Cfg	SERDES6G_SER_CFG
0x1F	SERDES6G Common Cfg	SERDES6G_COMMON_CFG
0x20	SERDES6G Pll Cfg	SERDES6G_PLL_CFG

6.23.10 SERDES6G Analog Status Register

Table 221. SERDES6G_ANA_STATUS

Address	Short Description	Register Name
0x21	SERDES6G Pll Status	SERDES6G_PLL_STATUS

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6.23.11 SERDES6G Digital Configuration Registers

Table 222. SERDES6G_DIG_CFG

Address	Short Description	Register Name
0x22	SERDES6G Digital Configuration register	SERDES6G_DIG_CFG
0x23	SERDES6G DFT Configuration register 0	SERDES6G_DFT_CFG0
0x24	SERDES6G DFT Configuration register 1	SERDES6G_DFT_CFG1
0x25	SERDES6G DFT Configuration register 2	SERDES6G_DFT_CFG2
0x26	SERDES6G Test Pattern Configuration	SERDES6G_TP_CFG0
0x27	SERDES6G Test Pattern Configuration	SERDES6G_TP_CFG1
0x28	SERDES6G Misc Configuration	SERDES6G_MISC_CFG
0x29	SERDES6G OB ANEG Configuration	SERDES6G_OB_ANEG_CFG

6.23.12 MCB SERDES6G Configuration Register

Table 223. MCB_SERDES6G_CFG

Address	Short Description	Register Name
0x2B	MCB SERDES6G Address Cfg	MCB_SERDES6G_ADDR_CFG

6.23.13 VAUI channel Configuration Registers

Table 224. VAUI_CHANNEL_CFG

Address	Short Description	Register Name
0x2C - 0x2F	Configuration for VAUI channel	VAUI_CHANNEL_CFG

6.23.14 ANEG Configuration Registers

Table 225. ANEG_CFG (16 instances)

Address	Short Description	Register Name
0x30	ANEG Configuration	ANEG_CFG
0x31	ANEG Advertised Ability 0	ANEG_ADV_ABILITY_0
0x32	ANEG Advertised Ability 1	ANEG_ADV_ABILITY_1
0x33	ANEG Next Page 0	ANEG_NEXT_PAGE_0
0x34	ANEG Next Page 1	ANEG_NEXT_PAGE_1

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6.23.15 ANEG Status Registers

Table 226. ANEG_STATUS (16 instances)

Address	Short Description	Register Name
0x80	ANEG Link Partner Advertised Ability 0	ANEG_LP_ADV_ABILITY_0
0x81	ANEG Link Partner Advertised Ability 1	ANEG_LP_ADV_ABILITY_1
0x82	ANEG Status	ANEG_STATUS

6.24 General configuration block.

6.24.1 General registers

Table 227. CHIP_REGS

Address	Short Description	Register Name
0x00	general purpose register	GENERAL_PURPOSE
0x01	SI registers	SI
0x02	Chip Id	CHIP_ID

6.24.2 Registers for software/software interaction

Table 228. SW_REGS

Address	Short Description	Register Name
0x05	Semaphore SW interrupt enable	SEMA_INTR_ENA
0x06	Clear of semaphore SW interrupt enables	SEMA_INTR_ENA_CLR
0x07	Masking of semaphore	SEMA_INTR_ENA_SET
0x08 - 0x0F	Semaphore register	SEMA
0x10	Semaphore status	SEMA_FREE
0x11	Manually assert software interrupt	SW_INTR
0x12	Mailbox register.	MAILBOX
0x13	Mailbox register atomic clear.	MAILBOX_CLR
0x14	Mailbox register atomic set.	MAILBOX_SET

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6.24.3 Registers for access to the VCore-III SBA

Table 229. VCORE_ACCESS

Address	Short Description	Register Name
0x15	Control register for VCore-II accesses	VA_CTRL
0x16	Address register for VCore-II accesses	VA_ADDR
0x17	Data register for VCore-II accesses	VA_DATA
0x18	Data register for VCore-II accesses (w. auto increment of address)	VA_DATA_INCR
0x19	Data register for VCore-II accesses (will not initiate access)	VA_DATA_INERT

6.24.4 GPIO registers

Table 230. GPIO

Address	Short Description	Register Name
0x1A	GPIO output set	GPIO_OUT_SET
0x1B	GPIO output clear	GPIO_OUT_CLR
0x1C	GPIO output	GPIO_OUT
0x1D	GPIO input	GPIO_IN
0x1E	GPIO Pin Direction	GPIO_OE
0x1F	GPIO interrupt	GPIO_INTR
0x20	GPIO interrupt enable	GPIO_INTR_ENA
0x21		GPIO_INTR_IDENT
0x22		GPIO_ALT

6.24.5 Control of resets in the chip

Table 231. DEVCPU_RST_REGS

Address	Short Description	Register Name
0x24	Reset part or the whole chip	SOFT_CHIP_RST
0x25	Soft reset of devcpu non-configruation logic	SOFT_DEVCPU_RST

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6.24.6 Miim controller

Table 232. MIIM (2 instances)

Address	Short Description	Register Name
0x28	MIIM Status	MII_STATUS
0x2A	MIIM Command	MII_CMD
0x2B	MIIM Reply Data	MII_DATA
0x2C	MIIM Configuration	MII_CFG
0x2D	MIIM Scan 0	MII_SCAN_0
0x2E	MIIM Scan 1	MII_SCAN_1
0x2F	MIIM Results	MII_SCAN_LAST_RSLTS
0x30	MIIM Results	MII_SCAN_LAST_RSLTS_VLD

6.24.7

Table 233. MIIM_READ_SCAN

Address	Short Description	Register Name
0x3A - 0x3B	MIIM Results	MII_SCAN_RSLTS_STICKY

6.24.8 Group for the control signals of the vaui2 mux.

Table 234. VAUI2_MUX

Address	Short Description	Register Name
0x3C	DEV10G, DEV2G5 mux configuration	VAUI2_MUX

QS RAM status

Table 235. RAM_STAT

Address	Short Description	Register Name
0x3F		RAM_INTEGRITY_ERR_STICKY

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6.24.9 Temperature sensor control

Table 236. TEMP_SENSOR

Address	Short Description	Register Name
0x40		TEMP_SENSOR_CTRL
0x41		TEMP_SENSOR_DATA

6.24.10 Serial IO control configuration

Table 237. SIO_CTRL (2 instances)

Address	Short Description	Register Name
0x42 - 0x45	Input data registers	SIO_INPUT_DATA
0x46 - 0x49	Interrupt polarity for each GPIO	SIO_INT_POL
0x4A	Interrupt enable register for each port.	SIO_PORT_INT_ENA
0x4B - 0x6A	Configuration of output data values	SIO_PORT_CONFIG
0x6B	Port enable register	SIO_PORT_ENABLE
0x6C	General configuration register	SIO_CONFIG
0x6D	Configuration of the serial IO clock frequency	SIO_CLOCK
0x6E - 0x71	Interrupt register	SIO_INT_REG

6.24.11 Configuration registers for PTP

Table 238. PTP_CFG

Address	Short Description	Register Name
0xA2	Misc Configuration Register for PTP	PTP_MISC_CFG
0xA3	Configuration register for master counter upper limit	PTP_UPPER_LIMIT_CFG
0xA4	Configuration register for master counter upper limit one time adjustment	PTP_UPPER_LIMIT_1_TIME_ADJ_CFG
0xA5	Sync Interrupt enable register	PTP_SYNC_INTR_ENA_CFG
0xA6	Generated external clock high period configuration register	GEN_EXT_CLK_HIGH_PERIOD_CFG
0xA7	Generated external clock low period configuration register	GEN_EXT_CLK_LOW_PERIOD_CFG
0xA8	Configuration register for syncing of ext. clk gen to internal master sync	GEN_EXT_CLK_CFG
0xA9	Configuration register for generated clock frequency adjustment	CLK_ADJ_CFG

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6.24.12 Status registers for PTP

Table 239. PTP_STAT

Address	Short Description	Register Name
0xAA	Current PTP master timer value	PTP_CURRENT_TIME_STAT
0xAB	External sync current time status register	EXT_SYNC_CURRENT_TIME_STAT
0xAC	Stick register for external sync current time status	PTP_EVT_STAT

6.24.13 Memory integrity monitor

Table 240. MEMITGR

Address	Short Description	Register Name
0xAD	Monitor control	MEMITGR_CTRL
0xAE	Monitor status	MEMITGR_STAT
0xAF	Memory indication	MEMITGR_INFO
0xB0	Memory index	MEMITGR_IDX

6.25 CPU Device Queue System

6.25.1 Frame Extraction Related Registers

Table 241. XTR

Address	Short Description	Register Name
0x00 - 0x09	Frame Pruning	XTR_FRM_PRUNING
0x0A - 0x0D	Group Configuration	XTR_GRP_CFG
0x0E - 0x17	Map Queue to Group	XTR_MAP
0x18 - 0x1B	Read from Group FIFO	XTR_RD
0x1C - 0x1F	Software Controlled Queue Selection	XTR_QU_SEL
0x20	Queue Flush	XTR_QU_FLUSH
0x21	Extraction Status	XTR_DATA_PRESENT
0x22	Queue Debug	XTR_QU_DBG

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6.25.2 Frame Injection Related Registers

Table 242. INJ

Address	Short Description	Register Name
0x23 - 0x27	Group Configuration	INJ_GRP_CFG
0x28 - 0x2C	Write to Group FIFO	INJ_WR
0x2D - 0x31	Injection Control	INJ_CTRL
0x32	Injection Status	INJ_STATUS
0x33 - 0x37	Injection Errors	INJ_ERR
0x38	Group Configuration	VTSS_DBG

6.26 Device CPU

6.26.1 Registers for the parallel interface

Table 243. PI

Address	Short Description	Register Name
0x00	Control of PI accesses	PI_CTRL
0x01	Configruation of PI accesses	PI_CFG
0x02	Status for PI accesses	PI_STAT
0x03	Mode of the parallel interface	PI_MODE
0x04 - 0x05	Slow Data	PI_SLOW_DATA

6.26.2 Parallel Interface Master Configuration

6.26.3 Configurations for the CPU system.

Table 244. CPU_SYSTEM_CTRL

Address	Short Description	Register Name
0x00 - 0x07	General Purpose Register	GPR
0x09	Reset Settings	RESET
0x0A	General control	GENERAL_CTRL

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6.26.4 Parallel Interface Master Configuration

Table 245. PI_MST

Address	Short Description	Register Name
0x0C	PI Master Configuration	PI_MST_CFG
0x0D - 0x10	PI Master Control Register	PI_MST_CTRL
0x11 - 0x14	PI Master Status Registers	PI_MST_STATUS

6.26.5 SPI Master Configuration

Table 246. SPI_MST

Address	Short Description	Register Name
0x15	SPI Master Configuration	SPI_MST_CFG
0x16 - 0x19	SPI Master Status Registers	SPI_MST_STATUS
0x1A	Software Pin control mode register	SW_MODE

6.26.6 Interrupt Registers

Table 247. INTR

Address	Short Description	Register Name
0x1B	Interrupt sticky bits	INTR
0x1C	Interrupt enable	INTR_ENA
0x1D	Clear interrupt enable	INTR_ENA_CLR
0x1E	Set interrupt enable	INTR_ENA_SET
0x1F	Raw of interrupt source	INTR_RAW
0x20	Enable output interrupt: MIPS IRQ0	MIPS_IRQ0_ENA
0x21		MIPS_IRQ0_IDENT
0x22	Enable output interrupt: MIPS IRQ1	MIPS_IRQ1_ENA
0x23		MIPS_IRQ1_IDENT
0x24	Enable output interrupt: EXT IRQ0	EXT_IRQ0_ENA
0x25		EXT_IRQ0_IDENT
0x26	Enable output interrupt: EXT IRQ1	EXT_IRQ1_ENA
0x27		EXT_IRQ1_IDENT
0x28	Device interrupts	DEV_IDENT
0x29	Configuration register for EXT0 interrupt	EXT0_INTR_CONFIG
0x2A	Configuration register for EXT1 interrupt	EXT1_INTR_CONFIG
0x2B	Configuration register for SW0 interrupt	SW0_INTR_CONFIG

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Table 247. INTR *(continued)*

Address	Short Description	Register Name
0x2C	Configuration register for SW1 interrupt	SW1_INTR_CONFIG
0x2D	Configuration register for PI_SD0 interrupt	PI_SD0_INTR_CONFIG
0x2E	Configuration register for PI_SD1 interrupt	PI_SD1_INTR_CONFIG
0x2F	Configuration register for UART interrupt	UART_INTR_CONFIG
0x30	Configuration register for TIMER0 interrupt	TIMER0_INTR_CONFIG
0x31	Configuration register for TIMER1 interrupt	TIMER1_INTR_CONFIG
0x32	Configuration register for TIMER2 interrupt	TIMER2_INTR_CONFIG
0x33	Configuration register for FDMA interrupt	FDMA_INTR_CONFIG
0x34	Configuration register for TWI interrupt	TWI_INTR_CONFIG
0x35	Configuration register for GPIO interrupt	GPIO_INTR_CONFIG
0x36	Configuration register for SGPIO interrupt	SGPIO_INTR_CONFIG
0x37	Configuration register for DEV_ALL interrupt	DEV_ALL_INTR_CONFIG
0x38	Configuration register for BLK_ANA interrupt	BLK_ANA_INTR_CONFIG
0x39	Configuration register for XTR_RDY0 interrupt	XTR_RDY0_INTR_CONFIG
0x3A	Configuration register for XTR_RDY1 interrupt	XTR_RDY1_INTR_CONFIG
0x3B	Configuration register for XTR_RDY2 interrupt	XTR_RDY2_INTR_CONFIG
0x3C	Configuration register for XTR_RDY3 interrupt	XTR_RDY3_INTR_CONFIG
0x3D	Configuration register for INJ_RDY0 interrupt	INJ_RDY0_INTR_CONFIG
0x3E	Configuration register for INJ_RDY1 interrupt	INJ_RDY1_INTR_CONFIG
0x3F	Configuration register for INJ_RDY2 interrupt	INJ_RDY2_INTR_CONFIG
0x40	Configuration register for INJ_RDY3 interrupt	INJ_RDY3_INTR_CONFIG
0x41	Configuration register for INJ_RDY4 interrupt	INJ_RDY4_INTR_CONFIG
0x42	Configuration register for INTEGRITY interrupt	INTEGRITY_INTR_CONFIG
0x43	Configuration register for PTP_SYNC interrupt	PTP_SYNC_INTR_CONFIG

6.26.7 General Purpose DMA

Table 248. GPDMA

Address	Short Description	Register Name
0x44	Common Injection or Extraction Configuration	FDMA_CFG
0x46 - 0x4D	FDMA Channel Usage and Flow Control	FDMA_CH_CFG
0x4E - 0x52	FDMA Injection Parameters	FDMA_INJ_CFG
0x57 - 0x5A	Extraction Status for FDMA Engine	FDMA_XTR_STAT_LAST_DCB
0x5B	Frame Counter and Flow Control Status	FDMA_FRM_CNT
0x5C	FDMA Backpressure Timeout Interrupt	FDMA_BP_TO_INT
0x5D	FDMA Timeout Divider	FDMA_BP_TO_DIV

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6.26.8 Injection frame spacing

Table 249. INJ_FRM_SPC (8 instances)

Address	Short Description	Register Name
0x5E	Injection frame spacing timer	INJ_FRM_SPC_TMR
0x5F	Reload value for injection frame spacing timer	INJ_FRM_SPC_TMR_CFG
0x60	Lack counter	INJ_FRM_SPC_LACK_CNTR
0x61	Injection frame spacing configuration register	INJ_FRM_SPC_CFG

6.26.9 Timer Registers

Table 250. TIMERS

Address	Short Description	Register Name
0x7E	Watchdog Timer	WDT
0x7F	Timer Tick Divider	TIMER_TICK_DIV
0x80 - 0x82	Timer value	TIMER_VALUE
0x83 - 0x85	Timer Reload Value	TIMER_RELOAD_VALUE
0x86 - 0x88	Timer Control	TIMER_CTRL

6.26.10 DDR2/3 Memory Controller Registers

Table 251. MEMCTRL

Address	Short Description	Register Name
0x89	Control register	MEMCTRL_CTRL
0x8A	Configuration register	MEMCTRL_CFG
0x8B	Status register	MEMCTRL_STAT
0x8C	Refresh period configuration	MEMCTRL_REF_PERIOD
0x8E	Timing register 0	MEMCTRL_TIMING0
0x8F	Timing register 1	MEMCTRL_TIMING1
0x90	Timing register 2	MEMCTRL_TIMING2
0x91	Timing register 3	MEMCTRL_TIMING3
0x92	Mode Register 0 Value	MEMCTRL_MR0_VAL
0x93	Mode Register 1 / Extended Mode Register Value	MEMCTRL_MR1_VAL
0x94	Mode Register 2 / Extended Mode Register 2 Value	MEMCTRL_MR2_VAL
0x95	Mode Register 3 / Extended Mode Register 3 Value	MEMCTRL_MR3_VAL

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Table 251. MEMCTRL *(continued)*

Address	Short Description	Register Name
0x96	TBA	MEMCTRL_TERMRES_CTRL
0x98 - 0x99		MEMCTRL_DQS_DLY
0x9A - 0x9B		MEMCTRL_DQS_AUTO
0x9C	Control register	MEMPHY_CFG
0x9D	Design for test features	MEMPHY_DFT
0xA6	Impedance calibration	MEMPHY_ZCAL

6.26.11 Configuration registers

Table 252. TWI_DELAY

Address	Short Description	Register Name
0xAA	Configuration registers	TWI_CONFIG

6.26.12 UART registers

Table 253. UART

Address	Short Description	Register Name
0x00	Receive Buffer / Transmit Holding Register / Divisor (Low)	RBR_THR
0x01	Interrupt Enable Register / Divisor (High)	IER
0x02	Interrupt Identification Register / FIFO Control Register	IIR_FCR
0x03	Line Control Register	LCR
0x04	Modem Control Register	MCR
0x05	Line Status Register	LSR
0x06	Modem Status Register	MSR
0x07	Scratchpad Register	SCR
0x1F	UART Status Register	USR

6.26.13 Two-Wire Interface Controller Registers

Table 254. TWI

Address	Short Description	Register Name
0x00	TWI Configuration	CFG
0x01	Target Address	TAR

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Table 254. TWI *(continued)*

Address	Short Description	Register Name
0x02	Slave Address	SAR
0x04	Rx/Tx Data Buffer and Command	DATA_CMD
0x05	Standard Speed TWI Clock SCL High Count	SS_SCL_HCNT
0x06	Standard Speed TWI Clock SCL Low Count	SS_SCL_LCNT
0x07	Fast Speed TWI Clock SCL High Count	FS_SCL_HCNT
0x08	Fast Speed TWI Clock SCL Low Count	FS_SCL_LCNT
0x0B	Interrupt Status	INTR_STAT
0x0C	Interrupt Mask	INTR_MASK
0x0D	Raw Interrupt Status	RAW_INTR_STAT
0x0E	Receive FIFO Threshold	RX_TL
0x0F	Transmit FIFO Threshold	TX_TL
0x10	Clear Combined and Individual Interrupt	CLR_INTR
0x11	Clear RX_UNDER Interrupt	CLR_RX_UNDER
0x12	Clear RX_OVER Interrupt	CLR_RX_OVER
0x13	Clear TX_OVER Interrupt	CLR_TX_OVER
0x14	Clear RD_REQ Interrupt	CLR_RD_REQ
0x15	Clear TX_ABRT Interrupt	CLR_TX_ABRT
0x16	Clear RX_DONE Interrupt	CLR_RX_DONE
0x17	Clear ACTIVITY Interrupt	CLR_ACTIVITY
0x18	Clear STOP_DET Interrupt	CLR_STOP_DET
0x19	Clear START_DET Interrupt	CLR_START_DET
0x1A	Clear GEN_CALL Interrupt	CLR_GEN_CALL
0x1B	TWI Control	CTRL
0x1C	TWI Status	STAT
0x1D	Transmit FIFO Level	TXFLR
0x1E	Receive FIFO Level	RXFLR
0x20	Transmit Abort Source	TX_ABRT_SOURCE
0x25	SDA Setup	SDA_SETUP
0x26	ACK General Call	ACK_GEN_CALL
0x27	Enable Status	ENABLE_STATUS

6.26.14 Shared Bus arbiter registers

Table 255. SBA

Address	Short Description	Register Name
0x00	Arbitration Priority CPU Data Interface	PL1
0x01	Arbitration Priority CPU Instruction Interface	PL2
0x02	Arbitration Priority FDMA	PL3
0x13	Weighted-Token Arbitration Scheme Enable	WT_EN

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Table 255. SBA *(continued)*

Address	Short Description	Register Name
0x14	Clock Tokens Refresh Period	WT_TCL
0x15	Clock Tokens CPU Data Interface	WT_CL1
0x16	Clock Tokens CPU Instruction Interface	WT_CL2
0x17	Clock Tokens FDMA Interface	WT_CL3

6.26.15 Frame DMA Controller

6.26.16 DMA Channel Controller Configuration

Table 256. CH (8 instances)

Address	Short Description	Register Name
0x00	Source Address	SAR
0x02	Destination Address	DAR
0x04	Linked List Pointer	LLP
0x06	DMA Transfer Control	CTL0
0x07	DMA Transfer Control	CTL1
0x08	Source Status	SSTAT
0x0A	Destination Status	DSTAT
0x0C	Source Status Address Location	SSTATAR
0x0E	Destination Status Address Location	DSTATAR
0x10	DMA Transfer Configuration (CFG0)	CFG0
0x11	DMA Transfer Configuration (CFG1)	CFG1

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6.26.17 DMA Interrupt Configuration

Table 257. INTR

Address	Short Description	Register Name
0xB0	Raw Status for IntTfr Interrupt	RAW_TFR
0xB2	Raw Status for IntBlock Interrupt	RAW_BLOCK
0xB8	Raw Status for IntErr Interrupt	RAW_ERR
0xBA	Status for IntTfr Interrupt	STATUS_TFR
0xBC	Status for IntBlock Interrupt	STATUS_BLOCK
0xC2	Status for IntErr Interrupt	STATUS_ERR
0xC4	Mask for IntTfr Interrupt	MASK_TFR
0xC6	Mask for IntBlock Interrupt	MASK_BLOCK
0xCC	Mask for IntErr Interrupt	MASK_ERR
0xCE	Clear for IntTfr Interrupt	CLEAR_TFR
0xD0	Clear for IntBlock Interrupt	CLEAR_BLOCK
0xD6	Clear for IntErr Interrupt	CLEAR_ERR
0xD8	Status for each interrupt type	STATUSINT

6.26.18 Miscellaneous FDMA Register

Table 258. MISC

Address	Short Description	Register Name
0xE6	DMA Enable	DMA_CFG_REG
0xE8	DMA Channel Enable	CH_EN_REG

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7 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC7462 device.

7.1 DC Characteristics

This section contains the DC specifications for the VSC7462 device.

7.1.1 Internal Pull-Up or Pull-Down Resistors

Internal pull-up or pull-down resistors are specified in the following table. For more information about signals with internal pull-up or pull-down resistors, see "Pins by Function," page 241.

All internal pull-up resistors are connected to their respective I/O supply.

Table 259. Internal Pull-Up or Pull-Down Resistors

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Internal pull-up resistor	R_{PU}	34	39	90	kΩ
Internal pull-down resistor	R_{PD}	37	45	112	kΩ

7.1.2 Reference Clock

The following table shows the DC specifications for the differential RefClk signal. Differential and single-ended modes are supported. For more information about single-ended mode operation, see "Single-Ended RefClk Input," page 267.

Table 260. RefClk Input DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit
Input voltage range	V_{IP}, V_{IN}	–25	1260	mV
Input differential voltage	$\|V_{ID}\|$	150	1000	mVp-p
Input common-mode voltage	V_{CM}	0	1200(1)	mV

1. The maximum common-mode voltage is given without any differential signal, because the input is internally AC-coupled. The common-mode voltage is only limited by the maximum and minimum input voltage range and the input signal's differential amplitude.

7.1.3 DDR2 SDRAM Interface

The DDR2 SDRAM interface supports the requirements of SDRAM devices as described in the JEDEC DDR2 specifications. The SDRAM interface signals are compatible with JESD79-2E (DDR2 SDRAM SPECIFICATION, April 2008) and the JESD8-15A (Stub Series Terminated Logic for 1.8V (SSTL_18), September 2003). The SSTL I/O buffers have programmable on-die termination (ODT).

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The following table shows the DC specifications for SDRAM interface signals. For more information about applications, see "DDR2 SDRAM Interface," page 271.

Table 261. DDR2 SDRAM Signal DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input voltage reference(1)	DDR_V_{REF}	49% V_{DD_IODDR}	51% V_{DD_IODDR}	V	
Input voltage high	$V_{IH(DC)}$	DDR_V_{REF} + 0.125	V_{DD_IODDR} + 0.3	V	
Input voltage low	$V_{IL(DC)}$	–0.3	DDR_V_{REF} – 0.125	V	
Input leakage current	I_L	–1.4	18.3	µA	$0V \le V_I \le V_{DD_IODDR}$
Output source DC current	I_{OH}	–12.6		mA	V_{DD_IODDR} = 1.7 V $V_{OUT} \ge$ 1.420 V
Output sink DC current	I_{OL}	12.6		mA	V_{DD_IODDR} = 1.7 V $V_{OUT} \le$ 280 mV

1. DDR_V_{REF} is expected to track variations in V_{DD_IODDR}. Peak-to-peak AC noise on DDR_V_{REF} must not exceed ±2% of DDR_V_{REF}.

7.1.4 SGMII Interface

This section provides the DC specifications for the SGMII interface.

The following figures illustrate the definitions of the SGMII potential. The first illustration shows the SGMII DC transmit test circuit, and the second illustration shows the SGMII DC definitions.

Figure 54. SGMII DC Transmit Test Circuit

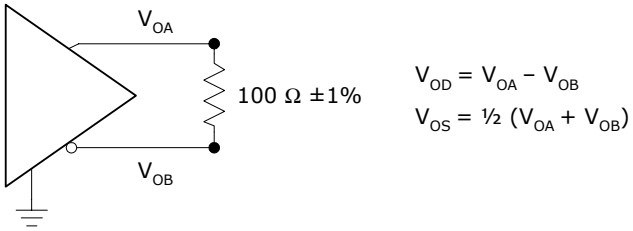

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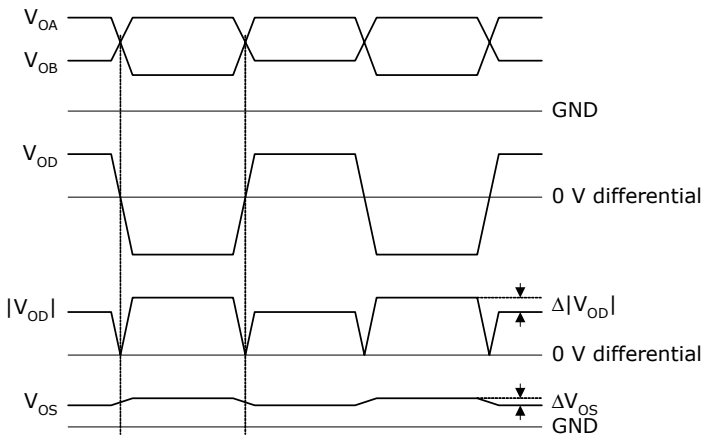
Figure 55. SGMII DC Definitions



$\Delta|V_{OD}| = | \, |V_{OAH} - V_{OBL}| - |V_{OBH} - V_{OAL}| \, |$

$\Delta V_{OS} = | \, ½(V_{OAH} + V_{OBL}) - ½(V_{OAL} + V_{OBH}) \, |$

The following table shows the DC specifications for the SGMII driver. The values are valid for all configurations, unless stated otherwise.

Table 262. SGMII Driver DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, V_{OA} or V_{OB}	V_{OH}		1260	mV	R_L = 100 Ω ±1%
Output low voltage, V_{OA} or V_{OB}	V_{OL}	0		mV	R_L = 100 Ω ±1%
Output differential peak voltage(1)	$\|V_{OD}\|$	150	400	mVp	$V_{DD_IOSGMII}$ = 1.0 V R_L = 100 Ω ±1%
		150	600	mVp	$V_{DD_IOSGMII}$ = 1.2 V R_L = 100 Ω ±1%
		150	400	mVp	SGMII mode
		400	600	mVp	1000BASE-KX mode $V_{DD_IOSGMII}$ = 1.2 V
		300	600	mVp	SFP mode
Output offset voltage(2)	V_{OS}	420	580	mV	$V_{DD_IOSGMII}$ = 1.0 V R_L = 100 Ω ±1%
		445	605	mV	$V_{DD_IOSGMII}$ = 1.2 V R_L = 100 Ω ±1%
DC output impedance, single-ended	R_O	40	140	Ω	SGMII mode R_L = 100 Ω ±1%
R_O mismatch between A and B(3)	ΔR_O		10	%	SGMII mode
Change in $\|V_{OD}\|$ between 0 and 1	$\Delta\|V_{OD}\|$		25	mV	SGMII mode R_L = 100 Ω ±1%
Change in V_{OS} between 0 and 1	ΔV_{OS}		25	mV	SGMII mode R_L = 100 Ω ±1%

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Table 262. SGMII Driver DC Specifications *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output current	$\|I_{OSA}\|$, $\|I_{OSB}\|$		40	mA	SGMII mode, driver shorted to GND
Output current	$\|I_{OSAB}\|$		12	mA	SGMII mode, drivers shorted together

1. Voltage is adjustable in 14 steps.
2. Requires AC-coupling for SGMII compliance.
3. Matching of reflection coefficients. For more information about test methods, see IEEE Std 1596.3-1996.

Figure 56. SGMII DC Driver Output Impedance Test Circuit

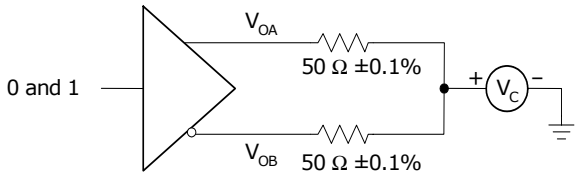
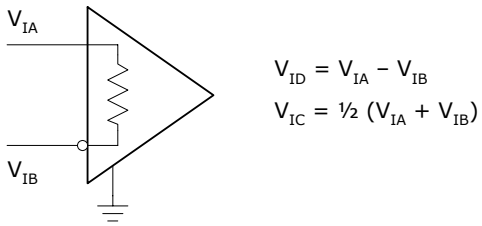


Figure 57. SGMII DC Input Definitions



The following table shows the DC specifications for the SGMII receivers.

Table 263. SGMII Receiver DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input voltage range, V_{IA} or V_{IB}	V_I	–25	1260	mV	
Input differential voltage	$\|V_{ID}\|$	50	1000	mVp-p	
Input common-mode voltage(1)	V_{IC}	0	1200(2)	mV	Without any differential signal (internally AC-coupled)
Receiver differential input impedance	R_I	80	120	Ω	
Input differential hysteresis	V_{HYST}	25		mV	SGMII mode

1. SGMII compliancy requires AC-coupling.
2. The maximum common-mode voltage is given without any differential signal, because the input is internally AC-coupled. The common-mode voltage is only limited by the maximum and minimum input voltage range and the input signal's differential amplitude.

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7.1.5 PI, GPIO, SI, JTAG, and Miscellaneous Signals

This section provides the DC specifications for the PI, GPIO, SI, JTAG, and miscellaneous signals.

The following I/O signals comply with the specifications provided in this section.

PI_Addr[25:0]	GPIO[23:0]	JTAG_nTRST	nReset
PI_Data[15:0]	SI_Clk	JTAG_TMS	Test_mode1
PI_nCS0	SI_DI	JTAG_TDO	TestCfg[3:0]
PI_nDone	SI_DO	JTAG_TCK	VCore_Cfg[1:0]
PI_nOE	SI_nCS0	JTAG_TDI	VCore_BE_en
PI_nWR			VCore_ICE_nEN
RefClk_Sel[2:0]			

The outputs and inputs meet or exceed the requirements of the LVTTL and LVCMOS standard, JEDEC JESD8-B (September 1999) standard, unless otherwise stated. The inputs are Schmitt-trigger for noise immunity.

Table 264. PI, SI, JTAG, and Miscellaneous Signals DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4		V	I_{OH} = –14 mA
Output low voltage	V_{OL}		0.4	V	I_{OL} = 14 mA
Input high voltage	V_{IH}	2.0	3.6	V	
Input low voltage	V_{IL}	–0.3	0.8	V	
Input high current(1)	I_{IH}		10	µA	$V_I = V_{DD_IO33}$
Input low current(1)	I_{IL}	–10		µA	V_I = 0 V

1. Input high current and input low current equals the maximum leakage current, excluding the current in the built-in pull resistors.

7.1.6 XAUI Interface

This section provides the DC specifications for the XAUI interface.

The XAUI interface operates in various modes, which are described in the following table. For more information about the parameter definitions, see Figure 54, page 201 and Figure 55, page 202.

The following table shows the DC specifications for the XAUI driver.

Table 265. XAUI Driver DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, V_{OA} or V_{OB}	V_{OH}		V_{DD_IOXAUI}	mV	R_L = 100 Ω ±1%
Output low voltage, V_{OA} or V_{OB}	V_{OL}	0		mV	R_L = 100 Ω ±1%

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Table 265. XAUI Driver DC Specifications *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output differential peak voltage(1)	$\|V_{OD}\|$	300	360	mVp	V_{DD_IOXAUI} = 1.0 V R_L = 100 Ω ±1% Maximum drive
		400	600	mVp	V_{DD_IOXAUI} = 1.2 V R_L = 100 Ω ±1% Maximum drive
		150	400	mVp	SGMII mode
		400	600	mVp	1000BASE-KX mode V_{DD_IOXAUI} = 1.2 V
		300	600	mVp	SFP mode
		400	600	mVp	XAUI mode V_{DD_IOXAUI} = 1.2 V
		400	600	mVp	10GBASE-CX4 mode $V_{DD_IOXAUII}$ = 1.2 V
		400	600	mVp	10GBASE-KX4 mode V_{DD_IOXAUI} = 1.2 V
		200	375	mVp	CEI-6G-SR mode
Output offset voltage(2)	V_{OS}	250	1050	mVp	V_{DD_IOXAUI} = 1.0 V R_L = 100 Ω ±1%
		460	1260	mV	V_{DD_IOXAUI} = 1.2 V R_L = 100 Ω ±1%
DC output impedance, single-ended	R_O	80	120	Ω	V_{DD_IOXAUI} = 1.0 V R_L = 100 Ω ±1%
R_O mismatch between A and B(3)	ΔR_O		10	%	SGMII mode See Figure 56, page 203.
Change in $\|V_{OD}\|$ between 0 and 1	$\Delta\|V_{OD}\|$		25	mV	SGMII mode R_L = 100 Ω ±1%
Change in V_{OS} between 0 and 1	ΔV_{OS}		25	mV	SGMII mode R_L = 100 Ω ±1%
Output current to GND	$\|I_{OSA}\|$, $\|I_{OSB}\|$		40	mA	SGMII mode Driver shorted to GND
			100	mA	CEI-6G-SR mode Driver shorted to GND
Output current	$\|I_{OSAB}\|$		12	mA	SGMII mode Drivers shorted together
			100	mA	CEI-6G-SR mode Drivers shorted together

1. Programmable differential voltage.
2. Requires AC-coupling for SGMII compliance.
3. Matching of reflection coefficients. For more information about test methods, see IEEE Std 1596.3-1996.

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The following table shows the DC specifications for the XAUI receivers.

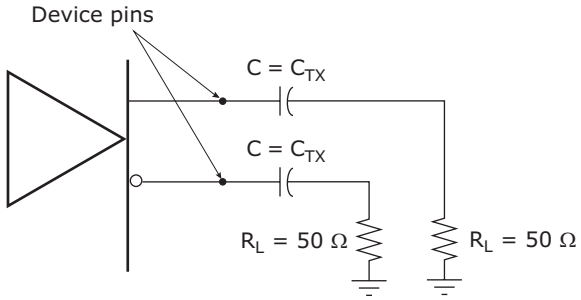
Table 266. XAUI Receiver DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input voltage range, V_{IA} or V_{IB}	V_I	–25	1200	mV	
Input differential voltage	$\|V_{ID}\|$		1200	mVp-p	
Input common-mode voltage(1)	V_{IC}	0	1200(2)	mV	Without any differential signal (internally AC-coupled)
Receiver differential input impedance	R_I	80	120	Ω	SGMII mode
Input differential hysteresis	V_{HYST}	25		mV	SGMII mode
Common-mode impedance		30	50	Ω	SGMII mode, CM-termination enabled

1. SGMII compliancy requires AC-coupling.
2. The maximum common-mode voltage is given without any differential signal, because the input is internally AC-coupled. The common-mode voltage is only limited by the maximum and minimum input voltage range and the input signal's differential amplitude.

The following illustration shows the test circuit for the XAUI interface.

Figure 58. XAUI Test Circuit



7.1.7 MII Management

The outputs and inputs of the MII Management (MIIM) interface meet or exceed the requirements of IEEE Std 802.3-2002 for the MII (Clause 22.4), except for 5.5 V input tolerance.

Each MIIM interface has a separate supply pin allowing operation in either 2.5 V or 3.3 V mode.

The following I/O signals comply with the specifications provided in this section.

MDC0

MDC1

MDIO0

MDIO1

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All MII Management outputs and inputs comply with the specifications in the following table.

Table 267. MIIM Interface DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.0		V	I_{OH} = –10 mA VDD_MIIM*x* = 2 5 V ±5%
		2.4		V	I_{OH} = –10 mA VDD_MIIM*x* = 3 3 V ±5%
Output low voltage	V_{OL}	–0.3	0.4	V	I_{OL} = 10 mA VDD_MIIM*x* = 2 5 V ±5%
			0.4	V	I_{OL} = 10 mA VDD_MIIM*x* = 3 3 V ±5%
Input high voltage	V_{IH}	1.7	2.8	V	VDD_MIIM*x* = 2 5 V ±5%
		2.0	3.6	V	VDD_MIIM*x* = 3 3 V ±5%
Input low voltage	V_{IL}	–0.3	0.7	V	VDD_MIIM*x* = 2 5 V ±5%
		–0.3	0.8	V	VDD_MIIM*x* = 3 3 V ±5%

7.1.8 Status Channel Interface

The status channel interfaces are compatible with the SPI-4.2 LVTTL status channel specifications defined in OIF-SPI-4-02.1.

The status channel interface has a separate dedicated I/O supply to allow operation in either 2.5 V or 3.3 V mode. The status channel I/O supply is common to both status channels.

The following I/O signals comply with the specifications provided in the following table.

STATA_IB_SCLK	STATB_IB_SCLK	STATA_OB_SCLK	STATB_OB_SCLK
STATA_IB_STAT0	STATB_IB_STAT0	STATA_OB_STAT0	STATB_OB_STAT0
STATA_IB_STAT1	STATB_IB_STAT1	STATA_OB_STAT1	STATB_OB_STAT1

Table 268. Status Channel Interface DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, 3.3 V mode	V_{OH}	2.4		V	I_{OH} = –15 mA
Output high voltage, 2.5 V mode	V_{OH}	2.0		V	I_{OH} = –15 mA
Output low voltage	V_{OL}		0.4	V	I_{OL} = 15 mA
Input high voltage, 3.3 V mode	V_{IH}	2.0	3.6	V	
Input high voltage, 2.5 V mode	V_{IH}	1.7	2.8	V	

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Table 268. Status Channel Interface DC Specifications *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input low voltage, 3.3 V mode	V_{IL}	–0.3	0.8	V	
Input low voltage, 2.5 V mode	V_{IL}	–0.3	0.7	V	

7.1.9 Recovered Clock Output

The following table shows the DC specifications for the RCVRD_CLK0 and RCVRD_CLK1 recovered clock output signals.

Table 269. Recovered Clock Output DC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4		V	I_{OH} = –15 mA V_{DD_IO33} = 3.3 V ±5%
Output low voltage	V_{OL}	0	0.4	V	I_{OL} = 15 mA V_{DD_IO33} = 3.3 V ±5%

7.1.10 Thermal Diode

The VSC7462 device includes an on-die diode and internal circuitry for monitoring die temperature (junction temperature). The operation and accuracy of the diode is not guaranteed and should only be used as a reference.

A thermal sensor, located on the board or in a stand-alone measurement kit, can monitor and display the die temperature of the switch for thermal management or instrumentation purposes.

Temperature measurement using a thermal diode is very sensitive to noise.

The following table provides the diode parameter and interface specifications. Note that the ThermDC pin is connected to VSS internally in the device.

Table 270. Thermal Diode Parameters

Parameter	Symbol	Typical	Maximum	Unit
Forward bias current	IFW		1	mA
Diode ideality factor	n	1.008		

Notes Vitesse does not support or recommend operation of the thermal diode under reverse bias.

The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{fw} = I_s \times e^{V_d \times \frac{q}{nkT} - 1}$$

where, Is = saturation current, q = electronic charge, Vd = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).

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7.2 AC Characteristics

This section provides the AC specifications for the VSC7462 device.

7.2.1 Reference Clock

The signal applied to the RefClk differential input must comply with the requirements listed in the following table at the pin of the device.

Table 271. RefClk AC Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
RefClk frequency	f	–100 ppm	125	100 ppm	MHz	RefClk_Sel = 000
		–100 ppm	156.25	100 ppm	MHz	RefClk_Sel = 001
		–100 ppm	25	100 ppm	MHz	RefClk_Sel = 100
Clock duty cycle		40		60	%	Measured at 50% threshold
Rise time and fall time	t_R, t_F			1.5	ns	20% to 80% threshold
RefClk input peak-to-peak jitter				TBD	ps	Jitter bandwidth between TBD kHz and TBD MHz
				TBD	ps	Jitter bandwidth between TBD kHz and TBD MHz
Jitter transfer from RefClk to SGMII output				TBD	dB	Jitter bandwidth between TBD kHz and TBD MHz
				TBD	dB	Jitter bandwidth between TBD kHz and TBD MHz
Jitter transfer between RefClk and XAUI output				TBD	dB	Jitter bandwidth between TBD kHz and TBD MHz
				TBD	dB	Jitter bandwidth between TBD kHz and TBD MHz

7.2.2 Reset Timing

The nReset signal waveform and the required measurement points for the timing specification are shown in the following illustration.

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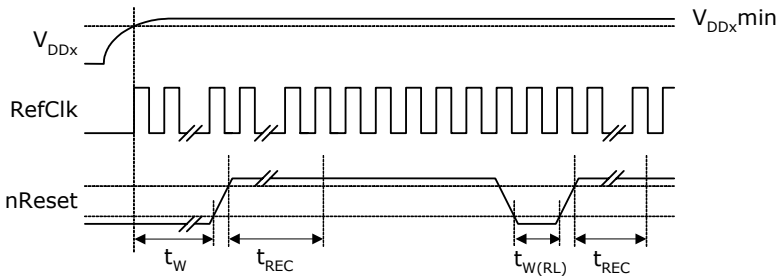
Figure 59. nReset Signal Timing Specifications



The signal applied to the nReset input must comply with the specifications listed in the following table at the reset pin of the device.

Table 272. nReset Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit
nReset assertion time after power supplies and clock stabilizes	t_W	2		ms
Recovery time from reset inactive to device fully active	t_{REC}		5	ms
nReset pulse width	$t_{W(RL)}$	100		ns

7.2.3 SGMII Interface

In SGMII mode, the SGMII interface is compliant with Serial-GMII Specification, version 1.9.

In 1000BASE-KX mode, the SGMII interface is compliant with IEEE 802.3 clause 70.

In SFP mode, the SGMII interface is compliant with the SFP MSA standard.

In 100BASE-FX mode, the SGMII interface is compliant with IEEE 802.3 clause 26.

The rise time and fall time parameters and other transient performance specifications are defined in the following illustration. The definition of V_S is the difference between the steady state high and low voltage of the differential signal.

In addition, the signals are monotonic between 20% and 80% of V_S when loaded with 100 Ω ±1%.

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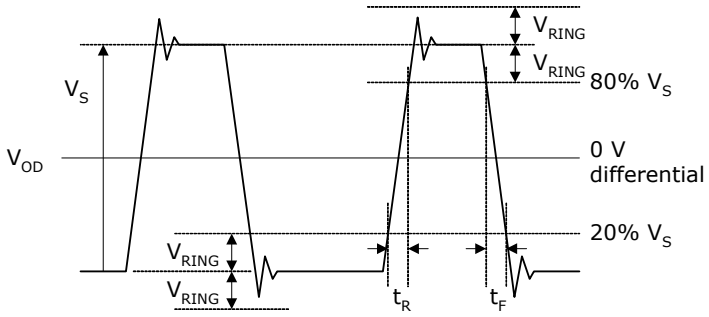
Figure 60. SGMII Transient Parameters



All SGMII driver signals comply with the conditions listed in the following table when measured with the test circuit shown in Figure 54, page 201.

7.2.4 SGMII Outputs

The values in the following table are valid for all configurations, unless stated in the conditions column.

Table 273. SGMII Output AC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
V_{OD} ringing compared to V_S	V_{RING}		±10	%	SGMII mode R_L = 100 Ω ±1%
V_{OD} rise time and fall time	t_R, t_F	100	200	ps	20% to 80% of V_S SGMII mode R_L = 100 Ω ±1%
Differential output voltage	V_{OD}		30	mVp-p	Tx disabled
Differential output return loss	RL_{TX_DIFF}	≥10		dB	50 MHz to 625 MHz 1000BASE-KX mode R_L = 100 Ω ±1%
		10–10 × log (f/625 MHz)		dB	625 MHz to 1250 MHz 1000BASE-KX mode R_L = 100 Ω ±1%
Common mode return loss	RL_{CM}	6		dB	1000BASE-KX mode 50 MHz to 625 MHz
Interpair skew	t_{SKEW}		20	ps	SGMII mode

7.2.5 SGMII Driver Jitter Characteristics

The following table shows the jitter characteristics for the SGMII driver.

Table 274. SGMII Driver Jitter Characteristics

Parameter	Symbol	Maximum	Unit	Condition
Total output jitter	$t_{JIT(O)}$	192	ps	Measured according to IEEE 802.3.38.5.

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Table 274. SGMII Driver Jitter Characteristics

Parameter	Symbol	Maximum	Unit	Condition
Deterministic output jitter	$t_{JIT(OD)}$	80	ps	Measured according to IEEE 802.3.38.5.

7.2.6 SGMII Inputs

The following table shows the AC specifications for the SGMII inputs.

Table 275. SGMII Input AC Specifications

Parameter	Symbol	Maximum	Unit	Condition
Differential input return loss, 50 MHz to 625 MHz		≥10	dB	1000BASE-KX mode R_L = 100 Ω ±1%
Differential input return loss, 625 MHz to 1250 MHz		10–10 × log (f/625 MHz)	dB	1000BASE-KX mode R_L = 100 Ω ±1%

7.2.7 SGMII Receiver Jitter Tolerance

The following table shows jitter tolerances for the SGMII receiver.

Table 276. SGMII Receiver Jitter Tolerance

Parameter	Symbol	Minimum	Unit	Condition
Total input jitter tolerance	$t_{JIT(I)}$	599	ps	1000BASE-KX and SFP mode Above 637 kHz Measured according to IEEE 802.3 38.6.8
Deterministic input jitter tolerance	$t_{JIT(ID)}$	370	ps	1000BASE-KX and SFP mode Above 637 kHz Measured according to IEEE 802.3 38.6.8
Cycle distortion input jitter tolerance	D_{CD}	1.4	ns	100BASE-FX mode Measured according to ISO/IEC 9314-3:1990
Data-dependent input jitter tolerance	D_{DJ}	2.2	ns	100BASE-FX mode Measured according to ISO/IEC 9314-3:1990
Random input jitter tolerance, peak-to-peak	R_J	2.27	ns	100BASE-FX mode Measured according to ISO/IEC 9314-3:1990

7.2.8 XAUI Interface

In XAUI mode, the XAUI interfaces meet or exceed the requirement of IEEE 802.3-2005 clause 47.3.

In SGMII mode, the XAUI interfaces are compliant with the Serial GMII Specification version 1.9.

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In 1000BASE-KX mode, the XAUI interfaces are compliant with IEEE 802.3 clause 70.

In SFP mode, the XAUI interfaces are compliant with the SFP MSA specifications.

In 100BASE-FX mode, the XAUI interfaces are compliant with IEEE 802.3 clause 26.

In 10GBASE-CX4 mode, the XAUI interfaces are compliant with IEEE 802.3-2005 clause 54.

In 10GBASE-KX4 mode, the XAUI interfaces are compliant with IEEE 802.3-2005 clause 71.

7.2.9 XAUI Outputs

The following table shows the AC specifications for the XAUI outputs. The values are valid for all configurations, unless otherwise noted.

Table 277. XAUI Output AC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Signal speed per lane		125M – 100 ppm	125M + 100 ppm	Baud	100BASE-FX mode.
		1.25 – 100 ppm	1.25 + 100 ppm	Baud	1000BASE-KX, SGMII, and SFP modes.
		3.125G – 100 ppm	3.125G + 100 ppm	Baud	XAUI, 2.5G, 10GBASE-KX4, and 10GBASE-CX4 modes.
		6.25G – 100 ppm	6.25G + 100 ppm	Baud	10G two-lane XAUI and 12G two-lane interconnect mode.
		3.75G – 100 ppm	3.75G + 100 ppm	Baud	Overclocked XAUI mode.
V_{OD} ringing compared to V_S	V_{RING}		±10	%	SGMII mode. R_L = 100 Ω ±1%.
V_{OD} rise time and fall time	t_R, t_F	100	200	ps	SGMII mode. 20% to 80% of V_S. R_L = 100 Ω ±1%.
		60	130	ps	10GBASE-CX4 mode. 20% to 80% of V_S. R_L = 100 Ω ±1%.
Differential output voltage	V_{OD}		30	mVp-p	Tx disabled.

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Table 277. XAUI Output AC Specifications *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Differential output return loss	RL_{TX_DIFF}	10		dB	1000BASE-KX mode. R_L = 100 Ω ±1%. 50 MHz to 625 MHz.
		10–10 × log (*f*/625 MHz)		dB	1000BASE-KX mode. R_L = 100 Ω ±1%. 625 MHz to 1250 MHz.
		10		dB	XAUI and 2.5G modes. 312.5 MHz to 625 MHz.
		10–10 × log (*f*/625 MHz)		dB	XAUI and 2.5G modes 625 MHz to 3.125 GHz.
		10		dB	10GBASE-CX4 and 10GBASE-KX4 modes. 100 MHz to 625 MHz.
		10–10 × log (*f*/625 MHz)		dB	10GBASE-CX4 and 10GBASE-KX4 modes. 625 MHz to 2 GHz.
		8		dB	CEI-6G-SR mode. 100 MHz to 4.69 GHz.
		8–16.6 × log (*f*/4.69 GHz)		dB	CEI-6G-SR mode. 4.69 GHz to 6.25 GHz.
Output common-mode return loss		6		dB	CEI-6G-SR mode. 100 MHz to 4.69 GHz.
Eye mask (X1)			0.125	UI	1000BASE-KX mode. Measured at near-end. See Figure 62, page 217.
			0.175	UI	XAUI and 2.5G modes. Measured at near-end. See Figure 62, page 217.
			0.15	UI	CEI-6G-SR mode. Measured at near-end. See Figure 62, page 217.
Eye mask (X2)			0.325	UI	1000BASE-KX mode. Measured at near-end. See Figure 62, page 217.
			0.390	UI	XAUI and 2.5G modes. Measured at near-end See Figure 62, page 217.
			0.4	UI	CEI-6G-SR mode. Measured at near-end. See Figure 62, page 217.

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Table 277. XAUI Output AC Specifications *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Eye mask (A1)		400		mV	1000BASE-KX and XAUI modes. Measured at near-end. See Figure 62, page 217.
		200		mV	CEI-6G-SR mode. Measured at near-end. See Figure 62, page 217.
Eye mask (A2)			800	mV	1000BASE-KX and XAUI modes. Measured at near-end. See Figure 62, page 217.
			375	UI	CEI-6G-SR mode. Measured at near-end. See Figure 62, page 217.

Table 278. XAUI Output Template Specifications

Parameter	Condition	Output template according to
Output template	10GBASE-CX4 mode	IEEE 802.3 54.6.3.6

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7.2.10 XAUI Inputs

The XAUI receiver operates with a bit error rate (BER) of better than 10^{-12} when receiving a compliant transmitter signal through a compliant channel as defined in the standard or specification on which the operation mode is based.

Table 279. XAUI Input AC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Differential input return loss	RL_{RX_DIFF}	10		dB	1000BASE-KX mode. R_L = 100 Ω ±1%. 50 MHz to 625 MHz.
		10–10 × log (ƒ/625 MHz)		dB	1000BASE-KX mode. R_L = 100 Ω ±1%. 625 MHz to 1250 MHz.
		10		dB	XAUI mode. 100 MHz to 2.5 GHz.
		10		dB	10GBASE-CX4 and 10GBASE-KX4 modes. 100 MHz to 625 MHz.
		10–10 × log (ƒ/625 MHz)		dB	10GBASE-CX4 and 10GBASE-KX4 modes. 625 MHz to 2 GHz.
		8		dB	CEI-6G-SR mode. 100 MHz to 4.69 GHz.
		8–16.6 × log (ƒ/4.69 GHz)		dB	CEI-6G-SR mode. 4.69 GHz to 6.25 GHz.
Input common-mode return loss(1)		6		dB	XAUI mode. 100 MHz to 2.5 GHz.
Eye mask (X1)			0.275	UI	XAUI mode. See Figure 62, page 217.
Eye mask (X2)			0.400	UI	XAUI mode. See Figure 62, page 217.
Eye mask (A1)		100		mV	XAUI mode. See Figure 62, page 217.
Eye mask (A2)			800	mV	XAUI mode. Measured at far-end See Figure 62, page 217.

1. 25 Ω reference common-mode impedance.

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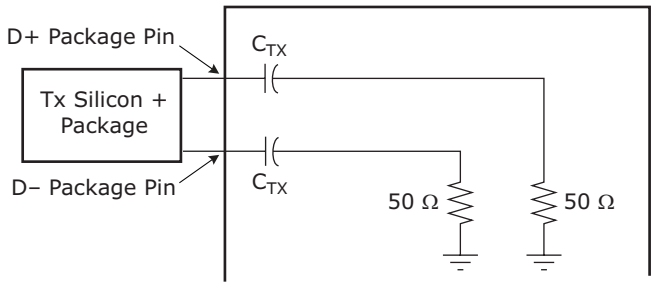
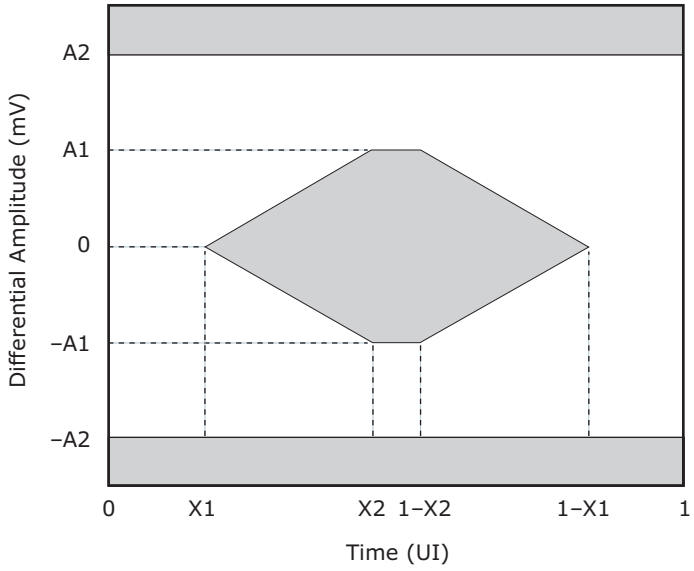
Figure 61. Compliance Test and Measurement Load



The following illustration shows the compliance mask for the XAUI and CEI-6G-SR inputs and outputs.

Figure 62. XAUI and CEI-6G-SR Inputs and Outputs Compliance Mask



7.2.11 MII Management

All AC specifications for the MII Management (MIIM) interface meet or exceed the requirements of IEEE Std 802.3-2002 (clause 22.2-4).

All MIIM AC timing requirements are specified relative to the input low and input high threshold levels. The levels are dependent on the MIIM interface supply mode.

Each MIIM interface has a separate supply pin, allowing operation in either 2.5 V or 3.3 V. mode.

The following illustration shows the MIIM waveforms and required measurement points for the signals.

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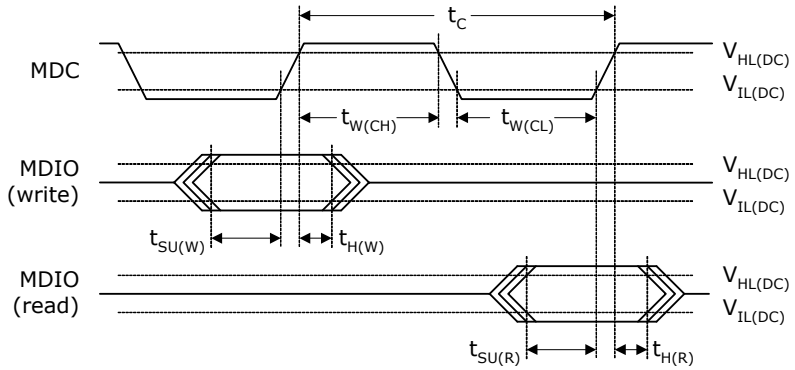
Figure 63. MIIM Timing Diagram



The setup time of MDIO relative to the rising edge of MDC is defined as the length of time between when the MDIO exits and remains out of the switching region and when MDC enters the switching region. The hold time of MDIO relative to the rising edge of MDC is defined as the length of time between when MDC exits the switching region and when MDIO enters the switching region.

All MIIM signals comply with the specifications in the following table. The MDIO signal requirements are requested at the pin of the device.

Table 280. MIIM Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
MDC frequency(1)	f	0.488	20.83	MHz	
MDC cycle time(2)	t_C	48	2048	ns	
MDC time high	$t_{W(CH)}$	20		ns	C_L = 50 pF
MDC time low	$t_{W(CL)}$	20		ns	C_L = 50 pF
MDIO setup time to MDC on write	$t_{SU(W)}$	15		ns	C_L = 50 pF
MDIO hold time from MDC on write	$t_{H(W)}$	15		ns	C_L = 50 pF
MDIO setup time to MDC on read	$t_{SU(R)}$	25		ns	C_L = 50 pF on MDC
MDIO hold time from MDC on read	$t_{H(R)}$	0		ns	C_L = 50 pF

1. For the maximum value, the device supports an MDC clock speed of up to 20 MHz for faster communication with the PHYs. If the standard frequency of 2.5 MHz is used, the MIIM interface is designed to meet or exceed the IEEE Std 802.3 requirements of the minimum MDC high and low times of 160 ns and an MDC cycle time of minimum 400 ns, which is not possible at faster speeds.
2. Calculated as $t_C = 1/f$.

7.2.12 Serial Interface (SI) Master Mode

All serial interface (SI) timing requirements for master mode are specified relative to the input low and input high threshold levels. The following illustration shows the timing parameters and measurement points.

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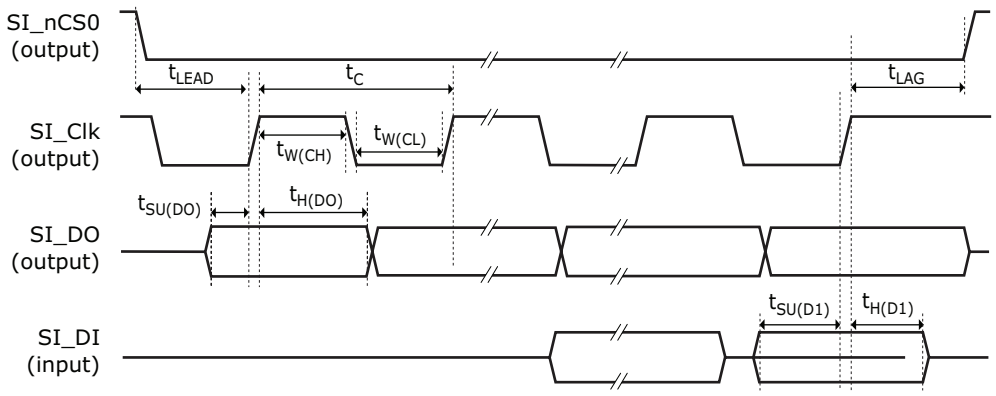
Figure 64. SI Timing Diagram for Master Mode



All SI signals comply with the specifications shown in the following table. The SI input timing requirements are requested at the pins of the device.

Table 281. SI Timing Specifications for Master Mode

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Clock frequency	f		25(1)	MHz	
Clock cycle time	t_C	40		ns	
Clock time high	$t_{W(CH)}$	16		ns	
Clock time low	$t_{W(CL)}$	16		ns	
Clock rise time and fall time	t_R, t_F		10	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.
DO setup time to clock	$t_{SU(DO)}$	5		ns	
DO hold time from clock	$t_{H(DO)}$	5		ns	
Enable active before first clock	t_{LEAD}	10		ns	
Enable inactive after clock	t_{LAG}	5		ns	
DI setup time to clock	$t_{SU(DI)}$	4		ns	
DI hold time from clock	$t_{H(DI)}$	4		ns	

1. Frequency is programmable. The startup frequency is 4 MHz.

7.2.13 Serial Interface (SI) for Slave Mode

All serial interface (SI) slave mode timing requirements are specified relative to the input low and input high threshold levels. The following illustrations show the timing parameters and measurement points for SI input and output data.

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Figure 65. SI Input Data Timing Diagram for Slave Mode

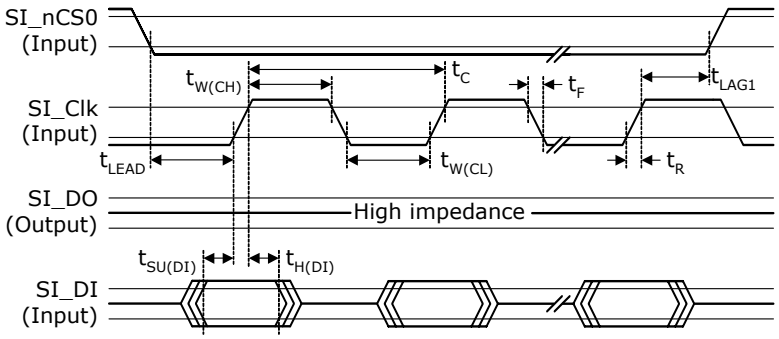
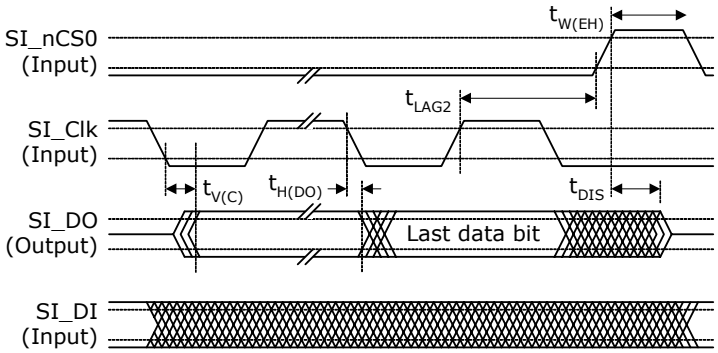


Figure 66. SI Output Data Timing Diagram for Slave Mode



All SI signals comply with the specifications shown in the following table. The SI input timing requirements are requested at the pins of the device.

Table 282. SI Timing Specifications for Slave Mode

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Clock frequency	f		25	MHz	
Clock cycle time	t_C	40		ns	
Clock time high	$t_{W(CH)}$	16		ns	
Clock time low	$t_{W(CL)}$	16		ns	
Clock rise time and fall time	t_R, t_F		10	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.
DI setup time to clock	$t_{SU(DI)}$	4		ns	
DI hold time from clock	$t_{H(DI)}$	4		ns	
Enable active before first clock	t_{LEAD}	10		ns	
Enable inactive after clock (input cycle)(1)	t_{LAG1}	25		ns	
Enable inactive after clock (output cycle)	t_{LAG2}	See note(2)		ns	
Enable inactive width	$t_{W(EH)}$	20		ns	
DO valid after clock	$t_{V(C)}$		12		C_L = 30 pF.

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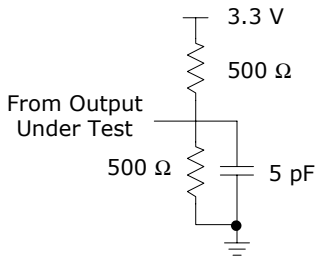
Table 282. SI Timing Specifications for Slave Mode *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
DO hold time from clock	$t_{H(DO)}$	0		ns	C_L = 0 pF.
DO disable time(3)	t_{DIS}		15	ns	See Figure 67, page 221.

1. t_{LAG1} is defined only for write operations to the device, not for read operations.
2. The last rising edge on the clock is necessary for the external master to read in the data. The lag time depends on the necessary hold time on the external master data input.
3. Pin begins to float when a 300 mV change from the loaded V_{OH} or V_{OL} level occurs.

Figure 67. SI_DO Disable Test Circuit



7.2.14 Parallel Interface (PI) Master Mode

The AC timing specifications in this section refer to the VCore-III CPU's external RAM/ROM interface. The timing is programmable and shown here as defined by default register values.

For information about V-Core-III functionality, see "VCore-III System and CPU Interfaces," page 108.

VCore-III CPU External PI Read Access

The VCore-III CPU timing parameters and required measurement points for external PI read access are defined in the following illustration. All VCore-II CPU signals for external PI read accesses comply with the specifications in the table following the illustration.

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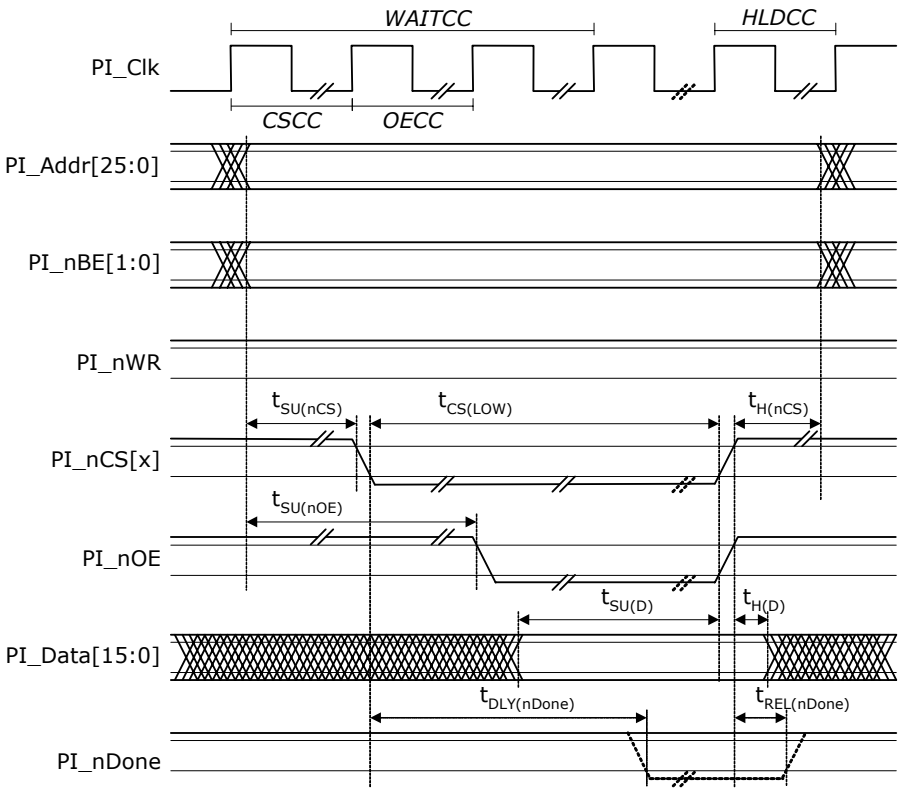
Figure 68. VCore-III CPU External PI Read Access Timing Diagram



The timing related to VCore-III external PI access is programmable. The programmable delays adjust timing in steps of the PI_Clk period. The PI_Clk period is determined by the dividers in registers CLOCK and PI_MST_CFG. The default settings correspond to a PI_Clk period of 297.6 ns. The condition used for these specifications corresponds to a PI_Clk period of 22.4 ns. Additionally, the default delay settings are used for WAITCC(1), CSCC(1), OECC(0) and HLDCC(0) as defined by PI_MST_CTRL registers.

Table 283. VCore-III CPU External PI Read Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Address/control setup time to chip select(1)	$t_{SU(nCS)}$	18		ns	C_L = 30 pF
Address/control hold time from chip select(2)	$t_{H(nCS)}$	–4		ns	C_L = 30 pF
Address/control setup time to output enable(3)	$t_{SU(nOE)}$	18		ns	C_L = 30 pF
Address/control hold time from output enable(4)	$t_{H(nOE)}$	–4		ns	C_L = 30 pF
Chip select low(5)	$t_{CS(low)}$	18	23	ns	C_L = 30 pF
Data setup time to chip select high	$t_{SU(D)}$	15		ns	C_L = 30 pF
Data hold time from chip select high	$t_{h(D)}$	0		ns	C_L = 30 pF
PI_nDone delay from chip select low(6)	$t_{DLY(nDone)}$	TBD	TBD	ns	C_L = 30 pF

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Table 283. VCore-III CPU External PI Read Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
PI_nDone release after chip select high(7)	$t_{REL(nDone)}$			ns	C_L = 30 pF

1. The minimum setup time of PI_Addr[25:0]/PI_nBE[1:0]/PI_nWR to PI_nCS[x] low may be expressed as WAITCC × 22.4 ns – 4 ns = 18.4 ns.
2. The minimum hold time of PI_Addr[25:0]/PI_nBE[1:0]/PI_nWR from PI_nCS[x] high may be expressed as HLDCC × 22.4 ns – 4 ns = –4 ns.
3. The minimum setup time of PI_Addr[25:0]/PI_nBE[1:0]/PI_nWR to PI_nOE low may be expressed as (WAITCC + OECC) × 22.4 ns – 4 ns = 18.4 ns.
4. The minimum hold time of PI_Addr[25:0]/PI_nBE[1:0]/PI_nWR from PI_nOE high may be expressed as HLDCC × 22.4 ns – 4 ns = –4 ns.
5. The maximum PI_nCS[x] low time may expressed as (WAITCC + 1 – CSCC) × 22.4 ns = 22.4 ns. The minimum is maximum 4 ns less than the maximum.
6. The interface may be operated in a device-paced mode according to the PI_MST_CTRL registers. This allows slow devices to delay the access cycle termination beyond the WAITCC setting. A timeout may be specified in the PI_MST_CTRL registers to terminate access cycles from non-responsive external devices.
7. In device-paced mode, PI_nDone must be released after PI_nCS[x] is observed high and before the next access cycle is started. Slow devices may require HLDCC to be adjusted accordingly.

VCore-III CPU External PI Write Access

The VCore-III CPU timing parameters and required measurement points for external PI write access are defined in the following illustration. All VCore-III CPU signals for the external PI write access comply with the specifications in the following table following the illustration.

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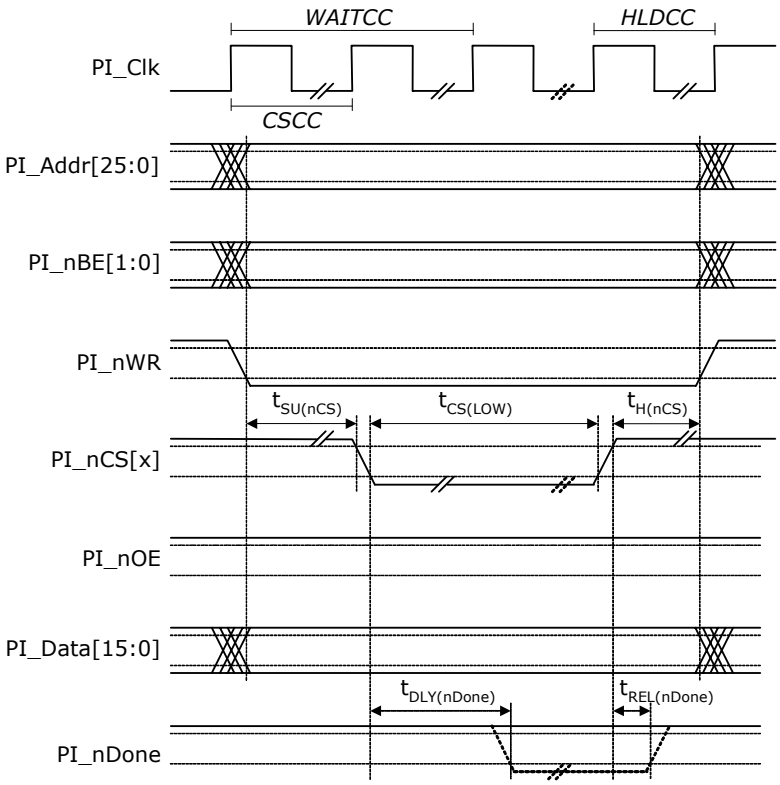
Figure 69. VCore-III CPU ROM/Flash Read Timing Diagram



The timing related to VCore-III external PI access is programmable. The programmable delays adjust timing in steps of the PI_Clk period. The PI_Clk period is determined by the dividers in registers CLOCK and PI_MST_CFG. The default settings correspond to a PI_Clk period of 297.6 ns. The condition used for these specifications corresponds to a PI_Clk period of 22.4 ns. Additionally, the default delay settings are used for WAITCC(1), CSCC(1), OECC(0) and HLDCC(0) as defined by PI_MST_CTRL registers.

Table 284. VCore-III CPU External PI Write Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Address/control setup time to chip select(1)	$t_{SU(nCS)}$	18		ns	C_L = 30 pF
Address/control hold time from chip select(2)	$t_{H(nCS)}$	–4		ns	C_L = 30 pF
Chip select low(3)	$t_{CS(low)}$	18	23	ns	C_L = 30 pF
Data setup time to chip select high	$t_{SU(D)}$	15		ns	C_L = 30 pF
PI_nDone delay from chip select low(4)	$t_{DLY(nDone)}$	TBD	TBD	ns	C_L = 30 pF
PI_nDone release after chip select high(5)	$t_{REL(nDone)}$	TBD	TBD	ns	C_L = 30 pF

1. The minimum setup time of PI_Addr[25:0]/PI_nBE[1:0]/PI_nWR to PI_nCS[x] low may be expressed as WAITCC × 22.4 ns – 4 ns = 18.4 ns.
2. The minimum hold time of PI_Addr[25:0]/PI_nBE[1:0]/PI_nWR from PI_nCS[x] high may be expressed as HLDCC × 22.4 ns – 4 ns = –4 ns.

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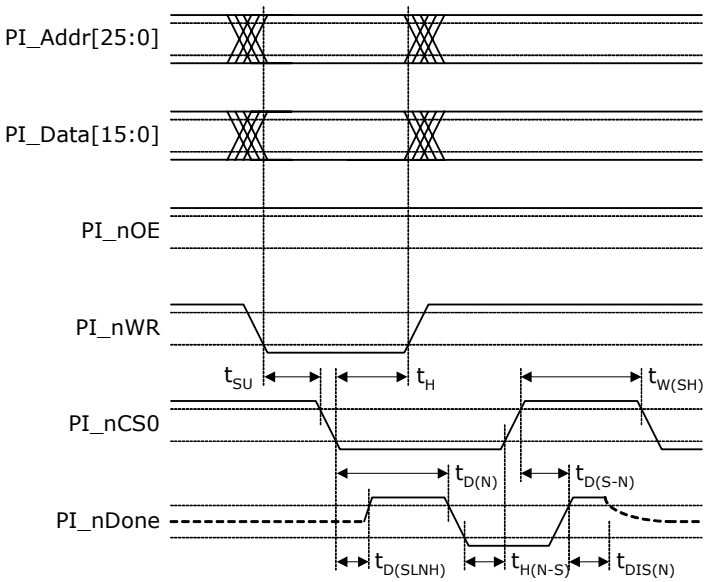
3. The maximum PI_nCS[x] low time may expressed as (WAITCC + 1 – CSCC) × 22.4 ns = 22.4 ns. The minimum is maximum 4 ns less than the maximum.
4. The interface may be operated in a device-paced mode according to the PI_MST_CTRL registers. This allows slow devices to delay the access cycle termination beyond the WAITCC setting. A timeout may be specified in the PI_MST_CTRL registers to terminate access cycles from non-responsive external devices.
5. In device-paced mode, PI_nDone must be released after PI_nCS[x] is observed high and before the next access cycle is started. Slow devices may require HLDCC to be adjusted accordingly.

7.2.15 Parallel Interface (PI) Slave Mode

The AC timing specifications provided in this section apply when an external CPU accesses the parallel CPU interface (slave mode operation).

All PI timing specifications are relative to the input low and input high threshold levels. The following two illustrations show the PI timing parameters and required measurement points.

Figure 70. PI Slave Write Cycle Timing Diagram



PI_nDone's polarity is programmable, shown here as active low.

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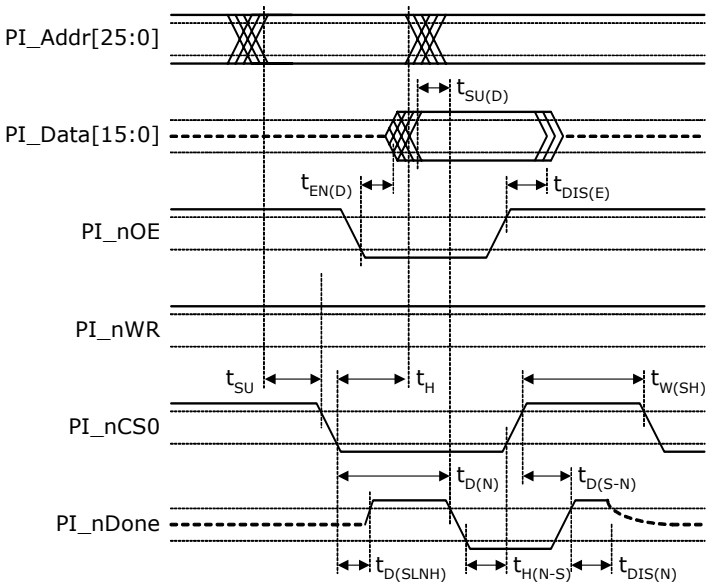
Figure 71. PI Slave Read Cycle Timing Diagram



PI_nDone's polarity is programmable, shown here as active low.

All PI signals comply with the timing parameters specified in the following table. The PI receive signal requirements are requested at the pin of the device.

Table 285. PI Slave Mode Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
PI_ADDR, PI_DATA, and PI_nWR setup to PI_nCS falling(1)	t_{SU}	–4		ns	Data only on write.
PI_ADDR, PI_DATA, and PI_nWR hold from nCS low(1)	t_{H}	25		ns	Data only on write.
Delay from PI_nCS low toPI_nDone rising(2)	$t_{D(SLNH)}$		10	ns	C_L = 30 pF.
Delay from PI_nCS low to PI_nDone falling(2)	$t_{D(N)}$		55	ns	C_L = 30 pF.
PI_nCS hold from PI_nDone falling(1), (2), (3)	$t_{H(N-S)}$	0		ns	
Delay from PI_nCS high to PI_nDone high(2)	$t_{D(S-N)}$		10	ns	C_L = 30 pF.
PI_nDone disable time from PI_nDone pulled inactive(2), (4)	$t_{DIS(N)}$		12	ns	See Figure 72, page 227.
Width of nCS high	$t_{W(SH)}$	10		ns	
PI_nOE and PI_nCS low to data enabled(1), (5)	$t_{EN(D)}$		15	ns	C_L = 30 pF.
Data setup time to PI_nDone falling on read(2)	$t_{SU(D)}$	0		ns	C_L = 30 pF.
Data disable time from either PI_nCS high or PI_nOE high(4), (5)	$t_{DIS(E)}$		15	ns	See Figure 72, page 227.

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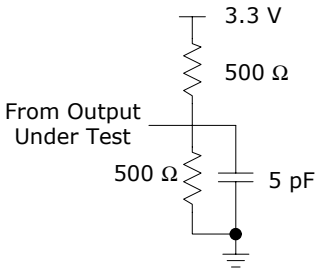
1. Before input data or conditions are sampled, an initial delay can be added in steps of 8 ns from 0 ns to 120 ns. The default delay is 104 ns to ensure operation with slow CPUs. Timing values in this table are shown with 0 ns delay.
2. PI_nDone polarity is programmable; it is shown as active low in the timing diagrams.
3. When using extended bus cycles, the response time can be up to 470 ns.
4. Pin begins to float when a 300 mV change from the loaded V_{OH}/V_{OL} level occurs.
5. Internal data output enable requires both nCS and nOE active. A time of 15 ns is valid only if PI_WAIT in the PI_CFG register (<<cross-ref to PI_CFG:PI_WAIT). If set to a value other than 0×00, the value shown for $t_{EN(D)}$ changes.

Figure 72. Signal Disable Test Circuit

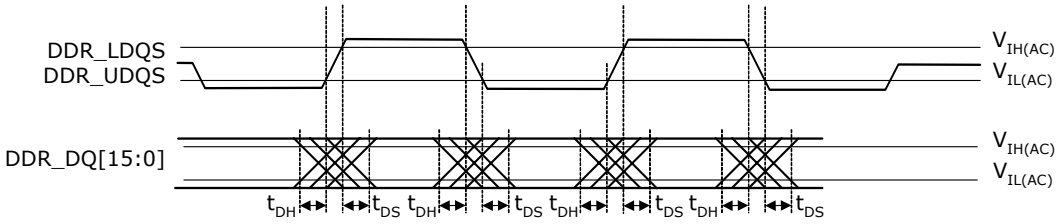


7.2.16 DDR2 SDRAM Signal

This section provides the AC characteristics for the DDR2 SDRAM interface.

The following illustration shows the DDR2 SDRAM input timing diagram.

Figure 73. DDR2 SDRAM Input Timing Diagram



The following table lists the AC specifications for the DDR2 SDRAM input signals.

Table 286. DDR2 SDRAM Input Signal AC Characteristics

Parameter	Symbol	Minimum	Maximum	Unit
Input voltage high	$V_{IH(AC)}$	DDR_V_{REF} + 0.20	V_{DD_IODDR} + 0.3	V
Input voltage low	$V_{IL(AC)}$	–0.3	DDR_V_{REF} – 0.20	V
Differential input voltage	$V_{ID(AC)}$	0.5	V_{DD_IODDR}	V
Differential crosspoint voltage	$V_{IX(AC)}$	0.5 × V_{DD_IODDR} – 0.175	0.5 × V_{DD_IODDR} + 0.175	V
DDR_DQ[7:0]/DDR_LDM input(1) setup time relative to DDR_LDQS	t_{DS}		TBD	ps

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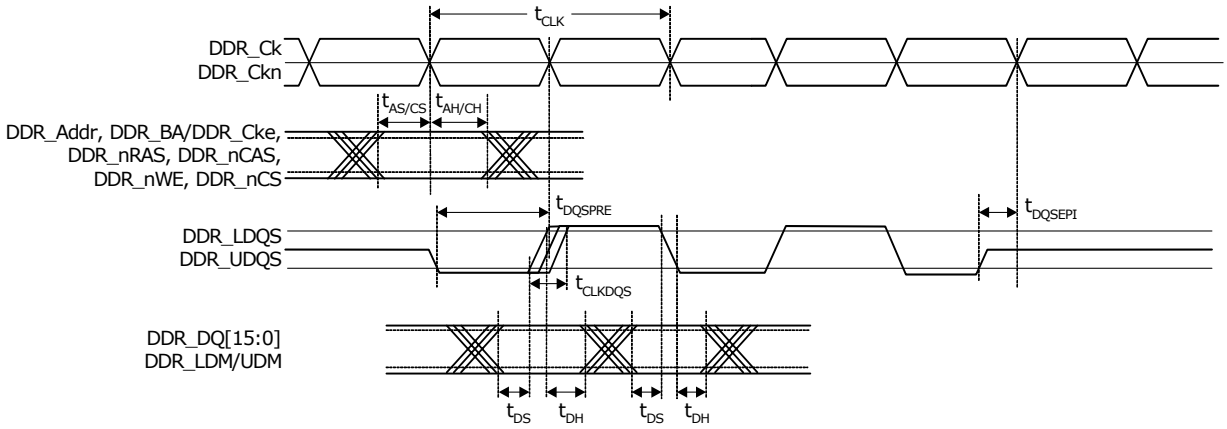
Table 286. DDR2 SDRAM Input Signal AC Characteristics *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit
DDR_DQ[15:8]/DDR_UDM input[1] setup time relative to DDR_UDQS	t_{DS}		TBD	ps
DDR_DQ[7:0]/DDR_LDM input hold time relative to DDR_LDQS[1]	t_{DH}		TBD	ps
DDR_DQ[15:8]/DDR_UDM input hold time relative to DDR_UDQS[1]	t_{DH}		TBD	ps

1. These requirements are dependent on the operation frequency of the DDR SDRAM interface. Stated limits are for DDR2-800.

The following illustration shows the timing diagram for the DDR2 SDRAM outputs.

Figure 74. DDR2 SDRAM Output Timing Diagram



The following table lists the AC characteristics for the DDR2 SDRAM output signals.

Table 287. DDR2 SDRAM Output Signal AC Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
DDR_Ck cycle time 200 MHz (DDR400)[1]	t_{CLK}		5.00		ns
DDR_Ck/Ckn duty cycle		48		52	%
DDR_A, DDR_BA, DDR_Cke, DDR_nRAS, DDR_nCAS, and DDR_nWE output setup time relative to DDR_Ck/Ckn	t_{AS}	2000			ps
DDR_A, DDR_BA, DDR_Cke, DDR_nRAS, DDR_nCAS, and DDR_nWE output hold time relative to DDR_Ck/Ckn	t_{AH}	2000			ps
DDR_Ck/Ckn to DDR_DQS skew	t_{CLKDQS}	–600		600	ps
DDR_DQ[7:0]/DDR_LDM output setup time with relative to DDR_LDQS	t_{DS}	700			ps
DDR_DQ[15:8]/DDR_UDM output setup time with relative to DDR_UDQS	t_{DS}	700			ps
DDR_DQ[7:0]/DDR_LDM output hold time relative to DDR_DQS	t_{DH}	700			ps

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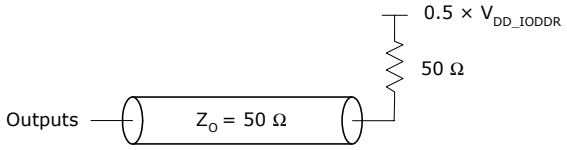
Table 287. DDR2 SDRAM Output Signal AC Characteristics *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit
DDR_DQ[15:8]/DDR_LDM output hold time relative to DDR_LDQS	t_{DH}	700			ps
DDR_DQS preamble start	t_{DQSPRE}	$0.5 \times t_{CLK} - 600$		$-0.5 \times t_{CLK} + 600$	ps
DDR_DQS epilogue end	t_{DQSEPI}	TBD		TBD	ps

1. Timing reference is DDR_Ck/DDR_Ckn crossing ±0.1 V.

The following illustration shows the test load circuit for the DDR2 outputs.

Figure 75. Test Load Circuit for DDR2 Outputs

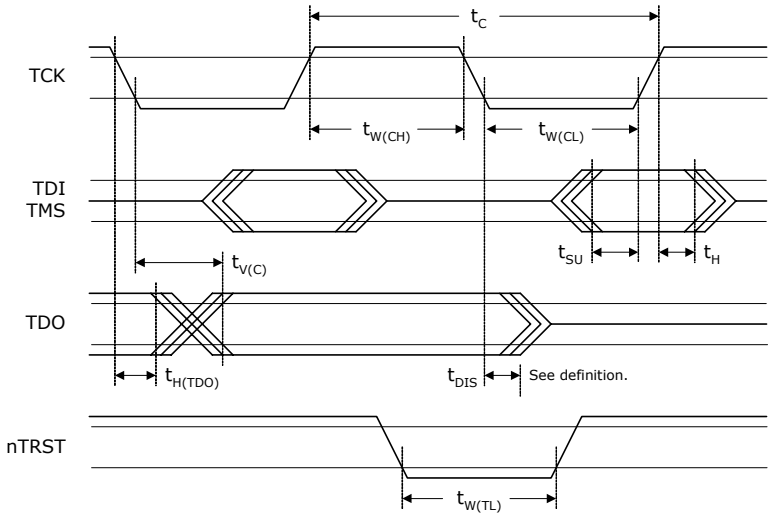


7.2.17 JTAG Interface

All AC specifications for the JTAG interface meet or exceed the requirements of IEEE Std 1149.1-2001.

The following illustration shows the JTAG transmit and receive waveforms and required measurement points for the different signals.

Figure 76. JTAG Interface Timing Diagram



All JTAG signals comply with the specifications in the following table. The JTAG receive signal requirements are requested at the pin of the device.

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The JTAG_nTRST signal is asynchronous to the clock and does not have a setup or hold time requirement.

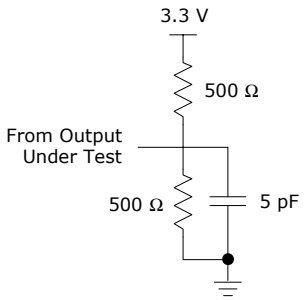
Table 288. JTAG Interface AC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TCK frequency	f		10	MHz	
TCK cycle time	t_C	100		ns	
TCK high time	$t_{W(CH)}$	40		ns	
TCK low time	$t_{W(CL)}$	40		ns	
Setup time to TCK rising	t_{SU}	10		ns	
Hold time from TCK rising	t_H	10		ns	
TDO valid after TCK falling	$t_{V(C)}$		28	ns	C_L = 10 pF
TDO hold time from TCK falling	$t_{H(TDO)}$	0		ns	C_L = 0 pF
TDO disable time(1)	t_{DIS}		30	ns	See Figure 77, page 230.
nTRST time low	$t_{W(TL)}$	30		ns	

1. The pin begins to float when a 300 mV change from the actual V_{OH}/V_{OL} level occurs.

The following illustration shows the test circuit for the TDO disable time.

Figure 77. Test Circuit for TDO Disable Time



7.2.18 Status Channel Interface

This section provides the AC specifications for the Status Channel interface.

The following I/O signals comply with the specifications provided in the following table.

STATA_IB_SCLK	STATB_IB_SCLK
STATA_IB_STAT0	STATB_IB_STAT0
STATA_IB_STAT1	STATB_IB_STAT1
STATA_OB_SCLK	STATB_OB_SCLK
STATA_OB_STAT0	STATB_OB_STAT0
STATA_OB_STAT1	STATB_OB_STAT1

The following illustration shows the timing diagram for the Status Channel interface.

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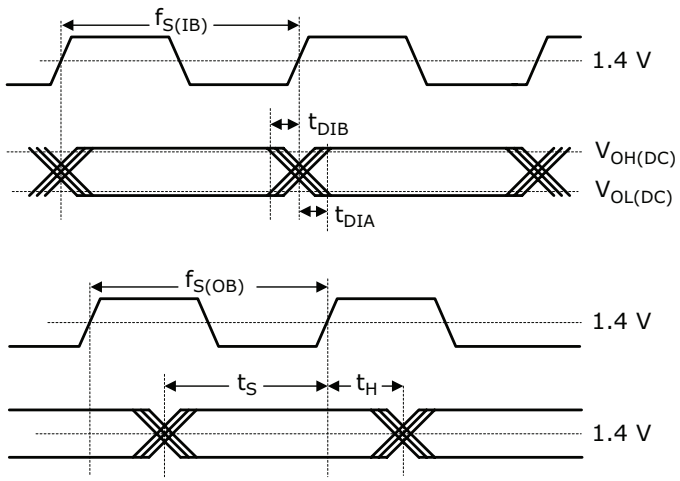
Figure 78. Status Channel Timing Diagram



The following table lists the timing specifications for the Status Channel interface.

Table 289. Status Channel Interface Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Outbound status clock frequency STAT[A:B]_OB_SCLK	$f_{S(OB)}$		125	MHz	
Outbound status clock duty cycle STAT[A:B]_OB_SCLK	$T_{S(OB)}$	40	60	%	
Inbound status clock frequency STAT[A:B]_IB_SCLK	$f_{S(IB)}$		125	MHz	
Inbound status clock duty cycle STAT[A:B]_IB_SCLK	$f_{S(IB)}$	45	55	MHz	25 pF, 500 Ω load
STAT[A:B]_IB_STAT[1:0] invalid window relative to STAT[A:B]_IB_SCLK edge	t_{DIB}	2.5		ns	25 pF, 500 Ω load
STAT[A:B]_IB_STAT[1:0] invalid window relative to STAT[A:B]_IB_SCLK edge	t_{DIB}	1		ns	25 pF, 500 Ω load
STAT[A:B]_OB_STAT[1:0] setup time to STAT[A:B]_OB_SCLK	t_S	2		ns	
STAT[A:B]_OB_STAT[1:0] hold time to STAT[A:B]_OB_SCLK	t_H	0.5		ns	

7.2.19 Serial LED Output Timing

The specifications for the serial LED output timing are shown in the following illustration and table. The serial LED output signals are GPIO4_LED_CLK, and GPIO5_LED_DO.

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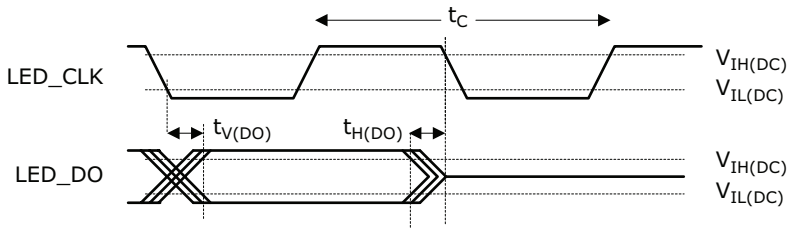
Figure 79. Serial LED Output Timing Diagram



The following table lists the timing specifications for the serial LED outputs.

Table 290. Serial LED Output Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit
LED_CLK frequency(1)	f		25	MHz
LED_CLK clock duty cycle	t_C	40	60	%
LED_DO valid after clock falling	$t_{V(DO)}$		TBD	ns
LED_DO hold time from clock falling	$t_{H(DO)}$		TBD	ns

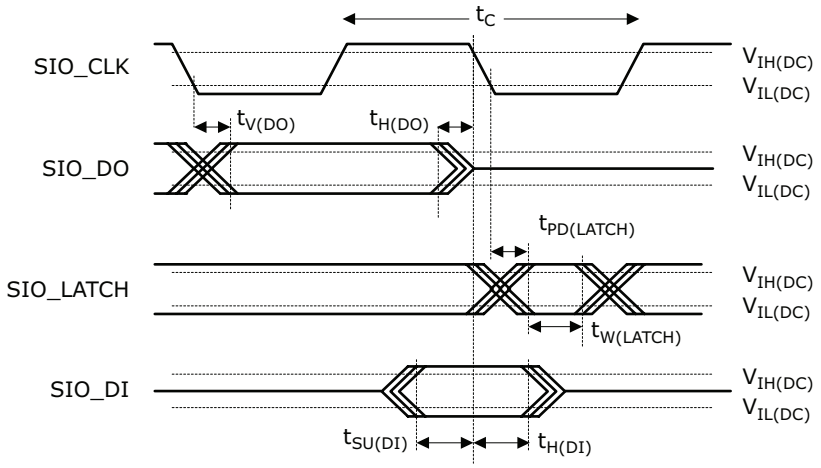
1. The SIO clock frequency is programmable.

7.2.20 Serial Inputs/Outputs

This section provides the AC characteristics for the serial I/O signals: GPIO0_SIO_CLK, GPIO1_SIO_DO, GPIO2_SIO_DI, and GPIO3_SIO_Latch.

The serial I/O timing diagram is shown in the following illustration.

Figure 80. Serial I/O Timing Diagram



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The following table lists the serial I/O timing specifications.

Table 291. Serial I/O Timing Specifications

Parameter	Symbol	Minimum	Maximum	Unit
Clock frequency(1)	f		25	MHz
SIO_CLK clock duty cycle	t_C	40	60	%
SIO_DO valid after clock falling	$t_{V(DO)}$		TBD	ns
SIO_DO hold time from clock falling	$t_{H(DO)}$		TBD	ns
SIO_Latch propagation delay from clock falling	$t_{PD(LTACH)}$		TBD	ns
SIO_Latch width	$t_{W(LATCH)}$	4		ns
SIO_DI setup time to clock	$t_{SU(DI)}$	4		ns
SIO_DI hold time from clock	$t_{H(DI)}$	TBD		ns

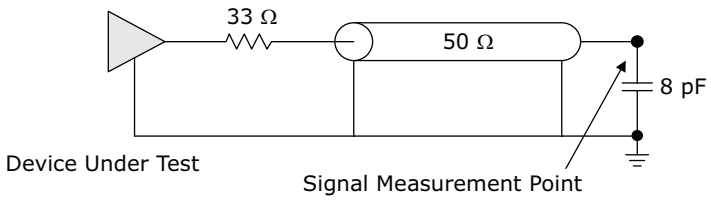
1. The SIO clock frequency is programmable.

7.2.21 Recovered Clock Outputs

This section provides the AC characteristics for the recovered clock output signals: RCVRD_CLK0 and RCVRD_CLK1.

The following illustration shows the test circuit for the recovered clock output signals.

Figure 81. Test Circuit for Recovered Clock Output Signals



The following table lists the AC specifications for the recovered clock outputs.

Table 292. Recovered Clock Output AC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
RCVRD_CLK[1:0] clock frequency	f		125	MHz	
Clock duty cycle	t_C	40	60	%	Measured at 50% threshold.
RCVRD_CLK[1:0] rise time and fall time	t_R, t_F		1.5	ns	
Squelching delay from SGMII signal to RCVRD_CLK[1:0]			TBD	ns	Squelch enabled.
Squelching delay from XAUI signal to RCVRD_CLK[1:0]			TBD	ns	Squelch enabled.
RCVRD_CLK[1:0] peak-to-peak jitter, bandwidth between TBD kHz and TBD MHz.(1)			TBD	ps	

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Table 292. Recovered Clock Output AC Specifications *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
RCVRD_CLK[1:0] peak-to-peak jitter, bandwidth between TBD kHz and TBD MHz.(1)			TBD	ps	

1. Maximum jitter on the recovered signal.

7.2.22 Two-Wire Serial Interface

This section provides the AC specifications for the two-wire serial interface signals GPIO14_TWI_SCL and GPIO15_TWI_SDA.

The two-wire serial interface signals are compatible with the Philps I2C-BUS specifications, except for the minimum rise time and fall time requirements for fast mode.

For the specifications listed in the following table, standard mode is defined as 100 kHz and fast mode is 400 kHz.

Table 293. Two-Wire Serial Interface AC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TWI_SCL clock frequency, standard mode	f		100	kHz	
TWI_SCL clock frequency, fast mode	f		400	kHz	
TWI_SCL low period, standard mode		4.7		µs	
TWI_SCL low period, fast mode		1.3		µs	
TWI_SCL high period, standard mode		4.0		µs	
TWI_SCL low period, fast mode		0.6		µs	
TWI_SCL and TWI_SDA rise time, standard mode			1000	ns	
TWI_SCL and TWI_SDA rise time, fast mode		1	300	ns	
TWI_SCL and TWI_SDA fall time, standard mode			300	ns	
TWI_SDA setup time to TWI_SCL fall, standard mode	$t_{SU(SDA)}$	250		ns	
TWI_SDA setup time to TWI_SCL fall, fast mode	$t_{SU(SDA)}$	100	300	ns	
TWI_SDA hold time to TWI_SCL fall, standard mode	$t_{H(SDA)}$	300	3450	ns	300 ns delay enabled in ICPU_CFG::TWI_CONFIG register.

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Table 293. Two-Wire Serial Interface AC Specifications *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TWI_SDA hold time to TWI_SCL fall, fast mode	$t_{H(SDA)}$	300	900	ns	300 ns delay enabled in ICPU_CFG::TWI_CONFIG register.
Pulse width of spike suppressed by input filter on TWI_SDA		0	50	ns	

7.2.23 IEEE 1588 Time Tick Outputs

This section provides the AC specifications for the IEEE 1588 time tick output signals GPIO8_TIME_TICK_0 and GPIO9_TIME_TICK_1.

Table 294. IEEE1588 Time Tick Output AC Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TIME_TICK[1:0] frequency(1)	f		25	MHz	
Clock duty cycle		TBD	TBD	%	Measured at 50% threshold.
TIME_TICK[1:0] rise time and fall time	t_R, T_F	1		ns	20% to 80% threshold.
TIME_TICK[1:0] peak-to-peak jitter, bandwidth between TBD kHz and TBD MHz			TBD	ps	
TIME_TICK[1:0] peak-to-peak jitter, bandwidth between TBD kHz and TBD MHz			TBD	ps	

1. Frequency is programmable.

7.3 Current and Power Consumption

This section provides the current and power consumption requirements for the VSC7462 device.

7.3.1 Current Consumption

The following table shows the absolute maximum operating current for the VSC7462 device over maximum traffic activity and worst-case process, temperature, and supply settings.

Table 295. Maximum Operating Current

Parameter	Symbol	Typical Voltage (V)	Maximum Current Consumption (A)
V_{DD} operating current	I_{DD}	1.0	TBD
V_{DD_A} operating current	I_{DD_A}	1.0	TBD
V_{DD_ref25} operating current	I_{DD_ref25}	2.5	TBD

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Table 295. Maximum Operating Current *(continued)*

Parameter	Symbol	Typical Voltage (V)	Maximum Current Consumption (A)
V_{DD_IOXAUI} operating current	I_{DD_IOXAUI}	1.0 or 1.2	TBD
$V_{DD_IOSGMII}$ operating current	$I_{DD_IOSGMII}$	1.0 or 1.2	TBD
V_{DD_IODDR} operating current(1)	I_{DD_IODDR}	1.8	TBD
V_{DD_IO33} operating current	I_{DD_IO33}	3.3	TBD
$V_{DD_IOSTATUS}$ operating current	$I_{DD_IOSTATUS}$	2.5 or 3.3	TBD
$V_{DD_IOMIIM0}$ operating current	$I_{DD_IOMIIM0}$	2.5 or 3.3	TBD
$V_{DD_IOMIIM1}$ operating current	$I_{DD_IOMIIM1}$	2.5 or 3.3	TBD

1. DDR2 on-die termination is disabled.

The following table shows the typical current consumption for the VSC7462 device over nominal supply settings at 25 °C case temperature and a full traffic load.

Table 296. Typical Operating Current

Parameter	Symbol	Typical Voltage (V)	Typical Current Consumption (A)
V_{DD} operating current	I_{DD}	1.0	TBD
V_{DD_A} operating current	I_{DD_A}	1.0	TBD
V_{DD_ref25} operating current	I_{DD_ref25}	2.5	TBD
V_{DD_IOXAUI} operating current	I_{DD_IOXAUI}	1.0 or 1.2	TBD
$V_{DD_IOSGMII}$ operating current	$I_{DD_IOSGMII}$	1.0 or 1.2	TBD
V_{DD_IODDR} operating current(1)	I_{DD_IODDR}	1.8	TBD
V_{DD_IO33} operating current	I_{DD_IO33}	3.3	TBD
$V_{DD_IOSTATUS}$ operating current	$I_{DD_IOSTATUS}$	2.5 or 3.3	TBD
$V_{DD_IOMIIM0}$ operating current	$I_{DD_IOMIIM0}$	2.5 or 3.3	TBD
$V_{DD_IOMIIM1}$ operating current	$I_{DD_IOMIIM1}$	2.5 or 3.3	TBD

1. DDR2 on-die termination is disabled.

7.3.2 Power Consumption

The following table shows the typical and maximum power consumption of the VSC7462 device, based on current consumption and with DDR2 on-die termination disabled. For more information about the current consumption, see Table 295, page 235 and Table 296, page 236.

Maximum power consumption values are over maximum temperature and all supplies at maximum voltages. Typical power consumption values are over nominal supplies and 25 °C case temperature.

Table 297. Power Consumption

Parameter	Value	Unit
Maximum power consumption, $V_{DD_IO_SGMII}$ and V_{DD_IOXAUI} = 1.0 V	TBD	W

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Table 297. Power Consumption *(continued)*

Parameter	Value	Unit
Maximum power consumption, $V_{DD_IO_SGMII}$ and V_{DD_IOXAUI} = 1.2 V	TBD	W
Typical power consumption, $V_{DD_IO_SGMII}$ and V_{DD_IOXAUI} = 1.0 V	TBD	W
Typical power consumption, $V_{DD_IO_SGMII}$ and V_{DD_IOXAUI} = 1.2 V	TBD	W

7.3.3 Power Supply Sequencing

During power on and off, V_{DD_A}, V_{DD_IOXAUI}, and $V_{DD_IOSGMII}$ must never be more than 300 mV below V_{DD}.

V_{DD_IOXAUI} and $V_{DD_IOSGMII}$ must be powered, even if the associated interface is not used. These power supplies must not remain at ground or left floating.

A maximum delay of 100 ms from V_{DD_IODDR} to V_{DD} is recommended. There is no requirement from V_{DD} to V_{DD_IODDR}.

There are no sequencing requirements for $V_{DD_IOSTATUS}$, $V_{DD_IOMIIM0}$, $V_{DD_IOMIIM1}$, and V_{DD_IO33}. These power supplies can remain at ground or left floating if not used.

The nReset and JTAG_nTRST inputs must be held low until all power supply voltages have reached their recommended operating condition values.

7.4 Operating Conditions

The following table shows the recommended operating conditions.

Table 298. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for core supply	V_{DD}	0.95	1.0	1.05	V
Power supply voltage for analog circuits	V_{DD_A}	0.95	1.0	1.05	V
Reference supply for SerDes and PLL	V_{DD_ref25}	2.375	2.5	2.625	V
Power supply voltage for XAUI interface	V_{DD_IOXAUI}	0.95	1.0	1.05	V
		1.14	1.2	1.26	V
Power supply voltage for SGMII interface	$V_{DD_IOSGMII}$	0.95	1.0	1.05	V
		1.14	1.2	1.26	V
Power supply voltage for DDR2 interface	V_{DD_IODDR}	1.71	1.8	1.89	V
Power supply voltage for PI and miscellaneous I/O	V_{DD_IO33}	3.13	3.3	3.47	V
Power supply voltage for status channel interface	$V_{DD_IOSTATUS}$	2.375	2.5	2.625	V
		3.13	3.3	3.47	

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Table 298. Recommended Operating Conditions *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for MIIM interface 0	$V_{DD_IOMIIM0}$	2.375	2.5	2.625	V
		3.13	3.3	3.47	V
Power supply voltage for MIIM interface 1	$V_{DD_IOMIIM1}$	2.375	2.5	2.625	V
		3.13	3.3	3.47	V
Operating temperature(1)	T	–40		125	°C

1. Lower limit of specification is ambient temperature, and upper limit is junction temperature.

7.5 Stress Ratings

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 299. Stress Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage for core supply	V_{DD}	–0.3	1.10	V
Power supply voltage for analog circuits	V_{DD_A}	–0.3	1.10	V
Reference supply for SerDes and PLL	V_{DD_ref25}	–0.3	2.75	V
Power supply voltage for XAUI interface	V_{DD_IOXAUI}	–0.3	1.32	V
Power supply voltage for SGMII interface	$V_{DD_IOSGMII}$	–0.3	1.32	V
Power supply voltage for DDR2 I/O buffers	V_{DD_IODDR}	–0.3	1.98	
Power supply voltage for PI and miscellaneous I/O	V_{DD_IO33}	–0.3	3.63	
Power supply voltage for status channel interface	$V_{DD_IOSTATUS}$	–0.3	3.63	
Power supply voltage for MIIM interface 0	$V_{DD_IOMIIM0}$	–0.3	3.63	
Power supply voltage for MIIM interface 1	$V_{DD_IOMIIM1}$	–0.3	3.63	
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–200	200	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	–2000	2000	V
Storage temperature	T_S	–40	125	°C

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

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8 Pin Descriptions

The section provides the pin diagram and descriptions.

The devices have 672 pins, which are described in this section.

8.1 Pin Diagram

The following illustration shows the pin diagram. For clarity, the devices are shown in two halves, the top left and the top right.

Figure 82. Pin Diagram, Top Left

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		PI_Addr22	PI_Data1	PI_Data3	PI_Data5	PI_Data7	PI_nOE	PI_nWR	GPIO20_PI_nCS2	GPIO0_SIO_CLK	GPIO4_LED_CLK	GPIO8_TIME_TICK_0	GPIO10_UART_RX
B	PI_Addr21	PI_Addr23	PI_Addr24	PI_Data0	PI_Data2	PI_Data4	PI_Data6	PI_nCS0	GPIO21_PI_nCS3	GPIO1_SIO_DO	GPIO5_LED_DO	GPIO9_TIME_TICK_1	GPIO11_UART_TX
C	PI_Addr19	PI_Addr20	PI_Addr25	PI_Data9	PI_Data11	PI_Data13	PI_Data15	PI_nDone	GPIO22_PI_nBE0	GPIO2_SIO_DI	GPIO6_INT0	GPIO12_UART_CTS	VSS_108
D	PI_Addr16	PI_Addr17	PI_Addr18	PI_Data8	PI_Data10	PI_Data12	PI_Data14	GPIO19_PI_nCS1	GPIO23_PI_nBE1	GPIO3_SIO_Latch	GPIO7_INT1	GPIO13_UART_RTS	VSS_111
E	PI_Addr12	PI_Addr13	PI_Addr14	PI_Addr15	VSS_168	VDD_IO33_9	VSS_21	VDD_IO33_10	VDD_IO33_4	VSS_18	VDD_IO33_13	VDD_IO33_14	VSS_157
F	PI_Addr8	PI_Addr9	PI_Addr10	PI_Addr11	VSS_121	VSS_146	VSS_22	VDD_IO33_11	VDD_IO33_5	VSS_19	VDD_IO33_12	VDD_IO33_3	VSS_20
G	PI_Addr4	PI_Addr5	PI_Addr6	PI_Addr7	VDD_IO33_0	VDD_IO33_2	VSS_107	VDD_30	VDD_0	VSS_100	VDD_14	VDD_16	VSS_5
H	PI_Addr0	PI_Addr1	PI_Addr2	PI_Addr3	VDD_IO33_1	VDD_IO33_8	VSS_158	VDD_31	VDD_1	VSS_104	VDD_15	VDD_17	VSS_52
J	DDR_LDQS	DDR_LDQSn	DDR_LDM	DDR_DQ6	VSS_23	VSS_72	VSS_77	VSS_8	VSS_7	VSS_99	VSS_102	VSS_70	VSS_48
K	DDR_DQ0	DDR_DQ7	DDR_DQ3	DDR_DQ1	VDD_IODDR_12	VDD_IODDR_11	VSS_177	VDD_2	VDD_4	VSS_95	VDD_18	VDD_20	VSS_69
L	DDR_DQ5	DDR_DQ2	DDR_nRAS	DDR_DQ4	VDD_IODDR_13	VDD_IODDR_10	VSS_109	VDD_3	VDD_5	VSS_97	VDD_19	VDD_21	VSS_68
M	DDR_A0	DDR_ODT	DDR_A2	DDR_nCAS	VSS_24	VSS_26	VSS_160	VSS_6	VSS_9	VSS_92	VSS_11	VSS_12	VSS_67
N	DDR_A8	DDR_A4	DDR_nWE	DDR_A6	VSS_25	VSS_27	VSS_90	VSS_106	VSS_117	VSS_89	VSS_85	VSS_114	VSS_66
P	DDR_Ckn	DDR_Ck	DDR_A11	DDR_A13	VDD_IODDR_9	VDD_IODDR_8	VSS_161	VDD_6	VDD_8	VSS_86	VDD_22	VDD_24	VSS_65
R	DDR_A12	DDR_A7	DDR_A9	DDR_A5	VDD_IODDR_7	VDD_IODDR_6	VSS_110	VDD_7	VDD_9	VSS_96	VDD_23	VDD_25	VSS_64
T	DDR_A3	DDR_A10	DDR_A1	DDR_BA1	VSS_28	VSS_115	VSS_178	VSS_74	VSS_14	VSS_40	VSS_16	VSS_103	VSS_63
U	DDR_BA0	DDR_BA2	DDR_Cke	VSS_167	VDD_IODDR_5	VDD_IODDR_3	VSS_91	VDD_10	VDD_12	VSS_10	VDD_26	VDD_28	VSS_41
V	DDR_DQ12	DDR_DQ11	DDR_DQ10	DDR_DQ13	VDD_IODDR_4	VDD_IODDR_2	VSS_163	VDD_11	VDD_13	VSS_42	VDD_27	VDD_29	VSS_17
W	DDR_DQ9	DDR_DQ14	DDR_DQ8	DDR_DQ15	VSS_75	VSS_71	VSS_112	VDD_A_0	VDD_A_2	VSS_44	VDD_A_12	VDD_A_14	VSS_156
Y	DDR_REXt	DDR_UDM	DDR_UDQS	DDR_UDQSn	VDD_IODDR_1	VDD_IODDR_0	VSS_31	VDD_A_1	VDD_A_11	VSS_15	VDD_A_13	VDD_A_15	VSS_34
AA	Reserved_1	Reserved_2	Reserved_3	VSS_184	VSS_32	VSS_73	VSS_29	VDD_IOSGMII_0	VDD_IOSGMII_2	VSS_88	VDD_IOSGMII_4	VDD_IOSGMII_6	VSS_35
AB	MDIO0	DDR_Vref	SERDES_RExt_1	SERDES_RExt_0	VSS_76	VSS_33	VSS_30	VDD_IOSGMII_1	VDD_IOSGMII_3	VSS_43	VDD_IOSGMII_5	VDD_IOSGMII_7	VSS_36
AC	MDC0	VDD_IOMIIM0	Reserved_51	Reserved_57	Reserved_59	Reserved_65	Reserved_67	Reserved_73	Reserved_75	Reserved_81	Reserved_83	Reserved_89	Reserved_91
AD	SGMII_NPI_TxN	SGMII_NPI_TxP	Reserved_50	Reserved_56	Reserved_58	Reserved_64	Reserved_66	Reserved_72	Reserved_74	Reserved_80	Reserved_82	Reserved_88	Reserved_90
AE	SGMII_NPI_RxN	SGMII_NPI_RxP	Reserved_53	Reserved_55	Reserved_61	Reserved_63	Reserved_69	Reserved_71	Reserved_77	Reserved_79	Reserved_85	Reserved_87	Reserved_93
AF		Reserved_0	Reserved_52	Reserved_54	Reserved_60	Reserved_62	Reserved_68	Reserved_70	Reserved_76	Reserved_78	Reserved_84	Reserved_86	Reserved_92

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Figure 83. Pin Diagram, Top Right

14	15	16	17	18	19	20	21	22	23	24	25	26	
GPIO14_TWI_SCL	SI_Clk	SI_DI	VCore_ICE_nEn	ThermDA	nReset	MDIO1	STATB_OB_SCLK	STATB_IB_SCLK	STATA_OB_SCLK	STATA_OB_STAT0	STATA_IB_SCLK		A
GPIO15_TWI_SDA	SI_DO	SI_nCS0	Test_mode1	ThermDC	TestCfg2	MDC1	STATB_OB_STAT1	STATB_IB_STAT0	STATB_IB_STAT1	STATA_OB_STAT1	STATA_IB_STAT1	STATA_IB_STAT0	B
core_sense	GPIO17_SPI_nCS2	RefClk_Sel1	RefClk_Sel2	VCore_BE_en	TestCfg1	VCore_Cfg0	STATB_OB_STAT0	RCVRD_CLK0	RCVRD_CLK1	JTAG_TDI	JTAG_TDO	JTAG_TCK	C
VSS_84	GPIO18_SPI_nCS3	GPIO16_SPI_nCS1	RefClk_Sel0	TestCfg3	TestCfg0	VCore_Cfg1	VDD_IOSTATUS_1	JTAG_TMS	JTAG_nTRST	VSS_62	Reserved_39	Reserved_38	D
VSS_13	VDD_IO33_6	VDD_IO33_7	VSS_145	VSS_151	VSS_120	VDD_IOSTATUS_0	VDD_IOSTATUS_2	Reserved_41	Reserved_40	VSS_61	Reserved_36	Reserved_37	E
VSS_87	VDD_IO33_15	VDD_IO33_16	VSS_105	VSS_170	VSS_118	VDD_IOMIIM1	VDD_IOSTATUS_3	Reserved_35	Reserved_34	VSS_60	Reserved_31	Reserved_30	F
VSS_0	VDD_32	VDD_35	VSS_164	VDD_47	VDD_49	VDD_IOXAUI_4	VDD_IOXAUI_6	Reserved_33	Reserved_32	VSS_59	Reserved_28	Reserved_29	G
VSS_1	VDD_33	VDD_34	VSS_165	VDD_48	VDD_53	VDD_IOXAUI_3	VDD_IOXAUI_5	Reserved_27	Reserved_26	VSS_58	Reserved_23	Reserved_22	H
VSS_81	VSS_39	VSS_132	VSS_179	VSS_144	VSS_143	VSS_152	VSS_174	Reserved_25	Reserved_24	VSS_57	Reserved_20	Reserved_21	J
VSS_98	VDD_36	VDD_42	VSS_113	VDD_51	VDD_56	VDD_IOXAUI_10	VDD_IOXAUI_12	Reserved_19	Reserved_18	VSS_56	Reserved_15	Reserved_14	K
VSS_2	VDD_50	VDD_41	VSS_180	VDD_55	VDD_57	VDD_IOXAUI_9	VDD_IOXAUI_11	Reserved_17	Reserved_16	VSS_55	Reserved_12	Reserved_13	L
VSS_80	VSS_94	VSS_182	VSS_142	VSS_183	VSS_149	VSS_176	VSS_154	Reserved_11	Reserved_10	VSS_54	REFCLK_N	REFCLK_P	M
VSS_3	VSS_83	VSS_130	VSS_141	VSS_129	VSS_128	VSS_126	VSS_125	HS_TST_P	HS_TST_N	VSS_53	XAUI1_Rx3P	XAUI1_Rx3N	N
VSS_82	VDD_37	VDD_39	VSS_138	VDD_58	VDD_60	VDD_IOXAUI_7	VDD_IOXAUI_8	XAUI1_Tx3P	XAUI1_Tx3N	VSS_51	XAUI1_Rx2P	XAUI1_Rx2N	P
VSS_4	VDD_38	VDD_40	VSS_139	VDD_59	VDD_61	VDD_IOXAUI_2	VDD_IOXAUI_13	XAUI1_Tx2P	XAUI1_Tx2N	VSS_50	XAUI1_Rx1P	XAUI1_Rx1N	R
VSS_79	VSS_133	VSS_181	VSS_137	VSS_93	VSS_123	VSS_153	VSS_122	XAUI1_Tx1P	XAUI1_Tx1N	VSS_49	XAUI1_Rx0P	XAUI1_Rx0N	T
VSS_101	VDD_43	VDD_45	VSS_135	VDD_62	VDD_52	VDD_A_9	VDD_IOXAUI_1	XAUI1_Tx0P	XAUI1_Tx0N	VSS_47	XAUI0_Rx3P	XAUI0_Rx3N	U
VSS_78	VDD_44	VDD_46	VSS_136	VDD_63	VDD_54	VDD_A_10	VDD_IOXAUI_0	XAUI0_Tx3P	XAUI0_Tx3N	VSS_46	XAUI0_Rx2P	XAUI0_Rx2N	V
VSS_116	VDD_A_16	VDD_A_3	VSS_124	VDD_A_5	VDD_A_7	VDD_ref25_0	VSS_148	XAUI0_Tx2P	XAUI0_Tx2N	VSS_45	XAUI0_Rx1P	XAUI0_Rx1N	W
VSS_119	VDD_A_17	VDD_A_4	VSS_134	VDD_A_6	VDD_A_8	VDD_ref25_1	VSS_172	XAUI0_Tx1P	XAUI0_Tx1N	VSS_171	XAUI0_Rx0P	XAUI0_Rx0N	Y
VSS_37	VDD_IOSGMII_8	VDD_IOSGMII_10	VSS_131	VDD_IOSGMII_12	VDD_IOSGMII_14	VDD_ref25_2	VSS_147	XAUI0_Tx0P	XAUI0_Tx0N	VSS_155	VSS_140	VSS_175	AA
VSS_38	VDD_IOSGMII_9	VDD_IOSGMII_11	VSS_127	VDD_IOSGMII_13	VDD_IOSGMII_15	VSS_150	VSS_169	VSS_173	VSS_159	VSS_166	VSS_162	Reserved_97	AB
SGMII11_TxP	SGMII12_TxP	SGMII13_TxP	SGMII14_TxP	SGMII15_TxP	SGMII16_TxP	SGMII17_TxP	SGMII18_TxP	SGMII19_TxP	SGMII20_TxP	SGMII21_TxP	SGMII22_TxP	Reserved_96	AC
SGMII11_TxN	SGMII12_TxN	SGMII13_TxN	SGMII14_TxN	SGMII15_TxN	SGMII16_TxN	SGMII17_TxN	SGMII18_TxN	SGMII19_TxN	SGMII20_TxN	SGMII21_TxN	SGMII22_TxN	Reserved_95	AD
SGMII11_RxP	SGMII12_RxP	SGMII13_RxP	SGMII14_RxP	SGMII15_RxP	SGMII16_RxP	SGMII17_RxP	SGMII18_RxP	SGMII19_RxP	SGMII20_RxP	SGMII21_RxP	SGMII22_RxP	Reserved_94	AE
SGMII11_RxN	SGMII12_RxN	SGMII13_RxN	SGMII14_RxN	SGMII15_RxN	SGMII16_RxN	SGMII17_RxN	SGMII18_RxN	SGMII19_RxN	SGMII20_RxN	SGMII21_RxN	SGMII22_RxN		AF

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8.2 Pins by Function

This section contains the functional pin descriptions.

8.2.1 Clock Circuits

The following table lists the pins associated with the system clock interface.

Table 300. System Clock Interface Pins

Name	Type	Description
RefClk_Sel[2:0]	I, PD	Reference clock frequency selection. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to V_{DD_IO33}. Coding: 000: 125 MHz (default). 001: 156.25 MHz. 010: Reserved. 011: Reserved. 100: 25 MHz. 101: Reserved. 110: Reserved. 111: Reserved.
REFCLK P REFCLK N	I, Diff	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to V_{DD_A}. Required applied frequency depends on RefClk_Sel[2:0] input state. See description for RefClk_Sel[2:0] pins.
RCVRD_CLK[1:0]	O	The output clock frequency can be between 25 MHz and 125 MHz, based on the selected active recovered media programmed for this pin and the divider configuration. For more information about supported output clock frequencies, see Table 8, page 50. These pins are not active when nReset is asserted. Clock outputs can be enabled or disabled from registers. When disabled, the pin is held low.
IEEE_1588_time_tick_[1:0](1)	I/O, PU, 3V	These two pins can be programmed independently to either output or input. The pins can be used as either an input pulse for synchronization of the internal 1588 master timer or as programmable divided-frequency outputs from the internal 1588 master timer. The programmable divided frequency is between 25 MHz and 1 pulse per second. The programmed output signals duty cycle depends on the programmed divider factor.

1. Available as an alternate function on the GPIO8 and GPIO9 pins.

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8.2.2 DDR2 SDRAM Interface

The following table lists the pins associated with the DDR2 SDRAM interface.

Table 301. DDR2 SDRAM Pins

Name	Type	Description
DDR_Ck DDR_Ckn	0, Diff	SDRAM differential clock. Differential clock to external SDRAM. DDR_Ck is the true part of the differential signal. DDR_nCk is the complement part.
DDR_Cke	O	SDRAM clock enable. 0: Disables clock in external SDRAM. 1: Enables clock in external SDRAM.
DDR_nRAS DDR_nCAS DDR_nWE	O	SDRAM command outputs. DDR_nRAS, DDR_nCAS, and DDR_nWE (along with DDR_nCS) define the command being entered.
DDR_LDM DDR_UDM	O	SDRAM data mask outputs. DDR_LDM and DDR_UDM are mask signals for data written to the SDRAM. DDR_LDM corresponds to data on DDR_DQ[7:0], and DDR_UDM corresponds to data on DDR_DQ[15:8].
DDR_BA[2:0]	O	SDRAM bank address outputs. DDR_BA[2:0] define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is applied.
DDR_A[13:0]	O	SDRAM address outputs. Provide row and column addresses to the SDRAM.
DDR_DQ[15:0]	I/O	SDRAM data bus.
DDR_LDQS DDR_LDQSn DDR_UDQS DDR_UDQSn	I/O, Diff	SDRAM differential data strobes. Bidirectional differential signal that follows data direction. Used by SDRAM to capture data on write operations. Edge-aligned with data from SDRAM during read operations and used by the device to capture data. DDR_LDQS corresponds to data on DDR_DQ[7:0], and DDR_UDQS corresponds to data on DDR_DQ[15:8].
DDR_ODT	O	Control signals for the attached DDR2 SDRAM devices on-die termination.
DDR_REXt	ABIAS	External DDR impedance calibration. Connect the pin through an external 240 Ω ±1% resistor to ground.
DDR_Vref	ABIAS	Input reference voltage. Provides the input switching reference voltage to the SSTL DDR signals.

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8.2.3 General-Purpose Inputs and Outputs

The following table lists the pins associated with general-purpose inputs and outputs.

Table 302. GPIO Pins

Name	Type	Description
GPIO0	I/O, PU, ST, 3V	General-purpose I/O Alternate function: SIO_CLK (output)
GPIO1	I/O, PU, ST, 3V	General-purpose I/O Alternate function: SIO_DO (output)
GPIO2	I/O, PU, ST, 3V	General-purpose I/O Alternate function: SIO_DI (input)
GPIO3	I/O, PU, ST, 3V	General-purpose I/O Alternate function: SIO_Latch (output)
GPIO4	I/O, PU, ST, 3V	General-purpose I/O Alternate function: LED_CLK (output)
GPIO5	I/O, PU, ST, 3V	General-purpose I/O Alternate function: LED_DO (output)
GPIO6	I/O, PU, ST, 3V	General-purpose I/O Alternate function: INT0
GPIO7	I/O, PU, ST, 3V	General-purpose I/O Alternate function: INT1
GPIO8	I/O, PU, ST, 3V	General-purpose I/O Alternate function: IEEE_1588_Time_Tick_0 (bidirectional)
GPIO9	I/O, PU, ST, 3V	General-purpose I/O Alternate function: IEEE_1588_Time_Tick_1 (bidirectional)
GPIO10	I/O, PU, ST, 3V	General-purpose I/O Alternate function: UART_RX (input)
GPIO11	I/O, PU, ST, 3V	General-purpose I/O Alternate function: UART_TX (output)
GPIO12	I/O, PU, ST, 3V	General-purpose I/O Alternate function: UART_CTS
GPIO13	I/O, PU, ST, 3V	General-purpose I/O Alternate function: UART_RTS
GPIO14	I/O, PU, ST, 3V	General-purpose I/O Alternate function: TWI_SCL (output)
GPIO15	I/O, PU, ST, 3V	General-purpose I/O Alternate function: TWI_SDA (bidirectional)
GPIO16	I/O, PU, ST, 3V	General-purpose I/O Alternate function: SPI_nCS1
GPIO17	I/O, PU, ST, 3V	General-purpose I/O Alternate function: SPI_nCS2
GPIO18	I/O, PU, ST, 3V	General-purpose I/O Alternate function: SPI_nCS3
GPIO19	I/O, PU, ST, 3V	General-purpose I/O Alternate function: PI_nCS1 (output)
GPIO20	I/O, PU, ST, 3V	General-purpose I/O Alternate function: PI_nCS2 (output)
GPIO21	I/O, PU, ST, 3V	General-purpose I/O Alternate function: PI_nCS3 (output)

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Table 302. GPIO Pins *(continued)*

Name	Type	Description
GPIO22	I/O, PU, ST, 3V	General-purpose I/O Alternate function: PI_nBE0 (output)
GPIO23	I/O, PU, ST, 3V	General-purpose I/O Alternate function: PI_nBE1 (output)

8.2.4 JTAG Interface

The following table lists the pins associated with the JTAG interface. The JTAG interface can be connected to the boundary scan TAP controller or the internal VCore-III TAP controller for software debug as described under the VCore_ICE_nEn signal.

The JTAG signals are not 5 V tolerant.

Table 303. JTAG Interface Pins

Name	Type	Description
JTAG_nTRST	I, PU, ST, 3V	JTAG test reset, active low. For normal device operation, JTAG_nTRST should be pulled low.
JTAG_TCK	I, ST, 3V	JTAG clock.
JTAG_TDI	I, PU, ST, 3V	JTAG test data in.
JTAG_TDO	OZ, 3V	JTAG test data out.
JTAG_TMS	I, PU, ST, 3V	JTAG test mode select.

8.2.5 MII Management Interface

The following table lists the pins associated with the MII Management interface.

Table 304. MII Management Interface Pins

Name	Type	Description
MDIO0 MDIO1	I/O, PU, 3V	Management data input/output. MDIO0 (MDIO1) is a bidirectional signal between a PHY and the device, used to transfer control and status information. Control information is driven by the device synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC0 (MDC1) and is sampled synchronously by the device.
MDC0 MDC1	O, 3V	Management data clock. MDC0 (MDC1) is sourced by the station management entity (the device) to the PHY as the timing reference for transfer of information on the MDIO0 (MDIO1) signal. MDC0 (MDC1) is an aperiodic signal.

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8.2.6 Miscellaneous Signals

The following table lists the pins associated with a particular interface or facility on the device.

Table 305. Miscellaneous Pins

Name	Type	Description
nReset	I, PU, ST, 3V	Global device reset, active low.
core_sense	A	Analog sense connected to the internal core V_{DD} supply. Leave floating or connect to a test measurement point.
VCore_Cfg[1:0]	I, PU, ST, 3V	Configuration signals for controlling the VCore-III CPU functions. For more information about pin configurations, see Table 21, page 109.
VCore_BE_en	I, PD, ST, 3V	VCore-III CPU endian mode selection 0: Little endian 1: Big endian
VCore_ICE_nEn	I, PD, 3V	VCore ICE nEn. 0: Enables the VCore-III JTAG Debug interface over the JTAG interface pins. 1: Enables normal IO-JTAG over the JTAG interface.
ThermDA	A	Thermal diode anode (p-junction).
ThermDC	A	Thermal diode cathode (n-junction). Connected on-die to V_{SS}.
TestCfg[3:0]	I, PD, ST, 3V	Leave floating.
Test_mode1	I, PD	Reserved. Leave floating.
Reserved_0	A	Tie to V_{SS}.
Reserved_1	A	Leave floating.
Reserved_[3:2] Reserved_[41:10] Reserved_[97:50]	I/O	Leave floating.
SERDES_RExt_[1:0]	A	Analog bias calibration. Connect an external 626 Ω ±1% resistor between SERDES_RExt_1 and SERDES_RExt_0.
HS_TST_N HS_TST_P	O, Diff	Reserved. Leave floating.
INT[1:0](1)	I/O, PU, 3V	Interrupt inputs or outputs to the internal VCore-III CPU system or an external processor. Signal polarity is programmable.

1. Available as an alternate function on the GPIO pins.

8.2.7 Parallel Interface

The parallel interface (PI) can operate in a Master mode or a Slave mode according to the VCore_Cfg[1:0] signal settings. In Master mode, the internal VCore-III CPU system

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controls the PI and can access external peripherals over it. In Slave mode, the PI can be used by an external CPU to access internal device resources.

Table 306. Parallel Interface VCore-III Master Mode Pins

Name	Type	Description
PI_Addr[25:0]	OZ, PU, 3V	External address bus. Used for addressing external memory space. PI_Addr0 is LSB.
PI_nBE[1:0](1)	OZ, PU, 3V	Byte Enable signals are used to enable byte-wide access on peripherals with 16-bit data interfaces. PI_nBE0 controls access on PI_Data[7:0]. PI_nBE1 controls access on PI_Data[15:8].
PI_Data[15:0]	I/O, PU, 3V	External data bus. PI_Data0 is LSB.
PI_nCS[0] (PI_nCS[3:1])(1)	OZ, PU, 3V	Programmable active low chip selects. PI_nCS[0] is used as default for booting from external memory (typically Flash). Three additional programmable chip selects (PI_nCS[3:1]) are available using the alternate GPIO functions.
PI_nDone	I, PU, 3V	Acknowledges an operation. Used for external device-paced access operation. Signal polarity is programmable.
PI_nOE	OZ, PU, 3V	Active low signal that signals external device to drive data bus during read access.
PI_nWR	OZ, PU, 3V	Active low signal that signals external access direction. Read (1) or write (0).

1. Available as an alternate function on the GPIO pins.

The following pins are associated with the parallel CPU interface slave mode.

Table 307. Parallel CPU Interface Slave Mode Pins

Name	Type	Description
PI_Addr[25:24]	I, PU, 3V	Leave floating or pull-up.
PI_Addr[23:0]	I, PU, 3V	Internal device register address bus. Controlled by external CPU. PI_Addr0 is LSB.
PI_Data[15:0]	I/O, PU, 3V	Data bus. PI_Data[0] is LSB.
PI_nCS[0]	I, PU, 3V	Device chip select.
PI_nDone	O, PU, 3V	Acknowledges an operation. Signal polarity is programmable.
PI_nOE	I, PU, 3V	Signals device to drive data bus during read operations.
PI_nWR	I, PU, 3V	Signals access direction. Read (1) or write (0).

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8.2.8 Power Supplies and Ground

The following table lists the power supply and ground pins.

Table 308. Power Supply and Ground Pins

Name	Type	Description
VDD	Power	1.0 V power supply voltage for core
VDD_A	Power	1.0 V power supply voltage for analog circuits
VDD_IOXAUI	Power	1.0 V or 1.2 V power supply for XAUI interface
VDD_IOSTATUS	Power	2.5 V or 3.3 V power supply for status channel interface
VDD_IOSGMII	Power	1.0 V or 1.2 V power supply for SGMII interface
VDD_IODDR	Power	1.8 V power supply for DDR interface
VDD_IO33	Power	3.3 V power supply for parallel CPU interface and miscellaneous I/Os
VDD_IOMIIM0	Power	2.5 V or 3.3 V power supply for MIIM interface 0
VDD_IOMIIM1	Power	2.5 V or 3.3 V power supply for MIIM interface 1
VDD_ref25	Power	2.5 V reference supply for SerDes and PLL
VSS	Ground	Ground reference

8.2.9 Serial CPU Interface

The serial CPU interface (SI) can be used as a serial slave, master, or boot interface.

As a slave interface, it allows external CPUs to access internal registers. As a master interface, it allows the device to access external devices using a programmable protocol. The serial CPU interface also allows the internal VCore-III CPU system to boot from an attached serial memory device when the VCore_Cfg signals are set appropriately.

The following table lists the pins associated with the serial CPU interface (SI).

Table 309. Serial CPU Interface Pins

Name	Type	Description
SI_nCS0	I/O, PU, ST, 3V	Slave mode: Input used to enable SI slave interface. 0 = Enabled 1 = Disabled Master mode: Output controlled directly by software through register bit. Boot mode: Output driven while booting from EEPROM or serial flash to internal VCore-III CPU system. Released when booting is completed.
SI_Clk	I/O, PU, ST, 3V	Slave mode: Input receiving serial interface clock from external master. Master mode: Output controlled directly by software through register bit. Boot mode: Output driven with clock to external serial memory device.

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Table 309. Serial CPU Interface Pins *(continued)*

Name	Type	Description
SI_DI	I, PU, ST, 3V	Slave mode: Input receiving serial interface data from external master. Master mode: Input directly read by software from register bit. Boot mode: Input boot data from external serial memory device.
SI_DO	OZ, PU, 3V	Slave mode: Output transmitting serial interface data to external master. Master mode: Output controlled directly by software through register bit. Boot mode: No function.

8.2.10 SGMII Interface

The following pins are associated with the SGMII interface.

Table 310. SGMII Interface Pins

Name	Type	Description
SGMII[22:11]_RxP, N	I, Diff, TD	Differential SGMII data inputs.
SGMII[22:11]_TxP, N	O, Diff	Differential SGMII data outputs.

8.2.11 SGMII Node Processor Interface

The following table lists the pins associated with the SGMII interface for an external processor.

Table 311. SGMII Node Processor Interface Pins

Name	Type	Description
SGMII_NPI_RxP, N	I, Diff, TD	Differential SGMII data inputs
SGMII_NPI_TxP, N	O, Diff	Differential SGMII data outputs

8.2.12 XAUI Interface

The following tables list the pins associated with the XAUI interface pins. The XAUI lanes can be swapped, and the differential pairs can be inverted using the registers. The descriptions in the tables are for the default configurations.

Table 312. XAUI Interface Pins

Name	Type	Description
XAUI[1:0]_Rx[3:0]P, N	I, Diff, TD	Differential XAUI data inputs
XAUI[1:0]_Tx[3:0]P, N	O, Diff	Differential XAUI data outputs

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Table 313. Two-Lane XAUI Interface Pins

Name	Type	Description
XAUI[1:0]_Rx[0,2]P, N	I, Diff, TD	Differential XAUI data inputs
XAUI[1:0]_Tx[0,2]P, N	O, Diff	Differential XAUI data outputs
XAUI[1:0]_Rx[1,3]P, N	I, Diff, TD	Leave floating
XAUI[1:0]_Tx[1,3]P, N	O, Diff	Leave floating

8.2.13 XAUI Status Channel Interface

The following table lists the pins associated with the XAUI status channels.

Table 314. XAUI Status Channel Interface Pins

Name	Type	Description
STATA_OB_SCLK STATB_OB_SCLK	I	Incoming SPI4 status clock
STATA_OB_STAT0 STATA_OB_STAT1 STATB_OB_STAT0 STATB_OB_STAT1	I	Incoming SPI4 status data
STATA_IB_SCLK STATB_IB_SCLK	O	Outgoing SPI4 status clock
STATA_IB_STAT0 STATA_IB_STAT1 STATB_IB_STAT0 STATB_IB_STAT1	O	Outgoing SPI4 status data

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8.3 Pins by Number

This section provides a numeric list of the pins.

A2	PI_Addr22
A3	PI_Data1
A4	PI_Data3
A5	PI_Data5
A6	PI_Data7
A7	PI_nOE
A8	PI_nWR
A9	GPIO20_PI_nCS2
A10	GPIO0_SIO_CLK
A11	GPIO4_LED_CLK
A12	GPIO8_TIME_TICK_0
A13	GPIO10_UART_RX
A14	GPIO14_TWI_SCL
A15	SI_Clk
A16	SI_DI
A17	VCore_ICE_nEn
A18	ThermDA
A19	nReset
A20	MDIO1
A21	STATB_OB_SCLK
A22	STATB_IB_SCLK
A23	STATA_OB_SCLK
A24	STATA_OB_STAT0
A25	STATA_IB_SCLK
AA1	Reserved_1
AA2	Reserved_2
AA3	Reserved_3
AA4	VSS_184
AA5	VSS_32
AA6	VSS_73
AA7	VSS_29
AA8	VDD_IOSGMII_0
AA9	VDD_IOSGMII_2
AA10	VSS_88
AA11	VDD_IOSGMII_4
AA12	VDD_IOSGMII_6
AA13	VSS_35
AA14	VSS_37
AA15	VDD_IOSGMII_8
AA16	VDD_IOSGMII_10
AA17	VSS_131
AA18	VDD_IOSGMII_12
AA19	VDD_IOSGMII_14
AA20	VDD_ref25_2
AA21	VSS_147
AA22	XAUI0_Tx0P
AA23	XAUI0_Tx0N
AA24	VSS_155
AA25	VSS_140
AA26	VSS_175
AB1	MDIO0
AB2	DDR_Vref
AB3	SERDES_RExt_1
AB4	SERDES_RExt_0
AB5	VSS_76
AB6	VSS_33
AB7	VSS_30
AB8	VDD_IOSGMII_1
AB9	VDD_IOSGMII_3
AB10	VSS_43
AB11	VDD_IOSGMII_5
AB12	VDD_IOSGMII_7
AB13	VSS_36
AB14	VSS_38
AB15	VDD_IOSGMII_9
AB16	VDD_IOSGMII_11
AB17	VSS_127
AB18	VDD_IOSGMII_13
AB19	VDD_IOSGMII_15
AB20	VSS_150
AB21	VSS_169
AB22	VSS_173
AB23	VSS_159
AB24	VSS_166
AB25	VSS_162
AB26	Reserved_97
AC1	MDC0
AC2	VDD_IOMIIM0
AC3	Reserved_51
AC4	Reserved_57
AC5	Reserved_59
AC6	Reserved_65
AC7	Reserved_67
AC8	Reserved_73
AC9	Reserved_75
AC10	Reserved_81
AC11	Reserved_83
AC12	Reserved_89
AC13	Reserved_91
AC14	SGMII11_TxP
AC15	SGMII12_TxP
AC16	SGMII13_TxP
AC17	SGMII14_TxP
AC18	SGMII15_TxP
AC19	SGMII16_TxP
AC20	SGMII17_TxP
AC21	SGMII18_TxP
AC22	SGMII19_TxP
AC23	SGMII20_TxP
AC24	SGMII21_TxP
AC25	SGMII22_TxP
AC26	Reserved_96
AD1	SGMII_NPI_TxN
AD2	SGMII_NPI_TxP
AD3	Reserved_50
AD4	Reserved_56
AD5	Reserved_58
AD6	Reserved_64
AD7	Reserved_66
AD8	Reserved_72
AD9	Reserved_74
AD10	Reserved_80
AD11	Reserved_82
AD12	Reserved_88
AD13	Reserved_90
AD14	SGMII11_TxN
AD15	SGMII12_TxN
AD16	SGMII13_TxN
AD17	SGMII14_TxN
AD18	SGMII15_TxN
AD19	SGMII16_TxN
AD20	SGMII17_TxN
AD21	SGMII18_TxN
AD22	SGMII19_TxN
AD23	SGMII20_TxN
AD24	SGMII21_TxN
AD25	SGMII22_TxN
AD26	Reserved_95
AE1	SGMII_NPI_RxN

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Pins by number *(continued)*

AE2	SGMII_NPI_RxP
AE3	Reserved_53
AE4	Reserved_55
AE5	Reserved_61
AE6	Reserved_63
AE7	Reserved_69
AE8	Reserved_71
AE9	Reserved_77
AE10	Reserved_79
AE11	Reserved_85
AE12	Reserved_87
AE13	Reserved_93
AE14	SGMII11_RxP
AE15	SGMII12_RxP
AE16	SGMII13_RxP
AE17	SGMII14_RxP
AE18	SGMII15_RxP
AE19	SGMII16_RxP
AE20	SGMII17_RxP
AE21	SGMII18_RxP
AE22	SGMII19_RxP
AE23	SGMII20_RxP
AE24	SGMII21_RxP
AE25	SGMII22_RxP
AE26	Reserved_94
AF2	Reserved_0
AF3	Reserved_52
AF4	Reserved_54
AF5	Reserved_60
AF6	Reserved_62
AF7	Reserved_68
AF8	Reserved_70
AF9	Reserved_76
AF10	Reserved_78
AF11	Reserved_84
AF12	Reserved_86
AF13	Reserved_92
AF14	SGMII11_RxN
AF15	SGMII12_RxN
AF16	SGMII13_RxN
AF17	SGMII14_RxN
AF18	SGMII15_RxN
AF19	SGMII16_RxN
AF20	SGMII17_RxN
AF21	SGMII18_RxN

AF22	SGMII19_RxN
AF23	SGMII20_RxN
AF24	SGMII21_RxN
AF25	SGMII22_RxN
B1	PI_Addr21
B2	PI_Addr23
B3	PI_Addr24
B4	PI_Data0
B5	PI_Data2
B6	PI_Data4
B7	PI_Data6
B8	PI_nCS0
B9	GPIO21_PI_nCS3
B10	GPIO1_SIO_DO
B11	GPIO5_LED_DO
B12	GPIO9_TIME_TICK_1
B13	GPIO11_UART_TX
B14	GPIO15_TWI_SDA
B15	SI_DO
B16	SI_nCS0
B17	Test_mode1
B18	ThermDC
B19	TestCfg2
B20	MDC1
B21	STATB_OB_STAT1
B22	STATB_IB_STAT0
B23	STATB_IB_STAT1
B24	STATA_OB_STAT1
B25	STATA_IB_STAT1
B26	STATA_IB_STAT0
C1	PI_Addr19
C2	PI_Addr20
C3	PI_Addr25
C4	PI_Data9
C5	PI_Data11
C6	PI_Data13
C7	PI_Data15
C8	PI_nDone
C9	GPIO22_PI_nBE0
C10	GPIO2_SIO_DI
C11	GPIO6_INT0
C12	GPIO12_UART_CTS
C13	VSS_108
C14	core_sense
C15	GPIO17_SPI_nCS2

C16	RefClk_Sel1
C17	RefClk_Sel2
C18	VCore_BE_en
C19	TestCfg1
C20	VCore_Cfg0
C21	STATB_OB_STAT0
C22	RCVRD_CLK0
C23	RCVRD_CLK1
C24	JTAG_TDI
C25	JTAG_TDO
C26	JTAG_TCK
D1	PI_Addr16
D2	PI_Addr17
D3	PI_Addr18
D4	PI_Data8
D5	PI_Data10
D6	PI_Data12
D7	PI_Data14
D8	GPIO19_PI_nCS1
D9	GPIO23_PI_nBE1
D10	GPIO3_SIO_Latch
D11	GPIO7_INT1
D12	GPIO13_UART_RTS
D13	VSS_111
D14	VSS_84
D15	GPIO18_SPI_nCS3
D16	GPIO16_SPI_nCS1
D17	RefClk_Sel0
D18	TestCfg3
D19	TestCfg0
D20	VCore_Cfg1
D21	VDD_IOSTATUS_1
D22	JTAG_TMS
D23	JTAG_nTRST
D24	VSS_62
D25	Reserved_39
D26	Reserved_38
E1	PI_Addr12
E2	PI_Addr13
E3	PI_Addr14
E4	PI_Addr15
E5	VSS_168
E6	VDD_IO33_9
E7	VSS_21
E8	VDD_IO33_10

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Pins by number *(continued)*

E9	VDD_IO33_4	G2	PI_Addr5	H21	VDD_IOXAUI_5
E10	VSS_18	G3	PI_Addr6	H22	Reserved_27
E11	VDD_IO33_13	G4	PI_Addr7	H23	Reserved_26
E12	VDD_IO33_14	G5	VDD_IO33_0	H24	VSS_58
E13	VSS_157	G6	VDD_IO33_2	H25	Reserved_23
E14	VSS_13	G7	VSS_107	H26	Reserved_22
E15	VDD_IO33_6	G8	VDD_30	J1	DDR_LDQS
E16	VDD_IO33_7	G9	VDD_0	J2	DDR_LDQSn
E17	VSS_145	G10	VSS_100	J3	DDR_LDM
E18	VSS_151	G11	VDD_14	J4	DDR_DQ6
E19	VSS_120	G12	VDD_16	J5	VSS_23
E20	VDD_IOSTATUS_0	G13	VSS_5	J6	VSS_72
E21	VDD_IOSTATUS_2	G14	VSS_0	J7	VSS_77
E22	Reserved_41	G15	VDD_32	J8	VSS_8
E23	Reserved_40	G16	VDD_35	J9	VSS_7
E24	VSS_61	G17	VSS_164	J10	VSS_99
E25	Reserved_36	G18	VDD_47	J11	VSS_102
E26	Reserved_37	G19	VDD_49	J12	VSS_70
F1	PI_Addr8	G20	VDD_IOXAUI_4	J13	VSS_48
F2	PI_Addr9	G21	VDD_IOXAUI_6	J14	VSS_81
F3	PI_Addr10	G22	Reserved_33	J15	VSS_39
F4	PI_Addr11	G23	Reserved_32	J16	VSS_132
F5	VSS_121	G24	VSS_59	J17	VSS_179
F6	VSS_146	G25	Reserved_28	J18	VSS_144
F7	VSS_22	G26	Reserved_29	J19	VSS_143
F8	VDD_IO33_11	H1	PI_Addr0	J20	VSS_152
F9	VDD_IO33_5	H2	PI_Addr1	J21	VSS_174
F10	VSS_19	H3	PI_Addr2	J22	Reserved_25
F11	VDD_IO33_12	H4	PI_Addr3	J23	Reserved_24
F12	VDD_IO33_3	H5	VDD_IO33_1	J24	VSS_57
F13	VSS_20	H6	VDD_IO33_8	J25	Reserved_20
F14	VSS_87	H7	VSS_158	J26	Reserved_21
F15	VDD_IO33_15	H8	VDD_31	K1	DDR_DQ0
F16	VDD_IO33_16	H9	VDD_1	K2	DDR_DQ7
F17	VSS_105	H10	VSS_104	K3	DDR_DQ3
F18	VSS_170	H11	VDD_15	K4	DDR_DQ1
F19	VSS_118	H12	VDD_17	K5	VDD_IODDR_12
F20	VDD_IOMIIM1	H13	VSS_52	K6	VDD_IODDR_11
F21	VDD_IOSTATUS_3	H14	VSS_1	K7	VSS_177
F22	Reserved_35	H15	VDD_33	K8	VDD_2
F23	Reserved_34	H16	VDD_34	K9	VDD_4
F24	VSS_60	H17	VSS_165	K10	VSS_95
F25	Reserved_31	H18	VDD_48	K11	VDD_18
F26	Reserved_30	H19	VDD_53	K12	VDD_20
G1	PI_Addr4	H20	VDD_IOXAUI_3	K13	VSS_69

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Pins by number *(continued)*

K14	VSS_98	M7	VSS_160	N26	XAUI1_Rx3N
K15	VDD_36	M8	VSS_6	P1	DDR_Ckn
K16	VDD_42	M9	VSS_9	P2	DDR_Ck
K17	VSS_113	M10	VSS_92	P3	DDR_A11
K18	VDD_51	M11	VSS_11	P4	DDR_A13
K19	VDD_56	M12	VSS_12	P5	VDD_IODDR_9
K20	VDD_IOXAUI_10	M13	VSS_67	P6	VDD_IODDR_8
K21	VDD_IOXAUI_12	M14	VSS_80	P7	VSS_161
K22	Reserved_19	M15	VSS_94	P8	VDD_6
K23	Reserved_18	M16	VSS_182	P9	VDD_8
K24	VSS_56	M17	VSS_142	P10	VSS_86
K25	Reserved_15	M18	VSS_183	P11	VDD_22
K26	Reserved_14	M19	VSS_149	P12	VDD_24
L1	DDR_DQ5	M20	VSS_176	P13	VSS_65
L2	DDR_DQ2	M21	VSS_154	P14	VSS_82
L3	DDR_nRAS	M22	Reserved_11	P15	VDD_37
L4	DDR_DQ4	M23	Reserved_10	P16	VDD_39
L5	VDD_IODDR_13	M24	VSS_54	P17	VSS_138
L6	VDD_IODDR_10	M25	REFCLK_N	P18	VDD_58
L7	VSS_109	M26	REFCLK_P	P19	VDD_60
L8	VDD_3	N1	DDR_A8	P20	VDD_IOXAUI_7
L9	VDD_5	N2	DDR_A4	P21	VDD_IOXAUI_8
L10	VSS_97	N3	DDR_nWE	P22	XAUI1_Tx3P
L11	VDD_19	N4	DDR_A6	P23	XAUI1_Tx3N
L12	VDD_21	N5	VSS_25	P24	VSS_51
L13	VSS_68	N6	VSS_27	P25	XAUI1_Rx2P
L14	VSS_2	N7	VSS_90	P26	XAUI1_Rx2N
L15	VDD_50	N8	VSS_106	R1	DDR_A12
L16	VDD_41	N9	VSS_117	R2	DDR_A7
L17	VSS_180	N10	VSS_89	R3	DDR_A9
L18	VDD_55	N11	VSS_85	R4	DDR_A5
L19	VDD_57	N12	VSS_114	R5	VDD_IODDR_7
L20	VDD_IOXAUI_9	N13	VSS_66	R6	VDD_IODDR_6
L21	VDD_IOXAUI_11	N14	VSS_3	R7	VSS_110
L22	Reserved_17	N15	VSS_83	R8	VDD_7
L23	Reserved_16	N16	VSS_130	R9	VDD_9
L24	VSS_55	N17	VSS_141	R10	VSS_96
L25	Reserved_12	N18	VSS_129	R11	VDD_23
L26	Reserved_13	N19	VSS_128	R12	VDD_25
M1	DDR_A0	N20	VSS_126	R13	VSS_64
M2	DDR_ODT	N21	VSS_125	R14	VSS_4
M3	DDR_A2	N22	HS_TST_P	R15	VDD_38
M4	DDR_nCAS	N23	HS_TST_N	R16	VDD_40
M5	VSS_24	N24	VSS_53	R17	VSS_139
M6	VSS_26	N25	XAUI1_Rx3P	R18	VDD_59

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R19	VDD_61	U12	VDD_28	W5	VSS_75
R20	VDD_IOXAUI_2	U13	VSS_41	W6	VSS_71
R21	VDD_IOXAUI_13	U14	VSS_101	W7	VSS_112
R22	XAUI1_Tx2P	U15	VDD_43	W8	VDD_A_0
R23	XAUI1_Tx2N	U16	VDD_45	W9	VDD_A_2
R24	VSS_50	U17	VSS_135	W10	VSS_44
R25	XAUI1_Rx1P	U18	VDD_62	W11	VDD_A_12
R26	XAUI1_Rx1N	U19	VDD_52	W12	VDD_A_14
T1	DDR_A3	U20	VDD_A_9	W13	VSS_156
T2	DDR_A10	U21	VDD_IOXAUI_1	W14	VSS_116
T3	DDR_A1	U22	XAUI1_Tx0P	W15	VDD_A_16
T4	DDR_BA1	U23	XAUI1_Tx0N	W16	VDD_A_3
T5	VSS_28	U24	VSS_47	W17	VSS_124
T6	VSS_115	U25	XAUI0_Rx3P	W18	VDD_A_5
T7	VSS_178	U26	XAUI0_Rx3N	W19	VDD_A_7
T8	VSS_74	V1	DDR_DQ12	W20	VDD_ref25_0
T9	VSS_14	V2	DDR_DQ11	W21	VSS_148
T10	VSS_40	V3	DDR_DQ10	W22	XAUI0_Tx2P
T11	VSS_16	V4	DDR_DQ13	W23	XAUI0_Tx2N
T12	VSS_103	V5	VDD_IODDR_4	W24	VSS_45
T13	VSS_63	V6	VDD_IODDR_2	W25	XAUI0_Rx1P
T14	VSS_79	V7	VSS_163	W26	XAUI0_Rx1N
T15	VSS_133	V8	VDD_11	Y1	DDR_RExt
T16	VSS_181	V9	VDD_13	Y2	DDR_UDM
T17	VSS_137	V10	VSS_42	Y3	DDR_UDQS
T18	VSS_93	V11	VDD_27	Y4	DDR_UDQSn
T19	VSS_123	V12	VDD_29	Y5	VDD_IODDR_1
T20	VSS_153	V13	VSS_17	Y6	VDD_IODDR_0
T21	VSS_122	V14	VSS_78	Y7	VSS_31
T22	XAUI1_Tx1P	V15	VDD_44	Y8	VDD_A_1
T23	XAUI1_Tx1N	V16	VDD_46	Y9	VDD_A_11
T24	VSS_49	V17	VSS_136	Y10	VSS_15
T25	XAUI1_Rx0P	V18	VDD_63	Y11	VDD_A_13
T26	XAUI1_Rx0N	V19	VDD_54	Y12	VDD_A_15
U1	DDR_BA0	V20	VDD_A_10	Y13	VSS_34
U2	DDR_BA2	V21	VDD_IOXAUI_0	Y14	VSS_119
U3	DDR_Cke	V22	XAUI0_Tx3P	Y15	VDD_A_17
U4	VSS_167	V23	XAUI0_Tx3N	Y16	VDD_A_4
U5	VDD_IODDR_5	V24	VSS_46	Y17	VSS_134
U6	VDD_IODDR_3	V25	XAUI0_Rx2P	Y18	VDD_A_6
U7	VSS_91	V26	XAUI0_Rx2N	Y19	VDD_A_8
U8	VDD_10	W1	DDR_DQ9	Y20	VDD_ref25_1
U9	VDD_12	W2	DDR_DQ14	Y21	VSS_172
U10	VSS_10	W3	DDR_DQ8	Y22	XAUI0_Tx1P
U11	VDD_26	W4	DDR_DQ15	Y23	XAUI0_Tx1N

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Y24	VSS_171
Y25	XAUI0_Rx0P
Y26	XAUI0_Rx0N

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8.4 Pins by Name

This section provides an alphabetical list of the pins.

core_sense	C14
DDR_A0	M1
DDR_A1	T3
DDR_A2	M3
DDR_A3	T1
DDR_A4	N2
DDR_A5	R4
DDR_A6	N4
DDR_A7	R2
DDR_A8	N1
DDR_A9	R3
DDR_A10	T2
DDR_A11	P3
DDR_A12	R1
DDR_A13	P4
DDR_BA0	U1
DDR_BA1	T4
DDR_BA2	U2
DDR_Ck	P2
DDR_Cke	U3
DDR_Ckn	P1
DDR_DQ0	K1
DDR_DQ1	K4
DDR_DQ2	L2
DDR_DQ3	K3
DDR_DQ4	L4
DDR_DQ5	L1
DDR_DQ6	J4
DDR_DQ7	K2
DDR_DQ8	W3
DDR_DQ9	W1
DDR_DQ10	V3
DDR_DQ11	V2
DDR_DQ12	V1
DDR_DQ13	V4
DDR_DQ14	W2
DDR_DQ15	W4
DDR_LDM	J3
DDR_LDQS	J1
DDR_LDQSn	J2
DDR_nCAS	M4
DDR_nRAS	L3
DDR_nWE	N3
DDR_ODT	M2
DDR_RExt	Y1
DDR_UDM	Y2
DDR_UDQS	Y3
DDR_UDQSn	Y4
DDR_Vref	AB2
GPIO0_SIO_CLK	A10
GPIO1_SIO_DO	B10
GPIO2_SIO_DI	C10
GPIO3_SIO_Latch	D10
GPIO4_LED_CLK	A11
GPIO5_LED_DO	B11
GPIO6_INT0	C11
GPIO7_INT1	D11
GPIO8_TIME_TICK_0	A12
GPIO9_TIME_TICK_1	B12
GPIO10_UART_RX	A13
GPIO11_UART_TX	B13
GPIO12_UART_CTS	C12
GPIO13_UART_RTS	D12
GPIO14_TWI_SCL	A14
GPIO15_TWI_SDA	B14
GPIO16_SPI_nCS1	D16
GPIO17_SPI_nCS2	C15
GPIO18_SPI_nCS3	D15
GPIO19_PI_nCS1	D8
GPIO20_PI_nCS2	A9
GPIO21_PI_nCS3	B9
GPIO22_PI_nBE0	C9
GPIO23_PI_nBE1	D9
HS_TST_N	N23
HS_TST_P	N22
JTAG_nTRST	D23
JTAG_TCK	C26
JTAG_TDI	C24
JTAG_TDO	C25
JTAG_TMS	D22
MDC0	AC1
MDC1	B20
MDIO0	AB1
MDIO1	A20
nReset	A19
PI_Addr0	H1
PI_Addr1	H2
PI_Addr2	H3
PI_Addr3	H4
PI_Addr4	G1
PI_Addr5	G2
PI_Addr6	G3
PI_Addr7	G4
PI_Addr8	F1
PI_Addr9	F2
PI_Addr10	F3
PI_Addr11	F4
PI_Addr12	E1
PI_Addr13	E2
PI_Addr14	E3
PI_Addr15	E4
PI_Addr16	D1
PI_Addr17	D2
PI_Addr18	D3
PI_Addr19	C1
PI_Addr20	C2
PI_Addr21	B1
PI_Addr22	A2
PI_Addr23	B2
PI_Addr24	B3
PI_Addr25	C3
PI_Data0	B4
PI_Data1	A3
PI_Data2	B5
PI_Data3	A4
PI_Data4	B6
PI_Data5	A5
PI_Data6	B7
PI_Data7	A6
PI_Data8	D4
PI_Data9	C4
PI_Data10	D5
PI_Data11	C5
PI_Data12	D6
PI_Data13	C6
PI_Data14	D7
PI_Data15	C7
PI_nCS0	B8
PI_nDone	C8

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Pins by name *(continued)*

PI_nOE	A7	Reserved_50	AD3	Reserved_95	AD26
PI_nWR	A8	Reserved_51	AC3	Reserved_96	AC26
RCVRD_CLK0	C22	Reserved_52	AF3	Reserved_97	AB26
RCVRD_CLK1	C23	Reserved_53	AE3	SERDES_RExt_0	AB4
REFCLK_N	M25	Reserved_54	AF4	SERDES_RExt_1	AB3
REFCLK_P	M26	Reserved_55	AE4	SGMII_NPI_RxN	AE1
RefClk_Sel0	D17	Reserved_56	AD4	SGMII_NPI_RxP	AE2
RefClk_Sel1	C16	Reserved_57	AC4	SGMII_NPI_TxN	AD1
RefClk_Sel2	C17	Reserved_58	AD5	SGMII_NPI_TxP	AD2
Reserved_0	AF2	Reserved_59	AC5	SGMII11_RxN	AF14
Reserved_1	AA1	Reserved_60	AF5	SGMII11_RxP	AE14
Reserved_2	AA2	Reserved_61	AE5	SGMII11_TxN	AD14
Reserved_3	AA3	Reserved_62	AF6	SGMII11_TxP	AC14
Reserved_10	M23	Reserved_63	AE6	SGMII12_RxN	AF15
Reserved_11	M22	Reserved_64	AD6	SGMII12_RxP	AE15
Reserved_12	L25	Reserved_65	AC6	SGMII12_TxN	AD15
Reserved_13	L26	Reserved_66	AD7	SGMII12_TxP	AC15
Reserved_14	K26	Reserved_67	AC7	SGMII13_RxN	AF16
Reserved_15	K25	Reserved_68	AF7	SGMII13_RxP	AE16
Reserved_16	L23	Reserved_69	AE7	SGMII13_TxN	AD16
Reserved_17	L22	Reserved_70	AF8	SGMII13_TxP	AC16
Reserved_18	K23	Reserved_71	AE8	SGMII14_RxN	AF17
Reserved_19	K22	Reserved_72	AD8	SGMII14_RxP	AE17
Reserved_20	J25	Reserved_73	AC8	SGMII14_TxN	AD17
Reserved_21	J26	Reserved_74	AD9	SGMII14_TxP	AC17
Reserved_22	H26	Reserved_75	AC9	SGMII15_RxN	AF18
Reserved_23	H25	Reserved_76	AF9	SGMII15_RxP	AE18
Reserved_24	J23	Reserved_77	AE9	SGMII15_TxN	AD18
Reserved_25	J22	Reserved_78	AF10	SGMII15_TxP	AC18
Reserved_26	H23	Reserved_79	AE10	SGMII16_RxN	AF19
Reserved_27	H22	Reserved_80	AD10	SGMII16_RxP	AE19
Reserved_28	G25	Reserved_81	AC10	SGMII16_TxN	AD19
Reserved_29	G26	Reserved_82	AD11	SGMII16_TxP	AC19
Reserved_30	F26	Reserved_83	AC11	SGMII17_RxN	AF20
Reserved_31	F25	Reserved_84	AF11	SGMII17_RxP	AE20
Reserved_32	G23	Reserved_85	AE11	SGMII17_TxN	AD20
Reserved_33	G22	Reserved_86	AF12	SGMII17_TxP	AC20
Reserved_34	F23	Reserved_87	AE12	SGMII18_RxN	AF21
Reserved_35	F22	Reserved_88	AD12	SGMII18_RxP	AE21
Reserved_36	E25	Reserved_89	AC12	SGMII18_TxN	AD21
Reserved_37	E26	Reserved_90	AD13	SGMII18_TxP	AC21
Reserved_38	D26	Reserved_91	AC13	SGMII19_RxN	AF22
Reserved_39	D25	Reserved_92	AF13	SGMII19_RxP	AE22
Reserved_40	E23	Reserved_93	AE13	SGMII19_TxN	AD22
Reserved_41	E22	Reserved_94	AE26	SGMII19_TxP	AC22

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Pins by name *(continued)*

SGMII20_RxN	AF23	VDD_6	P8	VDD_51	K18
SGMII20_RxP	AE23	VDD_7	R8	VDD_52	U19
SGMII20_TxN	AD23	VDD_8	P9	VDD_53	H19
SGMII20_TxP	AC23	VDD_9	R9	VDD_54	V19
SGMII21_RxN	AF24	VDD_10	U8	VDD_55	L18
SGMII21_RxP	AE24	VDD_11	V8	VDD_56	K19
SGMII21_TxN	AD24	VDD_12	U9	VDD_57	L19
SGMII21_TxP	AC24	VDD_13	V9	VDD_58	P18
SGMII22_RxN	AF25	VDD_14	G11	VDD_59	R18
SGMII22_RxP	AE25	VDD_15	H11	VDD_60	P19
SGMII22_TxN	AD25	VDD_16	G12	VDD_61	R19
SGMII22_TxP	AC25	VDD_17	H12	VDD_62	U18
SI_Clk	A15	VDD_18	K11	VDD_63	V18
SI_DI	A16	VDD_19	L11	VDD_A_0	W8
SI_DO	B15	VDD_20	K12	VDD_A_1	Y8
SI_nCS0	B16	VDD_21	L12	VDD_A_2	W9
STATA_IB_SCLK	A25	VDD_22	P11	VDD_A_3	W16
STATA_IB_STAT0	B26	VDD_23	R11	VDD_A_4	Y16
STATA_IB_STAT1	B25	VDD_24	P12	VDD_A_5	W18
STATA_OB_SCLK	A23	VDD_25	R12	VDD_A_6	Y18
STATA_OB_STAT0	A24	VDD_26	U11	VDD_A_7	W19
STATA_OB_STAT1	B24	VDD_27	V11	VDD_A_8	Y19
STATB_IB_SCLK	A22	VDD_28	U12	VDD_A_9	U20
STATB_IB_STAT0	B22	VDD_29	V12	VDD_A_10	V20
STATB_IB_STAT1	B23	VDD_30	G8	VDD_A_11	Y9
STATB_OB_SCLK	A21	VDD_31	H8	VDD_A_12	W11
STATB_OB_STAT0	C21	VDD_32	G15	VDD_A_13	Y11
STATB_OB_STAT1	B21	VDD_33	H15	VDD_A_14	W12
Test_mode1	B17	VDD_34	H16	VDD_A_15	Y12
TestCfg0	D19	VDD_35	G16	VDD_A_16	W15
TestCfg1	C19	VDD_36	K15	VDD_A_17	Y15
TestCfg2	B19	VDD_37	P15	VDD_IO33_0	G5
TestCfg3	D18	VDD_38	R15	VDD_IO33_1	H5
ThermDA	A18	VDD_39	P16	VDD_IO33_2	G6
ThermDC	B18	VDD_40	R16	VDD_IO33_3	F12
VCore_BE_en	C18	VDD_41	L16	VDD_IO33_4	E9
VCore_Cfg0	C20	VDD_42	K16	VDD_IO33_5	F9
VCore_Cfg1	D20	VDD_43	U15	VDD_IO33_6	E15
VCore_ICE_nEn	A17	VDD_44	V15	VDD_IO33_7	E16
VDD_0	G9	VDD_45	U16	VDD_IO33_8	H6
VDD_1	H9	VDD_46	V16	VDD_IO33_9	E6
VDD_2	K8	VDD_47	G18	VDD_IO33_10	E8
VDD_3	L8	VDD_48	H18	VDD_IO33_11	F8
VDD_4	K9	VDD_49	G19	VDD_IO33_12	F11
VDD_5	L9	VDD_50	L15	VDD_IO33_13	E11

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VDD_IO33_14	E12	VDD_IOXAUI_6	G21	VSS_34	Y13
VDD_IO33_15	F15	VDD_IOXAUI_7	P20	VSS_35	AA13
VDD_IO33_16	F16	VDD_IOXAUI_8	P21	VSS_36	AB13
VDD_IODDR_0	Y6	VDD_IOXAUI_9	L20	VSS_37	AA14
VDD_IODDR_1	Y5	VDD_IOXAUI_10	K20	VSS_38	AB14
VDD_IODDR_2	V6	VDD_IOXAUI_11	L21	VSS_39	J15
VDD_IODDR_3	U6	VDD_IOXAUI_12	K21	VSS_40	T10
VDD_IODDR_4	V5	VDD_IOXAUI_13	R21	VSS_41	U13
VDD_IODDR_5	U5	VDD_ref25_0	W20	VSS_42	V10
VDD_IODDR_6	R6	VDD_ref25_1	Y20	VSS_43	AB10
VDD_IODDR_7	R5	VDD_ref25_2	AA20	VSS_44	W10
VDD_IODDR_8	P6	VSS_0	G14	VSS_45	W24
VDD_IODDR_9	P5	VSS_1	H14	VSS_46	V24
VDD_IODDR_10	L6	VSS_2	L14	VSS_47	U24
VDD_IODDR_11	K6	VSS_3	N14	VSS_48	J13
VDD_IODDR_12	K5	VSS_4	R14	VSS_49	T24
VDD_IODDR_13	L5	VSS_5	G13	VSS_50	R24
VDD_IOMIIM0	AC2	VSS_6	M8	VSS_51	P24
VDD_IOMIIM1	F20	VSS_7	J9	VSS_52	H13
VDD_IOSGMII_0	AA8	VSS_8	J8	VSS_53	N24
VDD_IOSGMII_1	AB8	VSS_9	M9	VSS_54	M24
VDD_IOSGMII_2	AA9	VSS_10	U10	VSS_55	L24
VDD_IOSGMII_3	AB9	VSS_11	M11	VSS_56	K24
VDD_IOSGMII_4	AA11	VSS_12	M12	VSS_57	J24
VDD_IOSGMII_5	AB11	VSS_13	E14	VSS_58	H24
VDD_IOSGMII_6	AA12	VSS_14	T9	VSS_59	G24
VDD_IOSGMII_7	AB12	VSS_15	Y10	VSS_60	F24
VDD_IOSGMII_8	AA15	VSS_16	T11	VSS_61	E24
VDD_IOSGMII_9	AB15	VSS_17	V13	VSS_62	D24
VDD_IOSGMII_10	AA16	VSS_18	E10	VSS_63	T13
VDD_IOSGMII_11	AB16	VSS_19	F10	VSS_64	R13
VDD_IOSGMII_12	AA18	VSS_20	F13	VSS_65	P13
VDD_IOSGMII_13	AB18	VSS_21	E7	VSS_66	N13
VDD_IOSGMII_14	AA19	VSS_22	F7	VSS_67	M13
VDD_IOSGMII_15	AB19	VSS_23	J5	VSS_68	L13
VDD_IOSTATUS_0	E20	VSS_24	M5	VSS_69	K13
VDD_IOSTATUS_1	D21	VSS_25	N5	VSS_70	J12
VDD_IOSTATUS_2	E21	VSS_26	M6	VSS_71	W6
VDD_IOSTATUS_3	F21	VSS_27	N6	VSS_72	J6
VDD_IOXAUI_0	V21	VSS_28	T5	VSS_73	AA6
VDD_IOXAUI_1	U21	VSS_29	AA7	VSS_74	T8
VDD_IOXAUI_2	R20	VSS_30	AB7	VSS_75	W5
VDD_IOXAUI_3	H20	VSS_31	Y7	VSS_76	AB5
VDD_IOXAUI_4	G20	VSS_32	AA5	VSS_77	J7
VDD_IOXAUI_5	H21	VSS_33	AB6	VSS_78	V14

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Pins by name *(continued)*

VSS_79	T14	VSS_134	Y17	VSS_179	J17
VSS_80	M14	VSS_135	U17	VSS_180	L17
VSS_81	J14	VSS_136	V17	VSS_181	T16
VSS_82	P14	VSS_137	T17	VSS_182	M16
VSS_83	N15	VSS_138	P17	VSS_183	M18
VSS_84	D14	VSS_139	R17	VSS_184	AA4
VSS_85	N11	VSS_140	AA25	VSS_100	G10
VSS_86	P10	VSS_141	N17	VSS_101	U14
VSS_87	F14	VSS_142	M17	VSS_102	J11
VSS_88	AA10	VSS_143	J19	VSS_103	T12
VSS_89	N10	VSS_144	J18	VSS_104	H10
VSS_90	N7	VSS_145	E17	VSS_105	F17
VSS_91	U7	VSS_146	F6	VSS_106	N8
VSS_92	M10	VSS_147	AA21	VSS_107	G7
VSS_93	T18	VSS_148	W21	VSS_108	C13
VSS_94	M15	VSS_149	M19	VSS_109	L7
VSS_95	K10	VSS_150	AB20	XAUI0_Rx0N	Y26
VSS_96	R10	VSS_151	E18	XAUI0_Rx0P	Y25
VSS_97	L10	VSS_152	J20	XAUI0_Rx1N	W26
VSS_98	K14	VSS_153	T20	XAUI0_Rx1P	W25
VSS_99	J10	VSS_154	M21	XAUI0_Rx2N	V26
VSS_110	R7	VSS_155	AA24	XAUI0_Rx2P	V25
VSS_111	D13	VSS_156	W13	XAUI0_Rx3N	U26
VSS_112	W7	VSS_157	E13	XAUI0_Rx3P	U25
VSS_113	K17	VSS_158	H7	XAUI0_Tx0N	AA23
VSS_114	N12	VSS_159	AB23	XAUI0_Tx0P	AA22
VSS_115	T6	VSS_160	M7	XAUI0_Tx1N	Y23
VSS_116	W14	VSS_161	P7	XAUI0_Tx1P	Y22
VSS_117	N9	VSS_162	AB25	XAUI0_Tx2N	W23
VSS_118	F19	VSS_163	V7	XAUI0_Tx2P	W22
VSS_119	Y14	VSS_164	G17	XAUI0_Tx3N	V23
VSS_120	E19	VSS_165	H17	XAUI0_Tx3P	V22
VSS_121	F5	VSS_166	AB24	XAUI1_Rx0N	T26
VSS_122	T21	VSS_167	U4	XAUI1_Rx0P	T25
VSS_123	T19	VSS_168	E5	XAUI1_Rx1N	R26
VSS_124	W17	VSS_169	AB21	XAUI1_Rx1P	R25
VSS_125	N21	VSS_170	F18	XAUI1_Rx2N	P26
VSS_126	N20	VSS_171	Y24	XAUI1_Rx2P	P25
VSS_127	AB17	VSS_172	Y21	XAUI1_Rx3N	N26
VSS_128	N19	VSS_173	AB22	XAUI1_Rx3P	N25
VSS_129	N18	VSS_174	J21	XAUI1_Tx0N	U23
VSS_130	N16	VSS_175	AA26	XAUI1_Tx0P	U22
VSS_131	AA17	VSS_176	M20	XAUI1_Tx1N	T23
VSS_132	J16	VSS_177	K7	XAUI1_Tx1P	T22
VSS_133	T15	VSS_178	T7	XAUI1_Tx2N	R23

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Pins by name *(continued)*

XAUI1_Tx2P	R22
XAUI1_Tx3N	P23
XAUI1_Tx3P	P22

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9 Package Information

The package is a 672-pin, thermally enhanced flip chip ball grid array (FCBGA) with a 27 mm × 27 mm size, 1 mm pitch, and 2.74 mm maximum height. The devices are also available a lead(Pb)-free package (second-level interconnect only).

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing and moisture sensitivity rating.

9.1 Package Drawing

The following illustration shows the package drawing. The drawing contains the top view, bottom view, side view, detail views, dimensions, tolerances, and notes.

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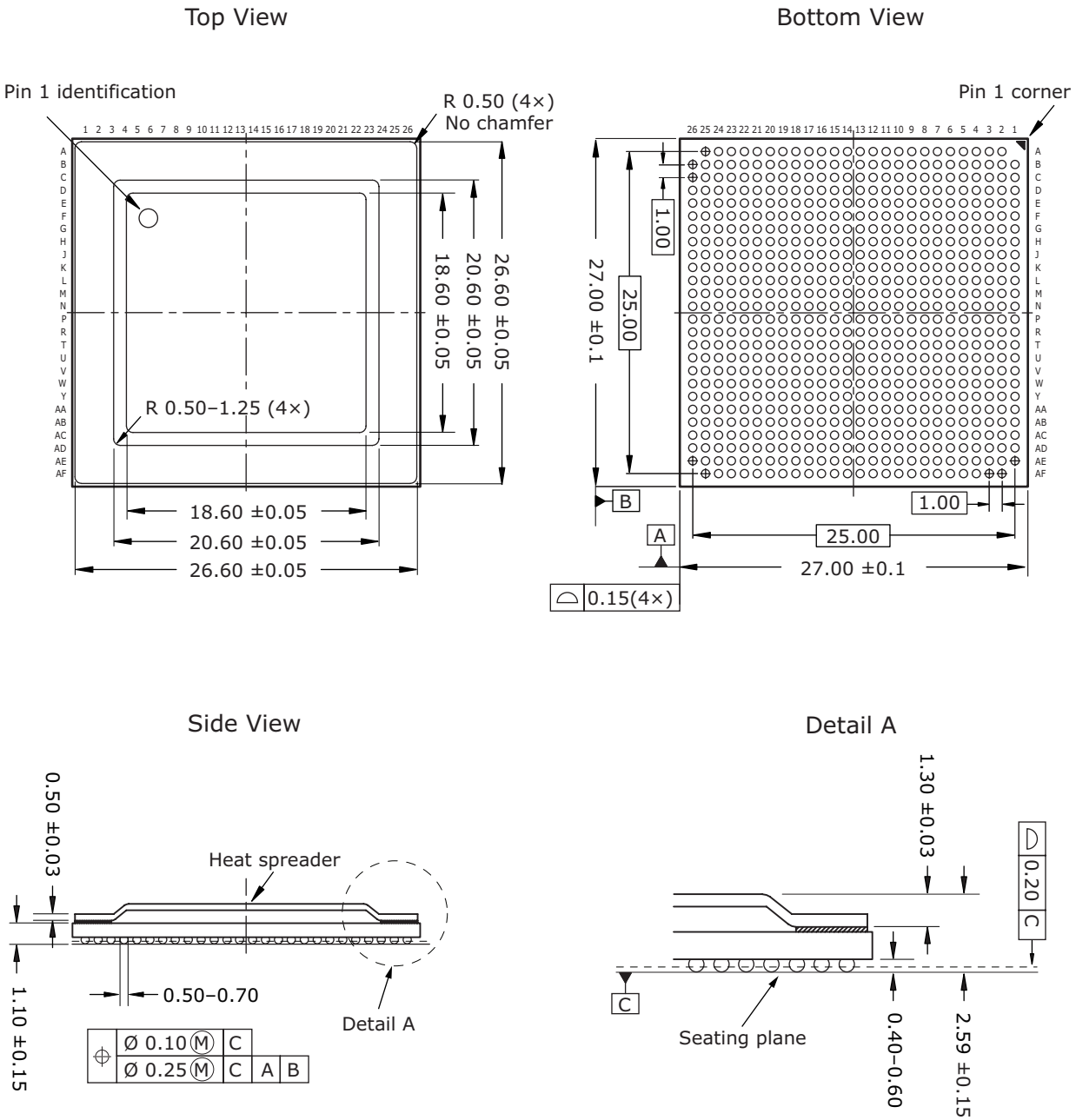
Figure 84. Package Drawing



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Radial true position is represented by typical values.

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9.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Thermal resistance (°C/W) measurements for this device include:

- Junction to case with heat flow through the top of the package (θ_{JCtop}) per JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- Junction to board (θ_{JB}) per JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, and per JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- Junction to ambient (θ_{JA}) per JESD51-2, *Integrated Circuit Thermal Measurement Method, Environmental Conditions, Natural Convection (Still Air)*
- Junction to moving air (θ_{JMA}) measured at an air speed of 1 m/s and 2 m/s per JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*

Table 315. Thermal Resistances

Part Order Number	θ_{JCtop}	θ_{JB}	θ_{JA}	θ_{JMA} at 1 m/s	θ_{JMA} at 2 m/s
VSC7462IH-01	0.62	9	13	10.7	9
VSC7462XIH-01	0.62	9	13	10.7	9

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about specific applications, see the following:

- JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
- JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*
- JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

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9.3 Moisture Sensitivity

Moisture sensitivity level ratings for Vitesse products comply with the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. All Vitesse products are rated moisture sensitivity level 4 or better unless specified otherwise. For more information, see the IPC and JEDEC standard.

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10 Design Guidelines

10.1 Power Supplies

The following guidelines apply to designing power supplies for use with the VSC7462 device:

- Make at least one unbroken ground plane (GND).
- Use the power and ground plane combination as an effective power supply bypass capacitor. The capacitance is proportional to the area of the two planes and inversely proportional to the separation between the planes. Typical values with a 0.25 mm (0.01 inch) separation are 100 pF / in2. This capacitance is more effective than a capacitor of equivalent value, because the planes have no inductance or Equivalent Series Resistance (ESR).
- Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less. Furthermore, place vias and clearances in a configuration that maintains the integrity of the plane. Groups of vias spaced close together often overlap clearances. This can form a large slot in the plane. As a result, return currents are forced around the slot, which increases the loop area and EMI emissions. Signals should never be placed on a ground plane, because the resulting slot forces return currents around the slot.
- Vias connecting power planes to the supply and ground balls should be at least 0.25 mm (0.010 inch) in diameter, preferably with no thermal relief and plated closed with copper or solder. Use separate (or even multiple) vias for each supply and ground ball.

10.2 Power Supply Decoupling

Each power supply voltage should have both bulk and high-frequency decoupling capacitors. Recommended capacitors are as follows:

- For bulk decoupling, use 10 µF high capacity and low ESR capacitors or equivalent, distributed across the board.
- For high-frequency decoupling, use 0.1 µF high frequency (for example, X7R) ceramic capacitors placed on the side of the PCB closest to the plane being decoupled, and as close as possible to the power ball. A larger value in the same housing unit produces even better results.
- Use surface mounted components for lower lead inductance and pad capacitance. Smaller form factor components are best (that is, 0402 is better than 0603).

10.3 Reference Clock

The device reference clock can be a 25 MHz, 125 MHz, or 156.25 MHz clock signal. It can be either a differential reference clock or a single-ended clock.

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10.3.1 Single-Ended RefClk Input

An external resistor network is required to use a single-ended reference clock. The network limits the amplitude and adjusts the center of the swing.

Configurations for a single-ended reference clock are shown in the following illustrations.

Figure 85. 2.5 V CMOS Single-Ended RefClk Input Resistor Network

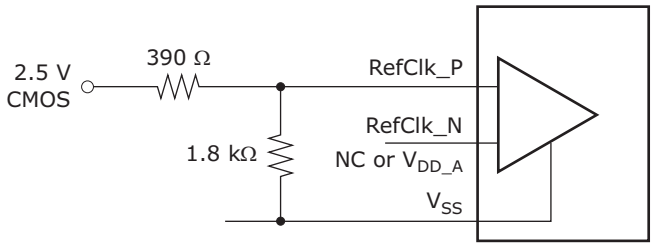


Figure 86. 3.3 V CMOS Single-Ended RefClk Input Resistor Network

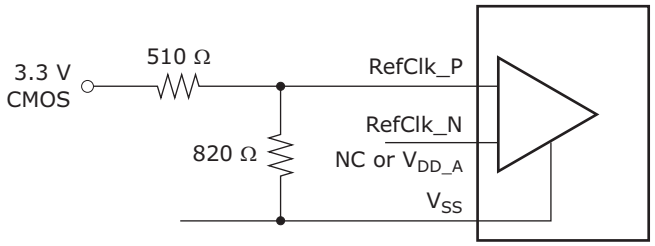
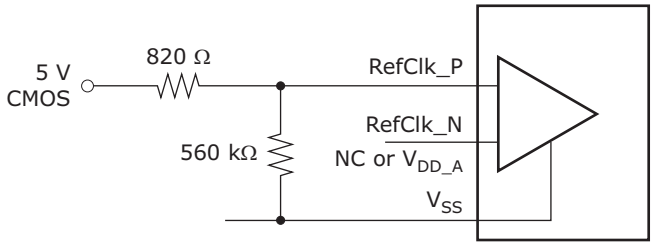


Figure 87. 5 V CMOS Single-Ended RefClk Input Resistor Network



10.4 Interfaces

This section provides general recommendations for all interfaces and information related to the specific interfaces on the device.

10.4.1 General Recommendations

High-speed signals require excellent frequency and phase response up to the third harmonic. The best design would provide excellent frequency and phase response up to

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the seventh harmonic. The following recommendations can improve signal quality and minimize transmission distances:

Keep traces as short as possible. Initial component placement should be considered very carefully.

- The impedance of the traces must match the impedance of the termination resistors, connectors, and cable. This reduces reflections due to impedance mismatches.
- Differential impedance must be maintained in a 100-Ω differential application. Routing two 50-Ω traces is not adequate. The two traces must be separated by enough distance to maintain differential impedance. When routing differential pairs, keep the two trace lengths identical. Differences in trace lengths translate directly into signal skew. Note that the differential impedance may be affected when separations occur.
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities.
- Do not group all the passive components together. The pads of the components add capacitance to the traces. At the frequencies encountered, this can result in unwanted reductions in impedance. Use surface-mounted 0603 components to reduce this effect.
- Eliminate or reduce stub lengths.
- Reduce, if not eliminate, vias to minimize impedance discontinuities. Remember that vias and their clearance holes in the power/ground planes can cause impedance discontinuities in nearby signals. Keep vias away from other traces.
- Keep signal traces away from other signals, which might capacitively couple noise into the signals. A good rule of thumb is to keep the traces apart by ten times the width of the trace.
- Do not route digital signals from other circuits across the area of the high-speed transmitter and receiver signals.
- Using grounded guard traces is typically not effective for improving signal quality. A ground plane is more effective. However, a common use of guard traces is to route them during the layout, but remove them prior to design completion. This has the benefit of enforcing keep-out areas around sensitive high-speed signals so that vias and other traces are not accidentally placed incorrectly.
- When signals in a differential pair are mismatched, the result is a common-mode current. In a well-designed system, common-mode currents should make up less than one percent of the total differential currents. Mode currents represent a primary source of EMI emissions. To reduce common-mode currents, route differential traces so that their lengths are the same. For example, a 5-mm (0.2-inch) length mismatch between differential signals having the rise and fall times of 200 ps results in the common-mode current being up to 18% of the differential current.

Notes

Due to the high application frequency, you must be careful to choose proper components (such as the termination resistors) in the designing of the layout of a

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printed circuit board. The use of surface-mount components is highly recommended to minimize parasitic inductance and lead length of the termination resistor.

Matching the impedance of the PCB traces, connectors, and balanced interconnect media is highly recommended. Impedance variations along the entire interconnect path must be minimized because they degrade the signal path and may cause reflections of the signal.

10.4.2 SGMII Interface

The SGMII interface consists of a Tx and Rx differential pair operating at 1250 Mbps.

The SGMII signals can be routed on any PCB trace layer with the following constraints:

- The Tx output signals in a pair should have matched electrical lengths.
- The Rx input signals in a pair should have matched electrical lengths.
- SGMII Tx and Rx pairs have to be routed as 100 Ω differential traces with ground plane as reference.
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities.
- AC-coupling of Tx and Rx may be needed depending on the PHY. If AC-coupled, the inputs are self-biased.
- To reduce the crosstalk between pairs or other PCB lines, it is recommended that the spacing on each side of the pair be larger than 4 times the track width.

10.4.3 Parallel Interface

This section applies when the parallel interface is enabled.

The parallel interface (PI) consists of PI_Addr[16:0], PI_Data[15:0], PI_nCS, PI_nDone, PI_nOE, PI_nWR, and PI_IRQ_[1,0]. If this interface is not used, all signals can be left floating.

When using the parallel interface, the timing parameter $t_{D(SLNH)}$ indicates when an issued command is sampled by the VSC7462. For more information about the $t_{D(SLNH)}$ timing parameter, see Table 285, page 226.

To ensure that the PI_nDone signal is driven inactive properly, add a 4.7-kΩ pull-up resistor to this signal, when used.

10.4.4 Serial Interface

If the serial CPU interface is not used, all input signals can be left floating.

The SI bus consists of the SI_Clk clock signal, the SI_DO and SI_DI data signals, and the SI_nCS0 device select signal.

When routing the SI_Clk signal, be sure to create clean edges. If the SI bus is connected to more than one slave device, it should be routed in a daisy chain

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configuration with no stubs. The SI_Clk signal should be terminated correctly to avoid reflections and double clocking.

If it is not possible (or desirable) to route the bus in a daisy chain configuration, the SI_Clk signal should be buffered and routed in a star topology from the buffers. Each buffered clock should be terminated at its source.

10.4.5 XAUI Interface

The XAUI interface can be used for fiber connections, backplanes, or direct coupler cable connections, such as the CX4 cable.

The XAUI interface can operate in several modes. The physical signal bit rate is between 125 Mbps to 6.25 Mbps.

The inputs are self-biased and have internal AC-coupling. In some modes, the interface requires external AC-coupling, because of the input DC voltage limitation. If external AC-coupling capacitors are required, it is recommended to use small form factor components, such as 0603. The small form factor minimizes impedance mismatch by the AC-coupling capacitors, because the size of the form factor approximately matches the trace width commonly used for these signals.

The XAUI interface can be directly connected to either 1 Gbps or 2.5 Gbps SFP modules. For these applications, external AC-coupling capacitors are not required, because the SFP module already includes capacitors.

The following table shows the AC-coupling requirements for common XAUI connections.

Table 316. XAUI Interface Coupling Requirements

XAUI Connection	Mode	External AC-Coupling Requirement
SFP modules	SFP	Not required
CX4 connector	CX4	Required
SGMII PHY	SGMII	Required(1)
XAUI device	XAUI	Required
Jaguar devices	CEI-6G-SR	Not required
XENPAK, XPAK, X2 fibre modules	XAUI	Not required(2)

1. AC-coupling is not required with direct connection to the VSC8512 PHY device.
2. AC-coupling is included.

The XAUI interface signals must be routed as a differential pair with a 100 Ω differential characteristic impedance. The differential intra-pair skew must be below 5 ps in the PCB trace.

To minimize crosstalk between transmitter and receiver, equal drive strength is recommended in both devices in a link.

To minimize crosstalk between differential pairs, the characteristic differential impedance of the signals must be determined only by the distance to the reference plane and the intra-pair coupling and not the distance to the neighboring traces. To separate the transmitter and receiver signals to minimize crosstalk, it is recommended to route the transmitter and receiver signals on as many different PCB layers as feasible.

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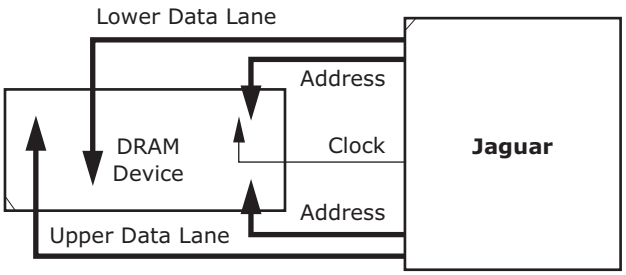
10.4.6 DDR2 SDRAM Interface

The DDR2 SDRAM interface is designed to interface direct with a single 16-bit DDR SDRAM device. The maximum supported density is 256 Mbyte (2 Gbps).

All signals on this interface must be connected one-to-one with the corresponding signals on the DDR SDRAM device. If the memory size of the DDR SDRAM is smaller than maximum, then the upper part of the address and bank address signals can be left unconnected. All 16 data bits must be used.

The placement of the VSC7462 DDR2 interface signals is optimized for point-to-point routing directly to a single DDR SDRAM device.

Figure 88. DDR2 SDRAM Point-to-Point Routing



Because reflections are absorbed by the driver, keep the physical distance of all the SDRAM interface signals below 1 ns to omit any external discrete termination on the address, command, control and clock lines.

When routing the DDR2 interface, attention must be paid to the skew, primary concern is skew within the byte lane between the differential strobe and the single-ended signals. Skew recommendations for the DDR2 interface are listed in the following table.

Table 317. Recommended Skew Budget

Description	Signal	Maximum Skew
Skew within byte lane 0	DDR_LDQS/DDR_LDQSn	50 ps
Skew within byte lane 1		50 ps
Skew within address, command, and control bus	DDR_CK/DDR_CKn DDR_nRAS DDR_Cke DDR_ODT DDR_nCAS DDR_nWE DDR_BA[2:0] DDR_A[13:0]	100 ps
Skew between control bus clock and byte lane clock	DDR_CK/DDR_CKn DDR_LQDS/DDR_LDQSn DDR_UDQS/DDR_UDQSn	1250 ps
Byte lane0 differential clock intra-pair skew	DDR_LDQS/DDR_LDQSn	5 ps
Byte lane1 differential clock intra-pair skew	DDR_UDQS/DDR_UDQSn	5 ps
Control bus differential clock intra-pair skew	DDR_CK/DDR_CKn	5 ps

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- Use a shared voltage reference between the VSC7462 device's DDR_Vref supply and the DDR device's reference voltage.
- Generate the DDR_Vref from the V_{DD_IODDR} supply using a resistor divider with value of 1 kΩ and an accuracy of 1% or better.
- Use a decoupling capacitance of at least 0.1 µF on the supply in a manner similar to V_{DD_IODDR} and V_{SS} to ensure tracking of supply variations; however, the time constant of the resistor divider and decoupling capacitance should not exceed the nReset assertion time after power on.

Recommend routing:

- DDR_Ck/DDR_Ckn must be routed as a differential pair with a 100 Ω differential characteristic impedance.
- DDR_LDQS/DDR_LDQSn must be routed as a differential pair with a 100 Ω differential characteristic impedance.
- DDR_UDQS/DDR_UDQSn must be routed as a differential pair with a 100 Ω differential characteristic impedance.
- To minimize crosstalk, the characteristic impedance of the single-ended signals should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces.
- The crosstalk should be below –20 dB.

10.4.7 Thermal Diode External Connection

The internal on-die thermal diode can be used with an external temperature monitor to easily and accurately measure the VSC7462 junction temperature.

The on-die thermal diode has internal connected the diode cathode to V_{SS}, the external temperature sensor must support the thermal diode cathode connected to V_{SS}.

Thermal diode is extremely sensitive to noise. To minimize the temperature measurement errors, follow these guidelines:

- Route the ThermDC and ThermDA signals as a differential pair with a differential impedance less than 100 Ω.
- Place the external temperature monitor as close as is possible to the VSC7462 device.
- Add a 47 Ω resistor in series with the external temperature monitor supply to filter noise.
- Place a de-coupling capacitor between the external temperature monitor supply pin and the ThermDC signal. Place the capacitor close to the external temperature sensor, as shown in the following illustration.
- Connect the external temperature monitor V_{SS} pin directly to the ThermDC pin, which has the connection to V_{SS}, as shown in the following illustration. Do not connect the external temperature monitor V_{SS} pin to the global V_{SS} plane.

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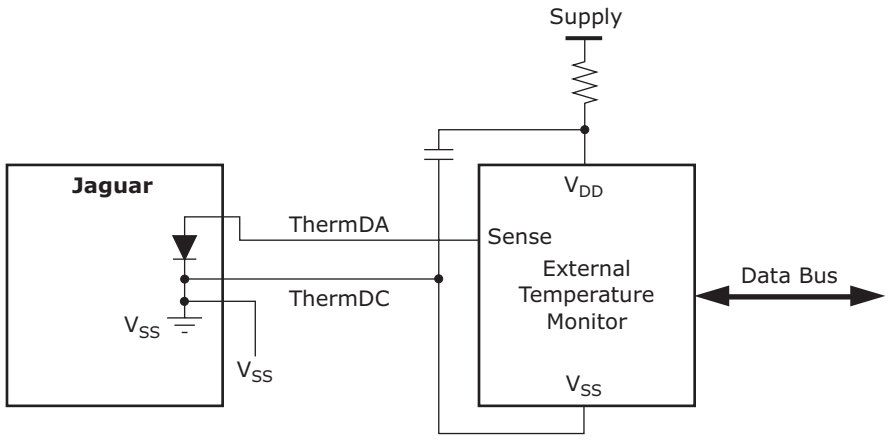
Figure 89. External Temperature Monitor Connection



10.4.8 Core Sense

The core_sense signal is internally connected to the V_{DD} net. The core_sense signal can be used to verify PCB power plane voltage drop in the 1.0 V supply.

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11 Ordering Information

The package is a 672-pin, thermally enhanced flip chip ball grid array (FCBGA) with a 27 mm × 27 mm size, 1 mm pitch, and 2.74 mm maximum height. The devices are also available a lead(Pb)-free package (second-level interconnect only).

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information.

Table 318. Ordering Information

Part Order Number	Description
VSC7462IH-01	672-pin, thermally enhanced flip chip ball grid array (FCBGA) with a 27 mm × 27 mm body size, 1.00 mm pin pitch, and 2.74 mm maximum height
VSC7462XIH-01	Lead(Pb)-free (second-level interconnect only), thermally enhanced 672-pin, flip chip ball grid array (FCBGA) with a 27 mm × 27 mm body size, 1.00 mm pin pitch, and 2.74 mm maximum height

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