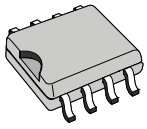
L6615

High/low-side load share controller

Datasheet - production data



SO8

Features

- Compliant with SSI specifications
- High/low-side current sensing
- Fully compatible with remote output voltage sensing
- Full differential low offset current sense
- 2.7 V to 22 V V_{CC} operating range
- 32 kΩ share sense amplifier input impedance
- Hysteretic UVLO

Applications

- Distributed power systems
- High density DC-DC converters
- (N+1) redundant systems, N up to 20
- SMPS for (web) servers

Description

This controller IC is specifically designed to achieve load sharing of paralleled and independent power supply modules in distributed power systems, by adding only few external components. Current sharing is achieved through a single wire connection (share bus) common to the paralleled modules. Load sharing is a technique used in all systems in which the load requires low voltage, high-current and/or redundancy: for this reason a modular power system with two or more power supplies or DC-DC converters in parallel is required. The device performs both high-side and low-side current sensing, in this manner the sense current resistor can be placed either in series to the power supply output or on the ground return. The L6615 drives the share bus to a voltage proportional to the output current of the master, which is the highest among the output currents delivered by the paralleled power supplies. The share bus dynamics is independent from the power supply output voltage and is clamped by the device supply voltage (V_{CC}) only. The output voltage of the other paralleled power supplies (slaves) is trimmed by the ADJ pin so that they can support their amount of load current. The slave power supplies work as current-controlled sources. Thanks to the sharing of the output currents, the thermal stress of the different modules can be equalized and provides more reliability. Moreover, the paralleled supply architecture allows redundancy to be achieved. The failure of one of the modules can be tolerated until the capability of the remaining power supplies is enough to provide the required load current.

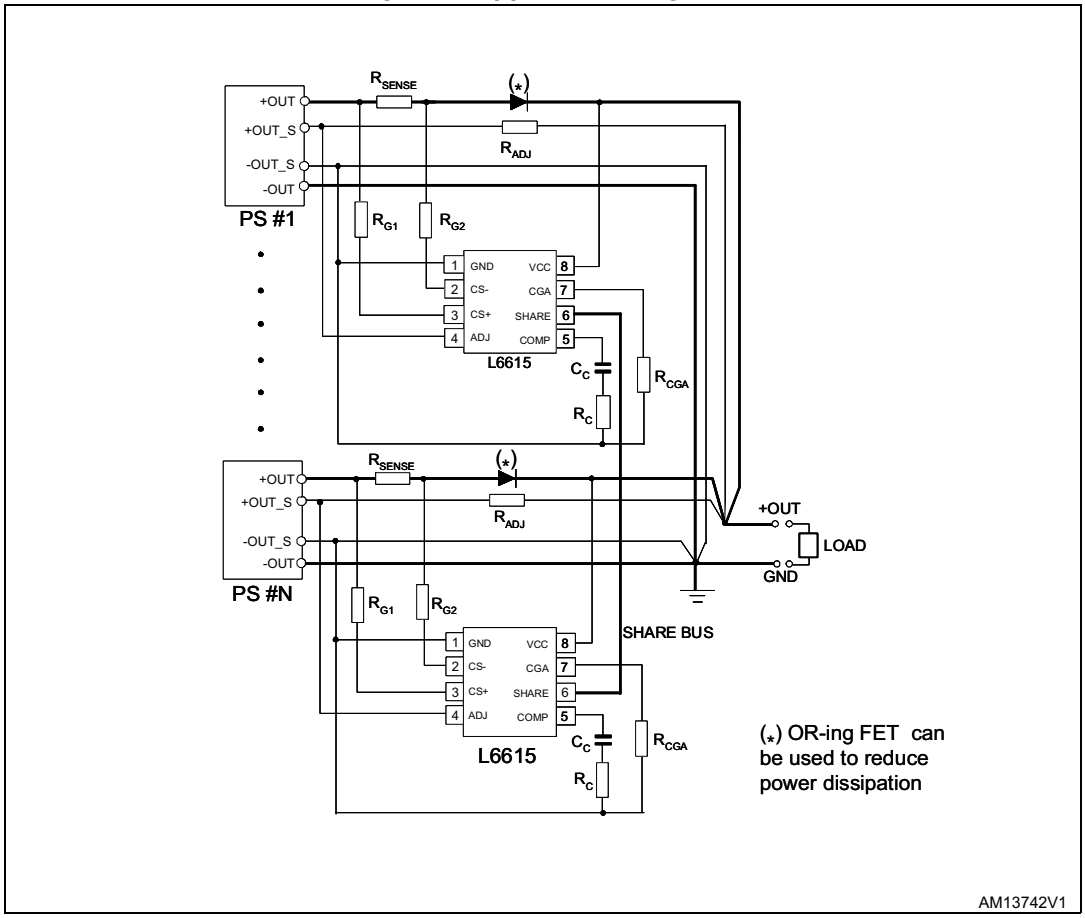
Table 1. Device summary

Order code	Package	Packaging
L6615D	SO8	Tube
L6615D013TR		Tape and reel

Contents

1 Typical application diagram

Figure 1. Application diagram



2 Pin connection

Figure 2. Pin connection (top view)

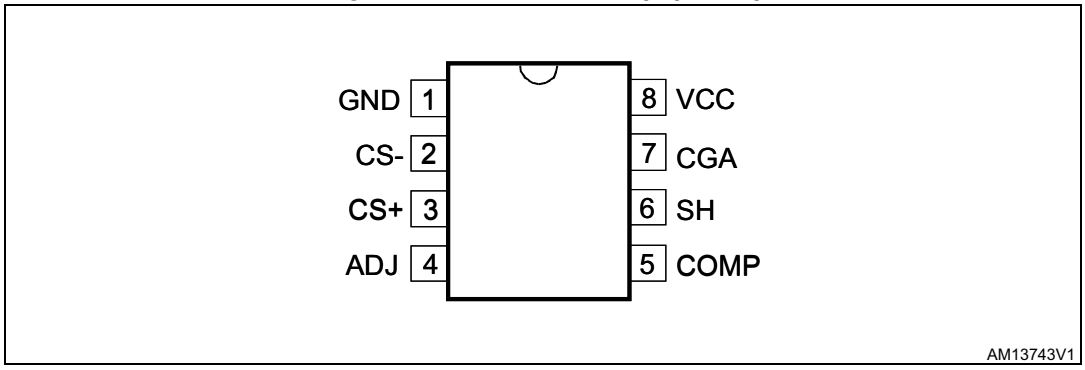


Table 2. Pin description

N.	Pin	Function
1	GND	Ground.
2	CS-	Input of current sense amplifier; it is connected to the negative side of the sense resistor through a resistor (R_{G2}).
3	CS+	Input of current sense amplifier. A resistor R_{G1}, with the same value as R_{G2}, is placed between this pin and the positive side of the sense resistor: its value defines the transconductance gain between I_{CGA} and V_{SENSE}.
4	ADJ	Output of adjust amplifier; it is connected to both the loads (through a resistor R_{ADJ}) and to the positive remote sense pin of the power system. This pin is an open collector diverting (from the feedback path) a current proportional to the difference between the current supplied to the load by the relevant power supply and the current supplied by the master.
5	COMP	Output of the current sharing (transconductance) error amplifier and input of ADJ amplifier. Typically, a compensation network is placed between this pin and ground. The maximum voltage is internally clamped to 1.5 V (typ.).
6	SH	Share bus pin. During the power supply slave operation, this pin acts as positive input from share bus. During the power supply master operation, it drives the share bus to a voltage proportional to the load current. The share bus connects the SH pins of all the paralleled modules. A capacitor between this pin and GND could be useful to reduce the noise present on the share bus.
7	CGA	Current gain adjust pin; current sense amplifier output. A resistor connected between this pin and ground defines the maximum voltage on the share bus and sets the gain of the current sharing system.
8	VCC	Supply voltage of the IC.

3 Electrical data

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	Supply voltage(1) (I_{CC} < 50 mA)	Self limited	V
I_{CS+}, I_{CS-}		Sense pin current	10	mA
V_{CS-}, V_{CS+}, V_{SH}, V_{ADJ}, V_{CGA}	2, 3, 6, 4, 7		-0.3 to V_{CC}	V
V_{COMP}	5	Error amplifier output	-0.3 to 1.5	V
(V_{CS+}) - (V_{CS-})		Differential input voltage (V_{CS+} from 0 V to 22 V)	-0.7 to 0.7	V
P_{tot}		Total power dissipation @ T_{amb} = 70 °C SO8	0.45	W
T_j		Junction temperature range	-40 to +125	°C
T_{stg}		Storage temperature	-55 to +150	°C

1. Maximum package power dissipation limits must be observed.

Note: All voltages are referred to pin1. Current is positive when it is in the specified terminal, it is negative when it is out of it.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	SO8	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction-to-ambient	120	°C/W

4 Electrical characteristics

(T_j = - 40 to 85 °C, V_{cc} = 12 V, V_{ADJ} = 12 V, C_{COMP} = 5 nF to GND, R_{CGA} = 16 kΩ, unless otherwise specified; $V_{SENSE} = I_L * R_{SENSE}$, $R_{G1} = R_{G2}$ = 200 Ω)

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{cc}						
V_{cc}	Operating range		2.7		22	V
I_{cc}	Quiescent current	V_{SH} = 1 V, V_{SENSE} = 0 V		5	6	mA
$V_{CC, ON}$	Turn-on voltage	V_{SH} = 0.2 V, V_{SENSE} = 0 V	2.45	2.60	2.75	V
$V_{CC,OFF}$	Turn-off voltage		2.35	2.5	2.65	V
V_H	Hysteresis			100		mV
V_z		I_{CC} = 20 mA	24	26		V
Current sense amplifier						
V_{OS}	Input offset voltage	0.1 V ≤ V_{SH} ≤ 10.0 V	-2	0.0	2	mV
V_{CGA}	Out high voltage	V_{SENSE} = 0.25 V	V_{CC-} 2.2			V
I_{CGAS}	Short-circuit current	V_{CGA} = 0 V, V_{SENSE} = 0.45 V	-1.5	-2.0		mV
$I_{B(CS-)}$	Input bias current (high-side sensing)	V_{SENSE} = 0 V, V_{CS+} = +12 V			1.0	µA
$I_{B(CS+)}$	Input bias current (low-side sensing)	V_{SENSE} = 0 V, V_{CS+}= 0 V			-1.0	µA
CMR	Common mode dynamics range	V_{CS-}, V_{CS+}	0		V_{CC}	V
VTH_{CS+}	Switchover threshold low-side to high-side sensing	V_{CS+}		1.6		V
SW_H	Switchover hysteresis			0.16		V
Share drive amplifier						
HV_{SH}	SH high output voltage	V_{SENSE} = 250 mV, I_{SH} = -1 mA	V_{cc-} 2.2			V
LV_{SH}	SH low output voltage	V_{CGA} = 0 mV, R_{SH} = 200 Ω			45	mV
(+)	High-side sensing mirror accuracy(1)			±1	±5	%
(-)	Low-side sensing mirror accuracy(1)			±1	±5	%

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SH}, I_{oad}	Load regulation	-1.0 mA ≤ ISDA(OUT) ≤ -4 mA			20	mV
I_{SC}	Short-circuit current	V_{SH} = 0 V, V_{SENSE} = 25 mV	-20	-13.5	-8	mA
SR	Slew rate	V_{SENSE} = -10 mV to 90 mV step, R_{SH} = 200 to GND	0.8	1.5	2.2	V/µs
		V_{SENSE} = 90 mV to -10 mV step, R_{SH} = 200 to GND	2	3	4	V/µs
Share sense amplifier						
R_i	Input impedance		22.4	32	41.6	KΩ
Error amplifier						
G_m	Transconductance		3	4	5	ms
V_{os}	Input offset voltage	V_{CGA} = 1 V	30	50	70	mV
I_{OH}	Source current	V_{COMP} = 1.5 V, V_{SH} ≥ 300 mV, V_{SENSE} = -10 mV	-150	-350	-400	µA
I_{OL}	Sink current	V_{COMP} = 1.5 V, V_{SENSE} = -10 mV 200 Ω resistor SH to GND	100	200	300	µA
$V_{COMP(L)}$	Low voltage		0.05	0.15	0.25	V
V_Z	Clamp Zener voltage	I_Z = 1 mA		1.5		V
ADJ amplifier						
I_{ADJ}	ADJ output current	V_{SH} = 1 V, V_{SENSE} = 0 V	6.5	10	13	mA
V_T	Threshold voltage	I_{ADJ} = 10 A		0.7		V
R_A	Emitter resistor	Guaranteed by design	60	100	140	Ω
$V_{ADJ(MIN)}$	Low saturation voltage	I_{ADJ} = 5 mA			1	V
		I_{ADJ} = 1 mA			0.4	V

1. Mirror accuracy is defined as follows (see *Equation 1*), and it represents the accuracy of the transfer between the voltage sensed and the voltage imposed on the share bus.

Equation 1

$$\left[\frac{V_{SH}}{V_{SENSE}\cdot\frac{R_{CGA}}{R_G}}-1\right]\cdot 100$$

Figure 3. Block diagram

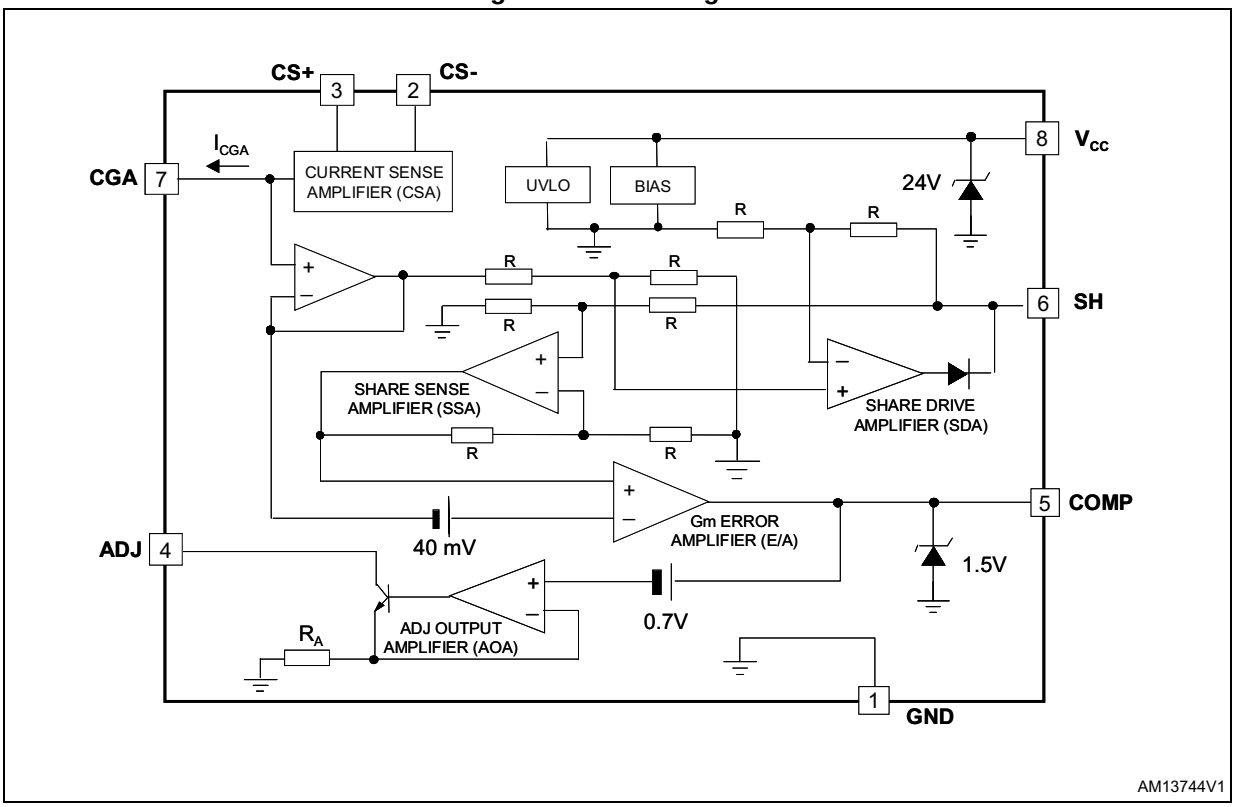


Figure 4. Turn-on and turn-off voltage

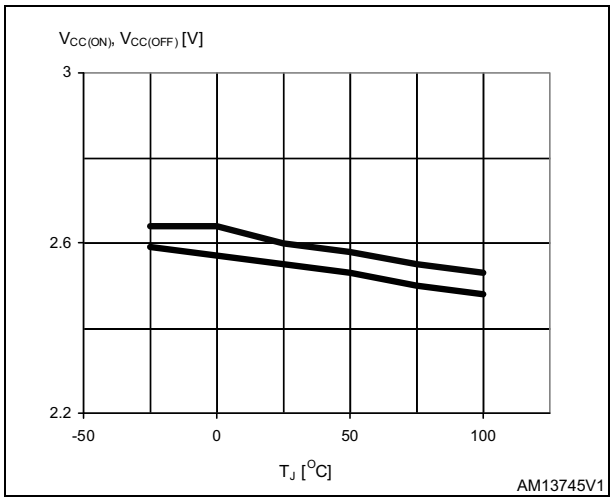


Figure 5. Max. CGA current

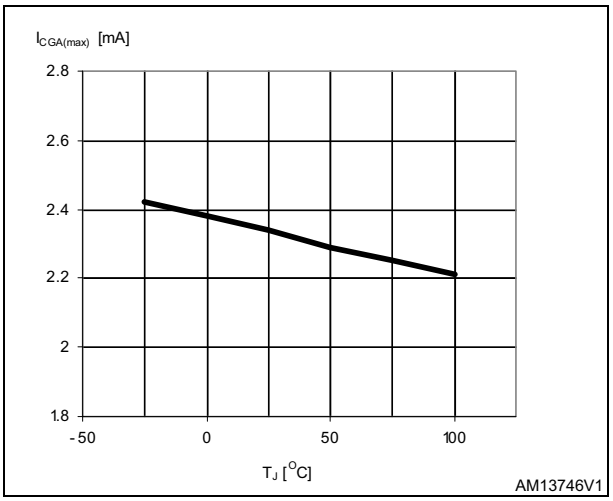


Figure 6. Supply current vs. supply voltage

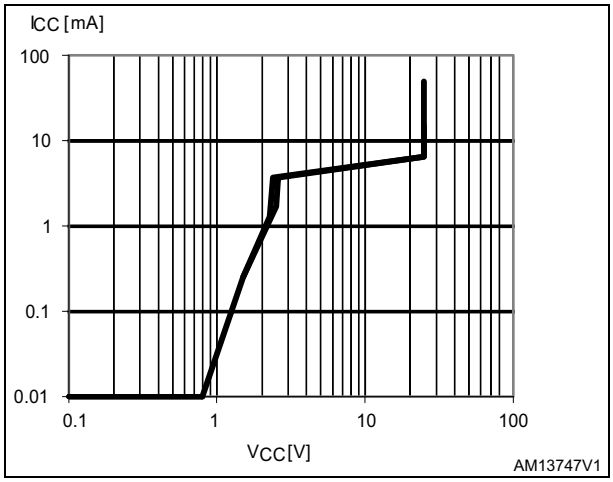


Figure 7. High-side/low-side sensing switchover threshold

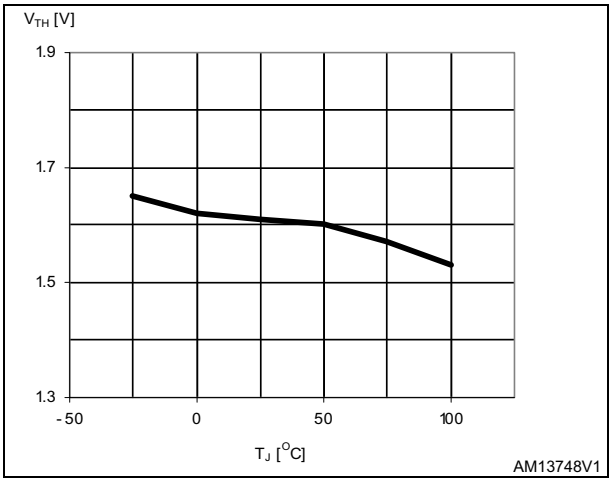


Figure 8. Supply current

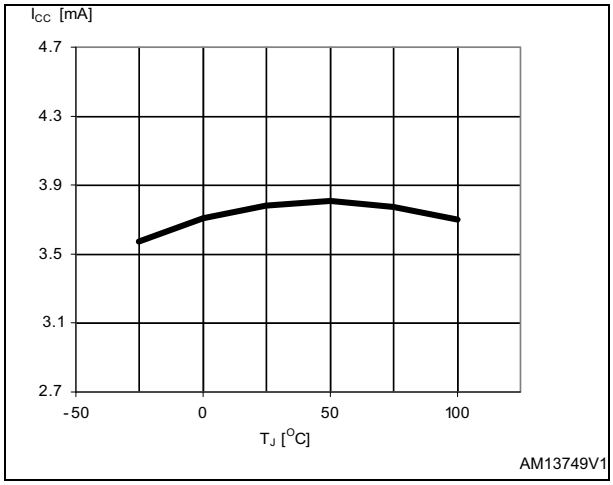


Figure 9. Max. share bus voltage at no load

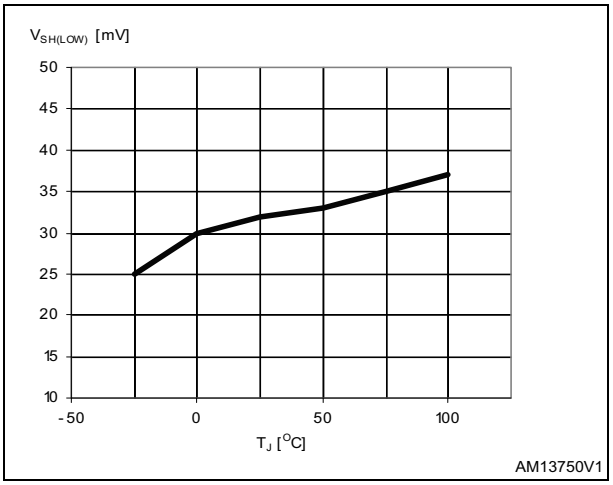


Figure 10. Share bus input impedance

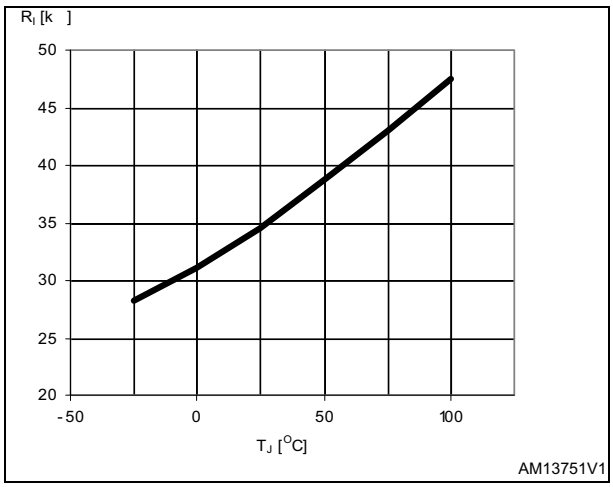
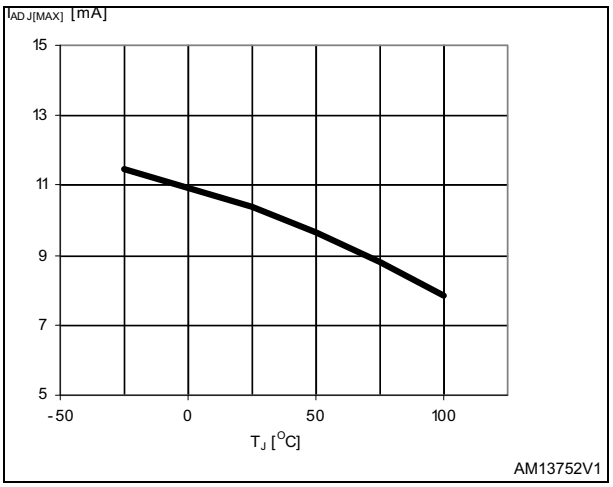


Figure 11. ADJ maximum current



5 Application information

The power supply systems are often designed by converters in parallel so to improve the performance and reliability.

To ensure a uniform distribution of stresses, the total load current should be shared appropriately among the converters.

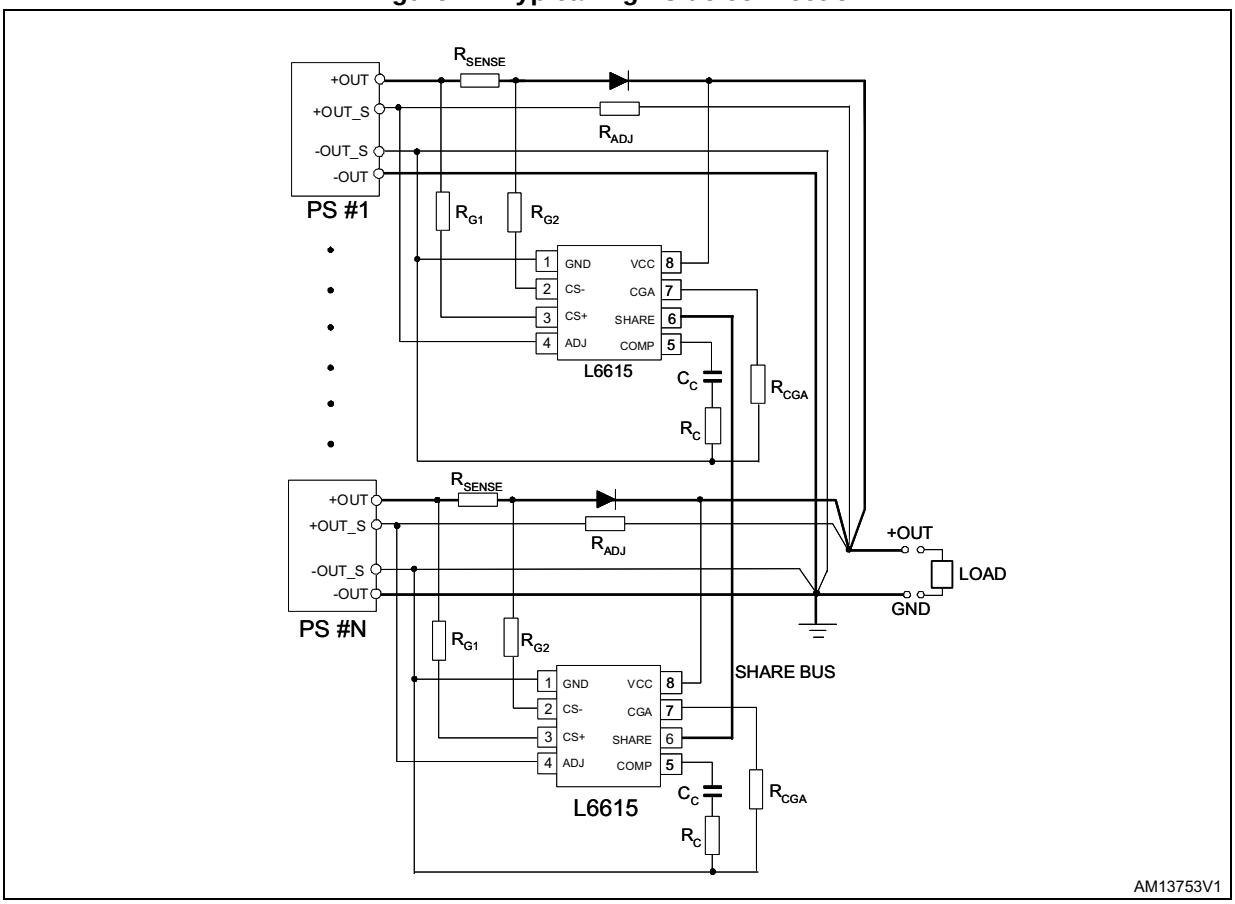
A typical application, relative to a series of N paralleled modules (PS#1 to PS#N), is showed in *Figure 12*. Each of them exhibits 4 terminals: two about the power outputs (+OUT, -OUT) and two about the remote sense signals (+OUT_S, -OUT_S).

The sense resistors R_{SENSE} (for the current sensing) and the OR-ing diodes (to avoid that the failure of one module shorts the load out) are placed on the power lines.

The L6615 allows an automatic master-slave current sharing architecture to be attained: one L6615 is associated to each power supply and all the ICs are linked each other through the share bus (referred to the common ground). This kind of system configuration is preferred to the systems in which a single current sharing controller is used, because of its robustness, reliability and flexibility.

To configure a load share controller, few passive components are used. A brief device explanation, together with the formulas useful to set these external components, follows.

Figure 12. Typical high-side connection



5.1 Current sense section

A sense resistor is typically used to generate the voltage drop, proportional to the load current, measured by the CSA (current sense amplifier), whose input pins (pins #2 and #3) are connected to R_{SENSE} through two identical resistors (RG1 and RG2) (see *Figure 12*).

The CSA consists of 2 sections (see *Figure 13* and *14*), one responsible for the high-side sensing, the other for low-side sensing. An internal comparator activates the relevant section in accordance with the voltage present at CS+ pin: if this voltage is higher than 1.6 V (typ.), the high-side sensing section is activated (*Figure 13*) otherwise the low-side sensing is activated (*Figure 14*). RG1= RG2= RG are considered for simplicity.

As the voltage drop I_{OUT}*R_{SENSE} is present at the input of the sense amplifier section, its output forces the controlled current mirror to:

- sink current from the CS+ pin in case of high-side sensing (neglecting input bias current, no current flows through CS- pin);

- source current from the CS- pin in case of low-side sensing (neglecting input bias current, no current flows through CS- pin).

The local feedback imposes the same voltage at the current sense input pins, so under closed loop condition $V_{SENSE} = V_{RG}$. The current I_{CS}

Equation 1

$$I_{CS} = \frac{I_{OUT} \cdot R_{SENSE}}{R_G}$$

(IC_{S+} in case of high-side, I_{CS-} in case of low-side) is then internally mirrored and sent to the CGA pin causing a drop across the R_{CGA} external resistor. Two internal buffers transfer V_{CGA} signal to the share pin so:

Equation 2

$$V_{SH} = \frac{V_{SNS}}{R_G} \cdot R_{CGA}$$

Only the L6615 V_{CC} limits the upper voltage at the CGA and SH pin, regardless the voltage present at the current sense pins.

In noisy applications, two capacitors of small value (e.g. 1 nF) connected between current sense pins and ground could be useful to clean the signal at the input of the current sense amplifier.

For low voltage buses see, *Section 5.6: Low voltage buses*.

Figure 13. Current sense (high-side)

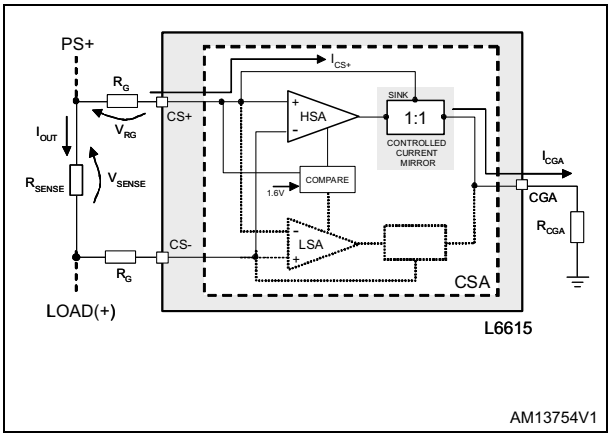
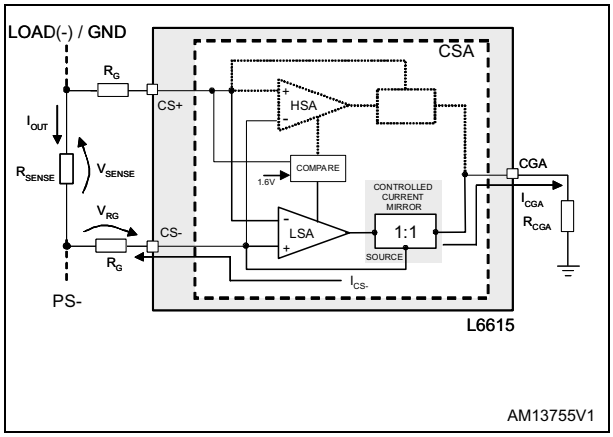


Figure 14. Current sense (low-side)



5.2 Share drive amplifier (SDA), error amplifier and adjustable amplifier

The gain between the output of CSA (CGA pin) and output of SDA (SH pin) is 1 (typ.) so, with regard to the master power supply, $V_{CGA} = V_{SH}$, the voltage on the share bus is imposed by the master.

In the slave converters, being $V_{CGA(SLAVE)} < V_{CGA(MASTER)}$, the diode at the output of SDA (see block diagram) isolates the output of this amplifier from the share bus.

The share sense amplifier (SSA) reads the bus voltage transferring the signal to the non-inverting input of the error amplifier where it is compared with CGA voltage.

Whenever a controller acts as the master in the system, the voltage difference between the E/A inputs is zero. In this condition, to guarantee a low output, a 40 mV offset, in series with the inverting input, is inserted.

Instead in the slave converters, the input voltage difference is proportional to the difference between the master load current and the relevant slave load current.

The transconductance E/A converts the ΔV at its inputs in a current equal to

Equation 3

$$I_{OUT} = G_M \cdot \Delta V$$

I_{OUT} flows through the compensation network connected between COMP pin and ground.

The E/A output voltage drives the adjustable amplifier to sink current from the ADJ pin, which is in turn connected to the output voltage through a small resistor along the sense path. The current, sunk by ADJ pin, is deviated from feedback path of the slave power supply, causing an increase of its duty cycle.

In steady-state the current, sunk by the ADJ pin, is proportional to the value of the error amplifier output.

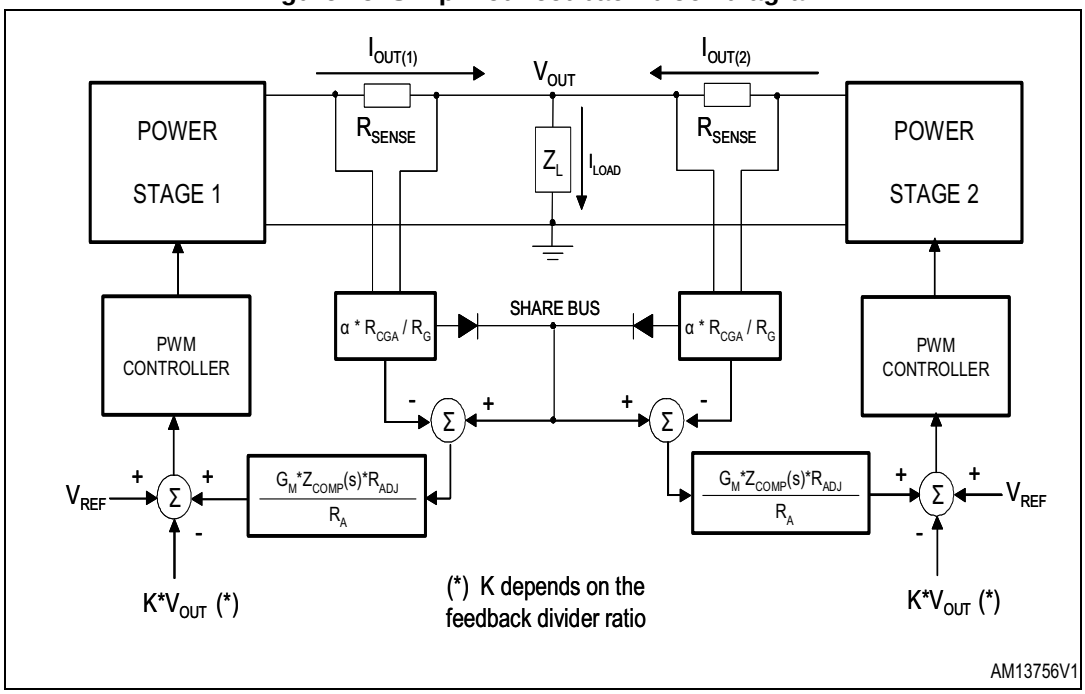
5.3 Designing with the L6615

The first design step is usually the choice of the sense resistor whose maximum value is limited by the power dissipation; this constraint must be traded-off against the precision of the L6615 current sensing. In fact, a small sense resistance value lowers the power dissipation but reduces the signal available at the inputs of the L6615 current sense amplifier.

Once R_{SENSE} is fixed then the R_G and R_{GCA} values are chosen in accordance with the application specifications: usually these specs define the share bus voltage ($V_{SH(MAX)}$) and the number of paralleled power supplies.

Their value must comply with the constraints imposed by the L6615:

Figure 15. Simplified feedback block diagram



– maximum share bus voltage is internally limited up to 2.2 V below the L6615 V_{CC} voltage (pin#8);

– $V_{SH(MAX)}$ represents an upper limit but the designer should select the full scale share bus voltage keeping in mind that each Volt on the share bus increases the master controller's supply current by approximately 45 µA for each slave unit connected in parallel; this total current, provided by the master share drive amplifier, must be lower than its minimum output capability (8 mA) so:

Equation 4

$$V_{SH(MAX)} < \frac{R_{i(MIN)}}{N} \cdot 8mA$$

This condition isn't met in normal applications, as the user can easily see by using sensible values for N (number of paralleled power supplies) and $V_{SH(MAX)}$. For example, $V_{SH(MAX)}$ = 8 V, solving for N, N_{MAX} = 20 is obtained;

- maximum share drive amplifier current capability ($I_{CGA(MAX)}$ = 2 mA);
- for safety reasons the following relation must be met:

Equation 5

$$R_G > \frac{1}{2} \cdot \left(\frac{V_{OUT}}{10mA} - 40 \right)$$

in this way no fault causes I_{CS+} (or I_{CS-}) to overcome its absolute maximum ratings.

At full load, $\Delta V_{SENSE(MAX)} = I_{OUT(MAX)} \cdot R_{SENSE(MAX)}$ is the maximum voltage drop across the resistor R_{SENSE} (typically few hundreds mV).

$I_{OUT(MAX)}$ is the maximum current carried by each of the paralleled power supplies; in non-redundant systems composed by N power supplies, each of them works at its nominal current, so:

Equation 6

$$I_{OUT(MAX)} = \frac{I_{LOAD}}{N}$$

This relationship is also true in N+M redundant system, even if in normal conditions each power supply provides $I_{LOAD}/(N+M)$.

For example, in a system composed by two paralleled power supplies 100% redundant (N=M=1), each module is sized to sustain the entire load current (in normal operation it carries one half only): for this reason, the sense resistor must be sized considering the whole load current.

The temperature variation of the sense resistor (hence its resistance value) has to be taken into account, so $R_{SENSE(MAX)}$ is the value at maximum operating temperature to avoid saturating the share bus. Once $V_{SENSE(MAX)}$ is fixed, the ratio R_{CGA}/R_G (gain from the sensing section to the share bus) can be calculated:

Equation 7

$$\frac{R_{CGA}}{R_G} = \frac{V_{SH(MAX)}}{V_{SENSE(MAX)}}$$

where $V_{SH(MAX)}$ is defined by the application. A small capacitor in parallel to R_{CGA} is useful to reduce the noise.

The effect of current sharing feedback loop is to force the voltages of the slave CGA pins to be equal to V_{SH} (that is to reduce the voltage difference at the inputs of the L6615 error amplifier). To simplify, 2 paralleled power supplies, under a closed loop condition(*Figure 15*), are considered:

Equation 8

$$I_{OUT(1)} \cdot \frac{R_{SNS(1)}}{R_{G(1)}} \cdot R_{CGA(1)} = I_{OUT(2)} \cdot \frac{R_{SNS(2)}}{R_{G(2)}} \cdot R_{CGA(2)}$$

Ideally all the external components match so:

Equation 9

$$I_{OUT(1)} = I_{OUT(2)} = \frac{I_{LOAD}}{2}$$

Any mismatch has an impact on the sharing precision: in particular the maximum difference between the output currents (sharing error) is given by the sum of the mismatches among the relevant values.

Figure 16. ADJ network

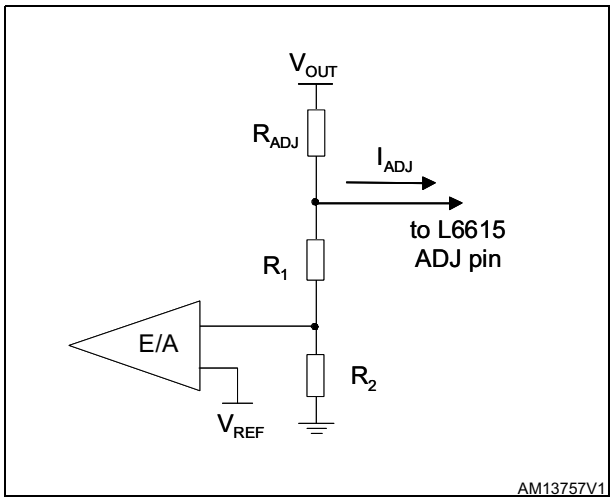
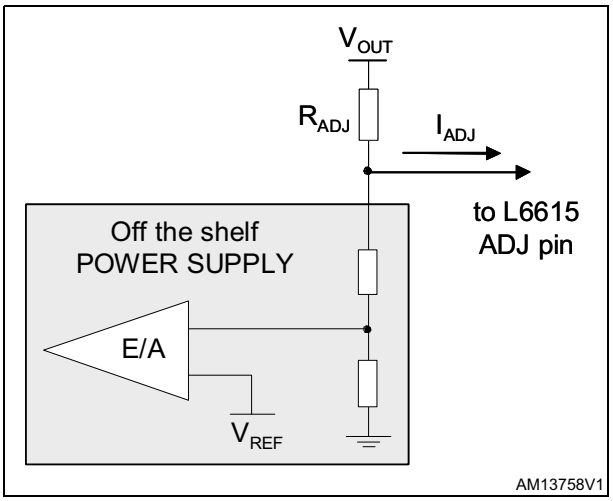


Figure 17. ADJ network for an "off-the-shelf" power supply



The tolerance required by the power supply output voltage ($V_{OUT} \pm V_O$) has to be known in order to set the R_{ADJ} value; the maximum difference between master and slave output voltage is 2* V_O and this amount represents the voltage that the L6615 must be able to correct.

Two different approaches are feasible, depending on whether the SMPS (whose output current must be shared) has to be completely designed or it is an "off-the-shelf" component and the current sharing section must be only designed.

The former: the adjustment resistor (R_{ADJ}) can be considered as a fraction of the high resistor of the feedback divider R_H (*Figure 16*). Typically the first step consists of fixing the current flowing, under steady-state condition, through the feedback divider I_{FB}; by choosing the value for R_2:

Equation 10

$$I_{FB} = \frac{V_{REF}}{R_2}$$

where:

Equation 11

$$R_H = R_1 + R_{ADJ} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R_2$$

R_{ADJ} has to be lower than (or equal to) one tenth of R1, considering that, in the worst conditions, it is:

Equation 12

$$I_{ADJ(max)} = \frac{\Delta V_{OUT}}{R_{ADJ}}$$

This value must not exceed the one indicated in *Section 4: Electrical characteristics*. This is very easy to meet, as the user can easily see by using ΔV_{OUT} and R_2 sensible values.

The latter (*Figure 17*): the feedback divider has already been designed by the SMPS manufacturer and cannot be modified. The R_{ADJ} design lets the L6615 correct the maximum spread without significantly shifting the SMPS regulation point. A minimum R_{ADJ} value can be found by:

Equation 13

$$R_{ADJ(MIN)} = \frac{\Delta V_{OUT}}{I_{ADJ(MAX)}}$$

where $I_{ADJ(MAX)}$ is 8 mA.

The adjustment network saturation must be avoided especially for low voltage output buses; the design must satisfy the following relationship:

Equation 14

$$V_{OUT} - R_{ADJ} \cdot (I_{ADJ} + I_{FB}) > V_{ADJ(MIN)}$$

where $V_{ADJ(MIN)}$ can be found in *Section 4: Electrical characteristics* for different I_{ADJ} values. The last point is the design of the compensation network $Z_{C(s)}$ connected between the COMP pin and ground.

The current sharing system introduces another outer loop besides the power supply feedback loop. To avoid the interaction between them, the bandwidth of the sharing loop has to be designed at least one order of magnitude lower than the bandwidth of the power supply loop. For the total system, the loop gain is:

Equation 15

$$G_{LOOP(s)} = R_{SENSE} \cdot \frac{R_{CGA}}{R_G} \cdot G_M \cdot Z_{C(s)} \cdot \frac{R_{ADJ}}{R_A} \cdot A_{PWR(s)} \cdot \frac{1}{R_{LOAD}}$$

where

- $A_{PWR(s)}$ is the transfer function of PWM controller and power stage (*Figure 15*)
- R_{LOAD} is the equivalent load resistance

Typically the compensation network is built by the R-C series. A resistor in series with C_C is required to boost the phase margin of the load share loop. Zero is placed at the load share loop crossover frequency, $f_{C(SH)}$.

If $f_{C(SH)}$ is the share loop crossover frequency, then:

Equation 16

$$C_C = \frac{1}{2 \cdot \pi \cdot f_{C(SH)}} \cdot \frac{R_{CGA} \cdot G_M}{R_G} \cdot \frac{R_{ADJ}}{R_A} \cdot \frac{R_{SENSE}}{R_{LOAD}} \cdot \left| A_{PWR(f_{C(SH)})} \right|$$

$$R_C = \frac{1}{2 \cdot \pi \cdot f_{C(SH)} \cdot C_C}$$

5.4 Current sense methods

There are several methods to sense the power supply output current; the simplest method is to use a power resistor (*Figure 18* a) but when the load current increases, an expensive resistor could be required to support the inherent power dissipation, imposing the use of several paralleled resistors.

Other methods to sense the output current are showed in *Figure 18* b and *Figure 18* c:

1. **$R_{DS(on)}$**: a power MOS is placed in series to the output and its channel resistance ($R_{DS(on)}$) is used as sense resistor (*Figure 18* b). The L6615 sense pins are connected, through RG resistors, to the drain and to the source of the MOS. Besides, providing the sense resistor, the FET is used as "OR-ing" element: driving properly its gate, the power supply output could be isolated from the load (the body diode is reversed biased so it doesn't conduct). This is useful whenever features as hot-swap or hot-plug are required; compared with the well-known solution using OR-ing diode, the OR-ing FET greatly reduces the power dissipation, in particular:

Equation 17

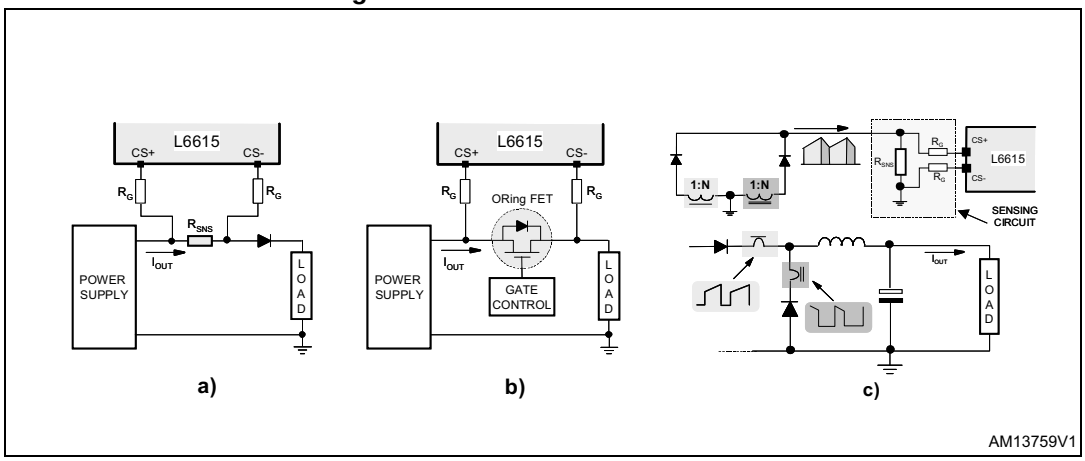
$$P_{(DIODE)} = V_F \cdot I_{OUT} + R_{SENSE} \cdot I_{OUT}^2$$

$$P_{(MOS)} = R_{DS(ON)} \cdot I_{OUT}^2$$

where V_F is the forward drop across the diode.

2. **Current transformer**: in case of very high load currents, a transformer allows a smaller current, obtained through a scaling factor equal to the transformer turn ratio, to be sensed. In this way, the sense resistor power dissipation requirements can be less tight: the drawback is the additional cost of the transformer. In *Figure 18* c, the simplified output stage of a power supply in forward configuration is showed: through two current transformers, the load current is reproduced in the sensing circuit scaled by a factor N. R_{SENSE} reads a ripple (at the switching frequency) superimposed on the average current value. This ripple doesn't affect the correct behavior of the current sharing system because its loop gain is designed with a low bandwidth (at least 2 orders of magnitude lower than the switching frequency), which cuts this high frequency.

Figure 18. Current sense methods



5.5 Application ideas

Figure 19 shows a single section of a system in which DC-DC modules are in parallel. This solution can be used whenever the load requires high-current at low voltage; the converter is designed for a step down configuration using a synchronous rectification controller (for example the L6910 [1] or the L6911 [2] ST device).

The L6615 reads the drop across the $R_{DS(on)}$ of the OR-ing FET and the LM293 drives its gate, pulling it down whenever a fault condition (e.g. short on the low-side) appears.

A charge pump could be necessary to be sure that the OR-ing FET V_{GS} is higher than $V_{GS(TH)}$ (depending on the input and output voltage).

Figure 19. 0.9 to 5 V DC-DC converter with current sharing and hot-plug output

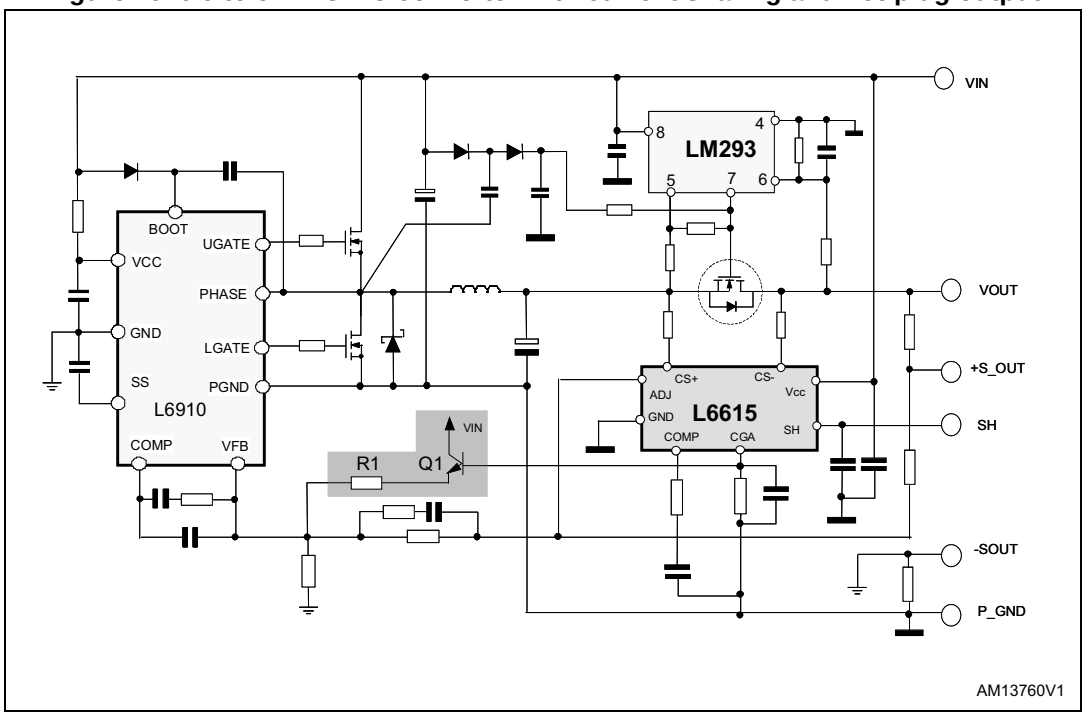
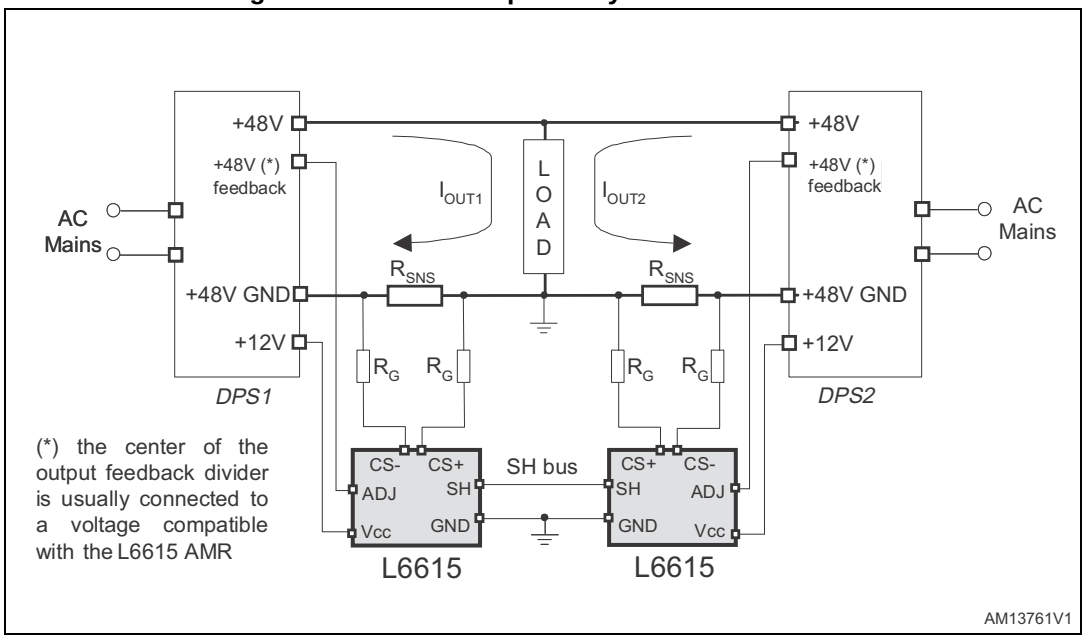


Figure 20. Distributed power system for +48 V bus



In this application, a circuit is inserted to protect the square current limit in case of overcurrent (R1- Q1). The voltage on CGA pin is directly proportional to the current carried by the relevant section, therefore the CGA resistor can be set to keep the CGA voltage lower than V_{REF}+0.7 as long as the output current is in the right range. As soon as this value is overcome, the bipolar pushes current in the feedback path, reducing the duty cycle and the output voltage accordingly.

Current sharing can be required in AC-DC applications like distributed power system (DPS) for telecom applications. If the output voltage is higher than the absolute maximum ratings of the current sense pins (CS+ and CS-), high-side sensing can not be performed unless adding other components; the current sense is performed on the ground return.

To maintain high-side sensing, two resistor dividers (between the edge of R_{SENSE} and ground) could be introduced to translate the sense signal into the L6615 input pin common mode range.

In *Figure 15* and *Figure 20* two AC-DC converters supply the same load through a +48 V bus; these converters usually exhibit also a +12 V auxiliary output useful to supply the L6615 whose ADJ pin works on the +48 V feedback section (COMP pin and CGA pin connections are not showed) in *Figure 20*.

5.6 Low voltage buses

The L6615 has a double sense structure, designed to perform both high-side and low-side sensing: the first solution is usually considered more convenient. Actually, low-side sensing means to split the ground return as many times as the paralleled power supplies are: on each of these paths, the sense resistor has to be placed by introducing a drop between the power supply ground and the common load negative reference.

The voltage at CS+ pin is read by an internal comparator and compared with a reference corresponding to the switchover threshold V_{THcs+} whose value is typically 1.6 V. If such value is overcome, then the comparator triggers the high-side amplifier (HSA); being the

threshold provided by hysteresis, then the low-side amplifier (LSA) is triggered as V_{CS+} is lower than 1.44 V (typ.).

Hence V_{THcs+} defines the threshold between the operating range of LSA, (referring to *Figure 13* and *Figure 14*) and the operating range of HSA. Usually LSA operates when the sense resistor is placed on the ground return, between the negative load terminal and the negative power supply output (*Figure 14*), while the HSA operates when the sense resistor is placed between the power supply positive output and the load.

The high-side sensing can be performed for applications whose output voltage is close to V_{THcs+} threshold (or even lower) exploiting the low sense internal structure (LSA).

For example, an application where V_{OUT} = 1.2 V and the sense resistor placed high-side; the voltage at CS+:

Equation 18

$$V_{CS+} = V_{OUT} - \Delta V_{SENSE}$$

is lower than 1.6 V so the internal comparator triggers on the LSA structure and the pin CS- sources the current I_{CS} (see *Section 5.4: Current sense methods*). The IC works properly because the dynamics of LSA spreads down to zero: in this case, ADJ network design must be taken into account.

Another example, an application with V_{OUT} = 1.5 V where, because of the drop across R_{SNS}, the voltage at CS+ pin could be very close to the threshold: if such voltage is overcome (startup, load regulation, overvoltage), then the HSA structure is activated; as nominal conditions are restored, the hysteresis keeps HSA active (unless V_{CS+} falls under the lower threshold).

5.7 Offset trimming

The current sharing accuracy strongly depends on the unbalance between the relevant parameters of the paralleled sections. Each percentage point on the relevant parameter tolerance introduces a maximum error equal to the double of the tolerance. The L6615 introduces an inherent error to current sharing due to the 40 mV offset at the negative input of the error amplifier; this offset guarantees the low value of the master COMP pin.

If all other parameters match, the offset introduces a percentage error equal to 4% divided by the voltage on the share bus:

Equation 19

$$I_{SLAVE} = I_{MASTER} \cdot \left(1 - \frac{40mA}{V_{SH}}\right)$$

Being V_{SH} directly proportional to the load current and fixed the ratio R_{CGA}/R_G, higher the currents involved in the sharing, lower the error.

Another error is introduced by the current sense amplifier due to its input offset whose amplitude can be ±2 mV: being typically the drop across R_{SNS} about one hundred mV at full load, the offset could lead to an error of some percentage point.

Whenever the application requires very high-current sharing accuracy, these offsets could be corrected through a triggering process, introducing a trimmer (R_K) between current sense input pins.

Referring to *Figure 21*, in case of high-side sensing, the equations are:

$$\frac{V_{OUT} - V_M}{R_G} = \frac{V_M}{(1-\delta)\cdot R_K}$$

$$\frac{V_{OUT} + V_{SENSE} - V_P}{R_G} - \frac{V_P}{\delta \cdot R_K} = I_G$$

$$V_P = V_M + V_O$$

where V_O is the current sense amplifier input offset. Solving the I_G, we get:

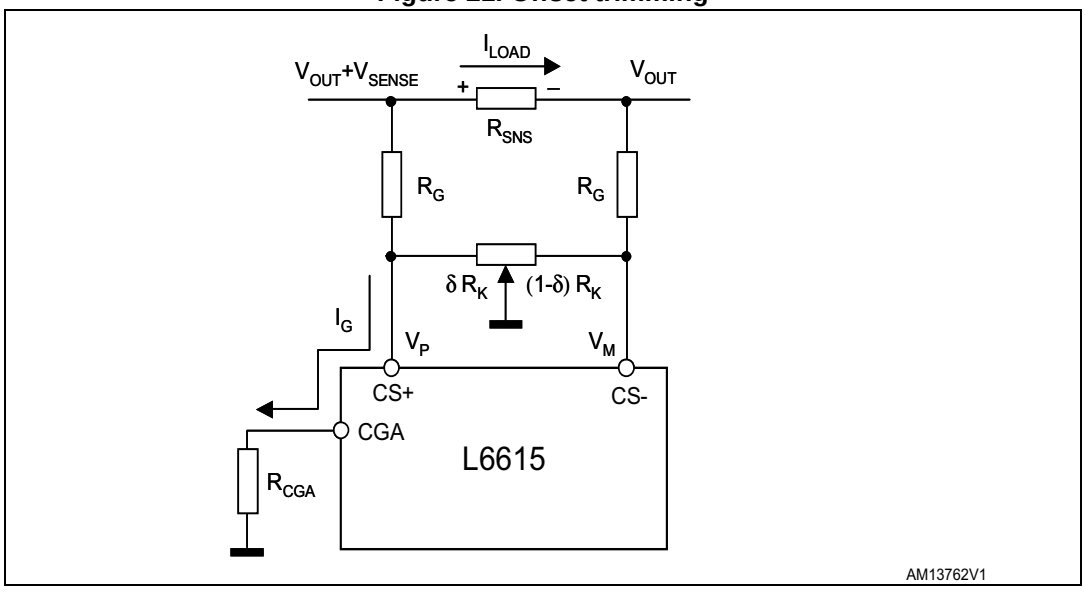
$$I_G = \frac{V_{SENSE}}{R_G} - \frac{\delta \cdot R_K + R_G}{\delta \cdot R_K \cdot R_{KG}} \cdot V_O + V_{OUT} \cdot \frac{2 \cdot \delta - 1}{\delta \cdot \left[R_K \cdot (1 - \quad) + R_G \right]}$$

Ideally I_G should be equal to the first term only: this current is sunk by CS+ pin, internally mirrored with 1:1 ratio and sent to CGA pin.

Imposing that the sum of two last terms is zero, the value of δ deleting the effect of the offset is:

$$\delta_{OPT} = \frac{1}{2} - \frac{2 \cdot V_{OUT} \cdot R_G - \sqrt{4 \cdot V^2_{OUT} \cdot R^2_G + V^2_O \cdot R^2_K + 4 \cdot V^2_O \cdot R_G \cdot R_K}}{2 \cdot V_O \cdot R_K}$$

Figure 21. Offset trimming



Because of the tolerance of the output voltage, the effect of the offset on CGA pin cannot be deleted completely on the whole output voltage range. If the trimming operation is performed at $V_{OUT(MIN)}$, the maximum residual voltage on CGA pin is present at $V_{OUT(MAX)}$ and its value is:

Equation 20

$$R_{CGA} \cdot (V_{OUT(MAX)} - V_{OUT(MIN)}) \cdot \frac{1 - 2 \cdot \delta_{OPT}}{\delta_{OPT} \cdot (R_K \cdot \delta_{OPT} - R_K - R_G)}$$

To simplify the procedure, the following step-by-step process can be followed:

- a trimmer has to be placed between sense pins of each section: the value of the trimmer resistance must be at least one order of magnitude higher than RG and it has to be set at one half of its range ($\delta = 0.5$);
- once the application is running at a load defined by the designer based on the required sharing accuracy, the master section has to be located;
- on the slave sections, the trimmer has to be fixed to equalize the output currents.

6 Reference

[1] L6910 - “Adjustable step down controller with synchronous rectification” (datasheet)

[2] L6911 - “5 bit programmable step down controller with synchronous rectification” (datasheet)

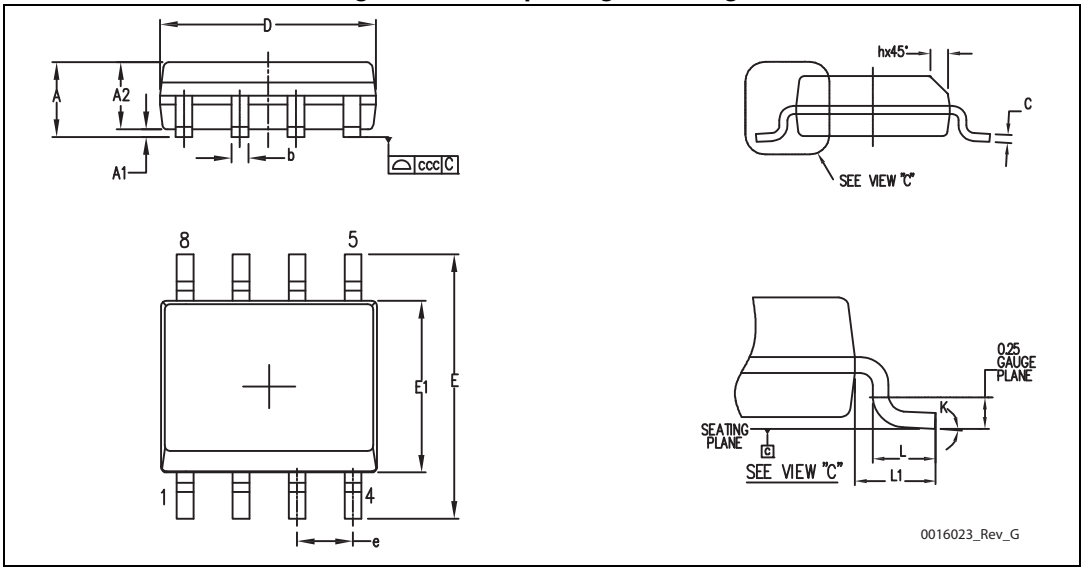
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 22. SO8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Figure 23. SO8 package drawings



8 Revision history

Table 6. Document revision history

Date	Revision	Changes
14-Jan-2008	4	
28-Aug-2013	5	Updated *Table 1: Device summary*. Changed min./max.V_{OS} values from 1.5/1.5 to -2/2 mV in *Table 5: Electrical characteristics*. Minor text changes.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT AUTHORIZED FOR USE IN WEAPONS. NOR ARE ST PRODUCTS DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com