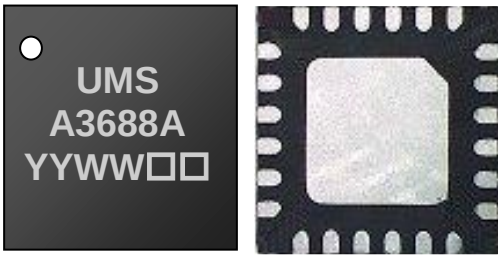
CHA3688aQDG

12.5-30 GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

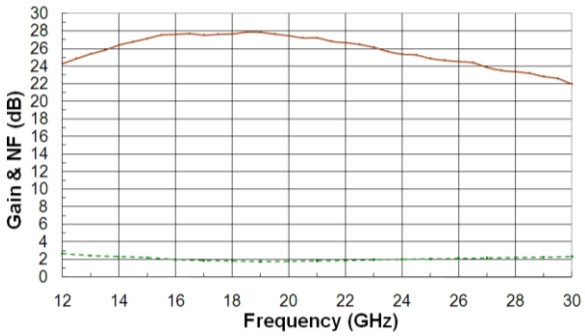
Description

The CHA3688aQDG is a three-stage self-biased wide band monolithic Low Noise Amplifier monolithic circuit.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 12.5-30GHz
- 2.1dB noise figure
- 26dB gain
- 26dBm Output IP3
- DC bias: Vd = 4V @ Id = 85 / 115mA
- 24L-QFN4x4
- MSL1



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	12.5		30	GHz
Gain	Linear Gain	21	26		dB
NF	Noise Figure		2.1	2.5	dB
OIP3	3rd order intercept point (16 - 30GHz)	24	26		dBm

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Specifications (low current configuration)

Tamb = +25°C, Vd1=Vd2=Vd3= +4V and Pads B, D not connected

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	12.5		30	GHz
Gain	Linear Gain (12.5 - 24GHz) Linear Gain (24.5 - 30GHz)	22 20	25 23		dB dB
ΔG	Gain flatness (12.5 - 24GHz) Gain flatness (24.5 - 30GHz)		±1.5 ±2		dB dB
NF	Noise figure (12.5 - 16GHz) Noise figure (16.5 - 24GHz) Noise figure (24.5 - 30GHz)		2.3 2.0 2.2	2.6 2.3 2.5	dB dB dB
S11	Input return loss (12.5 - 16GHz) (27 – 30GHz) Input return loss (16.5 - 26.5GHz)		2.5:1 2.0:1	3.0:1 2.5:1	dB dB
S22	Output return loss		2.0:1	2.5:1	dB
OIP3	3rd order intercept point @ Pout SCL < 8dBm from 16 to 30GHz	23	25		dBm
P1dB	Output power at 1dB gain compression	13	14		dBm
Id	Drain bias current		85	115	mA
Vd	Drain bias voltage		4		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Specifications (high current configuration)

Tamb = +25°C, Vd1=Vd2=Vd3= +4V and Pads B, D Grounded

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	12.5		30	GHz
Gain	Linear Gain (12.5 - 24GHz) Linear Gain (24.5 - 30GHz)	23 21	26 24		dB dB
ΔG	Gain flatness		±2		dB
NF	Noise figure (12.5 - 16GHz) Noise figure (16.5 - 24GHz) Noise figure (24.5 - 30GHz)		2.3 2.0 2.2	2.6 2.3 2.5	dB dB dB
S11	Input return loss (12.5 - 16GHz) (27 – 30GHz) Input return loss (16.5 - 26.5GHz)		2.5:1 2.0:1	3.0:1 2.5:1	dB dB
S22	Output return loss		2.0:1	2.5:1	dB
OIP3	3rd order intercept point @ Pout SCL < 8dBm from 16 to 30GHz	24	26		dBm
P1dB	Output power at 1dB gain compression	14	15		dBm
Id	Drain bias current		115	150	mA
Vd	Drain bias voltage		4		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

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Absolute Maximum Ratings [1]

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5V	V
Pin	RF input power	10	dBm
Tj	Junction temperature [2]	175	°C

[1] Operation of this device above anyone of these parameters may cause permanent damage.

[2] Thermal Resistance channel to ground paddle

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Symbol	**Pad Nº**	**Parameter**	**Values**	**Unit**
Vd1	23	DC Drain voltage	4	V
Vd2	21	DC Drain voltage	4	V
B	9	DC Gate voltage	Connected to ground or not	
D	11	DC Gate voltage		

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

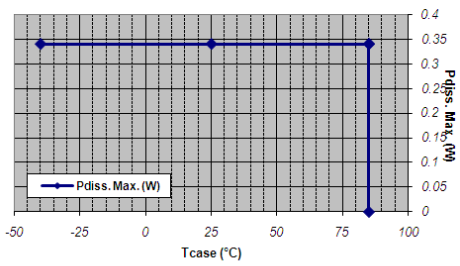
A de-rating must be applied on the dissipated power if the Tcase temperature cannot be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

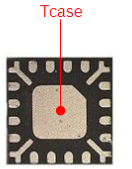
DEVICE THERMAL SPECIFICATION : CHA3688aQDG low current		
Recommended max. junction temperature (Tj max)	:	124 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power @ Tcase= 85 °C	:	0.3 W
=> Pdiss derating above Tcase(1)= 85 °C	:	9 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<114 °C/W
Minimum Tcase operating temperature(3)	:	-40 °C
Maximum Tcase operating temperature(3)	:	85 °C
Absolute maximum rating Tcase temperature(3)	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hottest junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





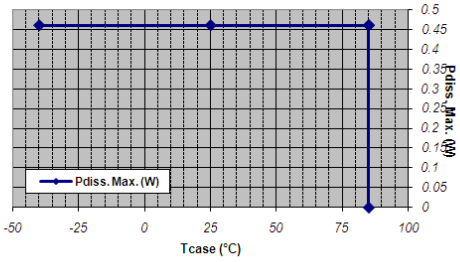
Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

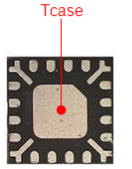
DEVICE THERMAL SPECIFICATION : CHA3688aQDG high current		
Recommended max. junction temperature (Tj max)	:	139 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power @ Tcase= 85 °C	:	0.5 W
=> Pdiss derating above Tcase(1)= 85 °C	:	9 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<116 °C/W
Minimum Tcase operating temperature(3)	:	-40 °C
Maximum Tcase operating temperature(3)	:	85 °C
Absolute maximum rating Tcase temperature(3)	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hottest junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

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Typical Package Sij parameters for low current configuration

Tamb = +25°C, Vd1=Vd2=Vd3= +4V, Id = 90mA and Pads B, D not connected

Freq (GHz)	Freq (GHz)	Freq (GHz)	Freq (GHz)	Freq (GHz)	Freq (GHz)	Freq (GHz)	Freq (GHz)	Freq (GHz)
2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0
5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0	5.0
6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0	6.0
7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0	7.0
8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0
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11.0	11.0	11.0	11.0	11.0	11.0	11.0	11.0	11.0
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38.0	38.0	38.0	38.0	38.0	38.0	38.0	38.0	38.0
39.0	39.0	39.0	39.0	39.0	39.0	39.0	39.0	39.0
40.0	40.0	40.0	40.0	40.0	40.0	40.0	40.0	40.0

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Typical Package Sij parameters for high current configuration

Tamb = +25°C, Vd1=Vd2=Vd3= +4V, Id = 115mA and Pads B, D Grounded

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-1.3	66	-75.4	159	-77.1	115	-1.4	61
3.0	-1.2	14	-62.1	-168	-56.8	7	-1.5	0
4.0	-1.1	-34	-74.0	65	-57.0	6	-1.7	-61
5.0	-1.0	-79	-79.6	-146	-30.6	-61	-2.6	-120
6.0	-0.9	-124	-84.9	160	-12.4	-144	-5.0	-178
7.0	-1.3	-178	-63.2	24	1.8	118	-9.8	128
8.0	-2.7	117	-64.3	31	9.9	23	-20.6	92
9.0	-4.9	42	-73.9	84	16.6	-62	-27.6	-18
10.0	-5.7	-27	-56.5	-150	20.2	-145	-13.9	-168
11.0	-5.3	-83	-57.7	126	22.7	142	-12.4	130
12.0	-4.8	-128	-54.9	86	24.3	74	-13.5	84
13.0	-4.7	-167	-55.2	30	25.4	13	-14.8	53
14.0	-5.1	158	-53.6	116	26.4	-44	-15.4	21
15.0	-6.2	122	-48.5	-47	27.2	-100	-13.0	-8
16.0	-7.4	91	-57.7	140	27.6	-156	-11.6	-44
17.0	-9.4	54	-55.6	135	27.6	152	-9.8	-75
18.0	-11.6	27	-51.6	119	27.7	103	-8.7	-112
19.0	-14.0	-5	-51.0	75	27.9	52	-8.5	-150
20.0	-16.4	-29	-48.8	58	27.5	2	-9.0	179
21.0	-19.3	-48	-49.5	59	27.2	-44	-10.0	148
22.0	-16.8	-72	-48.5	29	26.7	-92	-13.0	128
23.0	-15.0	-109	-47.6	25	26.2	-139	-15.5	117
24.0	-13.7	-149	-49.0	-17	25.4	177	-15.9	112
25.0	-12.0	-176	-47.4	3	24.9	131	-18.0	116
26.0	-10.3	158	-48.6	2	24.5	87	-16.6	113
27.0	-9.0	129	-47.1	-24	23.9	38	-14.4	102
28.0	-8.3	91	-38.4	-21	23.4	-7	-14.2	75
29.0	-7.5	51	-42.0	16	22.8	-58	-14.2	39
30.0	-6.3	2	-40.8	-34	22.0	-115	-14.9	-6
31.0	-5.1	-57	-41.5	-56	19.4	-175	-14.6	-54
32.0	-4.5	-107	-37.7	-58	15.3	134	-11.4	-98
33.0	-3.0	-142	-43.9	-115	11.8	84	-7.8	-133
34.0	-2.1	-173	-50.3	-135	7.2	38	-5.2	-163
35.0	-1.2	162	-39.6	-15	2.1	-6	-3.6	172
36.0	-1.2	139	-34.6	-45	-3.9	-45	-2.3	148
37.0	-1.4	122	-32.7	-105	-10.2	-74	-1.6	129
38.0	-1.3	105	-38.2	-109	-16.9	-92	-1.4	112
39.0	-1.7	90	-38.3	-142	-22.1	-91	-1.8	92
40.0	-2.4	70	-39.4	-105	-25.1	-73	-2.1	75

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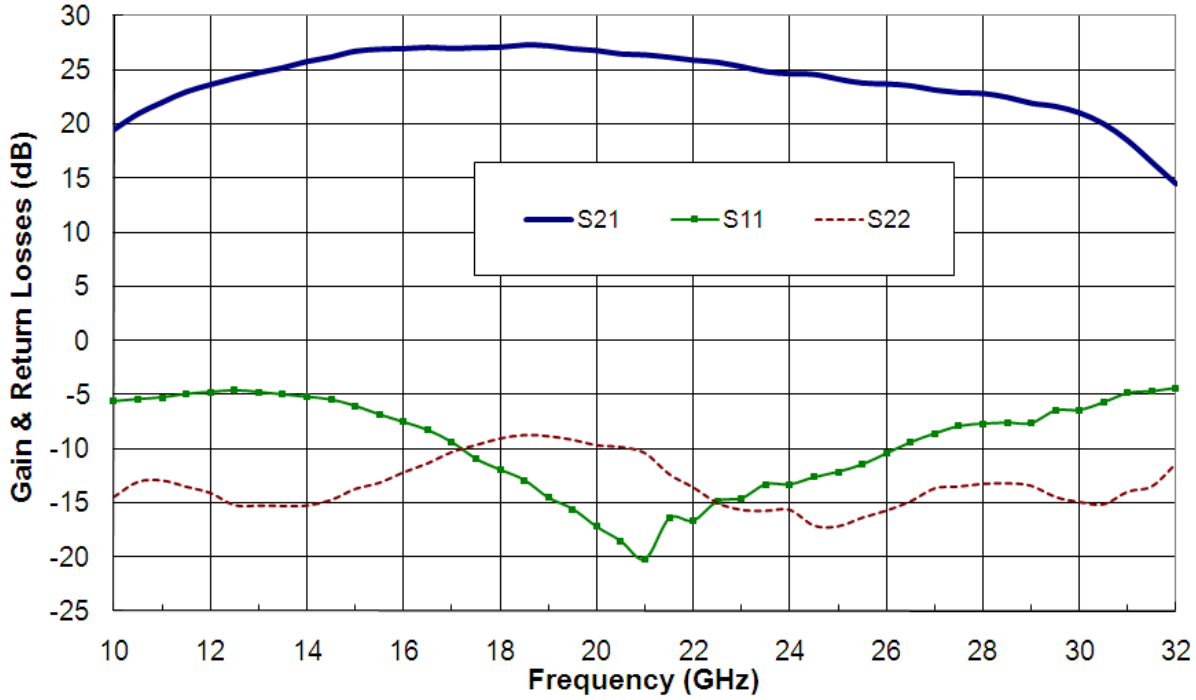
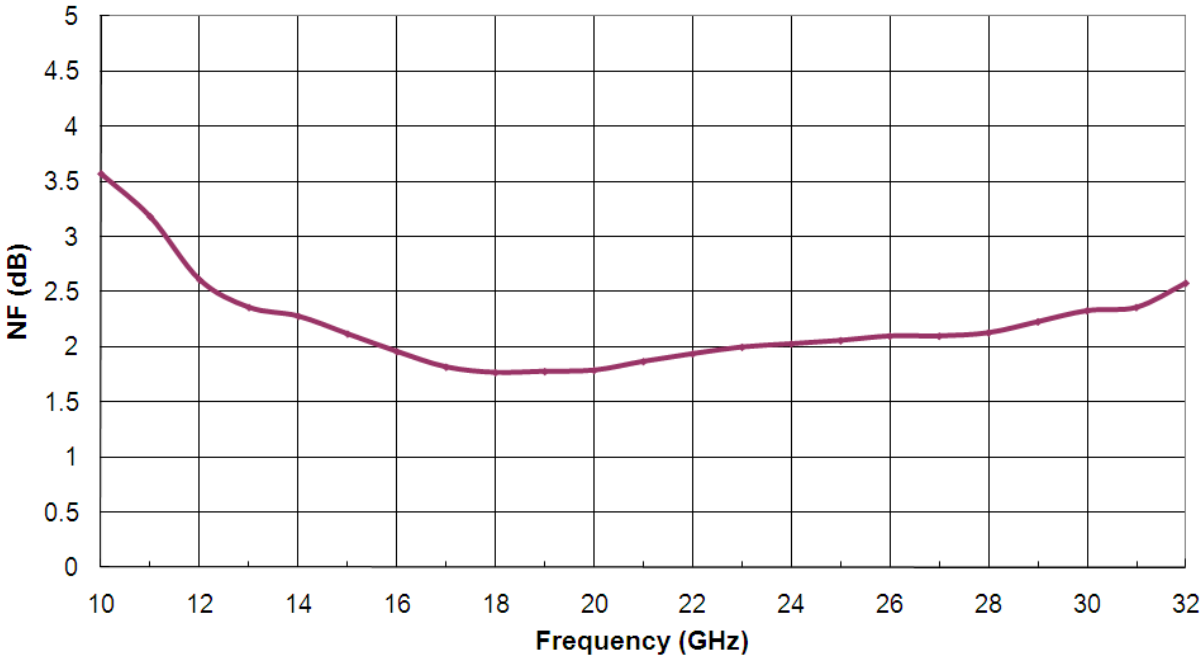
Typical Board Measurements

Tamb = +25°C, Vd1=Vd2=Vd3= +4V Id = 85mA
Pads B, D not connected (low current configuration)
Measurements are given in the package access planes. Losses are de-embedded.

Gain and return losses versus frequency



Noise figure versus frequency



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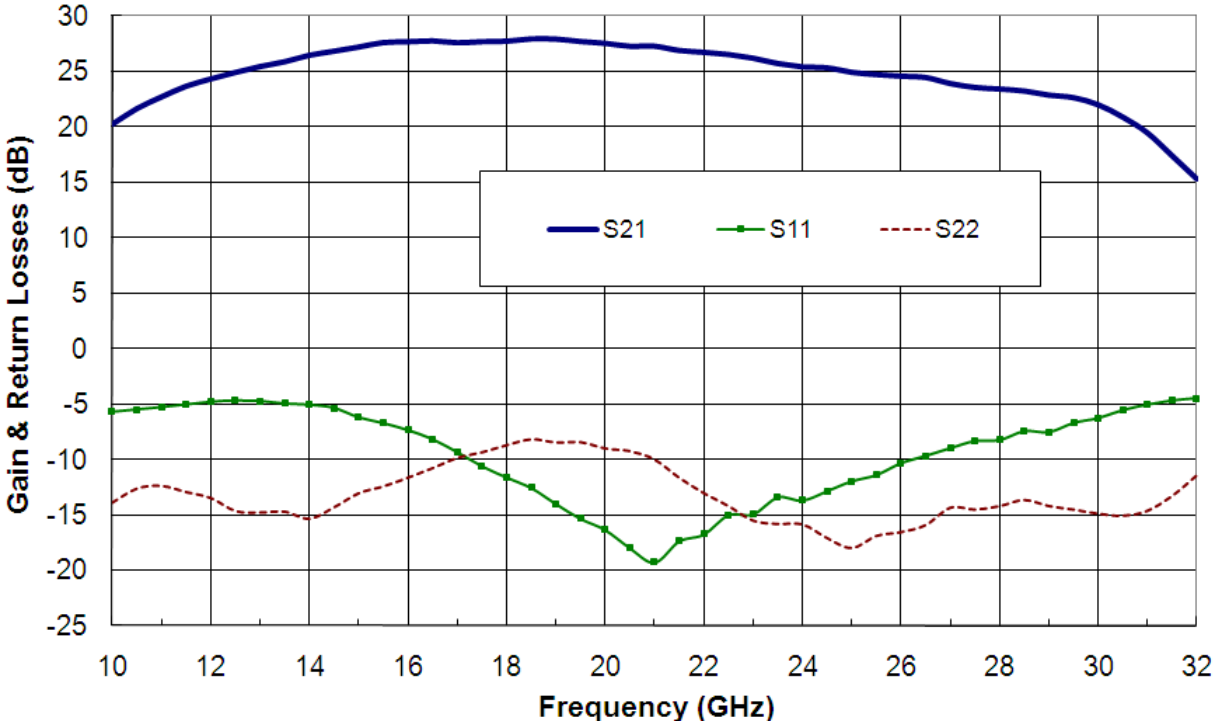
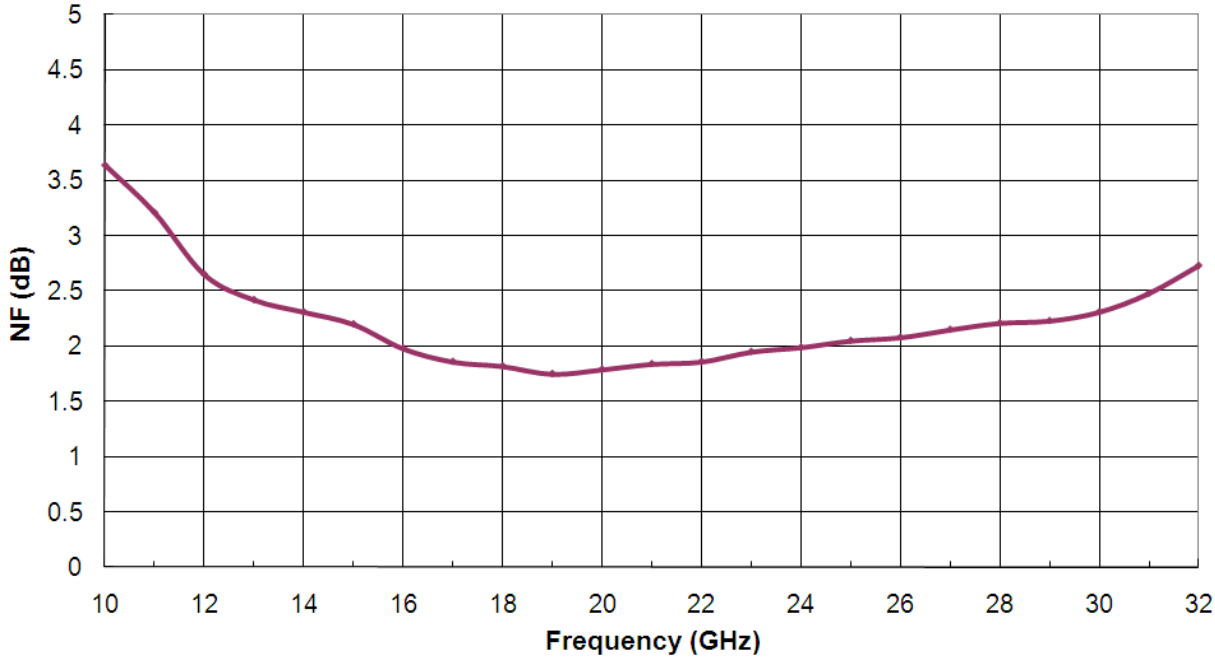
Typical Board Measurements

Tamb = +25°C, Vd1=Vd2=Vd3= +4V Id = 115mA
Pads B, D Grounded (high current configuration)
Measurements are given in the package access planes. Losses are de-embedded.

Gain and return losses versus frequency



Noise figure versus frequency



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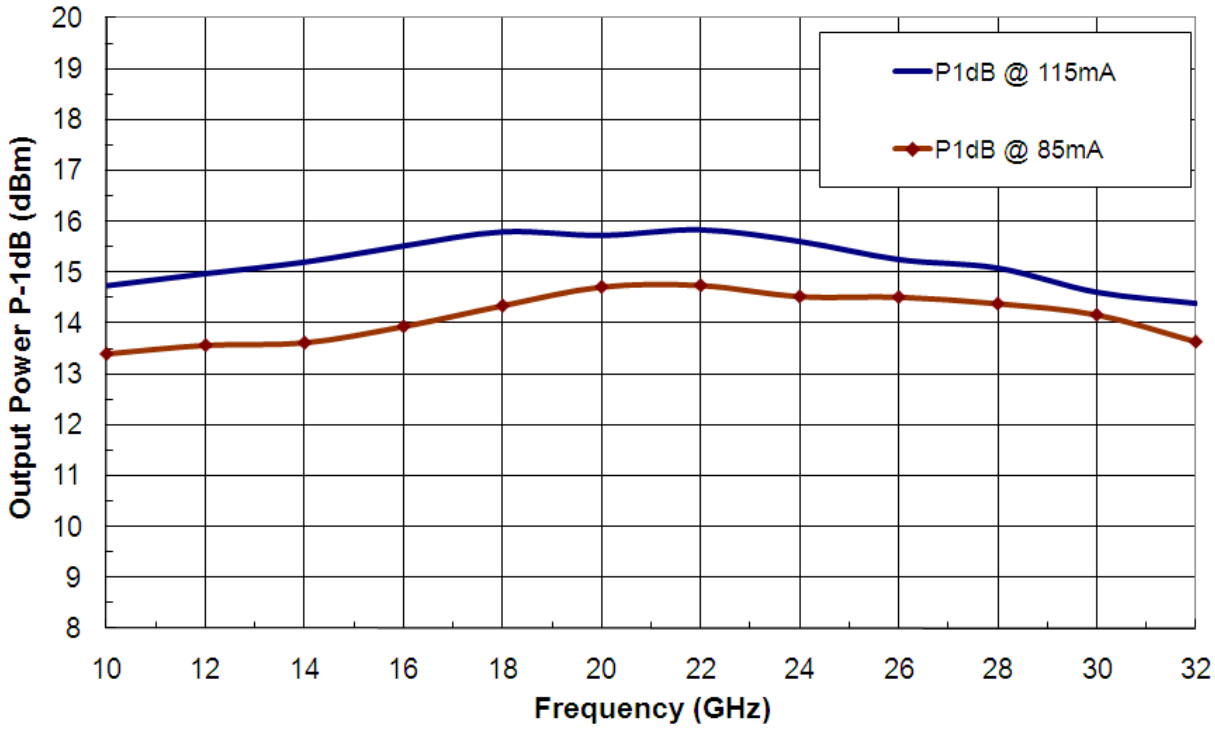
Typical Board Measurements

Measurements are given in the package access planes. Losses are de-embedded.
Tamb = +25°C, Vd1=Vd2=Vd3= +4V Id = 85/115mA

Output power -1dB for low and high current configurations



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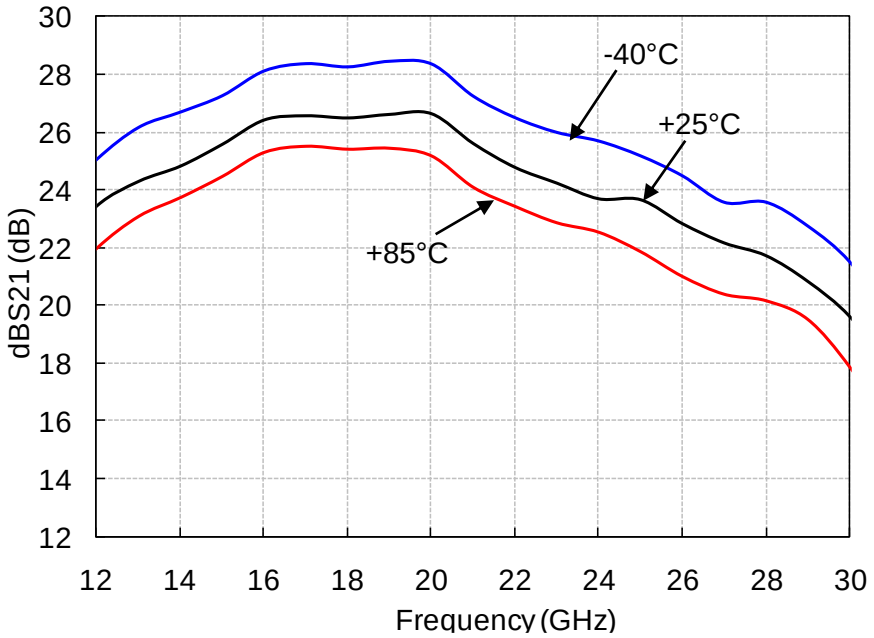
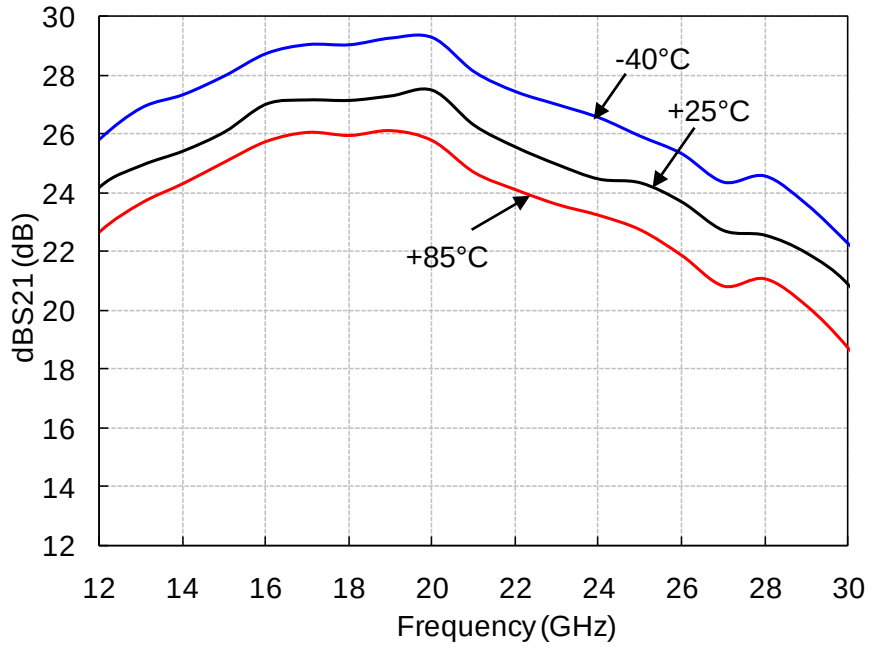
Typical Board Measurements

Tamb = -40°C / +25°C / +85°C, Vd1=Vd2=Vd3= +4V
Measurements are given in the package's access plans. Losses are de-embedded.

Gain measurement for low current configuration
Pads B, D not connected



Gain measurement for high current configuration
Pads B, D Grounded



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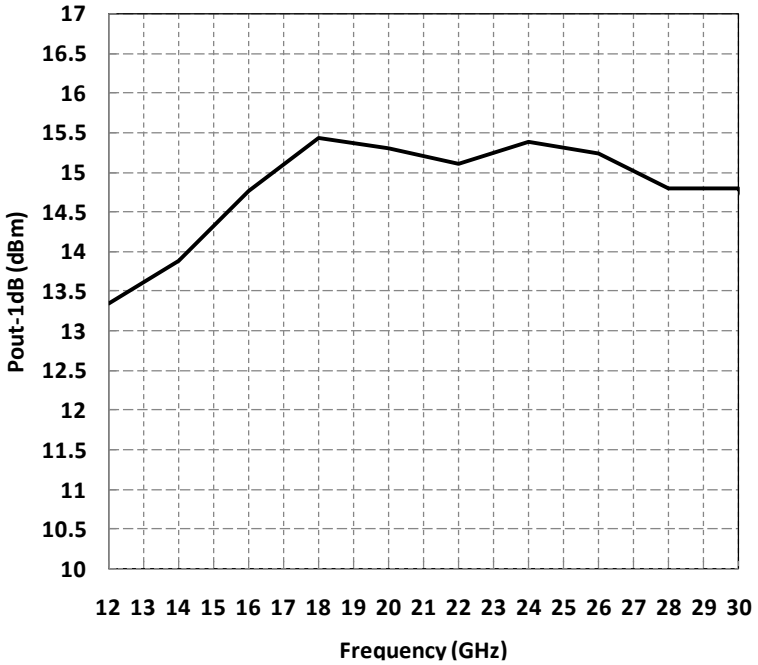
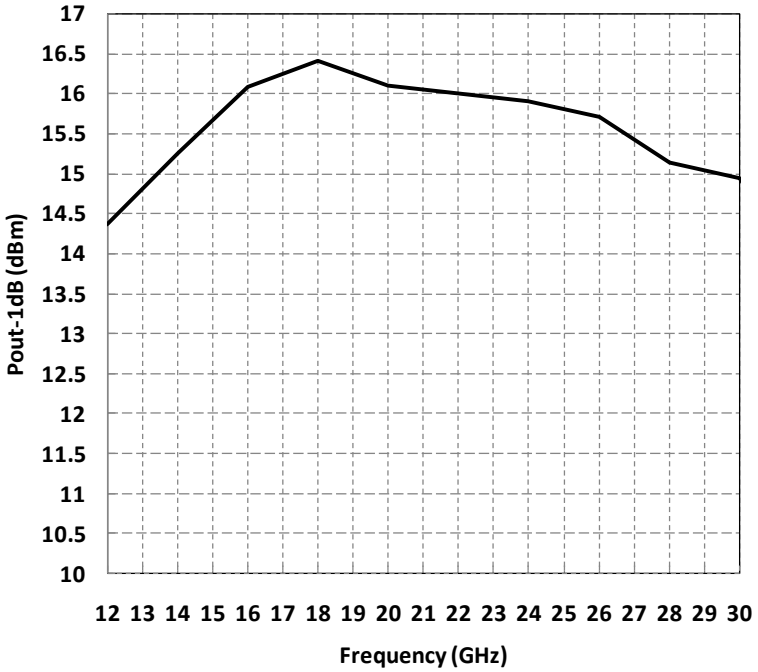
Typical Board Measurements

Tamb = -40°C / +25°C / +85°C, Vd1=Vd2=Vd3= +4V
Measurements are given in the connectors' access plans. Losses are not de-embedded.

Output power -1dB measurement for low current configuration
Pads B, D not connected



Output power -1dB measurement for high current configuration
Pads B, D Grounded



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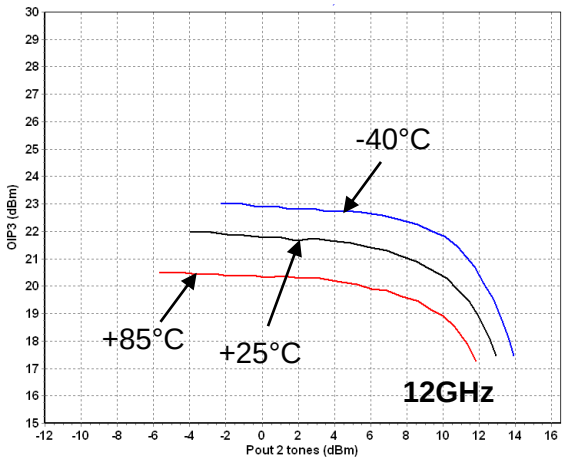
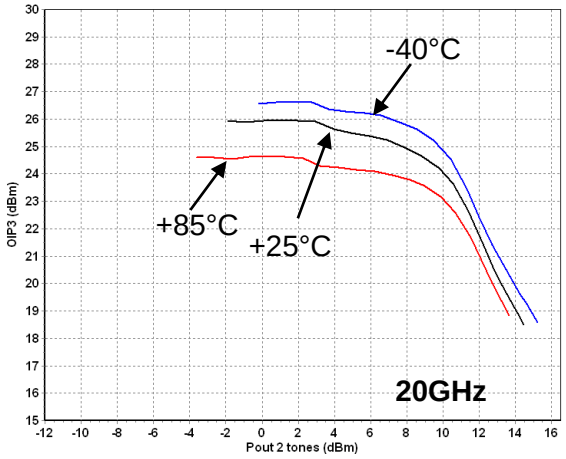
Typical Board Measurements

Tamb = -40°C / +25°C / +85°C, Vd1=Vd2=Vd3= +4V Id = 85mA
Pads B, D not connected (low current configuration)
Measurements are given in the connectors' access plans. Losses are not de-embedded.

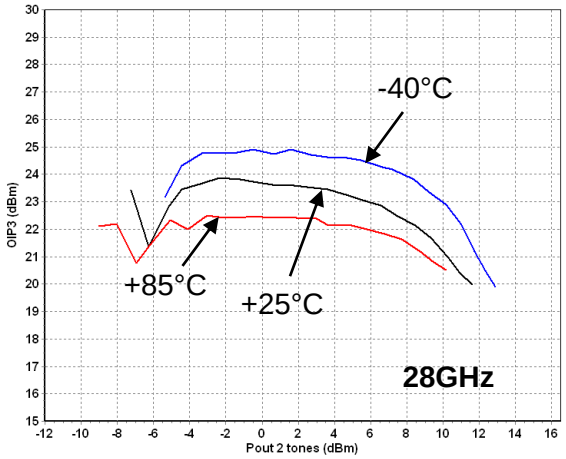
Output IP3 versus input power @ 12GHz



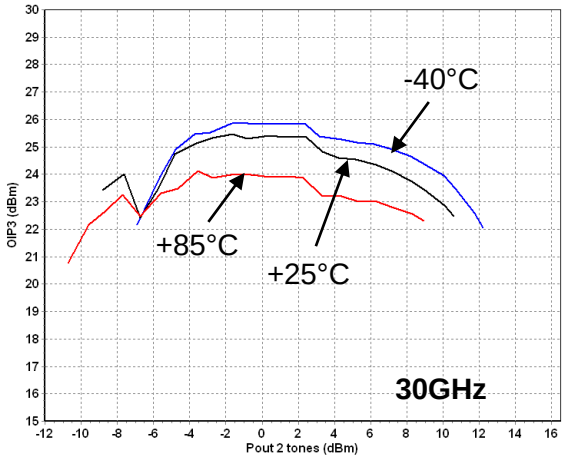
Output IP3 versus input power @ 20GHz



Output IP3 versus input power @ 28GHz



Output IP3 versus input power @ 30GHz



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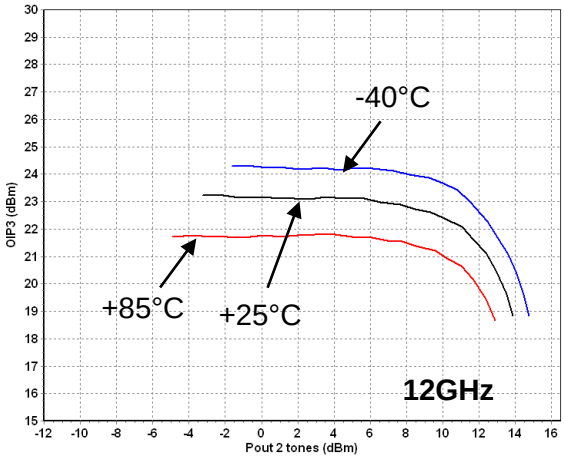
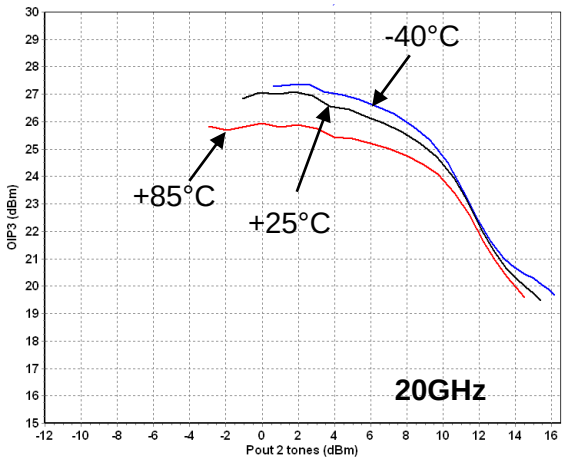
Typical Board Measurements

Tamb = -40°C / +25°C / +85°C, Vd1=Vd2=Vd3= +4V Id = 115 mA
Pads B, D = GND (**high current configuration**)
Measurements are given in the connectors' access plans. Losses are not de-embedded.

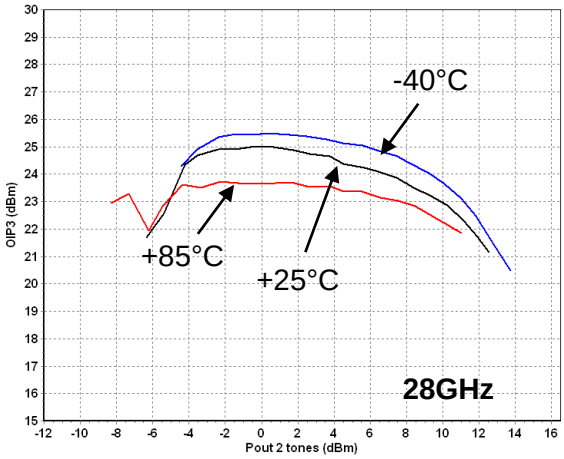
Output IP3 versus input power @ 12GHz



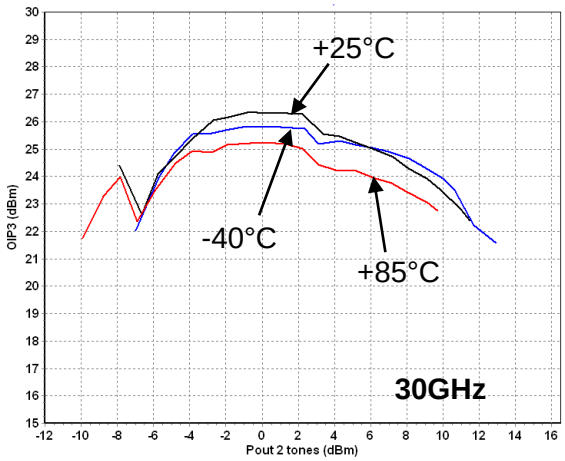
Output IP3 versus input power @ 20GHz



Output IP3 versus input power @ 28GHz



Output IP3 versus input power @ 30GHz



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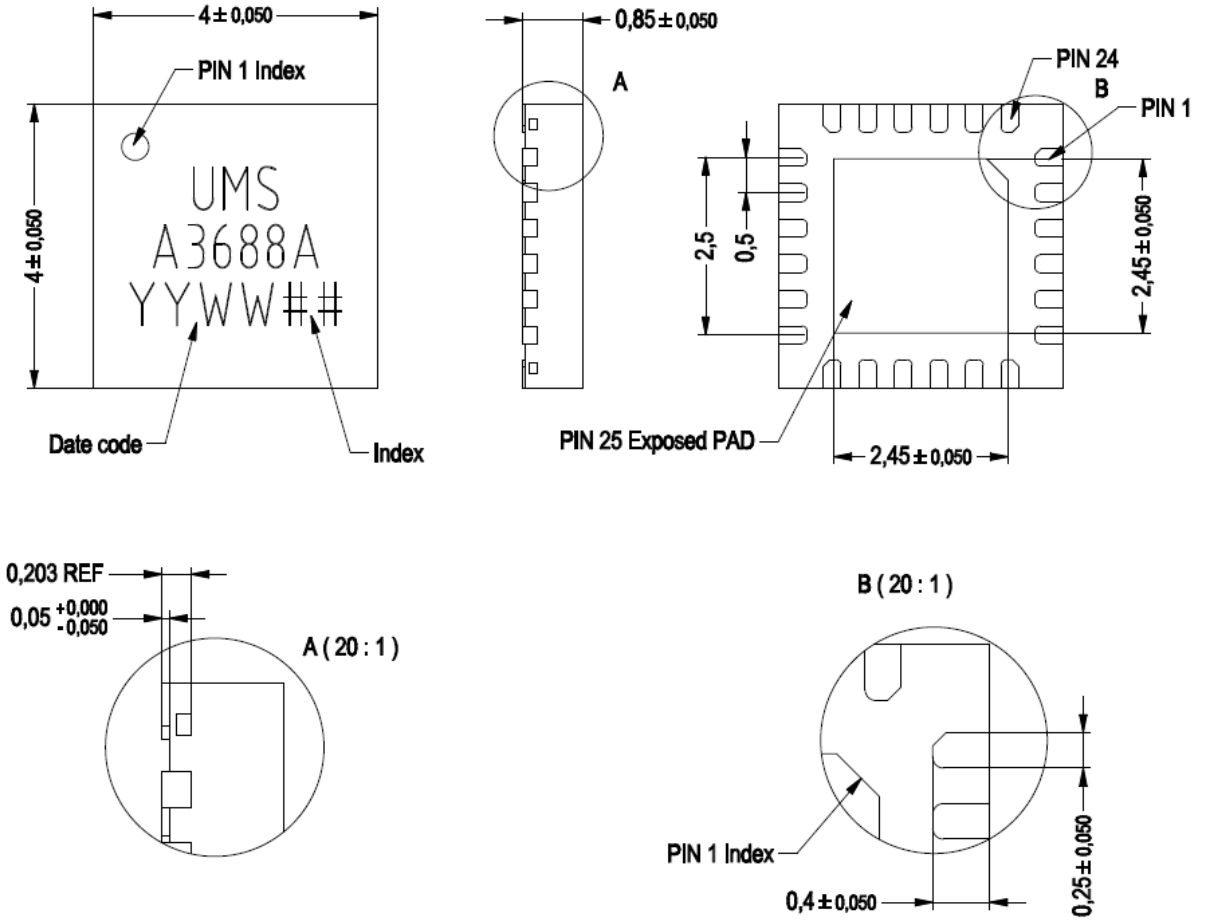
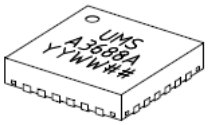
Package outline [1]



Units : mm
Finish : Matt tin
Lead free (Green)



Matt tin, Lead Free (Green)	1- Nc	9- B	17- GND
Units : mm	2- GND	10- Nc	18- Nc
From the standard : JEDEC MO-220 (VGGD)	3- GND	11- D	19- Vd3
	4- RF in	12- Nc	20- Nc
25- GND	5- GND	13- GND	21- Vd2
	6- GND	14- GND	22- Nc
	7- Nc	15- RF out	23- Vd1
	8- Nc	16- GND	24- Nc

[1] The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

[2] It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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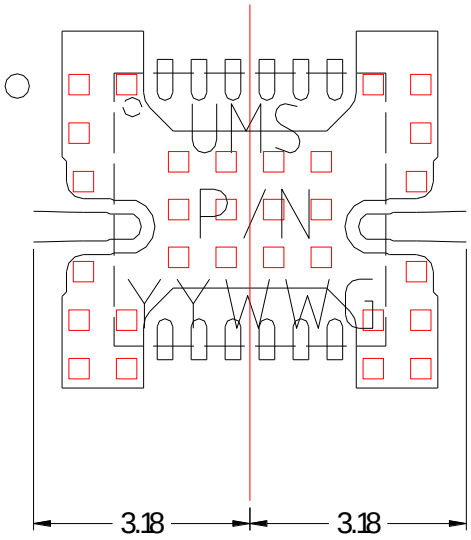
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



ESD sensitivity

Standard	Value
Jedec Jesd22 A114D	HBM Class 1B (>500V)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

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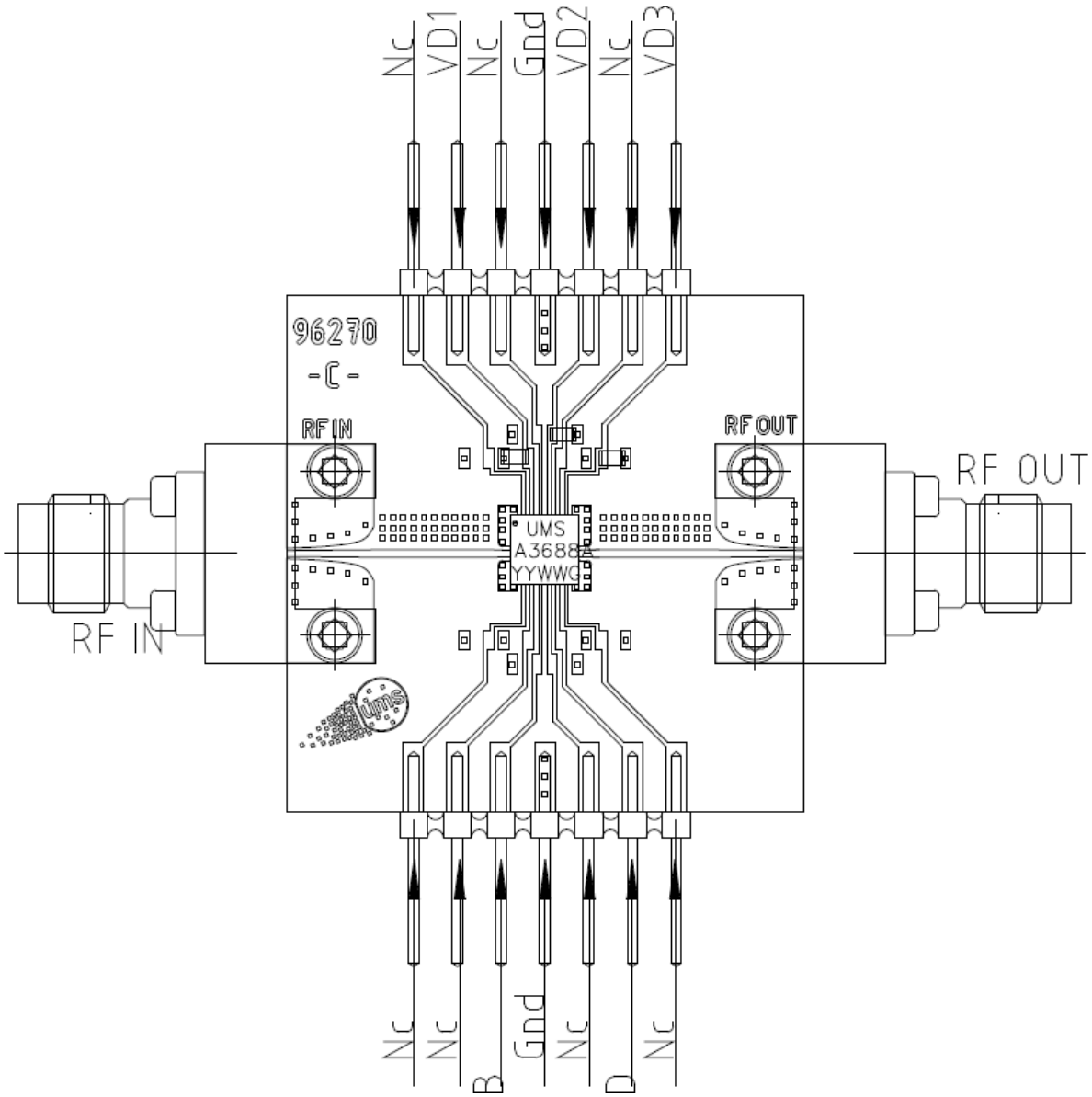
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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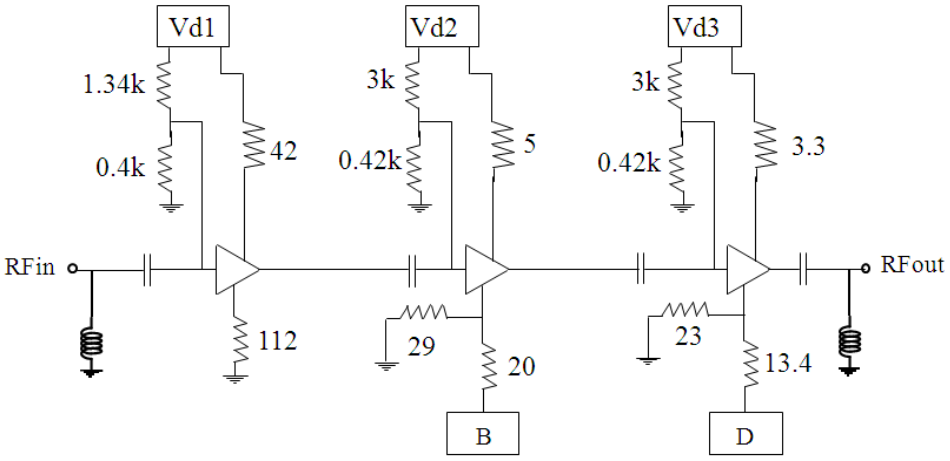
Chip Biasing options

This chip is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



The requirement is not to exceed Vds = 3.5Volt (internal Drain to Source voltage).

We propose two standard biasings:

- Low Noise and low consumption: Vd = 4V and B & D leads non connected (NC).
  Idd = 85mA & Pout-1dB = 14dBm Typical.
- Low Noise and higher output power: Vd = 4V and B, D grounded
  Idd = 115mA & Pout-1dB = 15dBm Typical.

Note

Due to ESD protection circuits, RFin and RFout are DC grounded and an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

The DC connections (Vd1, Vd2 and Vd3) do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (typically 10nF) on the PC board, as close as possible to the package.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHA3688aQDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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