Real-time Clock Module (I²C Bus)

Description

The PT7C4363C serial real-time clock is a low-power clock/calendar with a programmable square-wave output. Address and data are transferred serially via a 2-wire bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in the 24-hour format indicator.

Table 1 shows the basic functions of PT7C4363C. More details are shown in section: overview of functions.

Features

- Drop-In Replacement for PT7C4363
- Supports High-ESR Crystals Up To 100kΩ
- Uses external 32.768kHz quartz crystal
- Supports I²C-Bus's high speed mode (400kHz)
- Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- Oscillator stop flag
- Low backup current: typical 400nA at V_{DD} = 3V and T_A = 25°C
- Operating Range: 1.3V to 5.5V
- MSL 1 Rating
- Packaging (Pb-free & Green):
  - 8-pin, SOIC (W)
  - 8-Pin, WDFN (ZG)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Table 1. Basic Functions of PT7C4363C

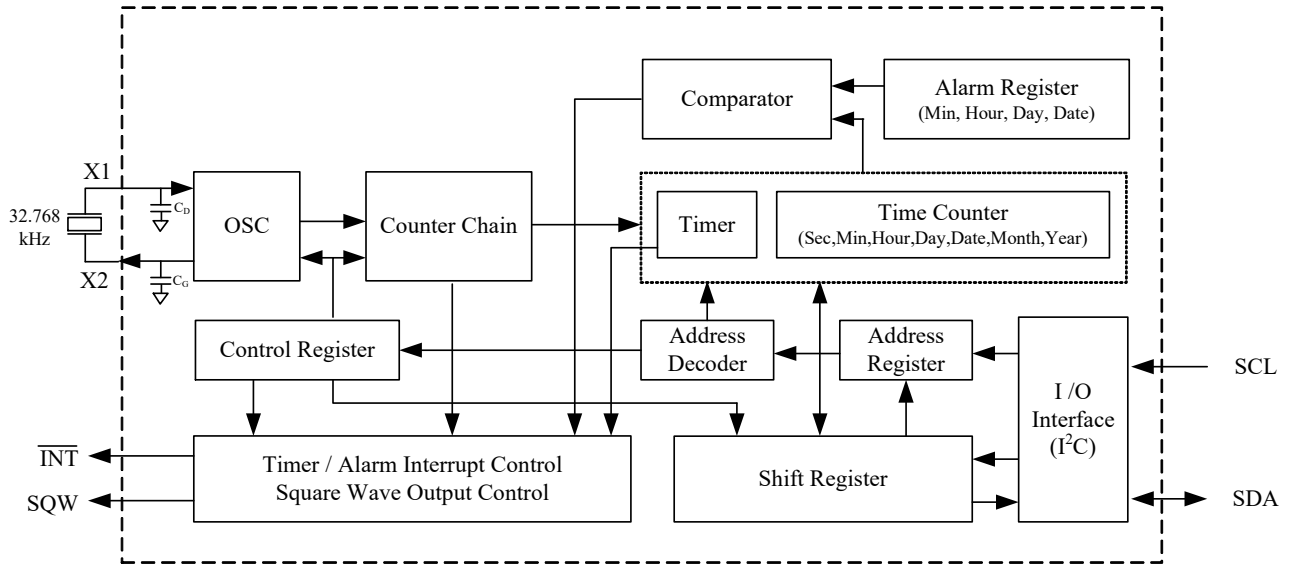
Item	Function			PT7C4363C
1	Oscillator	Source: Crystal: 32.768kHz		√
		Oscillator enable/disable		-
		Oscillator fail detect		√
2	Time	Time display	12-hour	-
			24-hour	√
		Century bit		√
		Time count chain enable/disable		√
3	Interrupt	Alarm interrupt		√
		Timer interrupt output		√
4	Programmable square wave output (Hz)			1, 32, 1.024k, 32.768k
5	Communication	2-wire I²C bus		√
		3-wire bus		-
		Burst mode		-
6	Control	Write protection		-
		External clock test mode		√
		Power-on reset override		√

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Function Block

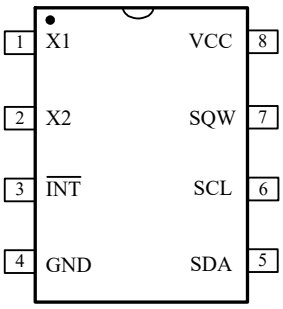


Note: PT7C4363C need to add a 10pF ~ 30pF capacitor between X1 and GND to get the accurate 32k frequency.

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Pin Configuration



Pin Description

Pin Number	Pin Name	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them.
3	$\overline{\text{INT}}$	O	**Interrupt Output.** Open drain, active low.
4	GND	P	**Ground.**
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
7	SQW	O	**Clock Output.** Open drain. Four frequencies selectable: 32.768k, 1.024k, 32, 1Hz when SQWE bit is set to 1.
8	VCC	P	**Power.**

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Maximum Ratings

Storage Temperature..... -65°C to +150°C
Ambient Temperature with Power Applied..... -40°C to +85°C
Supply Voltage to Ground Potential (V_{CC} to GND) ..... -0.3V to +6.5V
DC Input (All Other Inputs except V_{CC} & GND)..... -0.3V to (V_{cc}+0.3V)
DC Output Voltage (SDA, /INTA, /INTB pins)..... -0.3V to +6.5V
Power Dissipation.....320mW (Depend on package)
ESD ..... 2KV HBM

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CC}	Power voltage	1.3		5.5	V
V_{IH}	Input high level	0.7 V_{CC}		V_{CC}+0.3	
V_{IL}	Input low level	-0.3		0.3 V_{CC}	
T_A	Operating temperature	-40		85	°C

DC Electrical Characteristics

Unless otherwise specified, GND = 0, V_{CC} = 1.3 ~ 5.5V, T_A = -40°C to +85°C, f_{OSC} = 32.768kHz.

Symbol	Description	Pin	Conditions		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	V_{CC}	Interface inactive. T_A = 25°C (1)		1.1		5.5	V
			Interface active. f_{SCL} = 400kHz, T_A = 25°C (1)		1.3		5.5	
	Supply voltage for clock data integrity	V_{CC}			1.1		5.5	
I_{CCA}	Active Supply current	V_{CC}	Interface active	f_{SCL} = 400kHz			35	µA
				f_{SCL} = 100kHz			15	
I_{CCS}	Standby current	V_{CC}	Interface inactive (f_{SCL} = 0), pin 7 disabled, (2) T_A= -40 ~ 85°C	V_{CC} = 5.0V		450	700	nA
				V_{CC} = 3.0V		400	650	
			Interface inactive (f_{SCL} = 0), pin 7 enabled at 32kHz, (2) T_A= -40 ~ 85°C	V_{CC} = 5.0V		650	900	nA
				V_{CC} = 3.0V		600	850	
V_{IL1}	Low-level input voltage	SCL			0		0.3V_{CC}	V
V_{IH1}	High-level input voltage	SCL			0.7V_{CC}		V_{CC}	
I_{OL}	Low-level output voltage	SDA	V_{OL} = 0.4V, V_{CC} = 5V		-3			mA
		/INT, SQW	V_{OL} = 0.4V, V_{CC} = 5V		-1			
I_{IL}	Input leakage current	SCL			-1		1	µA
I_{OZ}	Output current when OFF				-1		1	µA

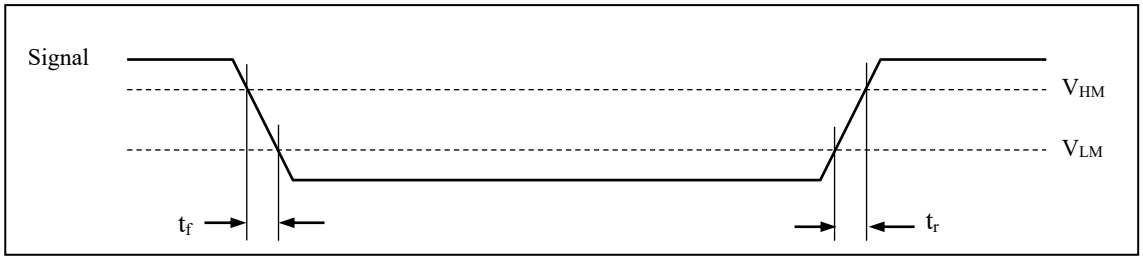
Note:
1) For reliable oscillator start-up at power-up: $V_{CC(min)power-up}$ = $V_{CC(min)}$ + 0.3V.
2) Timer source clock = $^1/_{60}$ Hz, voltage of SCL and SDA is V_{CC} or GND.

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AC Electrical Characteristics

Symbol	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.2 V_{CC}	V

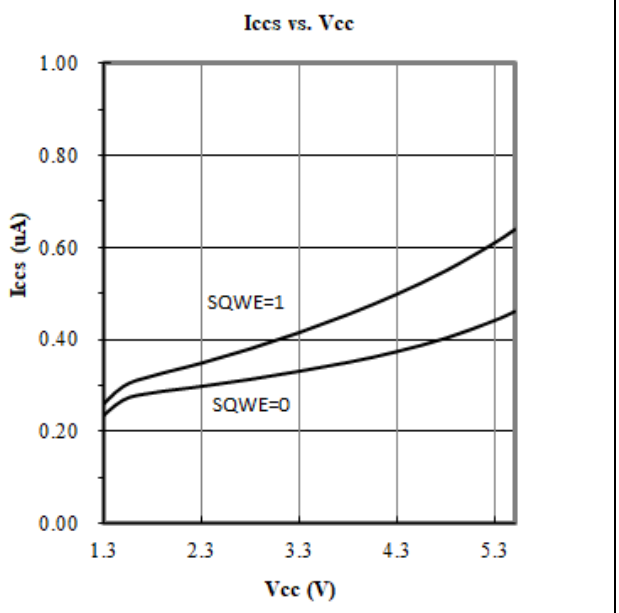


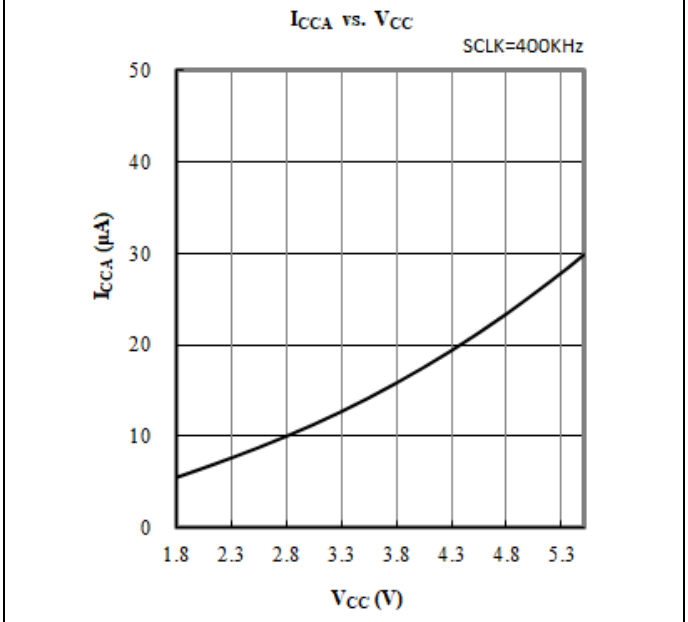
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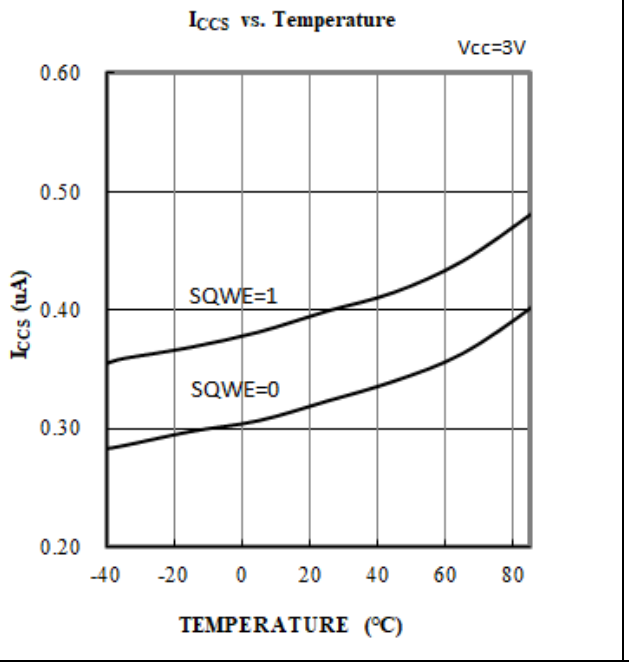
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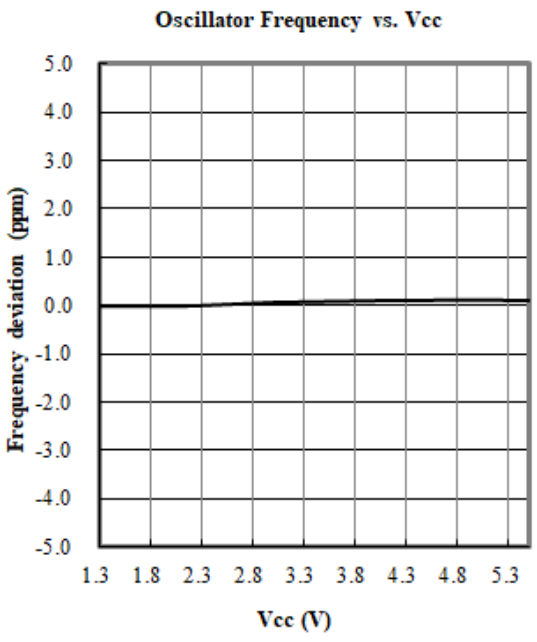
Typical Operation Characteristics

Unless otherwise specified, V_{CC} = 3.3V, T_A = 25°C









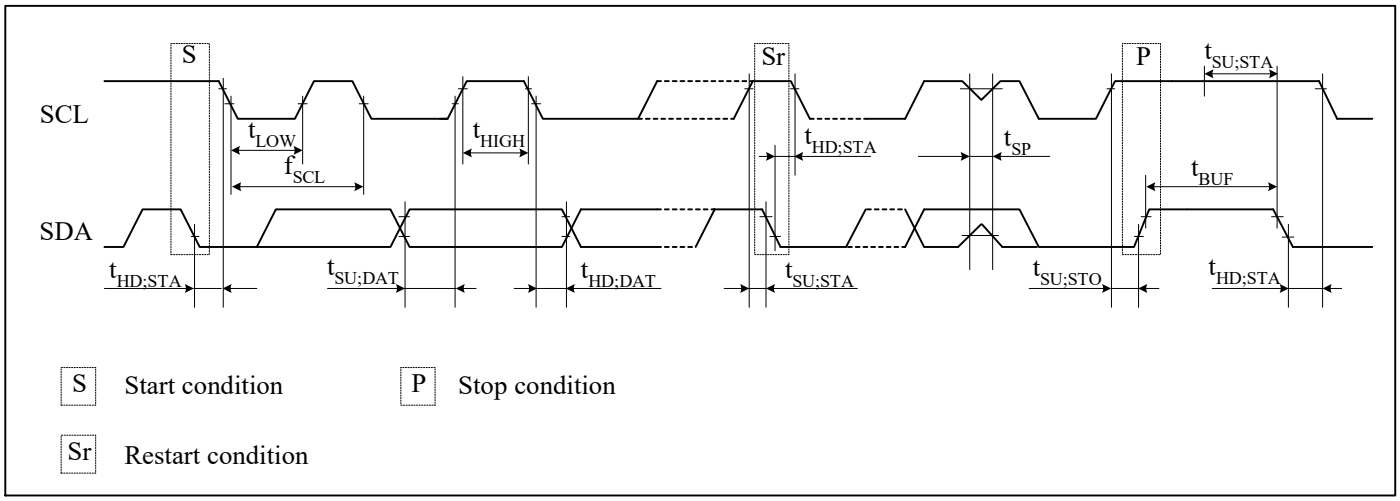
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Over the Operating Range

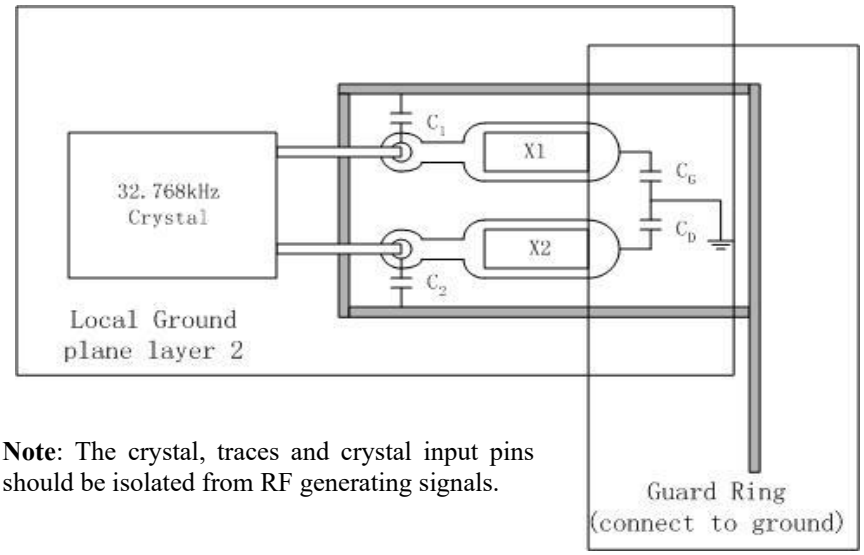
Symbol	Item	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency			400	kHz
$t_{SU;STA}$	START condition set-up time	0.6			µs
$t_{HD;STA}$	START condition hold time	0.6			µs
$t_{SU;DAT}$	Data set-up time (RTC read/write)	200			ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35			ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0			µs
$t_{SU;STO}$	STOP condition setup time	0.6			µs
t_{BUF}	Bus idle time between a START and STOP condition	1.3			µs
t_{LOW}	When SCL = "L"	1.3			µs
t_{HIGH}	When SCL = "H"	0.6			µs
t_r	Rise time for SCL and SDA			0.3	µs
t_f	Fall time for SCL and SDA			0.3	µs
t_{SP}*	Allowable spike time on bus			50	ns
C_B	Capacitance load for each bus line			400	pF

* **Note:** Only reference for design.



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Recommended Layout for Crystal



Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

Built-in Capacitors Specifications and Recommended External Capacitors

Symbol	Parameter		Typ.	Unit
C_G	Build-in capacitors	X1 to GND	5	pF
C_D		X2 to GND	20	pF
C_1	Recommended External capacitors	X1 to GND	20	pF
C_2		X2 to GND	0	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768Hz, C_1 and C_2 should meet the equation as below:

$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$

Cpar is all parasitical capacitor between X1 and X2.

C_L is crystal's load capacitance.

Crystal Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_O	Nominal Frequency		32.768		kHz
ESR	Series Resistance			100	kΩ
C_L	Load Capacitance		12.5		pF

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Function Description

Overview of Functions

1. Clock Function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100. Please note before reading time counter, user needs to initialize the date/time after RTC is powered up, or when the OSF bit is 1 (Oscillator failure).

2. Alarm Function

These devices have one alarm system that outputs interrupt signals from INT for PT7C4363C to CPU when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm may be selectable between on and off for matching alarm or repeating alarm.

3. Programmable Square Wave Output

A square wave output enable bit controls square wave output at pin 7. Four frequencies are selectable: 1, 32, 1.024k, and 32.768kHz.

4. Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).
Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.
The SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

5. Oscillator Fail Detect

When oscillator fail, OSF bit will be set.

6. Oscillator Enable/Disable

Only time count chain can be enable or disable by STOP bit.

7. Timer Function

The timer control register determines one of 4 source clock frequencies for the timer (4096Hz, 64Hz, 1Hz, or 1/60Hz) and enables or disables the timer. The timer counts down from software loaded 8-bit binary value. At the end of every countdown, the timer sets the Timer Flag (TF). The TF may only be cleared by software. The asserted TF can be used to generate an interrupt. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. Bit TI/TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

8. Reset Function

The PT7C4363C includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C-bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, OSF, TD1, TD0, TESTC and AE which are set to logic 1.

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Registers

1. Allocation of Registers

Addr. (hex) *1	Function (time range BCD format)	Register Definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Control/status 1	TEST1*	-	STOP*3	-	TESTC*4	-	-	-
01	Control/status 2	-	-	-	TI/TP*5	AF*6	TF*6	AIE*7	TIE*7
02	Seconds (00-59)	OSF*8	S40	S20	S10	S8	S4	S2	S1
03	Minutes (00-59)	×	M40	M20	M10	M8	M4	M2	M1
04	Hours (00-23)	×	×	H20	H10	H8	H4	H2	H1
05	Dates (01-31)	×	×	D20	D10	D8	D4	D2	D1
06	Days of the week (00-	×	×	×	×	×	W4	W2	W1
07	Months (01-12)	Century	×	×	MO10	MO8	MO4	MO2	MO1
08	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
09	Alarm: Minutes (00-59)	AE*9	M40	M20	M10	M8	M4	M2	M1
0A	Alarm: Hours (01-12)	AE*9	×	H20	H10	H8	H4	H2	H1
0B	Alarm: Dates (01-31)	AE*9	×	D20	D10	D8	D4	D2	D1
0C	Alarm: Weekday (00-06)	AE*9	×	×	×	×	W4	W2	W1
0D	SQW control	SQWE	×	×	×	×	×	RS1	RS0
0E	Timer control	TE*10	×	×	×	×	×	TD1*11	TD0*11
0F	Timer	Timer count down value							

Caution points:
*1. PT7C4363C uses 8 bits for address. For excess 0FH address, PT7C4363C will not respond.
*2. EXT_CLK test mode select bit.
*3. When the bit is logic 1, time count chain stops but oscillator still runs.
*4. Power-on reset override enable bit.
*5. Timer interrupt output select bit.
*6. Alarm and timer interrupt flag bits.
*7. Alarm and timer interrupt enable bits.
*8. Oscillator fail indicates. Indicate clock integrity.
*9. Alarm enable bit. Alarm will be active when related time is matching if AE = 0.
*10. Timer enable bit.
*11. Timer source clock frequency select.
*12. All bits marked with "×" are not implemented. All bits marked with "-" are not used bits and should always be written with logic 0. If read them, they could be logic 0 or 1.

2. Control and Status Register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Control/status 1	TEST1	-	STOP	-	TESTC	-	-	-
	(default)	0	Undefined	0	Undefined	1	Undefined	Undefined	Undefined
01	Control/status 2	-	-	-	TI/TP	AF	TF	AIE	TIE
	(default)	Undefined	Undefined	Undefined	0	Undefined	Undefined	0	0
0D	SQW control	SQWE	×	×	×	×	×	RS1	RS0
	(default)	1	Undefined	Undefined	Undefined	Undefined	Undefined	0	0
0E	Timer control	TE	×	×	×	×	×	TD1	TD0
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	1	1
0F	Timer	Timer count down value							
	(default)	Undefined							

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a) Timer

- **TE:** Timer Enable bit.

TE	Data	Description	
Read / Write	0	Timer disabled	Default
	1	Timer enabled	

- **TD1, TD0:** timer source clock frequency select. These bits determine the source clock for the countdown timer.

TD1, TD0	Data	Timer source clock freq. (Hz)	
Read / Write	00	4.096k	
	01	64	
	10	1	
	11	1/60	When not in use, TD1 TD0 should be set to 11 for power saving.

- **Timer:**

Timer	Data	Description	
Read / Write	00~FF	Count down value (n)	Countdown Period = n / Source Clock Frequency

For example: If TE = 1, TD1 TD0 = 10, Timer = 03 are written into PT7C4363C, timer counts down every 1 second from 03 to 01 then 03 cycled.

b) Timer Interrupt

- **TIE:** Timer Interrupt Enable bit.

TIE	Data	Description	
Read / Write	0	Timer interrupt disabled	Default
	1	Timer interrupt enabled	

- **TF:** Timer Flag

TF	Data	Description
Read	0	Timer flag inactive
	1	Timer flag active. At the end of a timer countdown, TF is set to 1.
Write	0	Timer flag is cleared
	1	Timer flag remains unchanged

- **TI/TP:** Timer Interrupt output select

TI/TP	Data	Description
Read / Write	0	$\overline{\text{INT}}$ is active when TF is active (subject to the status of TIE)
	1	$\overline{\text{INT}}$ pulses active according to source clock frequency and timer count down value (subject to the status of TIE).

Source clock (Hz)	INT negative pulse width (s)	
	n = 1	n > 1
4096	$^1/_{8192}$	$^1/_{4096}$
64	$^1/_{128}$	$^1/_{64}$
1	$^1/_{64}$	$^1/_{64}$
1/60	$^1/_{64}$	$^1/_{64}$

Note: TF and INT become active simultaneously.
n = loaded countdown value. Timer stopped when n = 0.

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Example 1: If TE = 1, TD1 TD0 = 00, Timer = 03, TIE = 1, TF = 0, TI/TP = 1 are written into PT7C4363C, timer register counts down every $^1/_{4.096kHz}$ seconds from 03 to 01 then 03 cycled and $\overline{INT}$ output negative pulse with $^1/_{4096}$ seconds width. See Fig.1.

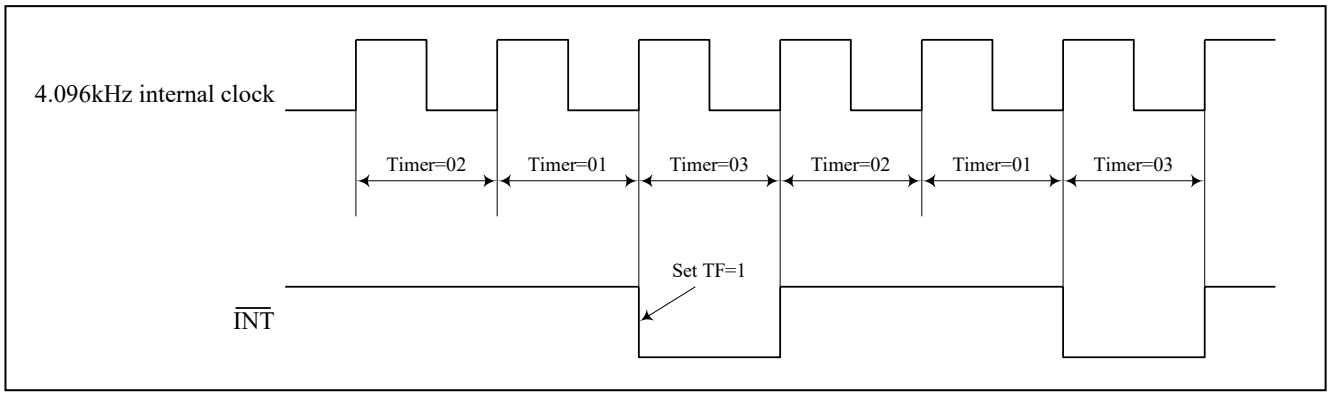


Figure 1. Example 1 of Timer Interrupts

Example 2: If TE = 1, TD1 TD0 = 10, Timer = 03, TIE = 1, TF = 0, TI/TP = 1 are written into PT7C4363C, timer counts down every $^1/_{4.096kHz}$ seconds from 03 to 01 then 03 cycled and $\overline{INT}$ output negative pulse with $^1/_{64}$ seconds width. See Fig.2.

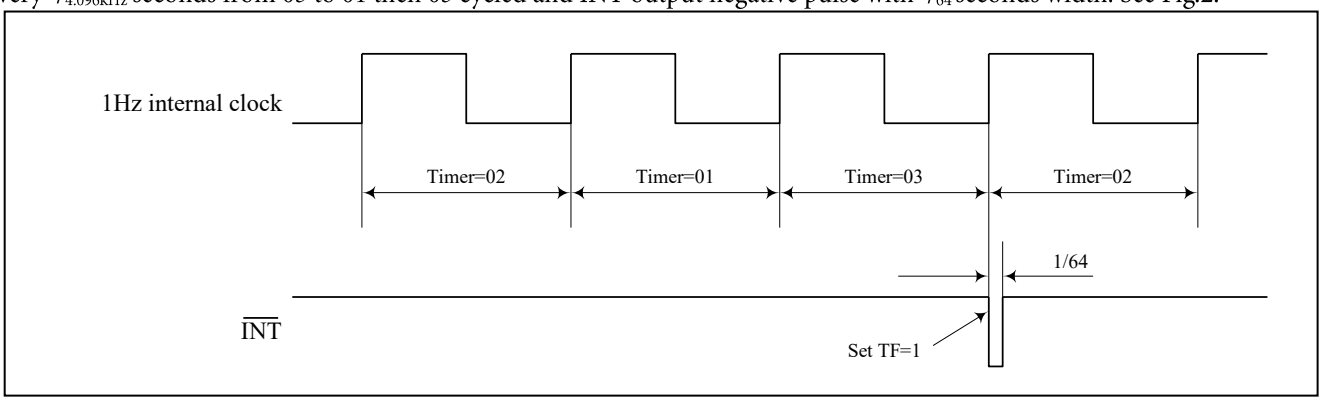


Figure 2. Example 2 of Timer Interrupts

c) Alarm Interrupt

- **AIE:** Alarm Interrupt Enable bit.

AIE	Data	Description	
Read / Write	0	Alarm interrupt disabled	Default
	1	Alarm interrupt enabled	

- **AF:** Alarm Flag

AF	Data	Description
Read	0	Alarm flag inactive
	1	Alarm flag active
Write	0	Alarm flag is cleared
	1	Alarm flag remains unchanged

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d) SQW Control

- **SQWE:** SQW output clock enable bit.

SQWE	Data	Description	
Read / Write	0	the SQW output is inhibited and SQW output is set to high-impedance	
	1	the SQW output is activated	Default

- **RS1, RS0:** SQW output frequency select.

RS1, RS0	Data	SQW output freq. (Hz)	
Read / Write	00	32.768k	Default
	01	1.024k	
	10	32	
	11	1	

e) Time Count

- **STOP**

STOP	Data	Description	
Read / Write	0	RTC source clock runs.	Default
	1	All RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (SQW at 32.768 kHz is still available)	

f) Test

- **TEST1**

TEST1	Data	Description	
Read / Write	0	Normal mode.	Default
	1	EXT_CLK test mode.	

- **TESTC**

TESTC	Data	Description	
Read / Write	0	Power-on reset override facility is disabled; set to logic 0 for normal operation.	
	1	Power-on reset override may be enabled	Default

3. Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
02	Seconds	OSF*1	S40	S20	S10	S8	S4	S2	S1
	(default)	1	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
03	Minutes	×	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
04	Hours	×	×	H20	H10	H8	H4	H2	H1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

***1 Note:** Indicate clock integrity. When the bit is 1, the clock integrity is no longer guaranteed and the time need be adjusted.
***2 Note:** Before reading time counter, user needs to initialize the date/time after RTC is powered up, or when the OSF bit is 1 (Oscillator failure).

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4. Days of the Week Counter

The day counter is a divide-by-7 counter that counts from 00 to 06 and up 06 before starting again from 00. Values that correspond to the day of week are user defined but must be sequential (i.e., if 0 equals Sunday, then 1 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
06	Days of the week	×	×	×	×	×	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

5. Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
05	Dates	×	×	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
07	Months	Century*1	×	×	M10	M8	M4	M2	M1
	(default)	Undefined	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
08	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

***1:** The century bit is toggled when the years register overflows from 99 to 00.

6. Alarm Register

PT7C4363C: Alarm Register

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
09	Alarm: Minutes	AE*1	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0A	Alarm: Hours	AE*2	×	H20	H10	H8	H4	H2	H1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0B	Alarm: Dates	AE*3	×	D20	D10	D8	D4	D2	D1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0C	Alarm: Weekday	AE*4	×	×	×	×	W4	W2	W1
	(default)	Undefined	0	0	0	0	Undefined	Undefined	Undefined

***1** Note: Minute alarm enable bit.
***2** Note: Hour alarm enable bit.
***3** Note: Date alarm enable bit.
***4** Note: Weekday alarm enable bit.

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Alarm Function

Related Register

	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	Control/status 2	-	-	-	TI/TP	AF	TF	AIE	TIE
02	Seconds	OSF	S40	S20	S10	S8	S4	S2	S1
03	Minutes	×	M40	M20	M10	M8	M4	M2	M1
04	Hours	×	×	H20	H10	H8	H4	H2	H1
05	Dates	×	×	D20	D10	D8	D4	D2	D1
06	Days of the week	×	×	×	×	×	W4	W2	W1
09	Alarm: Minutes	AE	M40	M20	M10	M8	M4	M2	M1
0A	Alarm: Hours	AE	×	H20	H10	H8	H4	H2	H1
0B	Alarm: Dates	AE	×	D20	D10	D8	D4	D2	D1
0C	Alarm: Weekday	AE	×	×	×	×	W4	W2	W1

When one or more of these registers are loaded with a valid minute, hour, day or weekday and its corresponding bit Alarm Enable (AE) is logic 0, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their bit AE at logic 1 will be ignored.

EXT_CLK Test Mode and POR Override

1. EXT_CLK Test Mode

A test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC. The test mode is entered by setting bit TEST1 in control/status1 register. Then pin SQW becomes an input. The test mode replaces the internal 64 Hz signal with the signal applied to pin SQW. Every 64 positive edges applied to pin SQW will then generate an increment of one second.

The signal applied to pin SQW should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal 64 Hz clock, now sourced from SQW, is divided down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using bit STOP. When bit STOP is set, the pre-scaler is
reset to 0 (STOP must be cleared before the pre-scaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on SQW. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

Operation example:

1. Set EXT_CLK test mode (control/status 1, bit TEST1 = 1)
2. Set STOP (control/status 1, bit STOP = 1)
3. Clear STOP (control/status 1, bit STOP = 0)
4. Set time registers to desired value
5. Apply 32 clock pulses to SQW
6. Read time registers to see the first change
7. Apply 64 clock pulses to SQW
8. Read time registers to see the second change.

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Repeat 7 and 8 for additional increments.

2. Power-On Reset (POR) override

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I²C-bus pins, SDA and SCL, be toggled in a specific order as shown in Fig 6.4.2. All timings are required minimums.

Once the override mode has been entered, the device immediately stops being reset and normal operation may commence i.e. entry into the EXT_CLK test mode via I²C-bus access.

The override mode may be cleared by writing a logic 0 to TESTC. TESTC must be set to logic 1 before re-entry into the override mode is possible. Setting TESTC to logic 0 during normal operation has no effect except to prevent from entering the POR override mode.

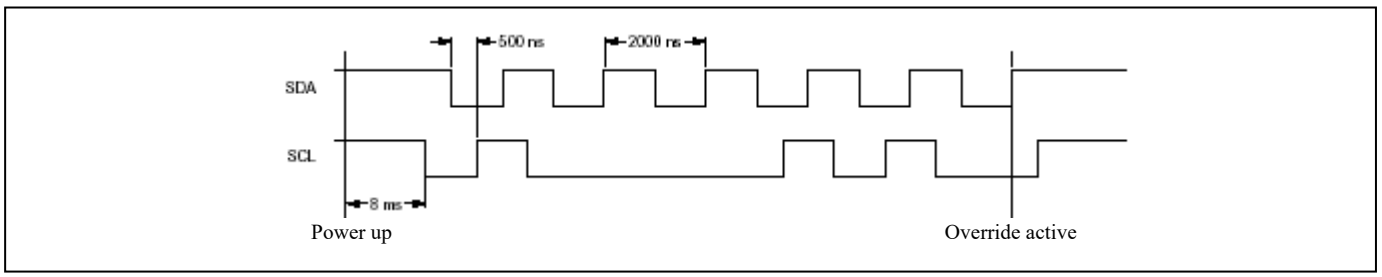


Figure 3. POR Override Sequence

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Communication

1. I²C Bus Interface

a) Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on.
Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

b) System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

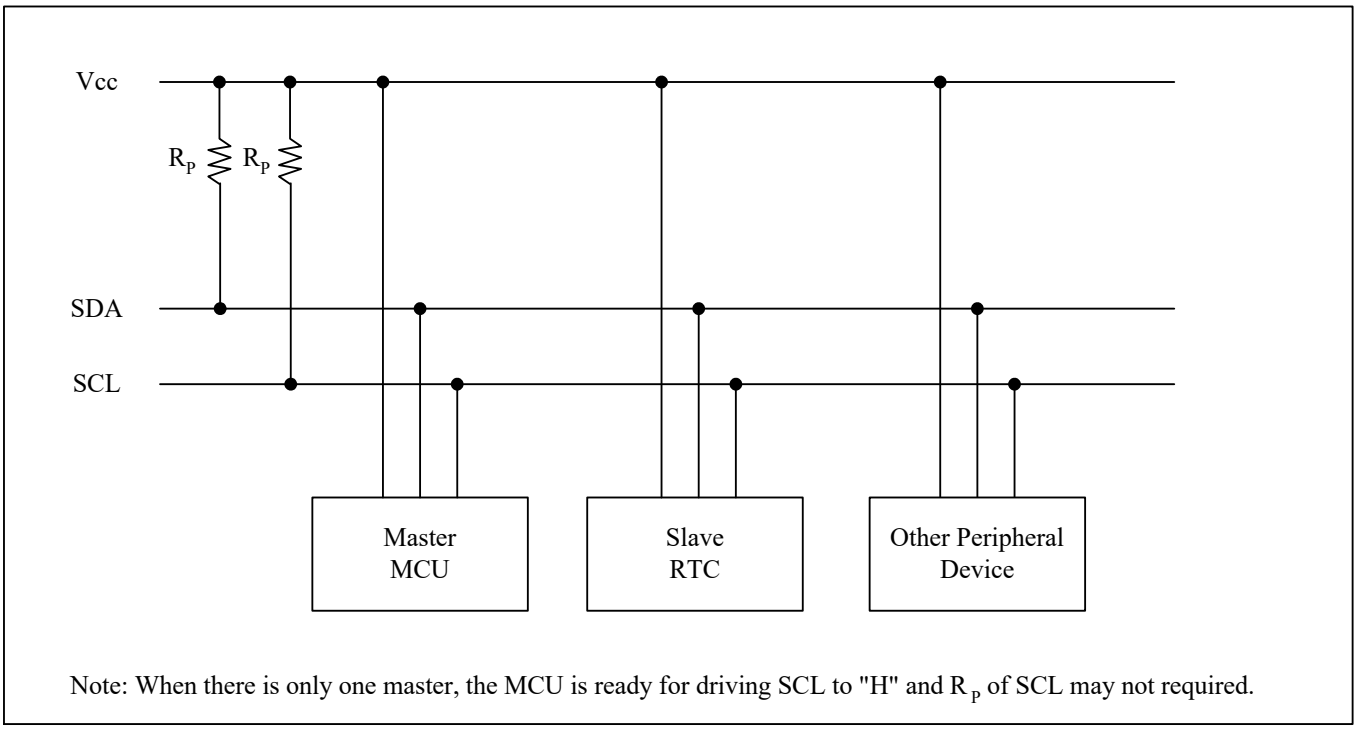


Figure 4. System Configuration

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c) Starting and Stopping I²C Bus Communications

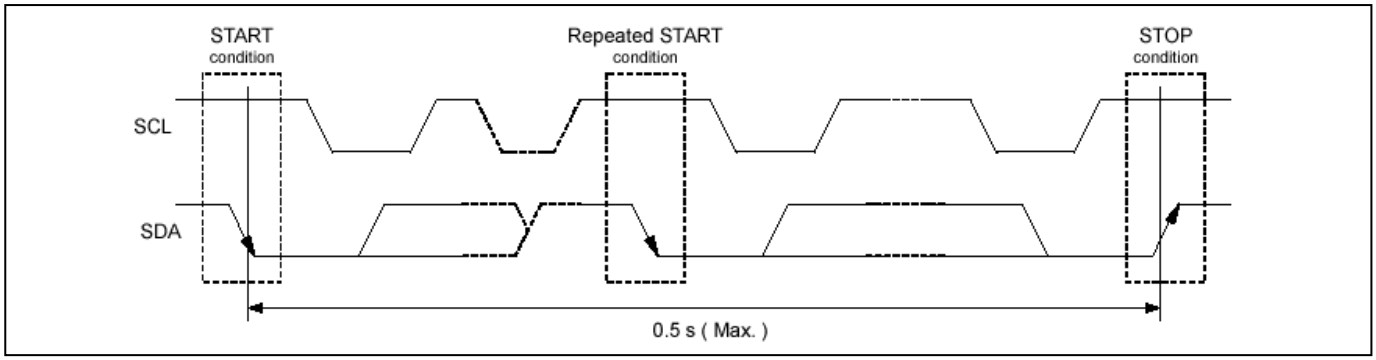


Figure 5. Starting and stopping on I²C bus

START condition, repeated START condition, and STOP condition

- START condition
  SDA level changes from high to low while SCL is at high level
- STOP condition
  SDA level changes from low to high while SCL is at high level
- Repeated START condition (RESTART condition)

In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

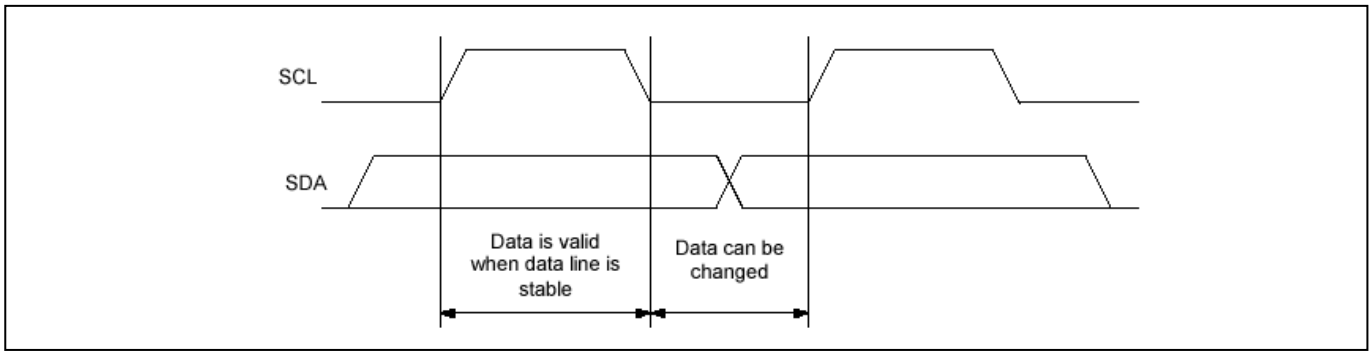
d) Data Transfers and Acknowledge Responses during I²C-BUS Communication

- **Data Transfers**

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.



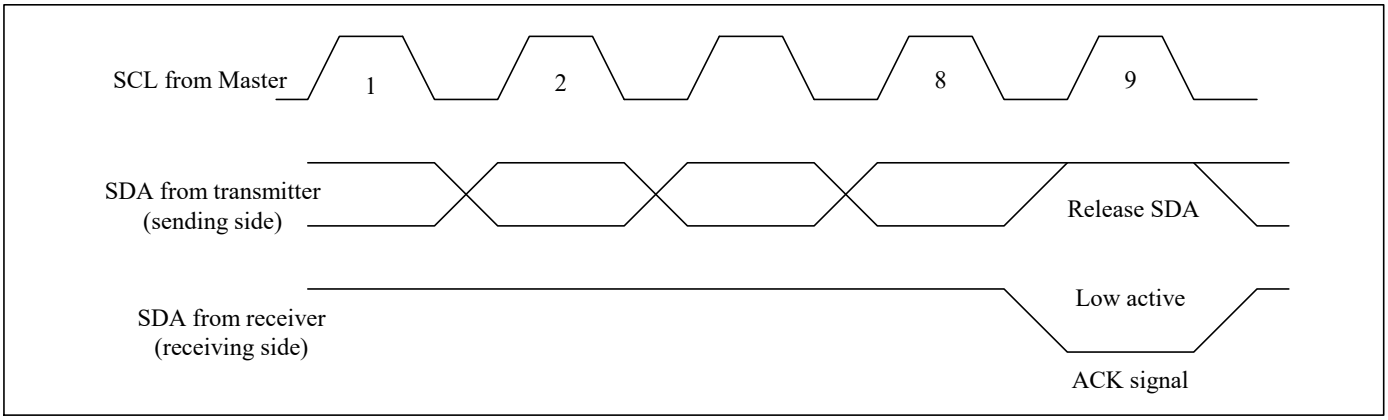
*Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

- **Data Acknowledge Response (ACK Signal)**

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.

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After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

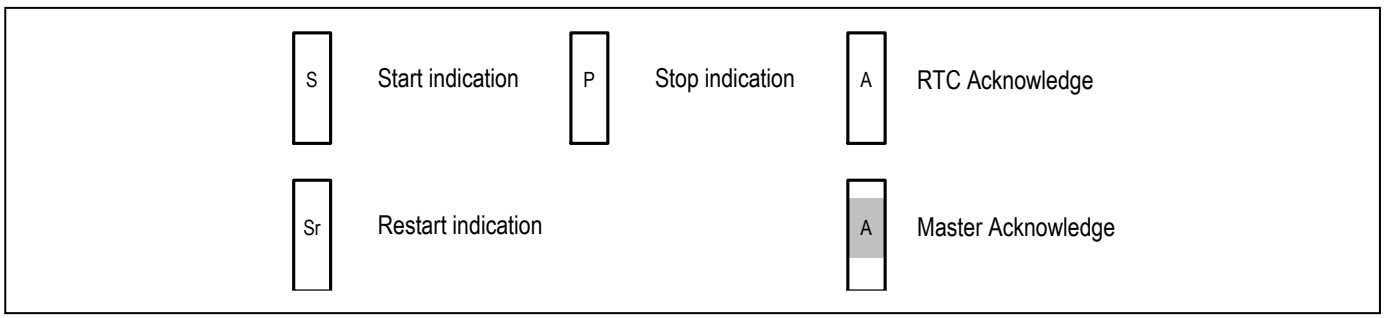
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

e) Slave Address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ $\overline{R}$/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.
Slave addresses have a fixed length of 7 bits. See table for the details.
An R/$\overline{W}$ bit is added to each 7-bit slave address during 8-bit transfers.

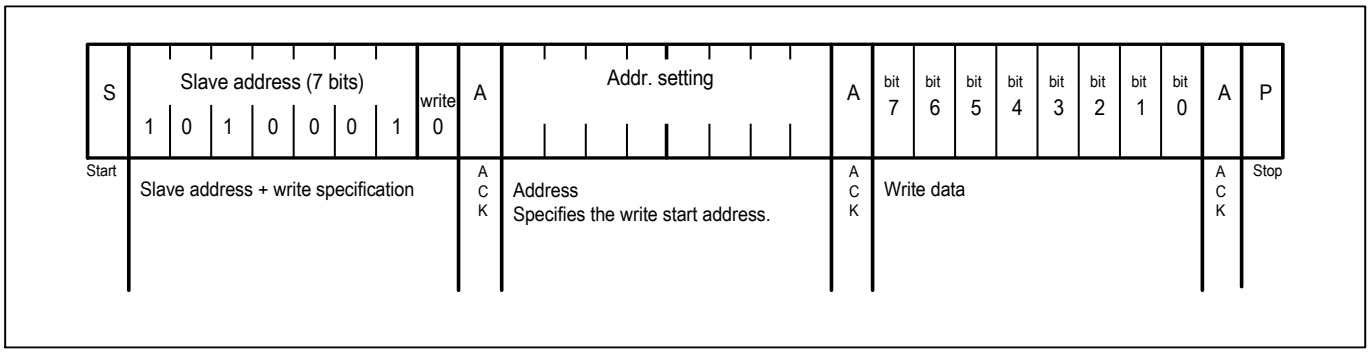
Operation	Transfer Data	Slave Address							R / $\overline{W}$ bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	A3 h	1	0	1	0	0	0	1	1 (= Read)
Write	A2 h								0 (= Write)

2. I²C Bus's Basic Transfer Format



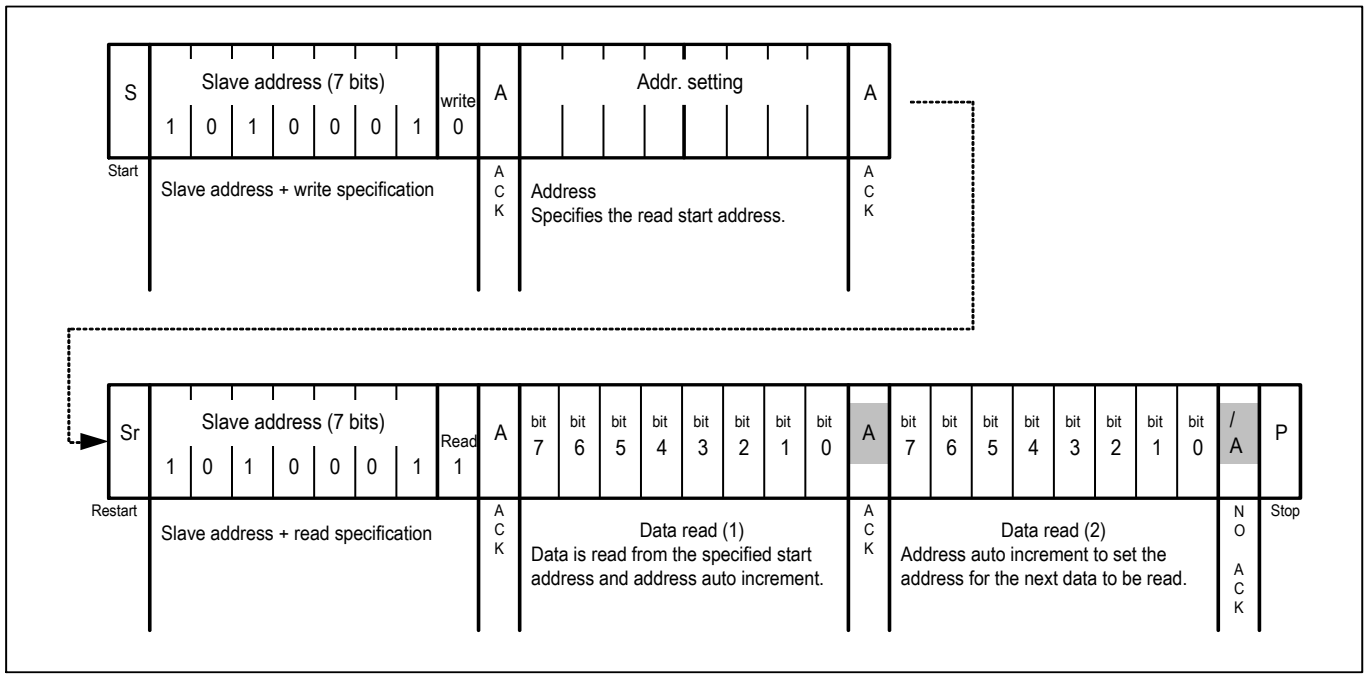
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a) Write via I²C Bus

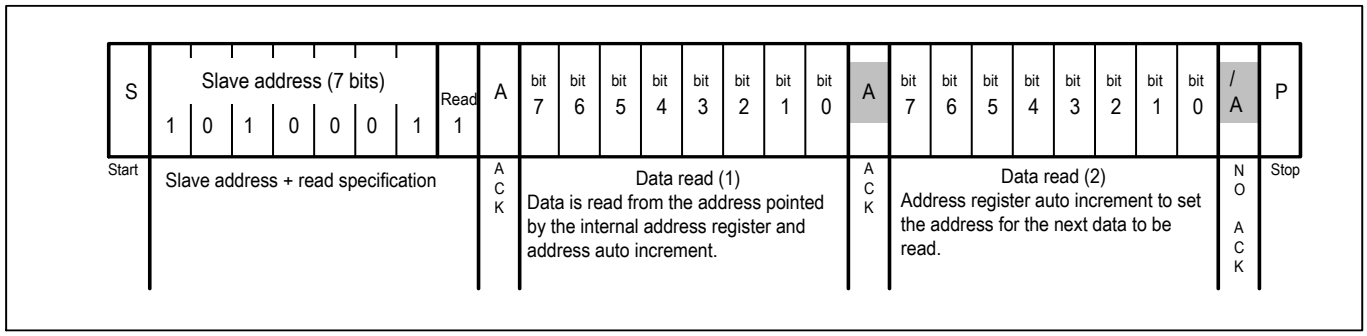


b) Read via I²C Bus

- **Standard Read**



- **Simplified Read**

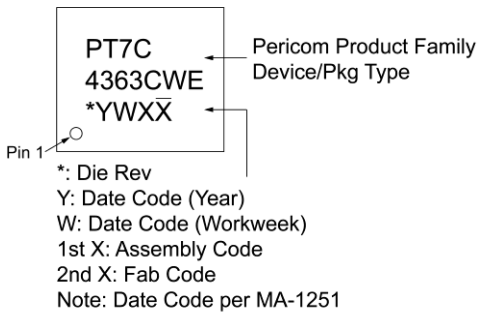


Note:
1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
2. 49H, 4AH are used as test mode address. Customer should not use the addresses.

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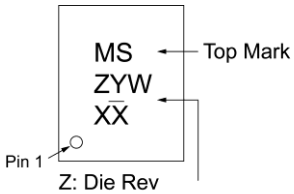
Part Marking

SOIC (W) Package



*: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Note: Date Code per MA-1251

W-DFN2030 (ZG) Package



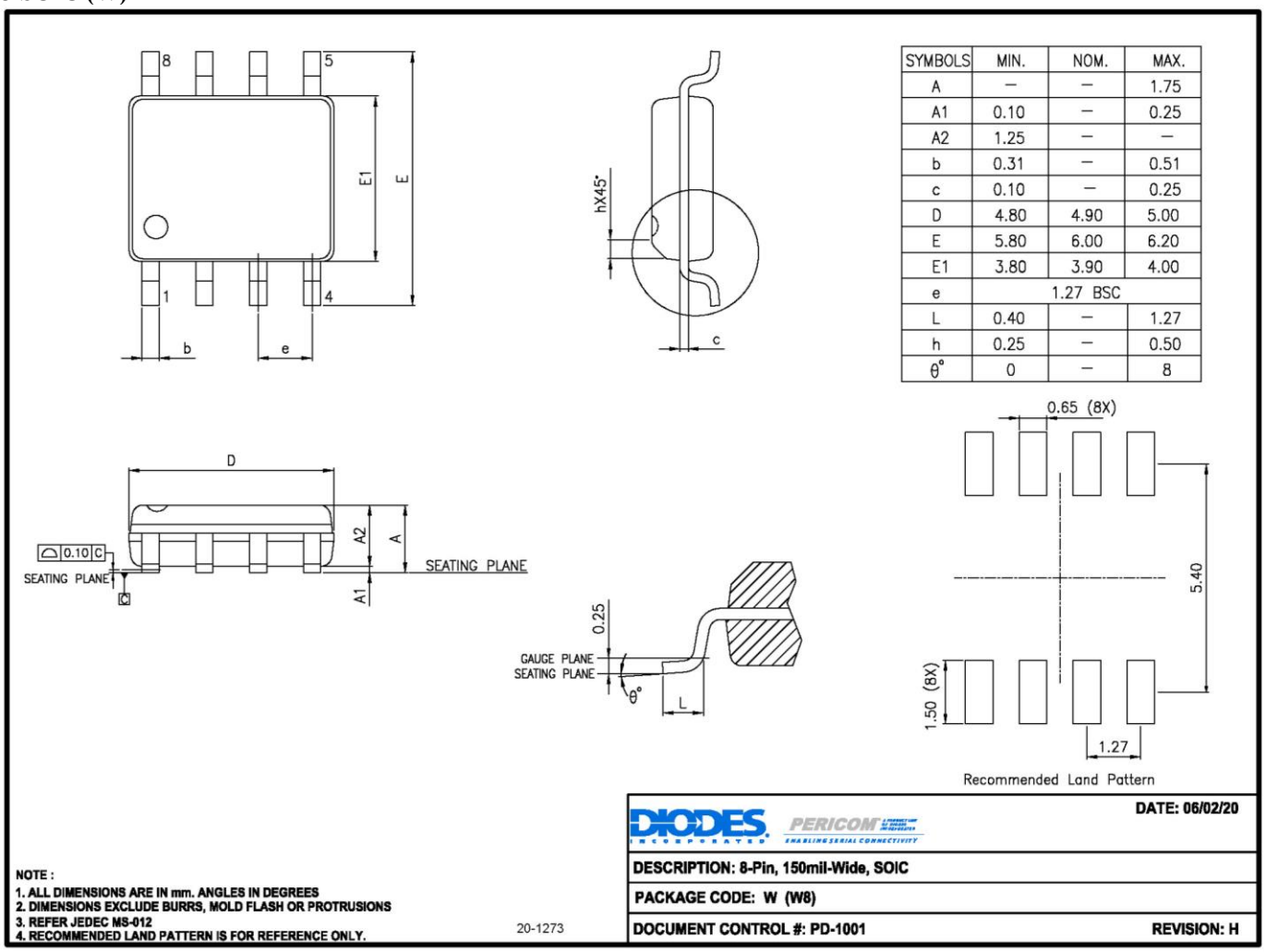
Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Note: Date Code per MA-1251

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Packaging Mechanical

8-SOIC (W)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

20-1273

DATE: 06/02/20

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

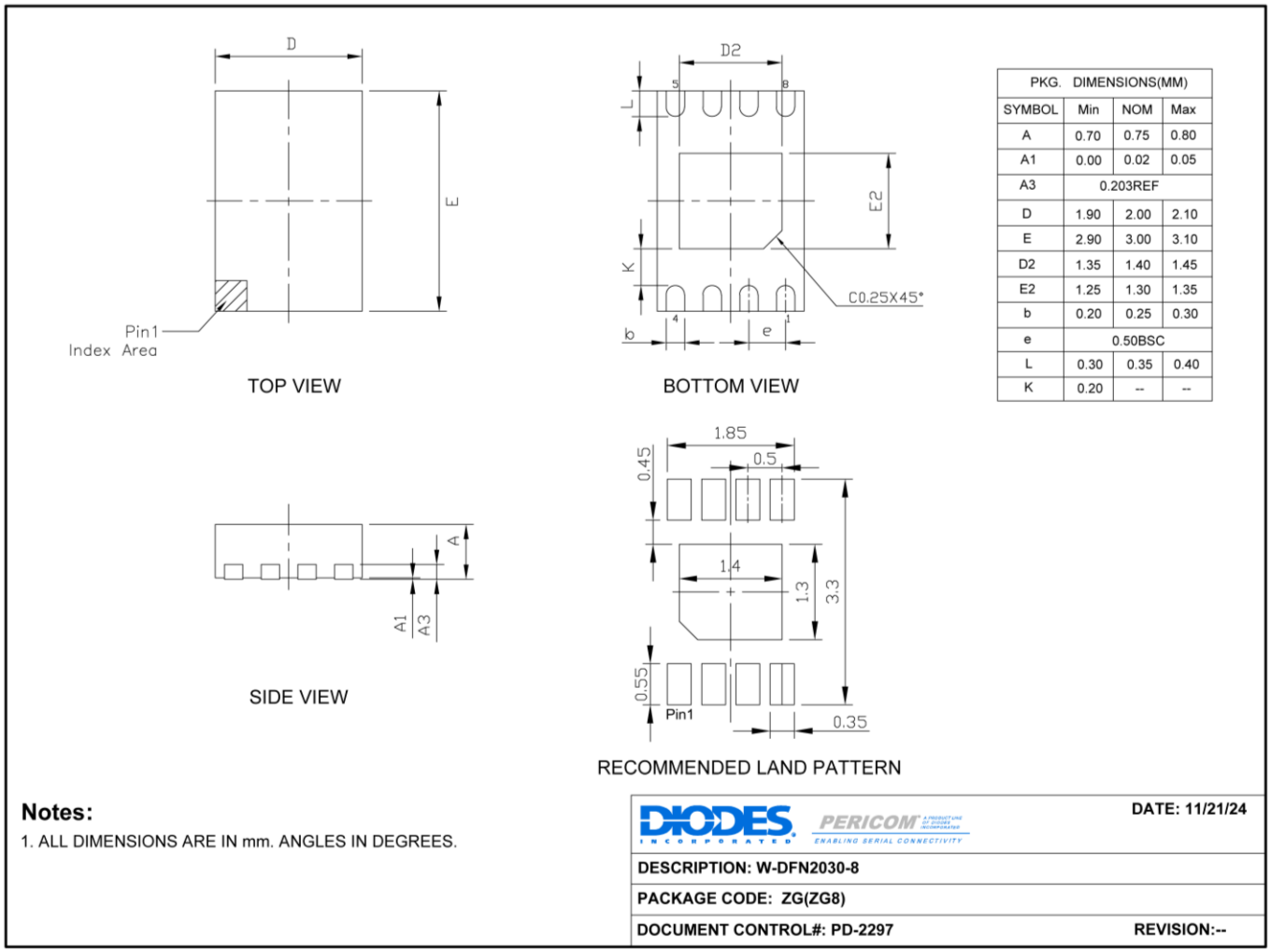
PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 REVISION: H

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8-WDFN2030 (ZG)



PKG. DIMENSIONS(MM)			
SYMBOL	Min	NOM	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203REF		
D	1.90	2.00	2.10
E	2.90	3.00	3.10
D2	1.35	1.40	1.45
E2	1.25	1.30	1.35
b	0.20	0.25	0.30
e	0.50BSC		
L	0.30	0.35	0.40
K	0.20	--	--

Notes:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.

DATE: 11/21/24

DESCRIPTION: W-DFN2030-8

PACKAGE CODE: ZG(ZG8)

DOCUMENT CONTROL#: PD-2297 REVISION:--

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Mechanical Data

SOIC-8 (W) Package

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin (Sn) Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.078719 grams (Approximate)

WDFN2030-8 (ZG) Package

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin (Sn) Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.01998 grams (Approximate)

Ordering Information

Orderable Part Number	Package Code	Package Description
PT7C4363CWEX	W	8-Pin, 150mil Wide (SOIC)
PT7C4363CZGEX	ZG	8-Pin, W-DFN2030-8 (WDFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
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