

Features

- Compliant with HDMI 1.4a specification up to 3.4 Gbps
- Low Intra-pair and Inter-pair skews
- Single 3.3 V Power Supply
- -40°C to 85°C Operating Temperature Range
- Integrated DP++ passive level shifter (48pin version only)
- HPD Detection
 - TMDS path auto-turn-off when HPD is not present
- Supports DC and AC Coupled inputs (48-contact TQFN version only)
- Integrated ESD protection to +/-4KV Contact on all I/O pins per IEC61000-4-2 standard
- Package (Pb-free and Green available)
 - 48-contact TQFN, 7mm x 7mm (ZBE)
 - 42-contact TQFN, 9mm x 3.5mm (ZHE)

Applications

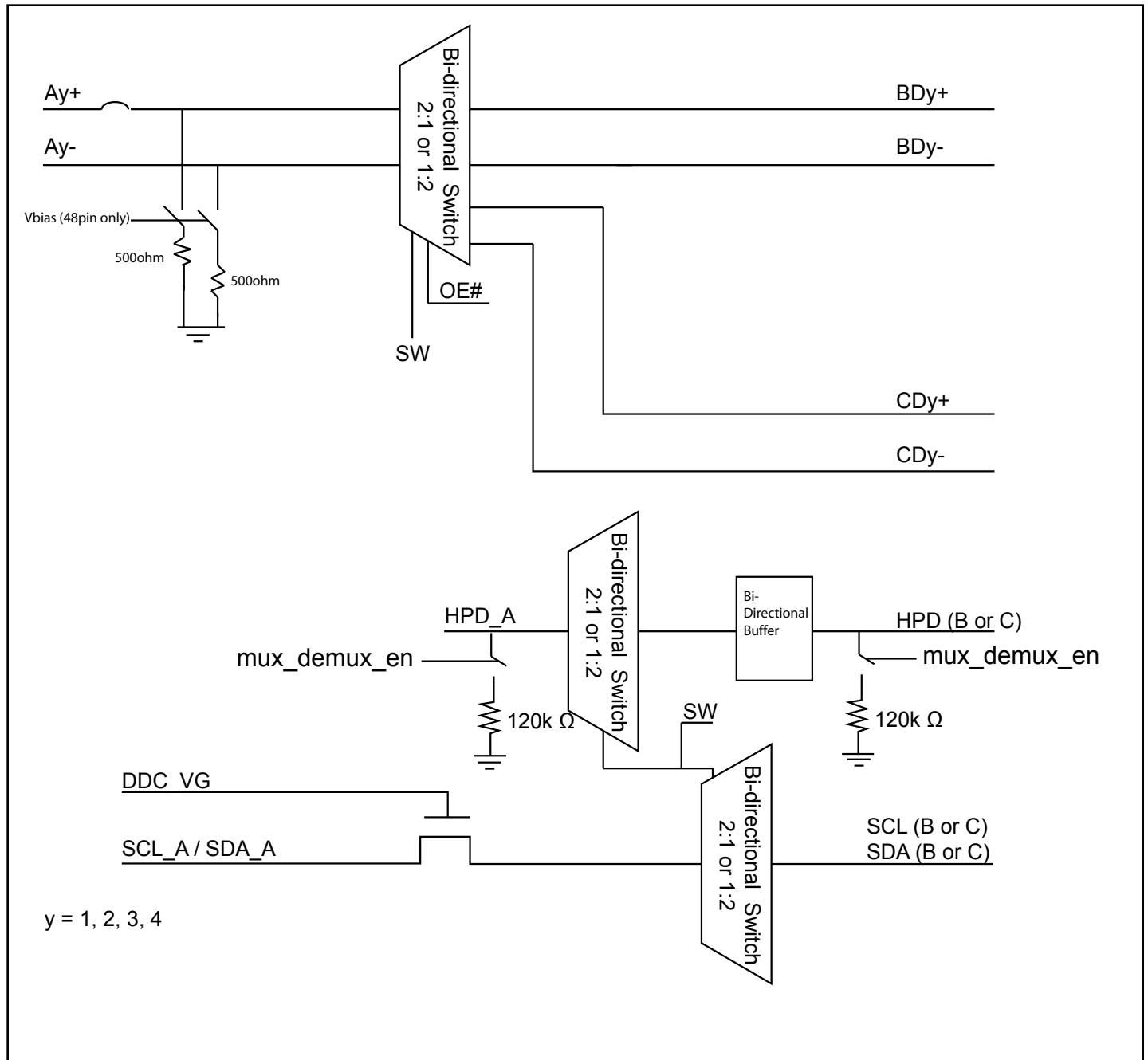
- HDMI Sink (monitor or DTV)
- PC Motherboard / Graphics Card
- Digital Set-Top-Box
- 1-to-2 DP & HDMI/DVI Switch Box
- DVD player
- HDMI/DVI monitor or TV

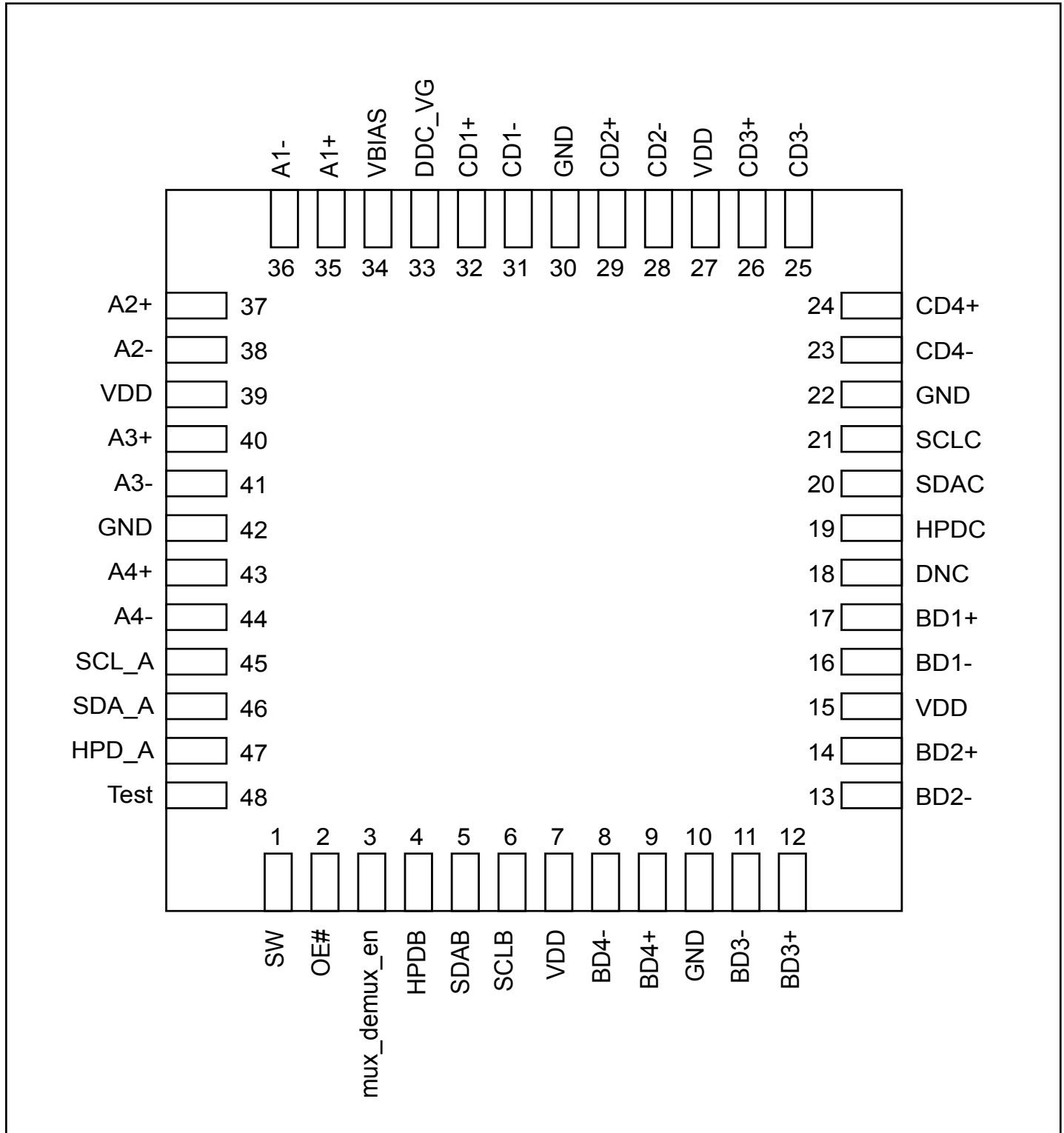
Description

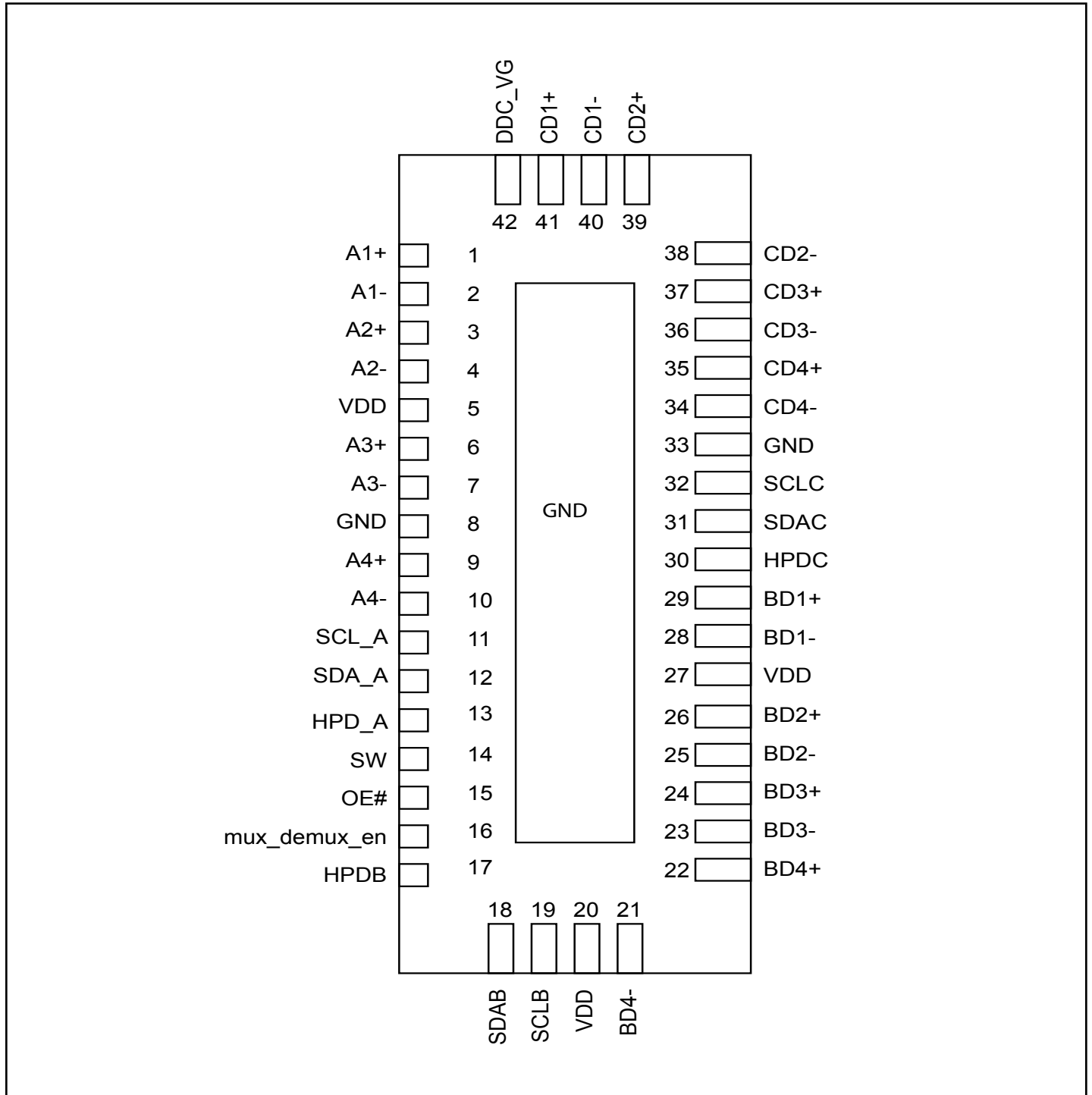
PI3HDMI1421 is industries lowest power HDMI mux/demux supporting up to 3.4Gbps signal throughput per channel. the PI-3HDMI1421 supports switching all TMDS channels, HPD channel, and the DDC channels. The part can behave as 1:2 demux or a 2:1 mux, since all signal paths are passive and therefore can support bi-directional data-traffic.

With integrated ESD protection up to +/-4kV contact per IEC61000-4-2, the PI3HDMI1421 is ideal for consumer applications.

Functional Block Diagram



Pin Configuration (TQFN-48)


Pin Configuration (TQFN-42)


Pin Description

Name	I/O	Description																
mux_demux_en	I	H=1:2 demux; L=2:1 mux																
DNC	-	Leave pin no connect (do not tie to GND or VDD)																
Ay+	I/O	y = 1, 2, 3, 4, for positive differential data or clock inputs.																
Ay-	I/O	y = 1, 2, 3, 4, for negative differential data or clock inputs.																
xDy+	I/O	x = B,C; y = 1, 2, 3, 4 for positive differential outputs.																
xDy-	I/O	x = B,C; y = 1, 2, 3, 4 for negative differential outputs.																
HPDx	I/O	When mux_demux_en=High, internal pull-down at ~120Kohm is enabled. HPDx is 5V tolerant.																
HPD_A	I/O	When mux_demux_en=Low, internal pull-down at ~120Kohm is enabled. HPD_A is 5V tolerant.																
SDA_A, SCL_A	I/O	DDC channel pins to SOURCE These pins are 5 V tolerant and should be connected to Source side.																
SDAx, SCLx	I/O	x = B, C. These pins are DDC channel pins SDAx/SCLx. These pins are 5V tolerant and should be connected to Sink side.																
Test	I	For normal operation, please tie to GND																
SW	I	<table><tr><td colspan="4">Output Port control</td></tr><tr><td>SW</td><td>Port A connects to B</td><td>Port A connects to C</td><td>HPD_A</td></tr><tr><td>0</td><td>Enable</td><td>Hi-Z</td><td>HPDB</td></tr><tr><td>1</td><td>Hi-Z</td><td>Enable</td><td>HPDC</td></tr></table>	Output Port control				SW	Port A connects to B	Port A connects to C	HPD_A	0	Enable	Hi-Z	HPDB	1	Hi-Z	Enable	HPDC
Output Port control																		
SW	Port A connects to B	Port A connects to C	HPD_A															
0	Enable	Hi-Z	HPDB															
1	Hi-Z	Enable	HPDC															
OE#	I	OE# = HIGH, the chip is in power down mode. OE# = LOW, the chip is in normal operation mode.																
VBIAS (48pin package only)	I	For HDMI/DVI source demultiplexer: Connect to VDD or do not connect. For dual mode DP source demultiplexer: Connect to GND. High speed channel Ax with 500ohm pulled to ground when Vbias is connected to GND																
GND		Ground connection																
VDD	Pwr	Power supply at 3.3V																
DDC_VG	I	GATE voltage for DDC FETs (connect to voltage from 2.5V to 3.6V)																

ABSOLUTE MAXIMUM RATINGS

Parameters	Comments	Unit
Supply Voltage Range		-0.5V to 4V
Normal I/O Voltage Range		-0.5V to 4V
5V Safe I/O Voltage Range	SCL_A, SDA_A, SCLx, SDAx, HPD_A, HPDx	-0.5V to 6V
ESD Pins Ax+/- and xDx+/-	Contact per IEC-61000-4-2	±4kV
	HBM per JESD22	±4kV
Pins SCL/SDA_A, HPD_A, SCL/SDAx, HPDx	Contact per IEC-61000-4-2 HBM per JESD22	±4kV

Normal Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage, VDD	3.0	3.3	3.6	V
Ambient Temperature	-40		+85	°C
Supply Current, I _{CC} (When HPDx = high and OE# = low)			150	uA
Supply Current, I _{CC} (When HPDx = low and OE# = low)			10	uA
Power down Supply Current, (When OE# = high)			10	uA

Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TMDS differential pins						
-3dB BW	-3dB bandwidth	See fig 5		3.7		GHz
R _{on}	Resistance through switch path when ON (A to B or A to C)	All A _x = 2.7V to 3.6V V _{IN} = 3.0V, I = 20mA		8.5		ohm
C _{on}	Capacitance through switch path when ON (A to B or A to C)	All A _x = 2.7V to 3.6V		3.5		pF
IN	insertion loss	@ 2.25Gbps, see fig 5		-1.5		dB
		@ 3.4Gbps, see fig 5		-1.8		
Xtalk	Crosstalk	@ 3.4Gbps. see fig 3		-38		dB
Iso _{off}	Off Isolation	@ 3.4Gbps. see fig 4		-29		dB
T _{SK}	Inter-pair Skew			20		ps
T _{SK}	Intra-pair Skew			10		ps
I _{OFF}	Off Leakage Current			12	20	μA
Control Pins						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _{IH}	High level digital input current(1)	V _{IH} = 2V or V _{DD}	-10		10	μA
I _{IL}	Low level digital input current(1)	V _{IL} = GND or 0.8V	-10		10	
V _{IH}	Input High Voltage		2.4			V
V _{IL}	Input Low Voltage				0.8	
V _{IK}	Input Clamp Voltage			-1.2		

DDC I/O Pins

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _{LK}	Input leakage current	V _I = 0.1 V _{DD} to V _{DD} to isolated DDC inputs	-20		20	μA
C _{IO}	Input/Output capacitance	V _I peak-peak = 1V, 100 KHz			5	pF
R _{ON}	Switch resistance	I _O = 3mA, V _O = 0.4V, DDC		12	15	Ω
V _{IH}	Single-ended high level input voltage		2.4			V
V _{IL}	Single-ended low level input voltage		GND		0.8	V
I _{OFF}	Off Leakage Current			20		μA

HPDx

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _{IH}	High level digital input current	V _{IH} = 2V or V _{DD}	+20		+40	μA
I _{IL}	Low level digital input current	V _{IL} = GND or 0.8V	-20		20	
V _{OL}	Single-ended low level output voltage	I _{OL} = +4mA	GND		0.4	V
V _{OH}	Single-ended high level output voltage	I _{OH} = -4mA	2.4			V
V _{IH}	Single-ended high level input voltage		2.4			V
V _{IL}	Single-ended low level input voltage		GND		0.8	V

Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1µF decoupling capacitor on each V_{DD} pin of our part. Four 0.1µF decoupling capacitors are put in Figure 1 with an assumption of only four V_{DD} pins on our part. If there is more or less V_{DD} pins on our part, the number of 0.1µF decoupling capacitors should be adjusted according to the actual number of V_{DD} pins. On top of 0.1µF decoupling capacitor on each V_{DD} pin, it is recommended to put a 10µF decoupling capacitor near our part's V_{DD}, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

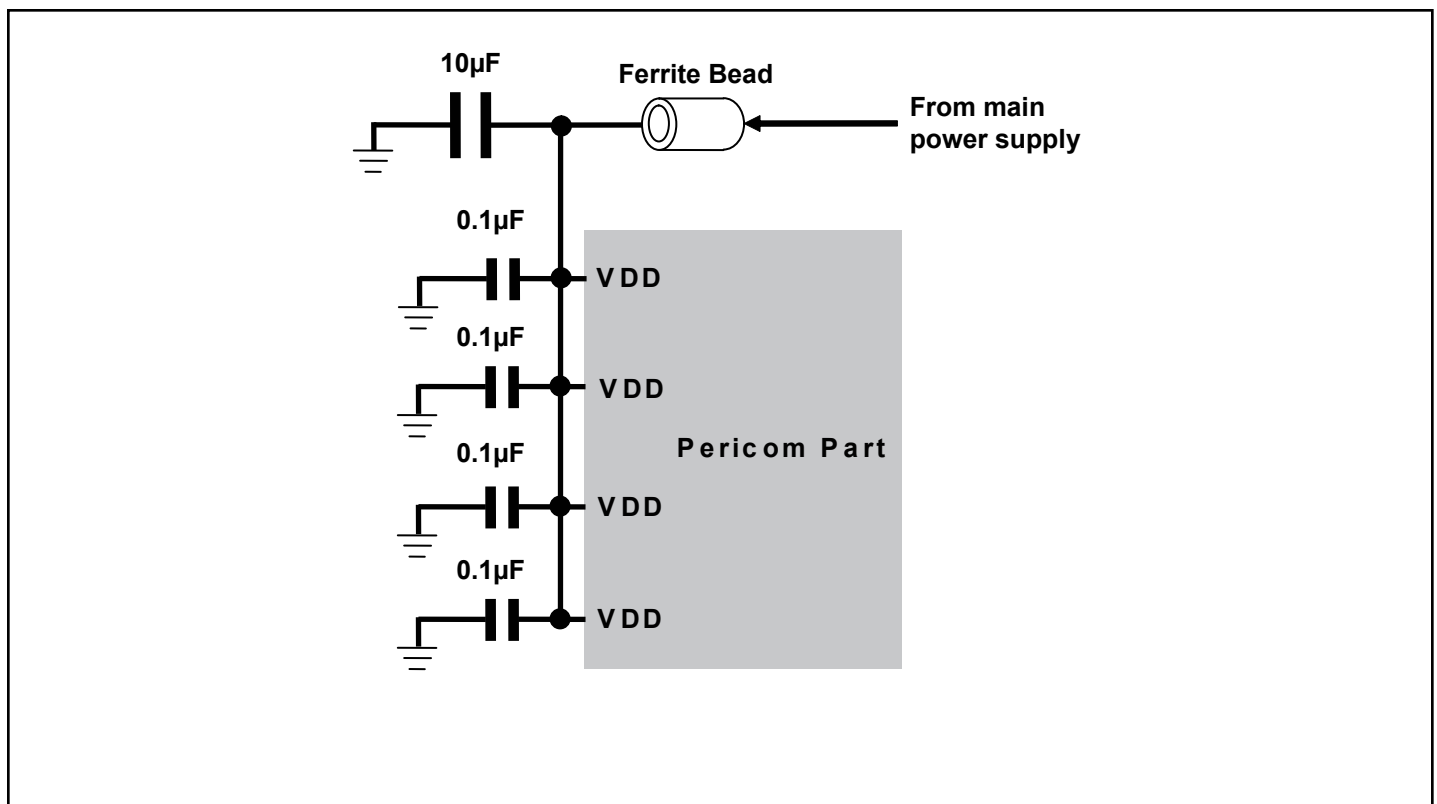


Figure 1: Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

- i. There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.
- ii. 0.1 μ F decoupling capacitor in 0402 package is recommended.

Layout and Decoupling Capacitor Placement Consideration

- i. Each 0.1 μ F decoupling capacitor should be placed as close as possible to each V_{DD} pin.
- ii. V_{DD} and GND planes should be used to provide a low impedance path for power and ground.
- iii. Via holes should be placed to connect to V_{DD} and GND planes directly.
- iv. Trace should be as wide as possible.
- v. Trace should be as short as possible.
- vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- vii. 10 μ F capacitor should also be placed close to our part and should be placed in the middle location of 0.1 μ F capacitors.
- viii. Avoid the large current circuit placed close to our part; especially when it is shared the same V_{DD} and GND planes, since large current flowing on our V_{DD} or GND planes will generate a potential variation on the V_{DD} or GND of our part.

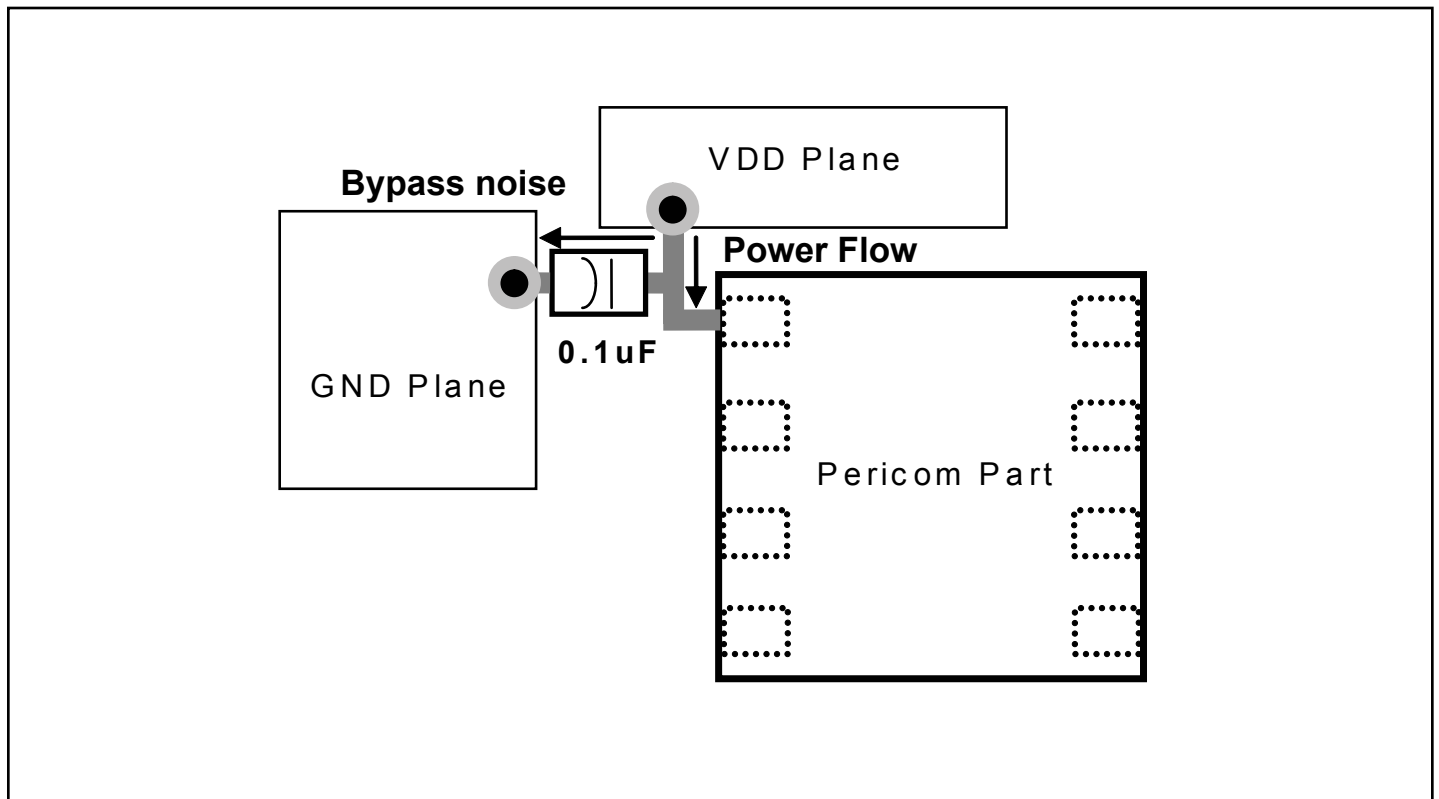


Figure 2: Layout and Decoupling Capacitor Placement Diagram

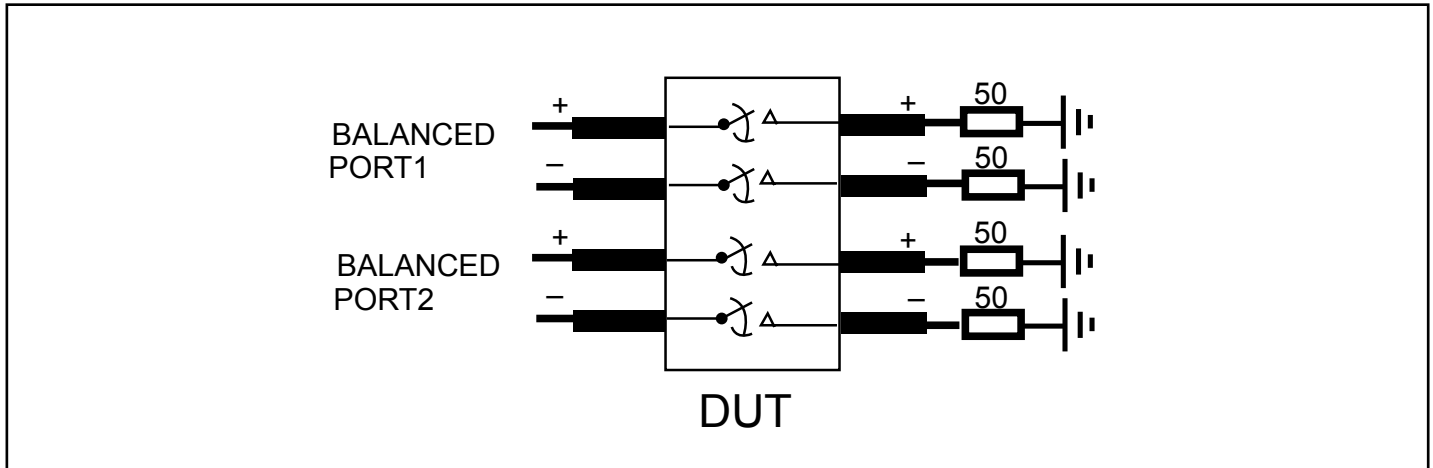


Fig 3: Crosstalk Setup

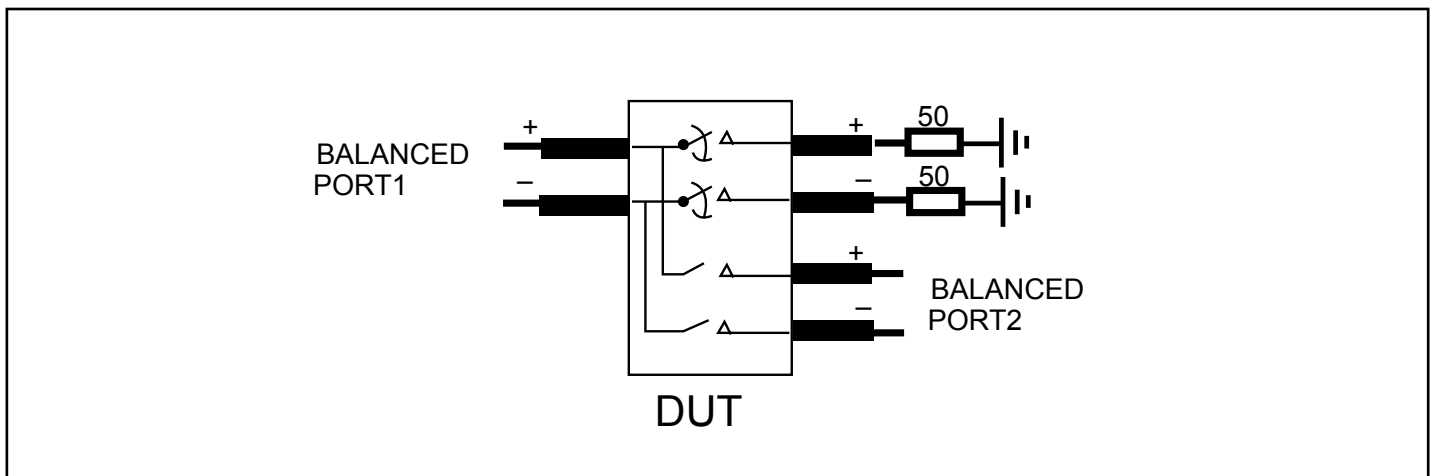


Fig 4: Off-isolation setup

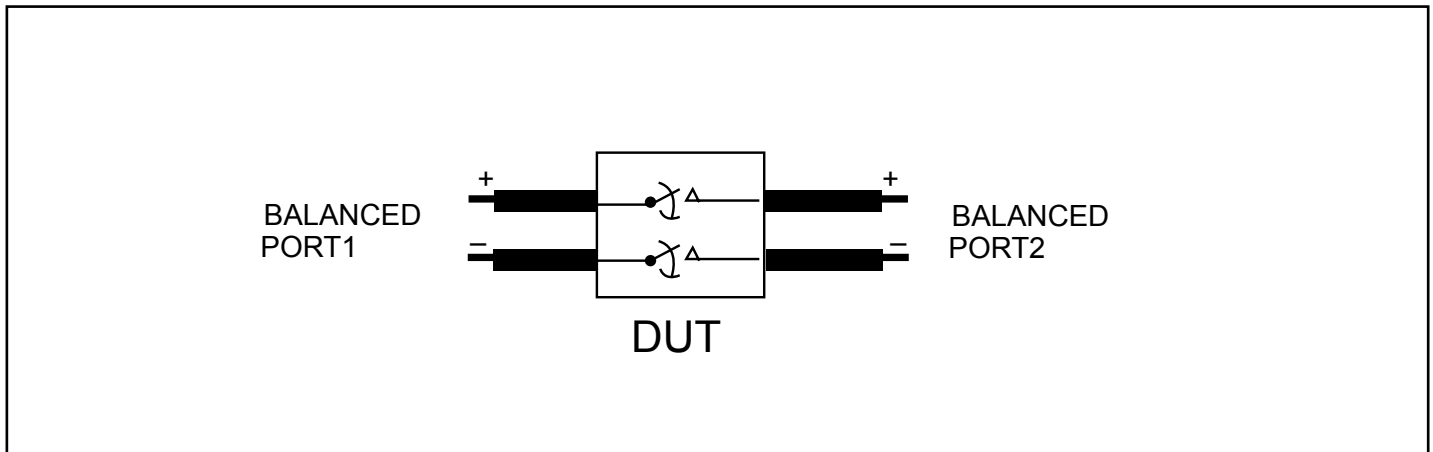


Fig 5: Differential Insertion Loss and -3dB Test Setup

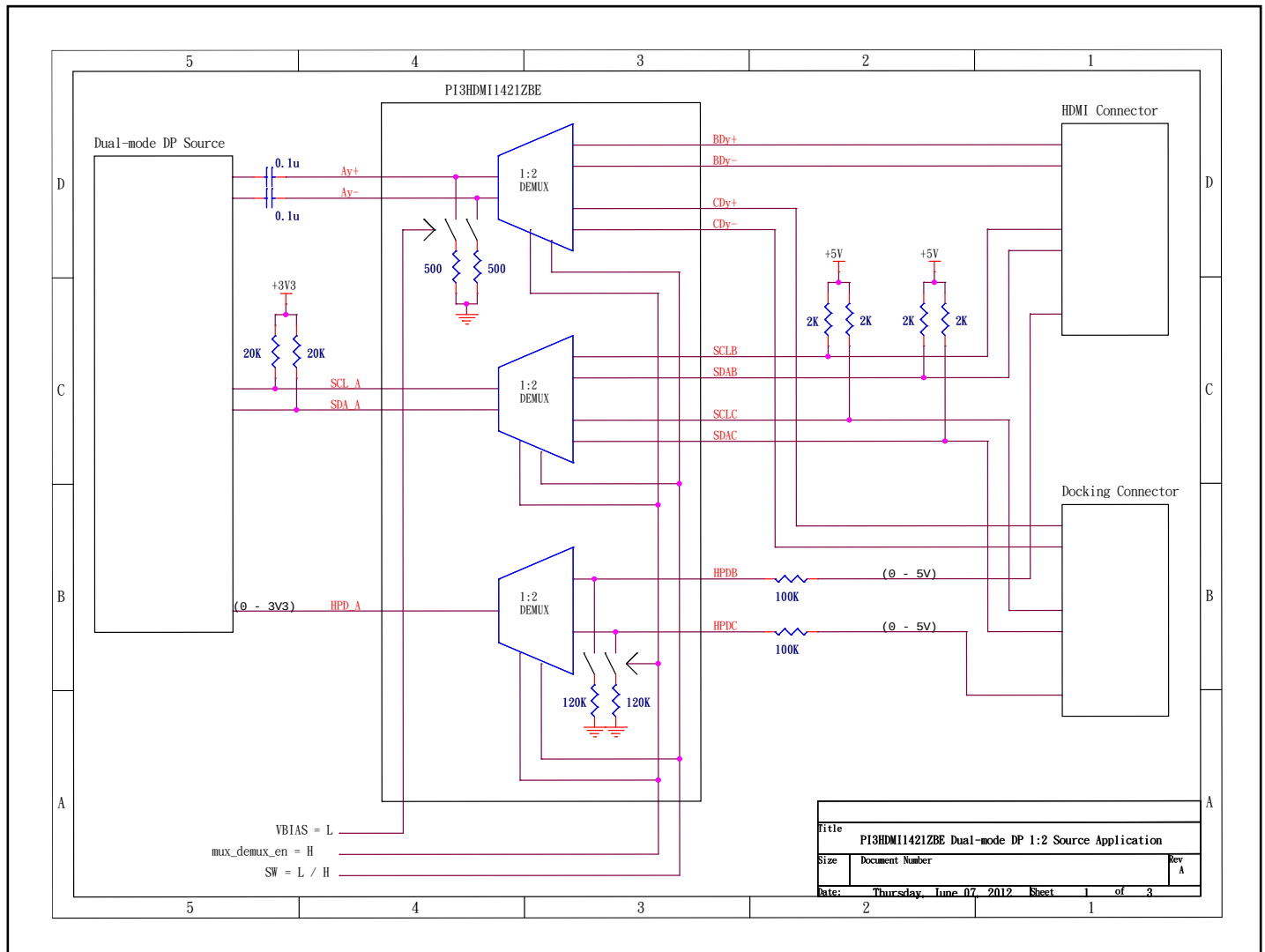


Fig 6: Dual-mode DP 1:2 Source Application Diagram

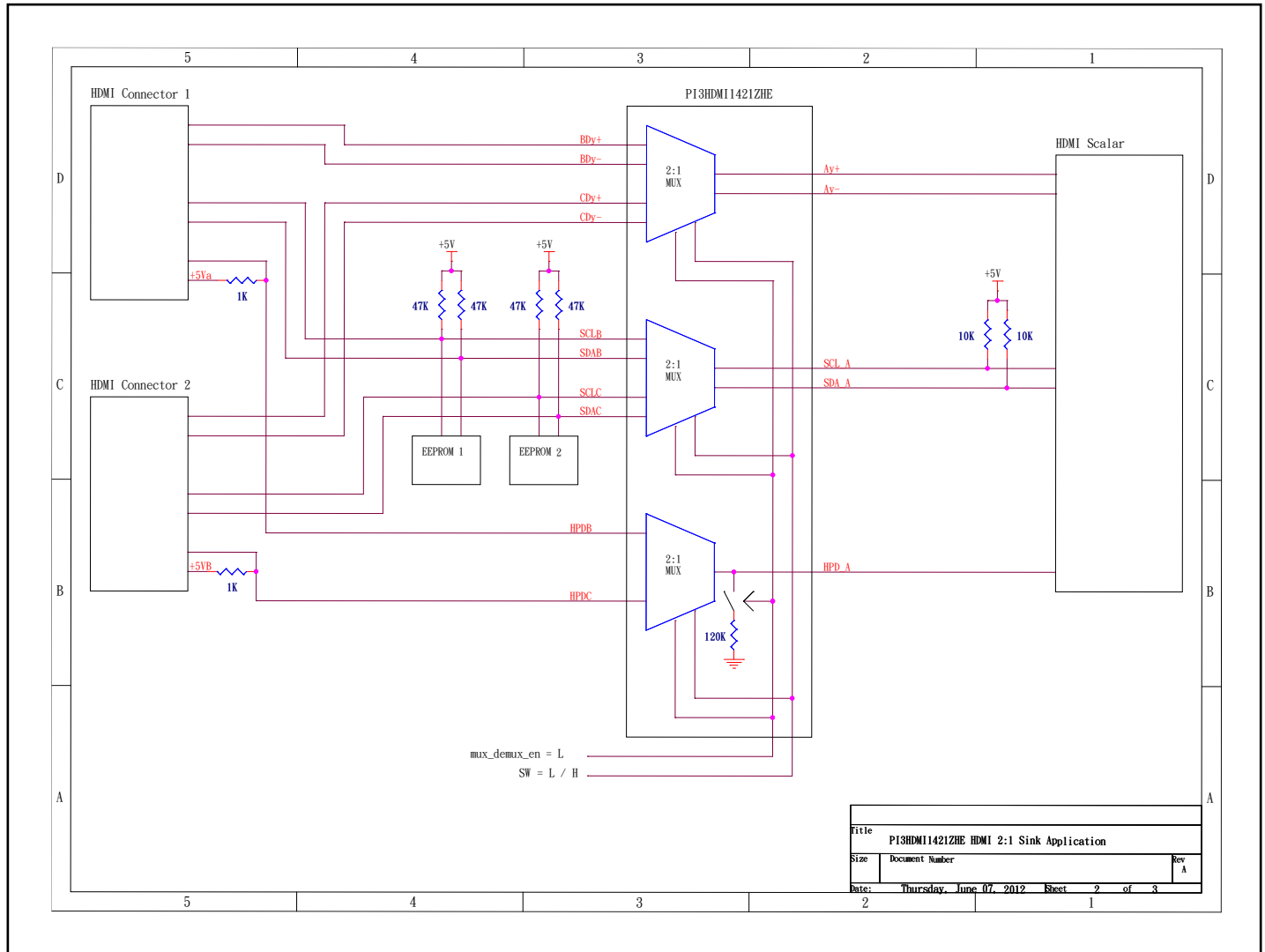
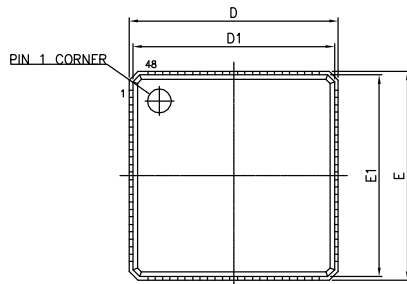
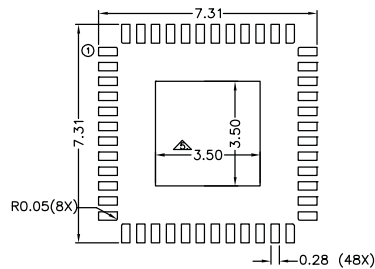


Fig 7: HDMI 2:1 Sink Application Diagram

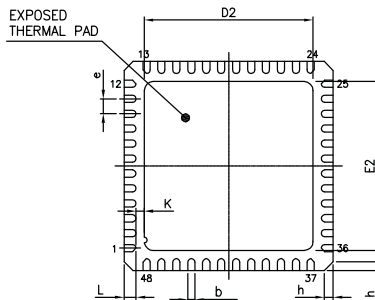
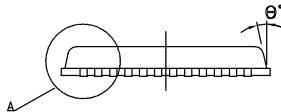
Package Mechanical: 48-pin, TQFN (ZB48)



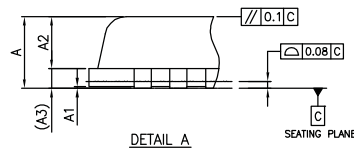
TOP VIEW



RECOMMENDED LAND PATTERN (TOP VIEW)



BOTTOM VIEW



DETAIL A

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	0.65 REF.		
A3	0.203 REF.		
b	0.18	0.25	0.30
h	0.24	0.42	0.60
D	6.90	7.00	7.10
D1	6.65	6.75	6.85
E	6.90	7.00	7.10
E1	6.65	6.75	6.85
e	0.50 BSC.		
K	0.20	—	—
L	0.30	0.40	0.50
θ°	0.00	—	12.00

UNIT : mm

PAD SIZE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
157X157MIL	3.40	3.60	3.80	3.40	3.60	3.80
213X213MIL	5.00	5.20	5.40	5.00	5.20	5.40
208X208MIL	4.90	5.10	5.30	4.90	5.10	5.30

UNIT: mm

Notes:

1. All dimensions are in millimeters, angles are in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area



DATE: 02/11/09

DESCRIPTION: 48-Pin, Thin Fine Pitch Quad Flat No-Lead (TQFN)

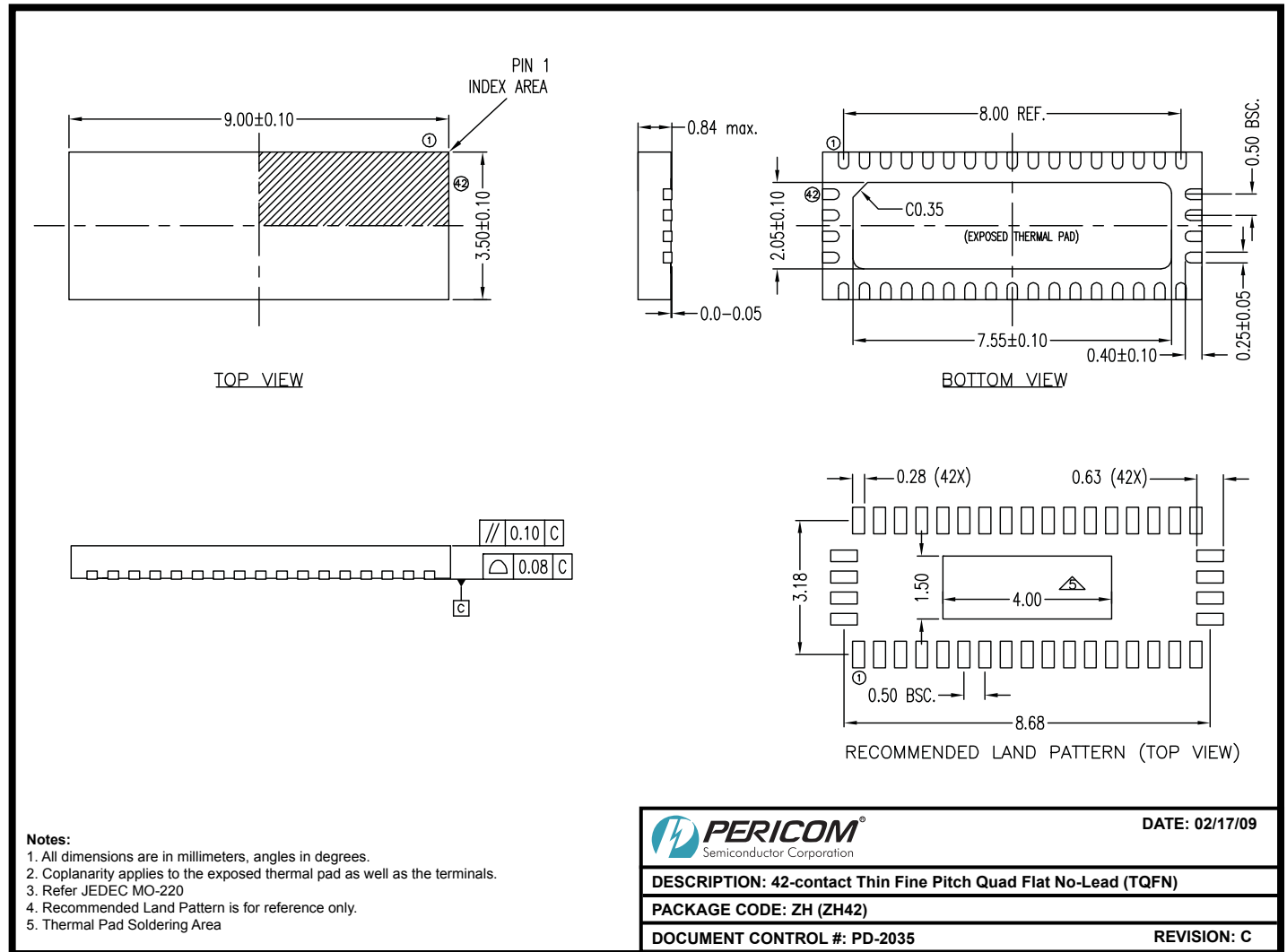
PACKAGE CODE: ZB48

DOCUMENT CONTROL #: PD-2080

REVISION: A

09-0091

Package Mechanical: 42-pin, TQFN (ZH42)



09-0116

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDMI1421ZBE	ZB	48-pin, Pb-free & Green TQFN
PI3HDMI1421ZHE	ZH	42-pin, Pb-free & Green TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel