Photoelectric Smoke Detector with Interconnect and Timer

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: May 17, 2023

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact factory.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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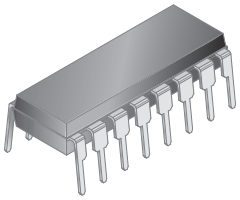
Photoelectric Smoke Detector with Interconnect and Timer

FEATURES AND BENEFITS

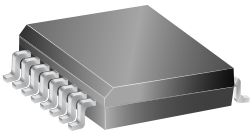
- Low average standby current for long battery life
- Interconnect up to 50 detectors
- Piezoelectric horn driver
- Low battery detection (all internal)
- Chamber sensitivity test and alarm
- Power-on reset (POR)
- Internal timer and control for reduced sensitivity mode
- Built-in circuits to reduce false triggering
- 6 to 12 V operating range
- ESD protection circuitry on all pins
- Temporal Horn Pattern, per UL217, NFPA72, and ISO8201
- UL Recognized for UL217 or UL268 applications

PACKAGES:

16-pin DIP
(Package A)



16-pin SOICW
(Package LW)



Not to scale

DESCRIPTION

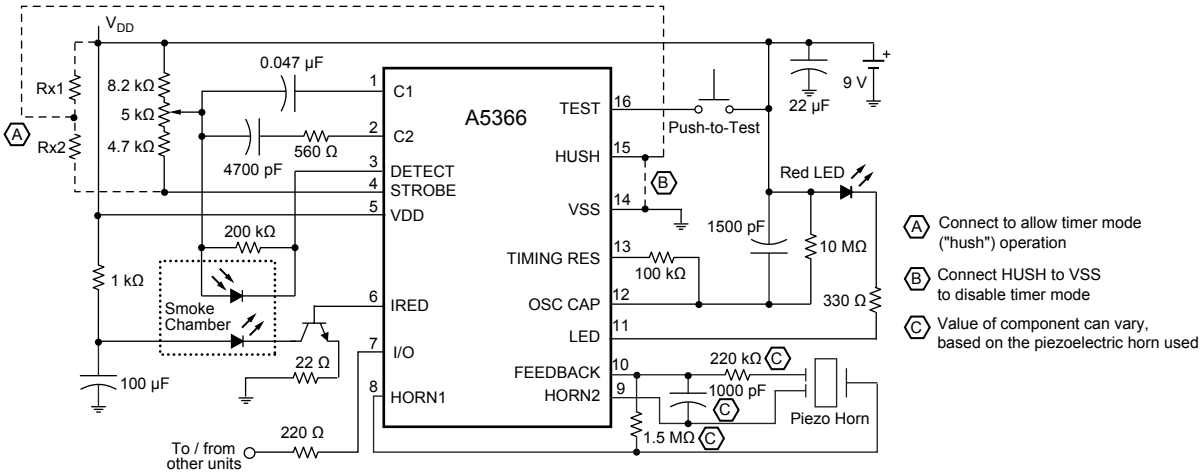
The A5366 is a low-current BiCMOS circuit providing all of the required features for a photoelectric type smoke detector. This device can be used with an infrared photoelectric chamber to sense scattered light from smoke particles. A networking capability allows as many as 50 units to be interconnected so that if any unit senses smoke all units will sound an alarm. Special features are incorporated in the design to facilitate calibration and testing of the finished detector. The device is recognized by Underwriters Laboratories for use in smoke alarms that comply with Standard UL217, or UL268, per file #S2113.

A variable-gain photoamplifier can be directly interfaced to an infrared emitter-detector pair. The amplifier gain levels are determined by two external capacitors and are internally selected depending on the operating mode. Low gain is selected during standby and timer modes. During a local alarm, this low gain is increased (internally) by approximately 10% to reduce false triggering. High gain is used during pushbutton test and to periodically monitor the chamber sensitivity during standby.

The internal oscillator and timing circuitry keep standby power to a minimum by sensing for smoke for only 100 µs every 10 s. A special three-stage–speedup sensing scheme is incorporated to minimize the time to an audible alarm and also to reduce false triggering. Chamber sensitivity is periodically monitored and two consecutive cycles of degraded sensitivity are required for a warning signal (chirp) to occur.

The A5366 is supplied in a 16-pin dual in-line plastic package (suffix A), and for surface mount, a 16-pin SOICW (suffix LW). The lead (Pb) free versions (suffix –T) have 100% matte-tin leadframe plating. The devices are rated for continuous operation over the temperature range of –25°C to 75°C.

Typical Application Diagram



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SELECTION GUIDE

Part Number	Pb-free	Package	Packing
A5366CA	–	16-pin DIP through hole	25 pieces / tube
A5366CA-T	Yes	16-pin DIP through hole	25 pieces / tube
A5366CLWTR-T	Yes	16-pin SOICW surface mount	1000 pieces / reel

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage Range	V_{DD}	Referenced to V_{SS}	–0.5 to 15	V
Input Voltage Range	V_{IN}	Referenced to V_{SS}	–0.3 to V_{DD}+0.3	V
Input Current	I_{IN}		10	mA
Operating Ambient Temperature Range	T_A		–25 to 75	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature Range	T_{stg}		–55 to 125	°C

*CAUTION: BiCMOS devices have input static protection but are susceptible to damage if exposed to extremely high static electrical charges.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package A, on 4-layer PCB based on JEDEC standard	38	°C/W
		Package LW, on 4-layer PCB based on JEDEC standard	48	°C/W

*Additional thermal information available on Allegro website.

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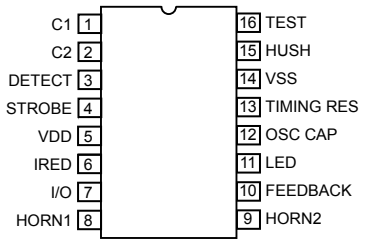
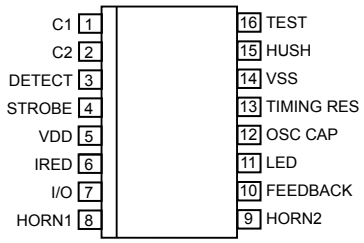
PINOUT DIAGRAMS AND TERMINAL LIST

Pinout Diagrams

Package A



Package LW



Terminal List Table

Number	Name	Function
1	C1	Sets photoamplifier gain in supervisory mode
2	C2	Sets photoamplifier gain in standby mode
3	DETECT	Photoamplifier input
4	STROBE	Strobed supply (V_{DD} – 5 V) for photoamplifier low-side reference
5	VDD	Positive supply voltage
6	IRED	Output to smoke chamber IR LED driver
7	I/O	Input-output to interconnected detectors
8	HORN1	Output for driving piezoelectric horn
9	HORN2	Complementary output for driving piezoelectric horn
10	FEEDBACK	Input for driving piezoelectric horn
11	LED	Output to drive visible LED
12	OSC CAP	Connection for capacitor to set clock frequency
13	TIMING RES	Connection for resistor to set clock frequency
14	VSS	Negative supply voltage
15	HUSH	Input for photoamplifier timer mode reference; can also disable timer mode
16	TEST	Enables push-to-test mode and diagnostic test/calibration mode; starts timer mode, if enabled

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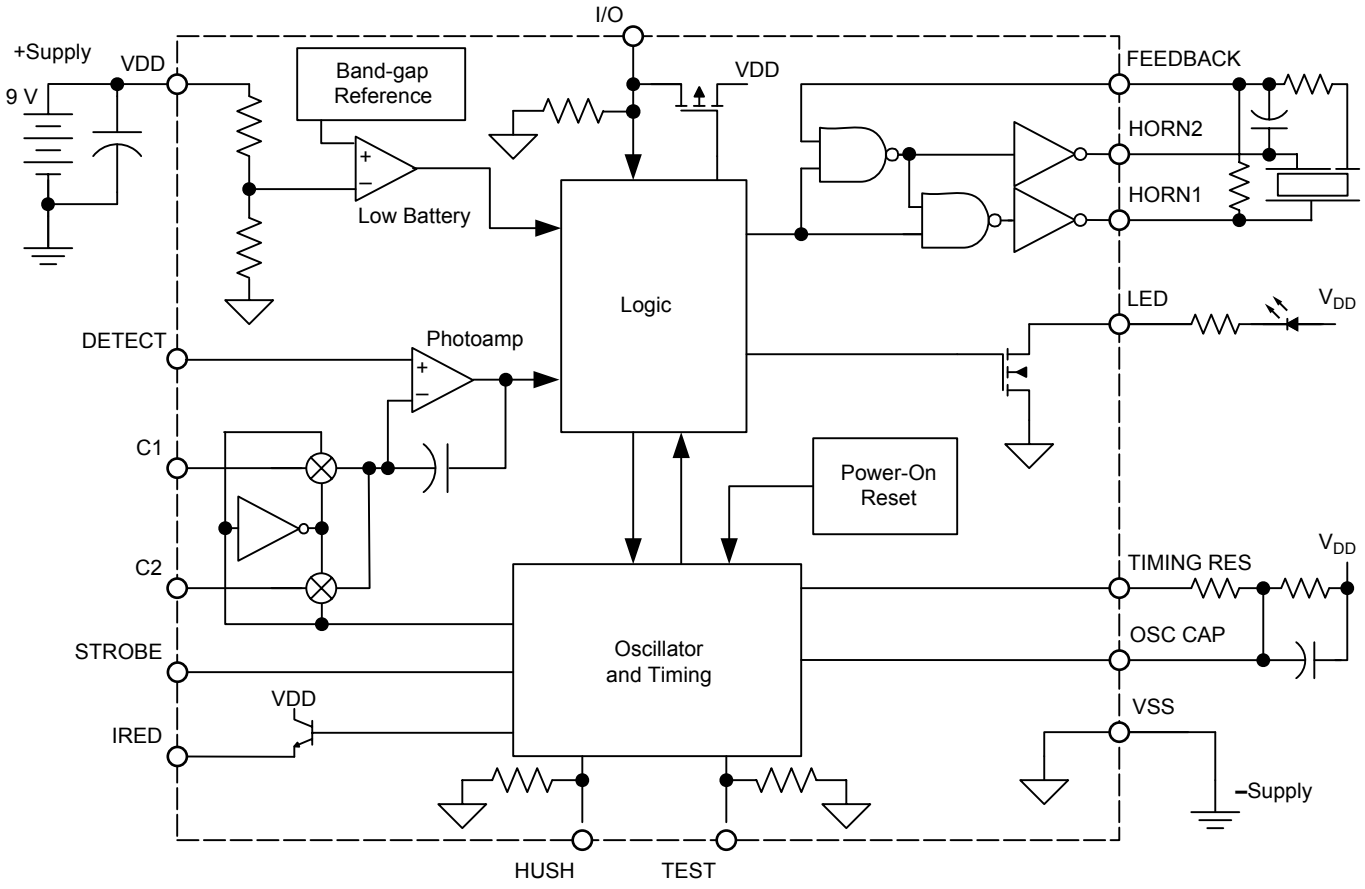
FUNCTIONAL BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS: Valid at T_A = –25°C to 75°C [1]. V_{SS} = 0 V, in typical application (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Test Pin	V_{DD}	Min.	Typ. [2]	Max.	Units
Supply Voltage Range	V_{DD}		5	–	6.0	–	12	V
Operating Supply Current	I_{DD}	Average in standby mode, configured per typical application	5	12	–	–	9	µA
		During STROBE on, IRED off, configured per typical application	5	12	–	–	2.0	mA
		During STROBE on, IRED on, configured per typical application	5	12	–	–	3.0	mA
Low-Level Input Voltage	V_{IL}		7	9	–	–	1.5	V
			10	9	–	–	2.7	V
			16	9	–	–	7.0	V
			15	9	–	–	0.5	V
High-Level Input Voltage	V_{IH}		7	9	3.2	–	–	V
			10	9	6.3	–	–	V
			16	9	8.5	–	–	V
			15	9	1.6	–	–	V
Input Leakage High	I_{IH}	$V_{IN} = V_{DD}$, STROBE active, OSC CAP = V_{DD}	1, 2	12	–	–	100	nA
		$V_{IN} = V_{DD}$	3, 10, 12	12	–	–	100	nA
Input Leakage Low	I_{IL}	$V_{IN} = V_{ST}$, STROBE active, OSC CAP = V_{DD}	1, 2, 3	12	–	–	–100	nA
		$V_{IN} = V_{SS}$	10, 12	12	–	–	–100	nA
			15, 16	12	–	–	–1.0	µA
Input Pull-Down Current	I_{IN}	$V_{IN} = V_{DD}$	16, 15	9	0.25	–	10	µA
		No local smoke, $V_{IN} = V_{DD}$	7	9	20	–	80	µA
		No local smoke, V_{IN} = 17 V	7	12	–	–	140	µA
Low-Level Output Voltage	V_{OL}	I_O = 10 mA	11	6.5	–	–	0.6	V
		I_O = 16 mA	8, 9	6.5	–	–	1.0	V
		I_O = 5 mA	13	6.5	–	0.5	–	V
High-Level Output Voltage	V_{OH}	I_O = –16 mA	8, 9	6.5	5.5	–	–	V
Strobe Output Voltage	V_{ST}	Inactive, I_O = –1 µA	4	12	V_{DD} – 0.1	–	–	V
		Active, I_O = 100 to 500 µA	4	9	V_{DD} – 5.25	–	V_{DD} – 4.75	V
Line Regulation	$\Delta V_{ST(\Delta VDD)}$	Active, V_{DD} = 6 to 12 V	4	–	–	–60	–	dB
Strobe Temperature Coefficient	α_{ST}	V_{DD} = 6 to 12 V	4	–	–	0.01	–	%/°C
IRED Output Voltage	V_{IRED}	Inactive, I_O = 1 µA, T_A = 25°C	6	12	–	–	0.1	V
		Active, I_O = –6 mA, T_A = 25°C	6	9	2.85	3.1	3.35	V

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DC ELECTRICAL CHARACTERISTICS (continued): Valid at T_A = –25°C to 75°C [1]. V_{SS} = 0 V, in typical application (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Test Pin	V_{DD}	Min.	Typ. [2]	Max.	Units
Line Regulation	$\Delta V_{IRED(\Delta VDD)}$	Active, V_{DD} = 6 to 12 V	6		–	–35	–	dB
IRED Temperature Coefficient	α_{IRED}	V_{DD} = 6 to 12 V	6	–	–	0.40	–	%/°C
High-Level Output Current	I_{OH}	V_{DD} = Alarm, I/O active, $V_O = V_{DD} – 2$ V	7	9	–4.0	–	–	mA
OFF Leakage Current High	I_{OZ}	$V_O = V_{DD}$	11, 13	12	–	–	1.0	µA
OFF Leakage Current Low	I_{OZ}	$V_O = V_{SS}$	11, 13	12	–	–	–1.0	µA
Low-Battery Alarm Threshold	$V_{DD(th)}$		5	–	6.9	7.2	7.5	V
Common Mode Voltage	V_{IC}	Any alarm condition	1, 2, 3	–	V_{DD} – 4	–	V_{DD} – 2	V
Smoke Comparator Reference Voltage	V_{REF}	Any alarm condition	Internal	–	V_{DD} – 3.7	–	V_{DD} – 3.3	V

[1] Limits over the operating temperature range are based on characterization data. Characteristics are production tested at 25°C only.
[2] Typical values are at 25°C and are given for circuit design information only.

AC ELECTRICAL CHARACTERISTICS: Valid at T_A = –25°C to 75°C [1]. V_{SS} = 0 V, in typical application (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Test Pin	V_{DD}	Min.	Typ. [2]	Max.	Units
Oscillator Period	t_{osc}		12	9	9.4	10.5	11.5	ms
LED Pulse Period	t_{led1}	No local or remote smoke	11	9	39	–	48	s
	t_{led3}	Local smoke	11	9	0.45	0.50	0.55	s
	t_{led4}	Remote smoke only	11	9	–	No LED Pulses	–	s
	t_{led6}	Pushbutton test, induced alarm	11	9	0.45	0.50	0.55	s
	t_{led7}	Timer mode, no alarm	11	9	9.67	10.75	11.83	s
LED Pulse Width	$t_{w(led)}$		11	9	9.5	–	11.5	ms
STROBE Pulse Period	t_{st1}	No local or remote smoke	4	9	9.6	–	11.9	s
	t_{st2}	After 1 of 3 valid samples	4	9	1.8	2.0	2.2	s
	t_{st3}	After 2 of 3 valid samples and during local alarm	4	9	0.8	1.0	1.1	s
	t_{st4}	Remote smoke only	4	9	7.2	8.0	8.9	s
	t_{st5}	Chamber test or low battery test, no local alarm	4	9	38.9	–	47.1	s
	t_{st6}	Pushbutton test, induced alarm	4	9	225	252	278	ms
STROBE Pulse Width	$t_{w(st)}$		4	9	9.5	–	11.5	ms

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AC ELECTRICAL CHARACTERISTICS (continued): Valid at T_A = –25°C to 75°C [1]. V_{SS} = 0 V, in typical application (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Test Pin	V_{DD}	Min.	Typ. [2]	Max.	Units
IRED Pulse Period	t_{ired1}	No local or remote smoke	6	9	9.6	–	11.9	s
	t_{ired2}	After 1 of 3 valid samples	6	9	1.8	2.0	2.2	s
	t_{ired3}	After 2 of 3 valid samples and during local alarm	6	9	0.8	1.0	1.1	s
	t_{ired4}	Remote smoke only	6	9	7.2	8.0	8.9	s
	t_{ired5}	Chamber test, no local alarm	6	9	38.9	–	47.1	s
	t_{ired6}	Pushbutton test, induced alarm	6	9	225	252	278	ms
IRED Pulse Width	$t_{w(ired)}$		6	9	94	–	116	µs
IRED Rise Time	$t_{r(ired)}$	10% to 90%	6		–	–	30	µs
IRED Fall Time	$t_{f(ired)}$	90% to 10%	6		–	–	200	µs
I/O to Active Delay	$t_{d(io)}$	Local alarm	7	9	–	0	–	s
I/O Charge Dump Duration	t_{dump}	End of local alarm or test	7	9	0.9	1.0	1.1	s
Rising Edge on I/O to Alarm	$t_{r(io)}$	No local alarm	7	9	–	–	13 × t_{OSC}	s
Horn Warning Pulse Period	t_{horn}	Low battery or degraded chamber sensitivity	8, 9	9	38.9	–	47.1	s
Horn Warning Pulse Width	$t_{w(horn)}$	Low battery or degraded chamber sensitivity	8, 9	9	9.5	–	11.5	ms
Horn On-Time	$t_{on(horn)}$	Local or remote alarm	8, 9	9	450	500	550	ms
Horn Off-Time	$t_{off1(horn)}$	Local or remote alarm (see Timing Diagrams section)	8, 9	9	450	500	550	ms
	$t_{off2(horn)}$	Local or remote alarm (see Timing Diagrams section)	8, 9	9	1350	1500	1650	ms

[1] Limits over the operating temperature range are based on characterization data. Characteristics are production tested at 25°C only.
[2] Typical values are at 25°C and are given for circuit design information only.

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Pin and Circuit Description
(In Typical Application)

C1 Pin
A capacitor connected to this pin determines the gain, A_e, of the photoamplifier during the push-to-test mode and during the chamber monitor test. A typical capacitor value for this high-gain (supervisory) mode is 0.047 µF, but it should be selected based on the photochamber background reflections reaching the detector and the desired level of sensitivity. $A_e = 1 + (C_1/10)$, where C_1 is in pF. A_e should not exceed 10,000 and thus C_1 should not exceed 0.1 µF. Coupling of other signals to the C1, C2, and DETECT inputs must be minimized.

C2 Pin
A capacitor connected to this pin determines the gain, A_e, of the photoamplifier during standby. A typical capacitor value for this low-gain mode is 4700 pF, but it should be selected based on a specific photochamber and the desired level of sensitivity to smoke. $A_e = 1 + (C_2/10)$, where C_2 is in pF. A_e should not exceed 10,000 and thus C_2 should not exceed 0.1 µF. This gain increases by a nominal 10% after a local alarm is detected (three consecutive detections). A resistor must be installed in series with the C2 capacitor.

DETECT Pin
This is the input to the photoamplifier and is connected to the cathode of the photodiode. The photodiode is operated at zero bias and should have low dark leakage current and low capacitance. A shunt resistor must be installed in parallel with the photodiode.

STROBE Pin
This output provides a strobed, regulated voltage of $V_{DD} - 5$ V. The minus side of all internal and external photoamplifier circuitry is referenced to this pin.

VDD Pin
This pin is connected to the positive supply potential and can range from 6 to 12 V with respect to V_{SS}.

IRED Pin
This output provides a pulsed base current for the external NPN transistor, which drives the IR emitter. Its beta should be greater than 100. To minimize noise impact, the IRED output is not active when the horn and visible LED outputs are active.

I/O Pin
A connection at this pin allows multiple smoke detectors to be interconnected. If any single unit detects smoke, its I/O pin is driven high, and all connected units will sound their associated horns.

As an input, the I/O is sampled every fourth clock cycle (nominally 42 ms). When the I/O pin is driven high by another device, three consecutive samples with I/O high plus one additional cycle (nominally 10.5 ms) are required to cause an alarm. If the I/O falls below its threshold at any time during those (nominally) 95 ms, an internal latch is reset and there will not be an alarm. Thus, depending on when during the (nominally) 42 ms sample cycle I/O is initially forced high, the I/O must remain high for a minimum of (nominally) 95 to 137 ms to cause an alarm. This filtering provides significant immunity to I/O noise.

The LED is suppressed when an alarm is signaled from an interconnected unit, and any local alarm condition causes this pin to be ignored as an input. An internal NMOS device acts as a charge dump to aid in applications involving large (distributed) capacitance, and is activated at the end of a local or test alarm. This pin has an on-chip pull-down device and must be left unconnected if not used. In the application, there should be a series current-limiting resistor to other smoke alarms.

HORN1, HORN2, FEEDBACK Pins
These three pins are used with a self-resonating piezoelectric transducer and horn-starting external passive components. The output HORN1 is connected to the piezo metal support electrode. The complementary output, HORN2, is connected to the ceramic electrode. The FEEDBACK input is connected to the feedback electrode. If the FEEDBACK pin is not used, it must be connected to VSS.

LED Pin
This open-drain NMOS output is used to directly drive a visible LED. The load for the low-battery test is applied to this output. If an LED is not used, it should be replaced with an equivalent resistor (typically 500 to 1000 Ω) such that the battery loading remains about 10 mA. The low-battery test does not occur coincident with any other test or alarm signal. The LED also indicates detector status as follows (with component values as in the typical application, all times nominal):

Condition	Pulse Occurrence
Standby	Every 43 s
Local Smoke	Every 0.5 s
Remote Alarm	No pulses
Test Mode	Every 0.5 s
Timer Mode	Every 10 s

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OSC CAP (Oscillator Capacitor) Pin

A capacitor between this pin and VDD, along with a parallel resistor, forms part of a two-terminal oscillator and sets the internal clock low time. With component values shown, this nominal time is 10.4 ms and essentially the oscillator period. The internal clock low time can be calculated by:

$$T_{low} = 0.693 \times R_{OSCCAP} \times C_{OSCCAP} \ .$$

TIMING RES (Timing Resistor) Pin

A resistor between this pin and OSC CAP is part of the two-terminal oscillator and sets the internal clock high time, which is also the IRED pulse width. With component values shown, this time is nominally 105 µs. The internal clock high time can be calculated by:

$$T_{high} = 0.693 \times R_{TIMINGRES} \times C_{OSCCAP} \ .$$

VSS Pin

This pin is connected to the negative supply potential (usually ground).

HUSH Pin

This input pin has an internal pull-down device and serves two purposes in standby mode. It serves to enable/disable entering the internal 10-minute (nominal) "hush" timer mode, and also as the reference for the smoke comparator during timer mode. When the voltage on this pin is greater than 1.5 V, entering timer mode is enabled, and a high-to-low transition on the TEST pin resets and starts timer mode. If use of timer mode is not desired, this pin can be connected to VSS or left open, and a voltage of less than 0.5 V on the pin will disable timer mode. During timer mode, the smoke comparator reference is established by a resistive divider (Rx1 and Rx2) between the VDD and STROBE pins and allows the detector to operate with reduced sensitivity during timer mode. This allows the user to hush alarms caused by nuisance smoke or steam (such as from cooking). When not in timer mode, the smoke comparator reference is set internally to approximately V_{DD} – 3.5 V.

TEST Pin

This pin has an internal pull-down device and is used to manually invoke two test modes and timer mode.

Push-to-Test mode is initiated by a voltage greater than approximately V_{DD} – 0.5 V on this pin (usually the depression of a normally-open pushbutton switch to VDD). After one oscillator cycle, the amplifier gain is increased by internal selection of C1 so that background reflections in the smoke chamber can be used to simulate a smoke condition, and IRED pulses every 252 ms (nominal). After the third IRED pulse (three consecutive simulated smoke conditions), the successful test activates the horn drivers and the I/O pin, and the LED blinks once every 0.5 s. If the test fails, the LED will not blink, the horn will not sound, and the I/O pin will remain low. When the pushbutton is released, the input returns to V_{SS} due to the internal pull down. After one oscillator cycle, the amplifier gain returns to normal, and after three additional IRED pulses (less than one second), the device exits this mode and returns to standby. This high-to-low transition on TEST also resets and starts the 10-minute (nominal) "hush" timer mode, if the mode is enabled via the HUSH pin.

Diagnostic Test/Calibration Mode is available to facilitate calibration and test of the IC and the assembled detector. It is initiated by pulling TEST below V_{SS} by continuously drawing 400 µA from the pin for at least one clock cycle on OSC CAP. The current should not exceed 800 µA and under these conditions, TEST pin voltage will clamp at approximately 250 mV below V_{SS}. One option is to connect TEST to a –5 V supply

Table 1. Alternate Pin Configuration During Diagnostic Test/ Calibration Mode

Pin Name	Alternate Configuration
I/O	Disabled as an output. A logic high on this pin places the photoamplifier output on C1 or C2 as determined by the HUSH pin. The amplifier output appears as pulses.
HUSH	If the I/O pin is high, this pin controls the amplifier gain capacitor. If this pin is low, normal gain is selected and the amplifier output is on pin C1. If this pin is high, supervisory gain is selected and the amplifier output is on C2. NOTE: If I/O is low, four rising edges on this pin will cause the device to exit diagnostic/calibration mode and enter an Allegro-defined test mode.
FEED-BACK	If the I/O pin is high and the HUSH pin is low (normal gain), taking this pin to a high logic level increases the amplifier gain by ≈10% (hysteresis).
OSC CAP	This pin may be driven by an external clock source. Driving this pin low and high drives the internal clock low and high. The external RC network may remain intact.
HORN1	This pin is reconfigured as the smoke integrator output. Three consecutive smoke detections will cause this pin to go high and three consecutive no-smoke detections cause this pin to go low.
LED	This pin becomes a low-battery indicator. The open-drain NMOS output is normally off. If V_{DD} falls below the low-battery threshold, the output turns on.

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through a 12 kΩ resistor. In this mode, certain device pins are reconfigured as described in table 1. The IRED pulse rate is increased to one pulse every OSC CAP cycle and the STROBE pin is always active. To exit this mode, the TEST pin should be floated, or returned to V_{SS}, for at least one OSC CAP cycle.

Alarm Indications

Alarm conditions include: local smoke detection, a remote alarm, low battery, or degraded chamber sensitivity. These are indicated by a combination of horn and LED signals, which continue until the alarm condition is resolved. A local alarm always overrides a remote alarm, and a local or remote alarm will inhibit warning signals for low battery or degraded chamber.

During a local or a remote alarm condition, the horn output is a continuous modulated tone (temporal horn pattern), nominally: 0.5 seconds on, 0.5 seconds off, 0.5 seconds on, 0.5 seconds off, 0.5 seconds on, and 1.5 seconds off. The visible LED distinguishes a local alarm from a remote alarm. During a local alarm, the LED blinks every 0.5 seconds (nominally), but during a remote alarm, the LED is disabled and does not blink.

The degraded-chamber test occurs periodically (nominally every 43 seconds). During this test, the gain of the photoamplifier is switched to the high (supervisory) level, set by C1. The device expects that the photodiode will receive enough reflected background light in the chamber to cause an alarm condition. If a faulty, dirty, or obstructed chamber prevents this for two consecutive tests, the device signals degraded chamber with one short (nominally 10 ms) horn chirp every 43 seconds, essentially halfway between LED flashes. The condition is resolved when the chamber is either cleared or cleaned.

The low-battery test also occurs periodically (also nominally every 43 seconds, but offset from the degraded-chamber test). During this test, the load of the LED is applied to the battery, and a resistive divider off V_{DD} is compared to an internal band-gap reference. If V_{DD} is below the threshold, the device signals low battery with one short (nominally 10 ms) horn chirp every 43 seconds, occurring almost simultaneously with the visible LED flash. The condition is resolved when the battery is replaced.

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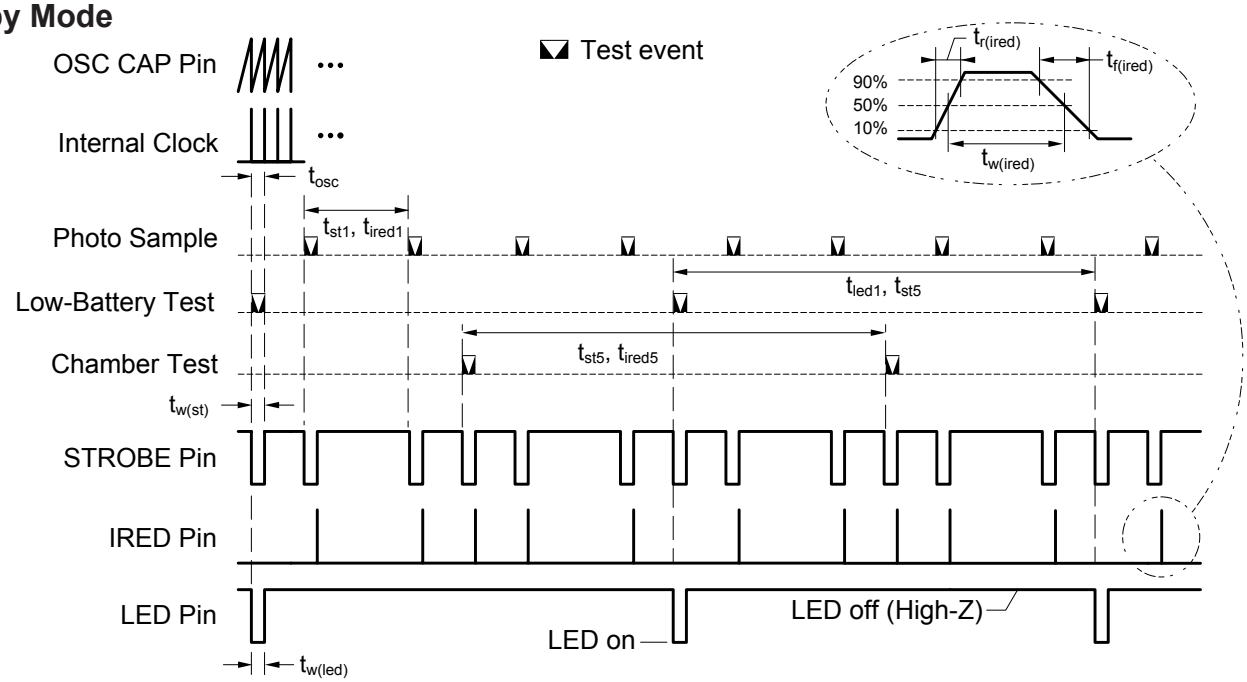
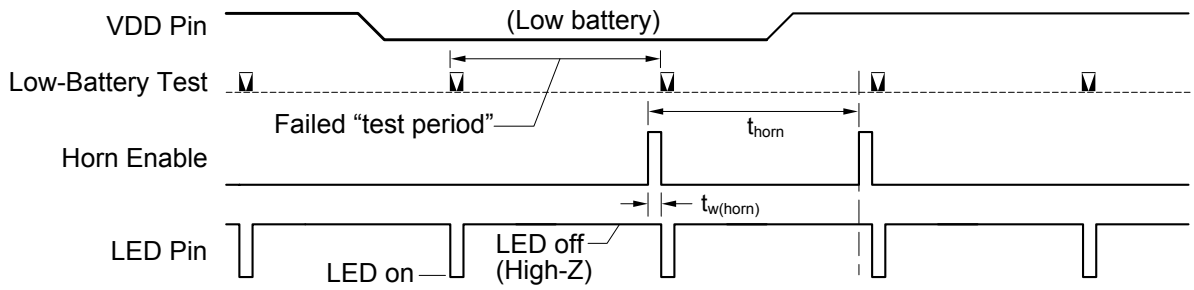
Timing Diagrams

(Not to Scale)

Standby Mode

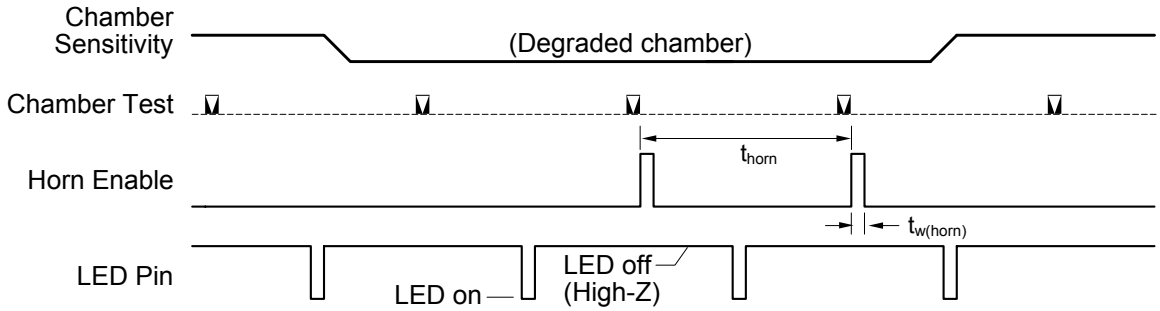


Low Battery Condition



Chirps occur at the end of a failed "test period," and are nearly coincident with LED flashes

Degraded Chamber Condition



Chirps occur after 2 consecutive failed tests, and are offset from LED flashes and from chirps that indicate failure of low-battery tests

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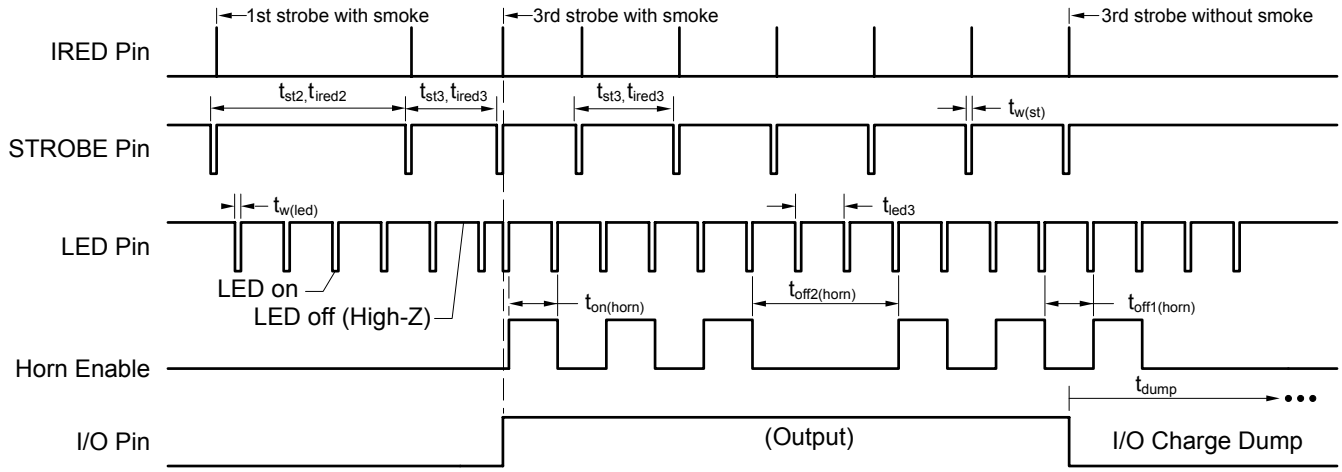
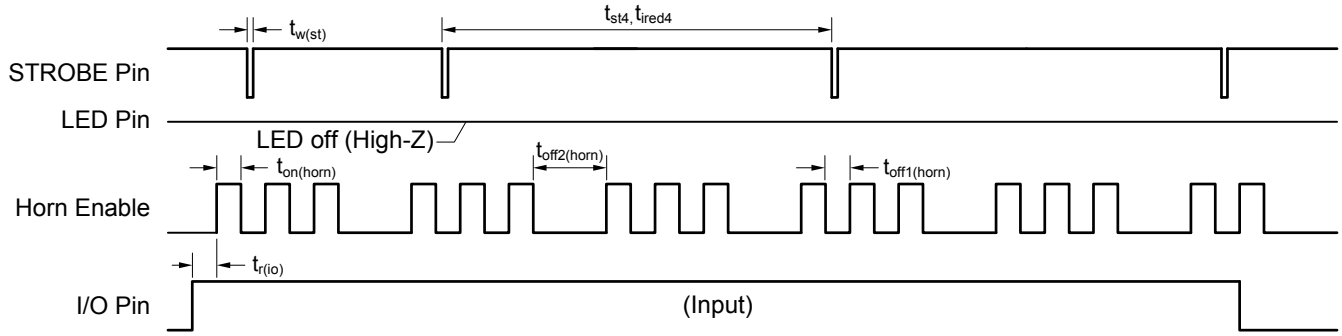
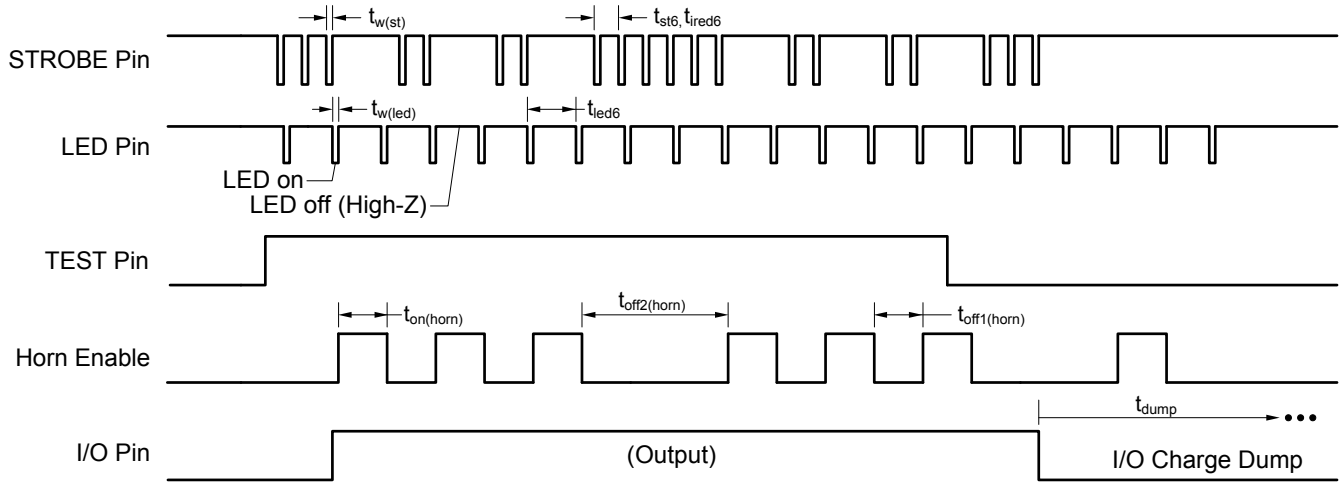
Local Smoke Detection Alarm Condition



Remote Alarm Condition



Test Alarm Mode



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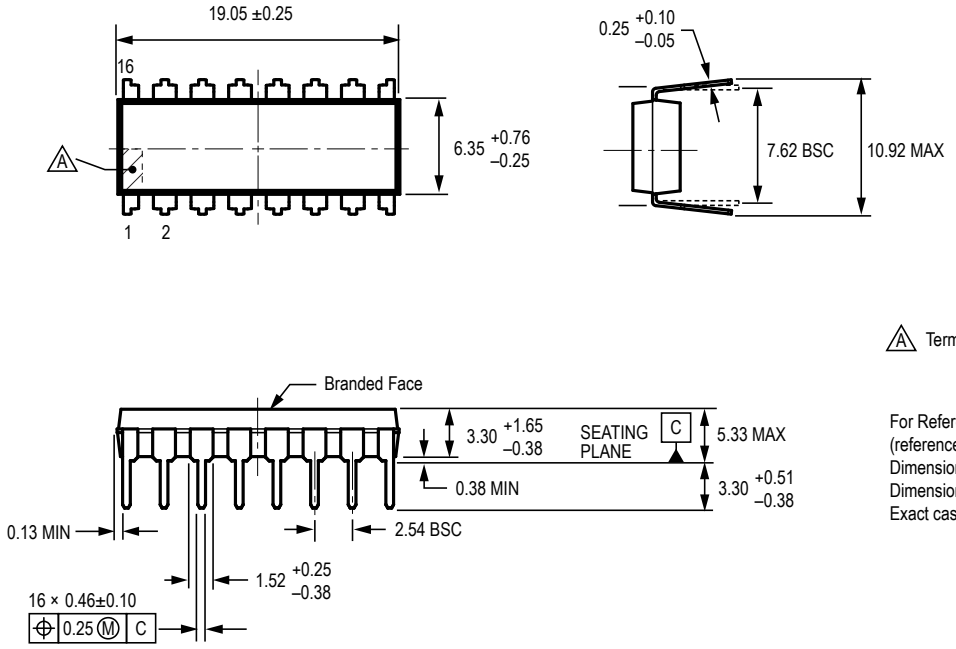
Package A, 16-Pin DIP



A Terminal #1 mark area

For Reference Only; not for tooling use
(reference Allegro DWG-0000370 or JEDEC MS-001BB)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

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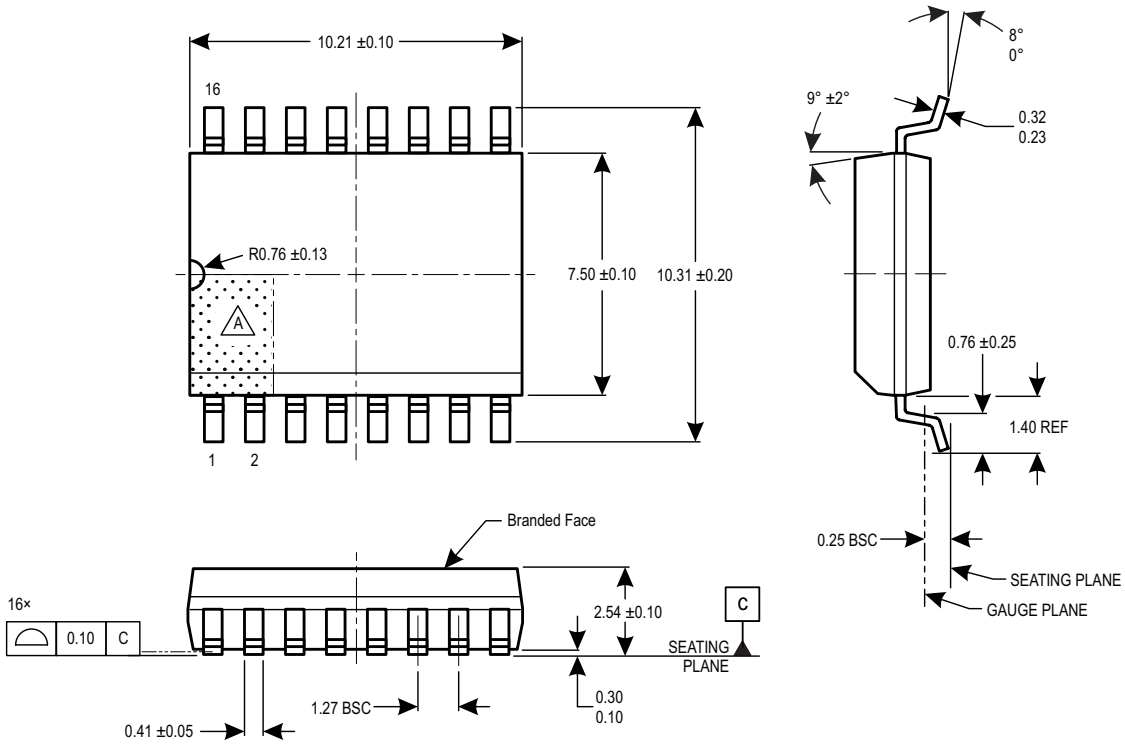
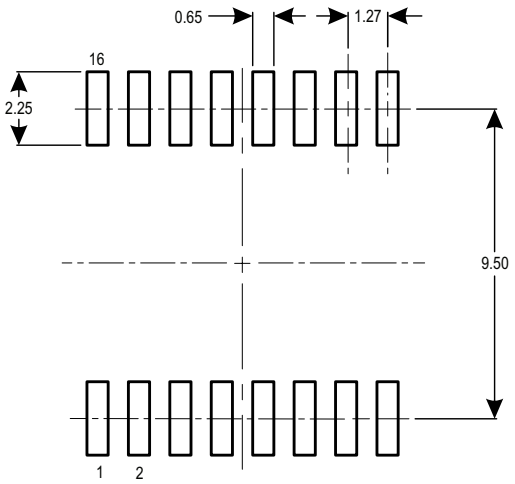
Package LW, 16-Pin SOIC

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 1 and JEDEC MS-013AA)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





B PCB Layout Reference View

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

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REVISION HISTORY

Number	Date	Description
9	July 1, 2020	Minor editorial updates
10	July 7, 2022	Updated package drawings (13-14) and minor editorial updates
11	October 1, 2022	Changed product status: Not for new design
12	May 17, 2023	Changed product status: Discontinued

The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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