

# TLP351

Inverter for Air Conditioner  
IGBT/Power MOS FET Gate Drive  
Industrial Inverter

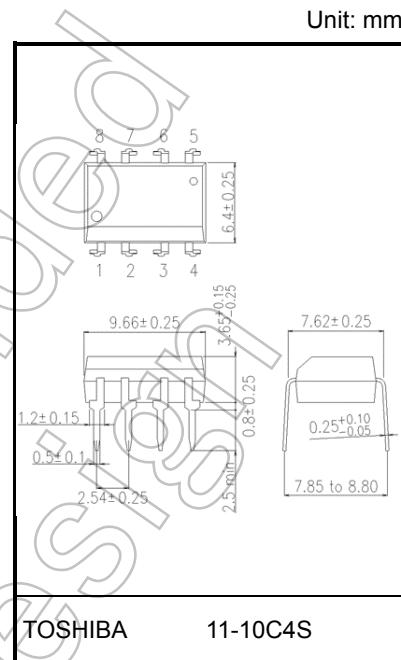
The TOSHIBA TLP351 consists of an infrared emitting diode and an integrated photodetector.

This unit is 8-lead DIP package.

TLP351 is suitable for gate driving circuit of IGBT or power MOS FET.

Especially TLP351 is capable of "direct" gate drive of lower Power IGBTs.

- Peak output current:  $\pm 0.6$  A (max)
- Guaranteed performance over temperature: -40 to 100°C
- Supply current: 2 mA (max)
- Power supply voltage: 10 to 30 V
- Threshold input current :  $I_F = 5$  mA (max)
- Switching time ( $t_{pLH}/t_{pHL}$ ) : 700 ns (max)
- Common mode transient immunity:  $\pm 10$  kV/μs
- Isolation voltage: 3750 Vrms
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A  
File No.E67349
- VDE-approved: EN 60747-5-5 (Note 1)



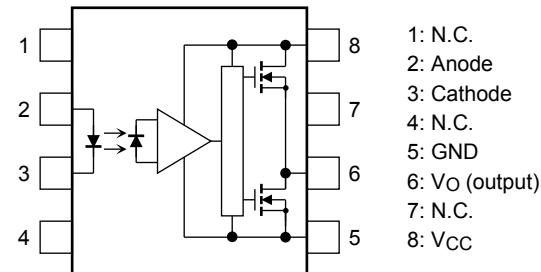
Weight: 0.54 g (typ.)

Note 1: When a VDE approved type is needed,  
please designate the **Option(D4)**.

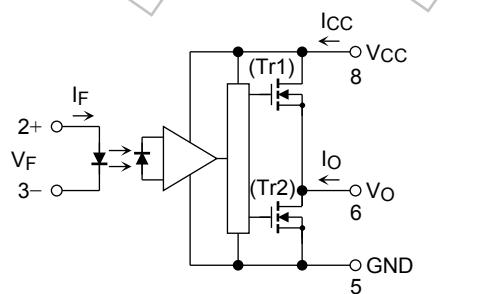
## Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

## Pin Configuration (top view)



## Schematic



A 0.1  $\mu$ F bypass capacitor must be connected between pin 8 and 5.

Start of commercial production  
2002-05

## Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I <sub>F</sub>	20	mA
	Forward current derating (Ta ≥ 85°C)	ΔI <sub>F</sub> /ΔT <sub>a</sub>	-0.54	mA/°C
	Peak transient forward current (Note 1)	I <sub>FP</sub>	1	A
	Reverse voltage	V <sub>R</sub>	5	V
	Power Dissipation	P <sub>D</sub>	40	mW
	Power Dissipation Derating (Ta ≥ 85°C)	ΔP <sub>D</sub> /°C	-1.0	mW/°C
	Junction temperature	T <sub>j</sub>	125	°C
Detector	"H" peak output current (Note 2)	I <sub>OPH</sub>	-0.6	A
	"L" peak output current (Note 2)	I <sub>OPL</sub>	0.6	A
	Output voltage	V <sub>O</sub>	35	V
	Supply voltage	V <sub>CC</sub>	35	V
	Output Power Dissipation	P <sub>O</sub>	260	mW
	Output Power Dissipation Derating (Ta ≥ 85°C)	ΔP <sub>O</sub> /°C	-6.5	mW/°C
	Junction temperature	T <sub>j</sub>	125	°C
Operating frequency (Note 3)		f	25	kHz
Storage temperature range		T <sub>STG</sub>	-55 to 125	°C
Operating temperature range		T <sub>OPR</sub>	-40 to 100	°C
Lead soldering temperature (10 s) (Note 4)		T <sub>SOL</sub>	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 5)		BV <sub>S</sub>	3750	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width PW ≤ 1 μs, 300 pps

Note 2: Exponential waveform pulse width PW ≤ 10 μs, f ≤ 15 kHz

Note 3: Exponential waveform IOPH ≤ -0.4 A (≤ 2.0 μs), IOPL ≤ +0.4 A (≤ 2.0 μs), Ta = 100 °C

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

## Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 7)	I <sub>F</sub> (ON)	7.5	—	10	mA
Input voltage, OFF	V <sub>F</sub> (OFF)	0	—	0.8	V
Supply voltage	V <sub>CC</sub>	10	—	30	V
Peak output current	I <sub>OPH</sub> /I <sub>OPL</sub>	—	—	±0.2	A
Operating temperature	T <sub>OPR</sub>	-40	—	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 7: Input signal rise time (fall time) < 0.5 μs

## Electrical Characteristics (Ta = -40 to 100°C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Forward voltage		VF	—	IF = 5 mA, Ta = 25 °C		—	1.55	1.70	V
Temperature coefficient of forward voltage		ΔVF/ΔTa	—	IF = 5 mA		—	-2.0	—	mV/°C
Input reverse current		IR	—	VR = 5 V, Ta = 25 °C		—	—	10	μA
Input capacitance		CT	—	V = 0 V, f = 1 MHz, Ta = 25 °C		—	45	—	pF
Output current (Note 8)	"H" Level	IOPH1	1	VCC = 15 V IF = 5 mA	V8-6 = 4 V	—	-0.4	-0.2	A
		IOPH2			V8-6 = 10 V	—	-0.67	-0.4	
	"L" Level	IOPL1	2	VCC = 15 V IF = 0 mA	V6-5 = 2 V	0.2	0.35	—	
		IOPL2			V6-5 = 10 V	0.4	0.63	—	
Output voltage	"H" Level	VOH	3	VCC = 10 V	IO = -100 mA, IF = 5 mA	6.0	8.5	—	V
	"L" Level	VOL	4		IO = 100 mA, VF = 0.8 V	—	0.4	1.0	
Supply current	"H" Level	ICCH	5	VCC = 10 to 30 V VO open	IF = 10 mA	—	1.4	2.0	mA
	"L" Level	ICCL	6		IF = 0 mA	—	1.3	2.0	
Threshold input current	L → H	IFLH	—	VCC = 15 V, VO > 1 V		—	2.5	5	mA
Threshold input voltage	H → L	VFHL	—	VCC = 15 V, VO < 1 V		0.8	—	—	V
Supply voltage		VCC	—	—		10	—	30	V

\*: All typical values are at Ta = 25°C

Note 8: Duration of IO time ≤ 50 μs

Note 9: This product is more sensitive than the conventional product to static electricity (ESD) because of a lowest power consumption design.

General precaution to static electricity (ESD) is necessary for handling this component.

## Isolation Characteristics (Ta = 25°C)

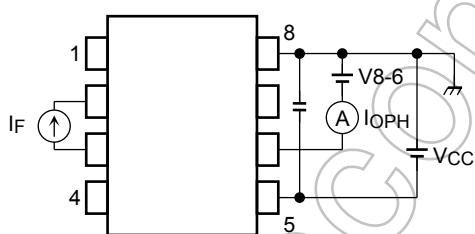
Characteristic	Symbol	Test Conditions		Min	Typ.	Max	Unit
Capacitance input to output	CS	Vs = 0V, f = 1MHz	(Note5)	—	1.0	—	pF
Isolation resistance	Rs	Vs = 500 V, R.H. ≤ 60 %	(Note5)	1×10 <sup>12</sup>	10 <sup>14</sup>	—	Ω
Isolation voltage	BVs	AC, 60 s		3750	—	—	V <sub>rms</sub>

Switching Characteristics ( $T_a = -40$  to  $100^\circ\text{C}$ , unless otherwise specified)

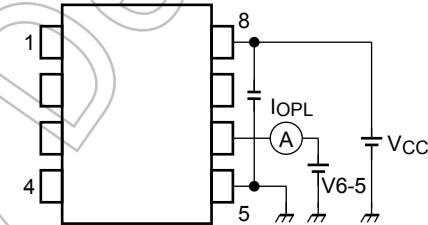
Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Propagation delay time	$L \rightarrow H$	$t_{pLH}$	7	$V_{CC} = 30 \text{ V}$	$I_F = 0 \rightarrow 5 \text{ mA}$	100	—	700	ns
	$H \rightarrow L$	$t_{pHL}$		$R_g = 47 \Omega$	$I_F = 5 \rightarrow 0 \text{ mA}$	100	—	700	
Propagation delay difference between any two parts or channels		PDD $ t_{pHL} - t_{pLH} $	7	$V_{CC} = 30 \text{ V}$ , $R_g = 47 \Omega$ $C_g = 3 \text{ nF}$		-500	—	500	ns
Output rise time (10-90%)		$t_r$		$V_{CC} = 30 \text{ V}$	$I_F = 0 \rightarrow 5 \text{ mA}$	—	50	—	ns
Output fall time (90-10%)		$t_f$	8	$R_g = 47 \Omega$	$I_F = 5 \rightarrow 0 \text{ mA}$	—	50	—	
Common mode transient immunity at high level output		CMH		$V_{CM} = 1000 \text{ Vp-p}$ $T_a = 25^\circ\text{C}$ $V_{CC} = 30 \text{ V}$	$I_F = 5 \text{ mA}$ $V_O(\text{min}) = 26 \text{ V}$	-10000	—	—	V/ $\mu$ s
Common mode transient immunity at low level output		CML			$I_F = 0 \text{ mA}$ $V_O(\text{max}) = 1 \text{ V}$	10000	—	—	

\*: All typical values are at  $T_a = 25^\circ\text{C}$ 

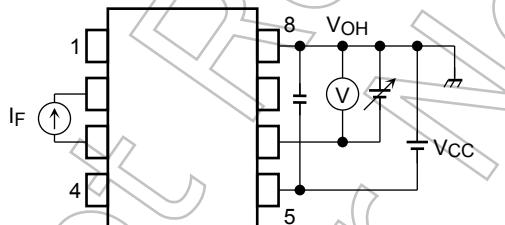
Test Circuit 1: IOPH



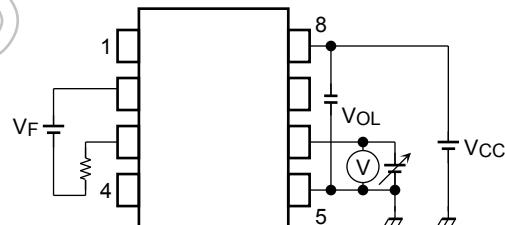
Test Circuit 2: IOPL



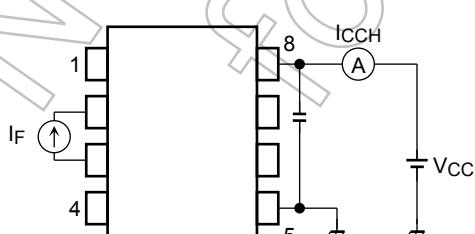
Test Circuit 3: VOH



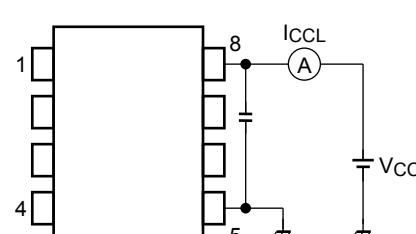
Test Circuit 4: VOL



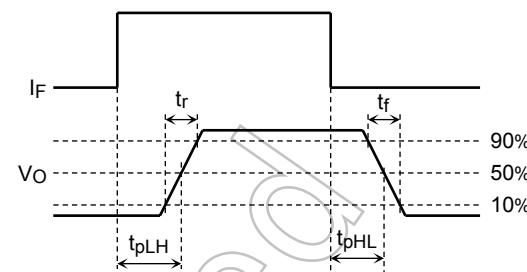
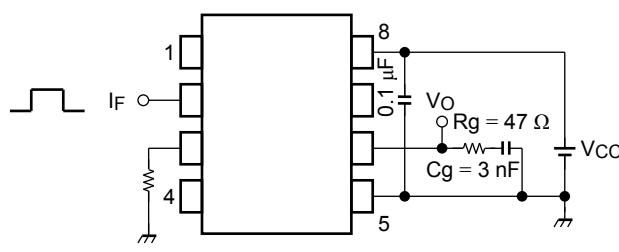
Test Circuit 5: ICCH



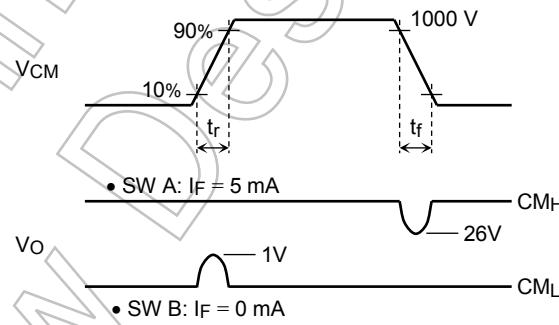
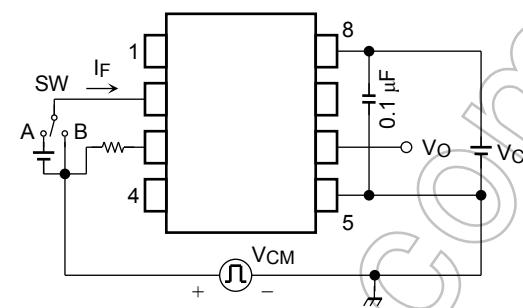
Test Circuit 6: ICCL



## Test Circuit 7: tpLH, tpHL, tr, tf, PDD

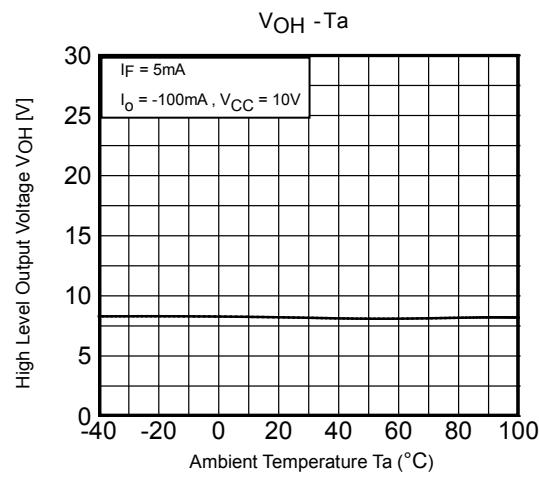
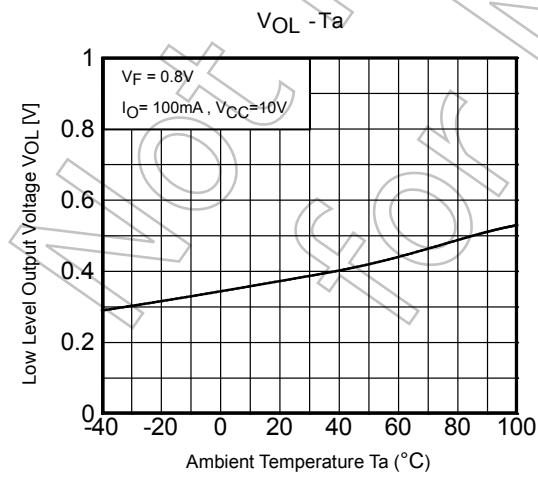
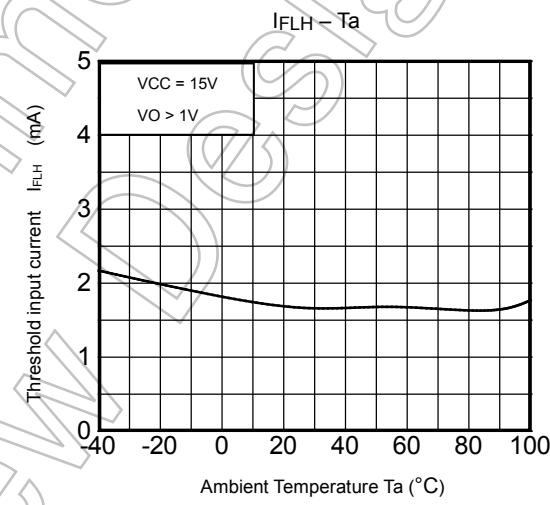
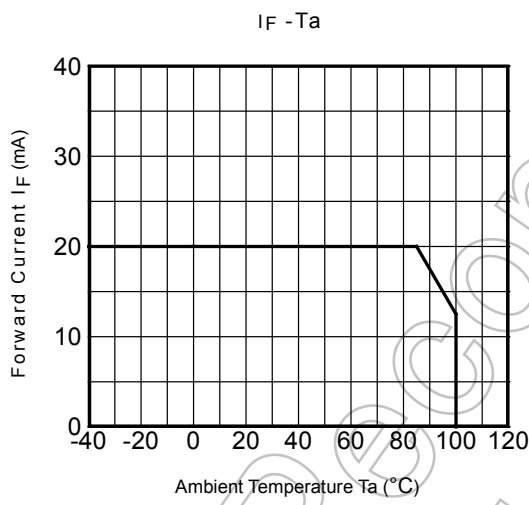
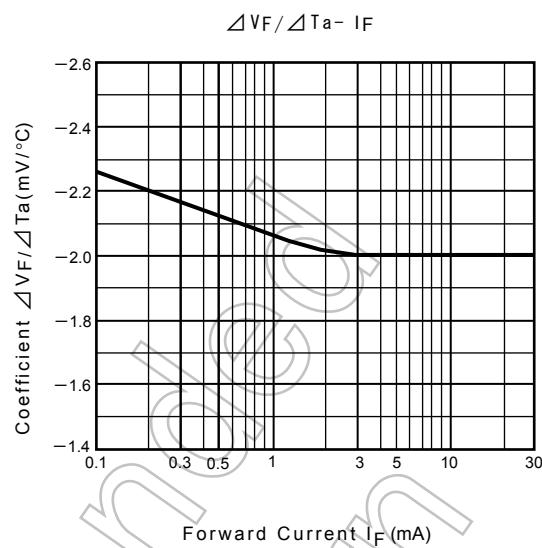
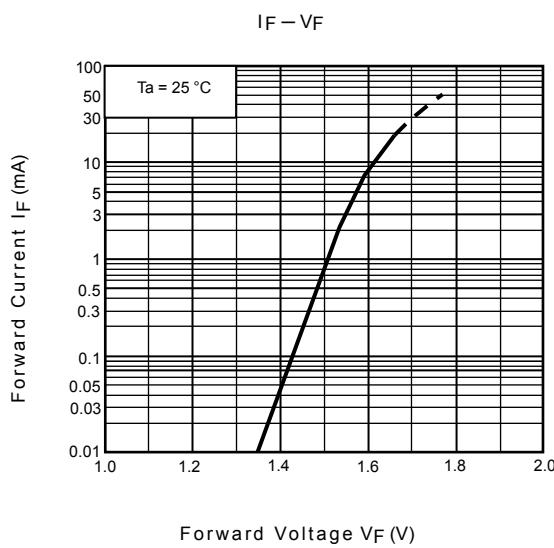


## Test Circuit 8: CMH, CML

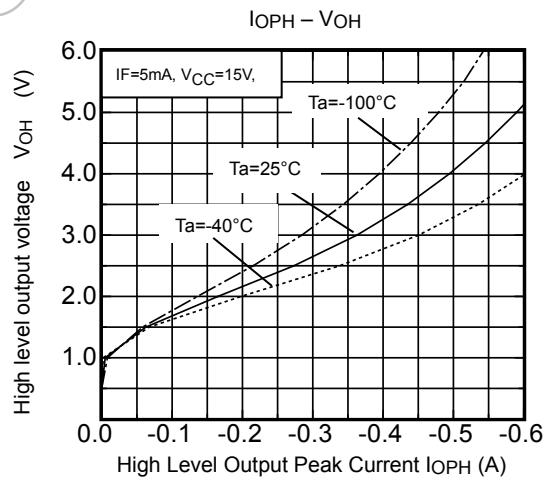
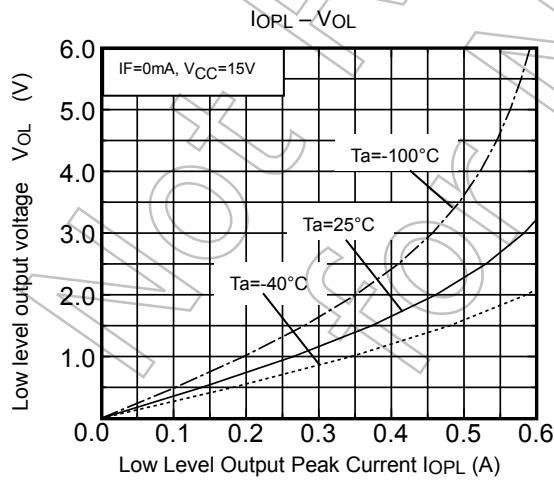
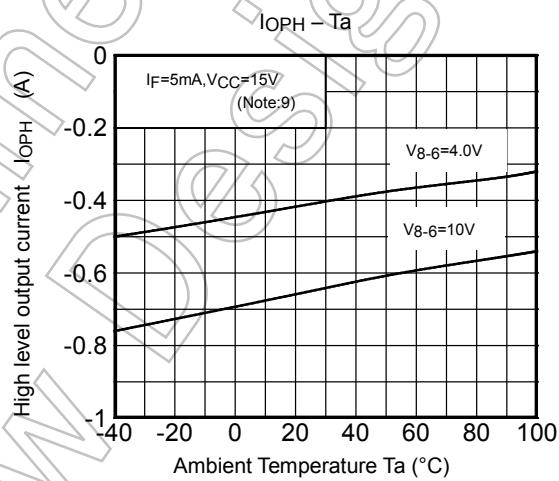
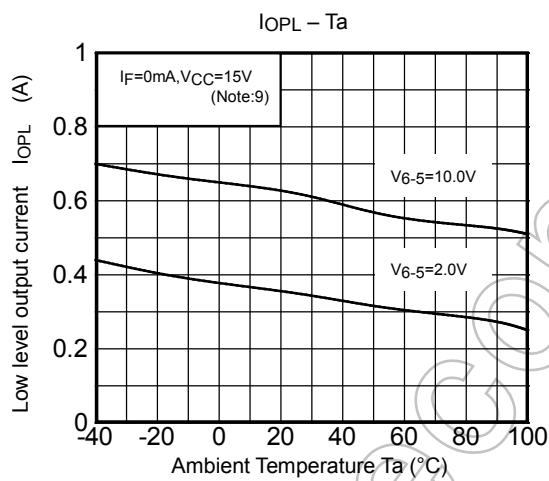
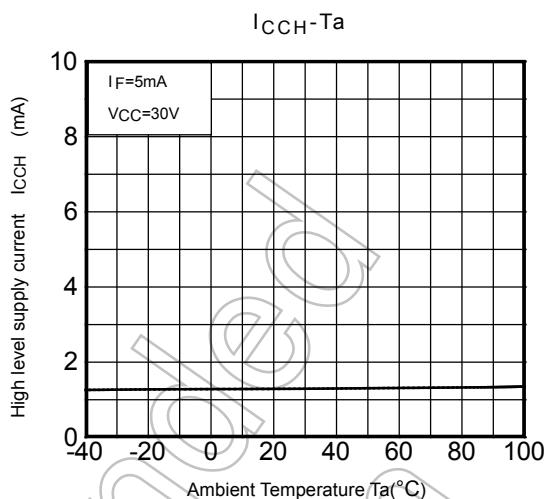
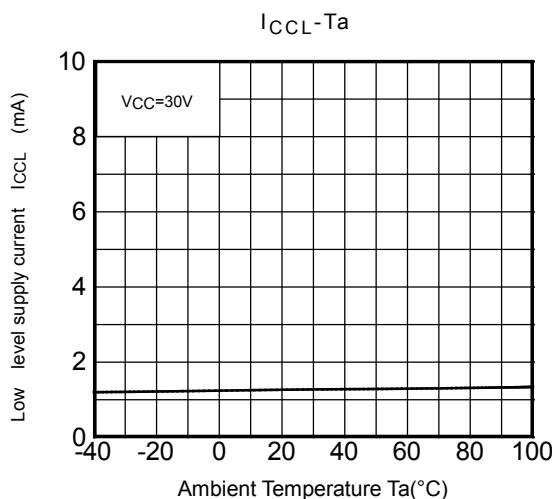


$$CM_L = \frac{800 \text{ V}}{tr \text{ } (\mu\text{s})}$$

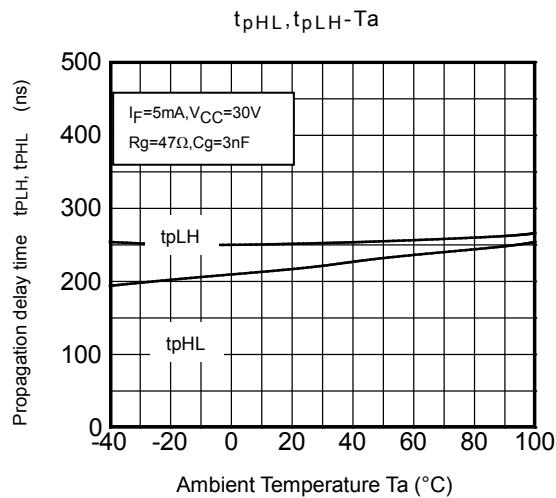
$$CM_H = \frac{800 \text{ V}}{tf \text{ } (\mu\text{s})}$$



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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Not Recommended  
for New Design

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