

Check for Samples: [TPS2394](#)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)<sup>(2)</sup>

| PARAMETERS                                           |                                             | VALUE       | UNIT |
|------------------------------------------------------|---------------------------------------------|-------------|------|
| Input voltage range                                  | RTN                                         | –0.3 to 100 | V    |
|                                                      | FLTTIM, RAMP, SENSE, OV, UV                 | –0.3 to 15  |      |
| Output voltage range                                 | $\overline{\text{FLT}}$ , PG <sup>(3)</sup> | –0.3 to 100 |      |
| Continuous output current                            | $\overline{\text{FLT}}$ , PG                | 10          | mA   |
| Operating junction temperature range, T <sub>J</sub> |                                             | –55 to 125  | °C   |
| ESD - Human body model (HBM)                         |                                             | 2           | kV   |
| ESD - Charged device model (CDM)                     |                                             | 1.5         |      |

(1) All voltages are with respect to SOURCE (unless otherwise noted).

(2) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

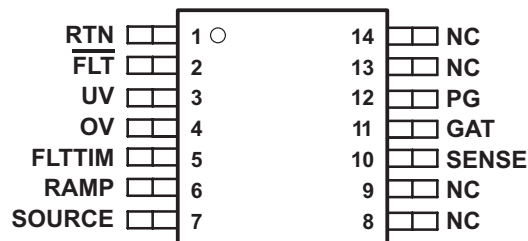
(3) With 10 k $\Omega$  minimum series resistance. Range limited to –0.3V to 80V from low impedance source.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|                                      | MIN | NOM | MAX | UNIT |
|--------------------------------------|-----|-----|-----|------|
| Input supply, SOURCE to RTN          | –80 | –48 | –12 | V    |
| Operating junction temperature range | –40 |     | 85  | °C   |

**TSSOP-14 PACKAGE  
(TOP VIEW)**



## PRODUCT INFORMATION<sup>(1)</sup>

| T <sub>A</sub> | PACKAGE  | PART NUMBER |
|----------------|----------|-------------|
| –40°C to 85°C  | TSSOP-14 | TPS2394PW   |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## THERMAL INFORMATION

| THERMAL METRIC <sup>(1)</sup> |                                              | TPS2394        | UNITS |
|-------------------------------|----------------------------------------------|----------------|-------|
|                               |                                              | PW (14 (PINS)) |       |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance       | 120.8          | °C/W  |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 62.8           |       |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 1              |       |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 56.5           |       |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## ELECTRICAL CHARACTERISTICS

SOURCE = -48 V, UV = 2.5 V, OV = 0.5 V, SENSE = 0 V, RAMP = 0 V, T<sub>A</sub> = -40°C to 85°C (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER                                       |                                            | TEST CONDITIONS                                       | MIN   | TYP   | MAX   | UNIT |
|-------------------------------------------------|--------------------------------------------|-------------------------------------------------------|-------|-------|-------|------|
| INPUT SUPPLY                                    |                                            |                                                       |       |       |       |      |
| I <sub>CC1</sub>                                | Supply current                             | SOURCE = -48 V                                        |       | 1000  | 1500  | μA   |
| I <sub>CC2</sub>                                | Supply current                             | SOURCE = -80 V                                        |       |       | 2000  |      |
| V <sub>UVLO_I</sub>                             | Internal UVLO threshold voltage            | To GAT pull up                                        | -11.8 | -10   | -8    | V    |
| V <sub>HYST</sub>                               | Internal UVLO hysteresis voltage           |                                                       | 50    | 240   | 500   | mV   |
| OVERVOLTAGE AND UNDERVOLTAGE INPUTS (OV AND UV) |                                            |                                                       |       |       |       |      |
| V <sub>THUV</sub>                               | UV threshold voltage, UV rising, to SOURCE | To GAT pull up, 25°C                                  | 1.391 | 1.400 | 1.409 | V    |
|                                                 |                                            | To GAT pull up, 0 to 70°C                             | 1.387 | 1.400 | 1.413 |      |
|                                                 |                                            | To GAT pull up, -40 to 85°C                           | 1.384 | 1.400 | 1.419 |      |
| I <sub>HYSUV</sub>                              | UV hysteresis                              | UV = -45.5 V                                          | -11   | -10   | -9    | μA   |
| I <sub>ILUV</sub>                               | UV low-level input current                 | UV = -47 V                                            | -1    |       | 1     |      |
| V <sub>THOV</sub>                               | OV threshold voltage, OV rising, to SOURCE | To GAT pull up                                        | 1.376 | 1.400 | 1.426 | V    |
| I <sub>HYSOV</sub>                              | OV hysteresis                              | OV = -45.5 V                                          | -11.1 | -10   | -8.6  | μA   |
| I <sub>ILOV</sub>                               | OV low-level input current                 | OV = -47 V                                            | -1    |       | 1     |      |
| LINEAR CURENT AMPLIFIER (LCA)                   |                                            |                                                       |       |       |       |      |
| V <sub>OH</sub>                                 | High level output, GAT-SOURCE              | SENSE = SOURCE                                        | 11    | 14    | 17    | V    |
| I <sub>SINK_f</sub>                             | GAT sink current in fault                  | SENSE – SOURCE = 80 mV,<br>GAT = -43 V, FLTTIME = 5 V | 30    | 75    |       | mA   |
| I <sub>SINK_I</sub>                             | GAT sink current in linear mode            | SENSE – SOURCE = 80 mV,<br>GAT = -43 V, FLTTIME = 2 V |       | 5     | 10    |      |
| I <sub>IN</sub>                                 | SENSE input current                        | 0 V < SENSE – SOURCE < 0.2 V                          | -1    |       | 1     | μA   |
| V <sub>REF_K</sub>                              | Reference clamp voltage, SENSE – SOURCE    | RAMP – SOURCE = 6 V                                   | 34    | 42    | 50    | mV   |
| V <sub>IO</sub>                                 | Input offset voltage, SENSE – SOURCE       | RAMP – SOURCE = 0 V                                   | -7    |       | 9     |      |

(1) All voltages are with respect to RTN unless otherwise stated.

(2) Currents are positive into and negative out of the specified terminal.

**ELECTRICAL CHARACTERISTICS (continued)**SOURCE = -48 V, UV = 2.5 V, OV = 0.5 V, SENSE = 0 V, RAMP = 0 V, T<sub>A</sub> = -40°C to 85°C (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER                                                     |                                                           | TEST CONDITIONS                                                                                            | MIN   | TYP  | MAX  | UNIT |
|---------------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-------|------|------|------|
| <b>RAMP GENERATOR</b>                                         |                                                           |                                                                                                            |       |      |      |      |
| I <sub>SRC1</sub>                                             | RAMP source current, slow turn-on rate                    | RAMP – SOURCE = 0.25 V                                                                                     | -800  | -550 | -300 | nA   |
| I <sub>SRC2</sub>                                             | RAMP source current, normal rate                          | RAMP – SOURCE = 1 V and 3 V                                                                                | -11.3 | -10  | -8.5 | μA   |
| V <sub>OL</sub>                                               | Low-level output voltage                                  | UV = SOURCE                                                                                                |       |      | 5    | mV   |
| A <sub>V</sub>                                                | Voltage gain, relative to SENSE                           | 0 V < RAMP – SOURCE < 5 V                                                                                  | 9.5   | 10   | 10.7 | mV/V |
| <b>OVERLOAD COMPARATOR</b>                                    |                                                           |                                                                                                            |       |      |      |      |
| V <sub>TH_OL</sub>                                            | SENSE current overload threshold                          |                                                                                                            | 100   | 120  | 140  | mV   |
| t <sub>RSP</sub>                                              | Response time                                             | SENSE – SOURCE = 200 mV                                                                                    | 2     | 4    | 7    | μs   |
| <b>FAULT TIMER</b>                                            |                                                           |                                                                                                            |       |      |      |      |
| V <sub>OL</sub>                                               | FLTTIM low-level output voltage, to SOURCE                | UV = -48 V                                                                                                 |       |      | 5    | mV   |
| I <sub>CHG</sub>                                              | FLTTIM charging current, current limit mode               | FLTTIM – SOURCE = 2 V                                                                                      | -54   | -50  | -41  | μA   |
| V <sub>FLT</sub>                                              | FLTTIM fault threshold voltage to SOURCE                  |                                                                                                            | 3.75  | 4.00 | 4.25 | V    |
| V <sub>RST</sub>                                              | Fault reset threshold to SOURCE                           |                                                                                                            |       | 0.5  |      |      |
| I <sub>DSG</sub>                                              | FLTTIM Discharge current, retry mode                      | FLTTIM – SOURCE = 2 V                                                                                      |       | 0.38 | 0.75 | μA   |
| D                                                             | Output duty cycle during retry cycles                     | SENSE – SOURCE = 80 mV,<br>FLTTIM – SOURCE = 2 V                                                           |       | 1%   | 1.5% |      |
| I <sub>RST</sub>                                              | FLTTIM discharge current, timer reset mode                | FLTTIM – SOURCE = 2 V, SENSE = V                                                                           |       | 1    |      | mA   |
| <b>LOGIC OUTPUTS (<math>\overline{\text{FLT}}</math>, PG)</b> |                                                           |                                                                                                            |       |      |      |      |
| I <sub>OHFLT</sub>                                            | $\overline{\text{FLT}}$ high-level output leakage current | UV = -48 V, $\overline{\text{FLT}}$ – SOURCE = 80 V                                                        | -10   |      | 10   | μA   |
| I <sub>OHPG</sub>                                             | PG high-level output leakage current                      | UV = -45 V, PG – SOURCE = 80 V                                                                             | -10   |      | 10   |      |
| R <sub>DS(on)</sub>                                           | $\overline{\text{FLT}}$ ON resistance                     | SENSE – SOURCE = 80 mV,<br>FLTTIM – SOURCE = 5 V, I <sub>(<math>\overline{\text{FLT}}</math>)</sub> = 1 mA |       | 50   | 80   | Ω    |
|                                                               | PG ON resistance                                          | UV = -48 V, I <sub>O</sub> (PG) = 1 mA                                                                     |       | 50   | 80   | Ω    |

## DEVICE INFORMATION

### PIN FUNCTIONS

| PIN                     |     | I/O | DESCRIPTION                                                                                               |
|-------------------------|-----|-----|-----------------------------------------------------------------------------------------------------------|
| NAME                    | NO. |     |                                                                                                           |
| $\overline{\text{FLT}}$ | 2   | O   | Open-drain, active-low indication that the part is in fault.                                              |
| FLTTIM                  | 5   | I/O | Connection for user programming of the fault timeout period.                                              |
| GAT                     | 11  | O   | Gate drive for external N-channel MOSFET that ramps load current and disconnects in the event of a fault. |
| NC                      | 9   |     | Not connected, leave floating                                                                             |
| NC                      | 8   |     | Not connected, leave floating                                                                             |
| NC                      | 14  |     | Not connected, leave floating                                                                             |
| NC                      | 13  |     | Not connected, leave floating                                                                             |
| OV                      | 4   | I   | Over voltage sense input.                                                                                 |
| PG                      | 12  | O   | Open-drain, active-high indication that the power MOSFET is fully enhanced.                               |
| RAMP                    | 6   | I/O | Programming input for setting the inrush current slew rate.                                               |
| RTN                     | 1   | I   | Supply return (for positive grounded system).                                                             |
| SENSE                   | 10  | I   | Positive current sense input.                                                                             |
| SOURCE                  | 7   | I/O | Negative current sense input.                                                                             |
| UV                      | 3   | I   | Under voltage sense input.                                                                                |

### PIN DESCRIPTIONS

**$\overline{\text{FLT}}$ :** Open-drain, active-low indication that TPS2394 has shut down due to a faulted load. This happens if the load current stays limited by the linear current amplifier (LCA) for more than the fault time (time to charge the FLTTIM capacitor).  $\overline{\text{FLT}}$  is cleared when input supply drops below the UV-comparator threshold or exceeds the OV-comparator threshold. The  $\overline{\text{FLT}}$  output is pulled to SOURCE. The  $\overline{\text{FLT}}$  output is able to sink 10 mA when in fault, withstand 80 V without leakage when not faulted, and withstand transients as high as 100 V when limited by a series resistor of at least 10 k $\Omega$ .

**FLTTIM:** Connection for user programming of the fault timeout period. An external capacitor connected from FLTTIM to SOURCE establishes the timeout period to declare a fault condition. This timeout protects against indefinite current sourcing into a faulted load, and also provides a filter against nuisance trips from momentary current spikes or surges. TPS2394 defines a fault condition as voltage at the SENSE pin at or greater than the 42-mV fault threshold. When a fault condition exists, the timer is active. The devices manage fault timing by charging the external capacitor to the 4-V fault threshold, then subsequently discharging it at approximately 1% the charge rate to establish the duty cycle for retrying the load. Whenever the fault latch is set (timer expired), GAT and  $\overline{\text{FLT}}$  are pulled low.

**GAT:** Gate drive for an external N-channel protection power MOSFET. When input supply is above the UV threshold and below the OV threshold, gate drive is enabled and the device begins charging the external capacitor connected to RAMP. RAMP develops the reference voltage at the non-inverting input of the internal LCA. The inverting input is connected to the current sense node, SENSE. The LCA acts to slew the pass MOSFET gate to force the SENSE voltage to track the reference. The reference is internally clamped to 42 mV, so the maximum current that can be sourced to the load is determined by the sense resistor value as  $I_{\text{MAX}} \leq 42 \text{ mV}/R_{\text{SENSE}}$ . Once the load voltage has ramped up to the input dc potential and current demand drops off, the LCA drives GAT 14 V above SOURCE to fully enhance the pass MOSFET, completing the low-impedance supply return path for the load.

**PG:** Open-drain, active-high indication that load current is below the current limit and the power MOSFET is fully enhanced. When commanded load current is more than the actual load current, the linear current amplifier (LCA) will raise the power MOSFET gate voltage to fully enhance the power MOSFET. At this time, the PG output will go high. This output can be used to enable a down-stream dc-to-dc converter. The PG output is pulled to SOURCE and is able to sink 10 mA when in fault, withstand 80 V without leakage when power is not good, and withstand transients as high as 100 V when limited by a series resistor of at least 10 k $\Omega$ .

**OV:** Over voltage comparator input. This input is typically connected to a voltage divider between RTN and SOURCE to sense the magnitude of the input supply. If OV is less than 1.4 V above SOURCE, and UV is more than 1.4 V above SOURCE, and there is no fault, the linear current amp will be enabled. In the event of a fault, pulling OV high or UV low will reset the fault latch and allow the IC to restart. OV can also be used as an active-low logic enable input. The over-voltage comparator hysteresis is programmed by the equivalent resistance seen looking into the divider at the OV input.

**RAMP:** Programming input for setting inrush current and current slew rate. An external capacitor connected between RAMP and SOURCE establishes turn-on current slew rate. During turn-on, TPS2394 charges this capacitor to establish the reference input to the LCA at 1% of the voltage from RAMP to SOURCE. The closed-loop control of the LCA and the pass MOSFET maintains the  $V(\text{SENSE} - \text{SOURCE})$  at the reference potential, so the load current slew rate is directly set by the voltage ramp rate at the RAMP pin. When fully charged, RAMP can exceed SOURCE by 6 V, but the reference is internally clamped to 42 mV, limiting load current to  $42 \text{ mV}/R_{\text{SENSE}}$ . When the output is disabled via OV, UV, or due to a load fault, the RAMP capacitor is discharged and held low to initialize for the next turn on.

The TPS2394 initiates ramp capacitor charging, and consequently load current slewing, at a reduced rate. This reduced rate applies until the voltage on the RAMP pin is about 0.5 V. The maximum di/dt rate, as set by [Equation 2](#), is effective once the device switches to a 10-mA charging source.

**RTN:** Positive supply input. For negative voltage systems, this pin connects directly to the return node of the input power bus.

**SENSE:** Current sense input. An external low-value resistor connected between SENSE and SOURCE is used to monitor current magnitude. There are two internal device thresholds associated with the voltage at the SENSE pin. During ramp-up of the load capacitance or during other periods of excessive demand, the linear current amp (LCA) will regulate this voltage to 42 mV. Whenever the LCA is in current regulation mode, the FLTTIM capacitor charges. If the LCA output is at its maximum, GAT is pulled 14 V above SOURCE. At this time, a fast fault such as a short circuit can cause the SENSE voltage to rapidly exceed 120 mV (the overload threshold). In this case, the GAT pin is pulled low rapidly, bypassing the fault timer.

**SOURCE:** Connection to the input supply negative rail.

**UV:** Under Voltage Comparator input. This input is typically connected to a voltage divider between RTN and SOURCE to sense the magnitude of the input supply. If UV is more than 1.4 V above SOURCE, OV is less than 1.4 V above SOURCE, and there is no fault, the LCA will be enabled. In the event of a fault, pulling UV low or OV high will reset the fault latch and allow restarting. UV can also be used as an active high logic enable input. The under-voltage comparator hysteresis is programmed by the equivalent resistance seen looking into the divider at the UV input.

## TYPICAL CHARACTERISTICS

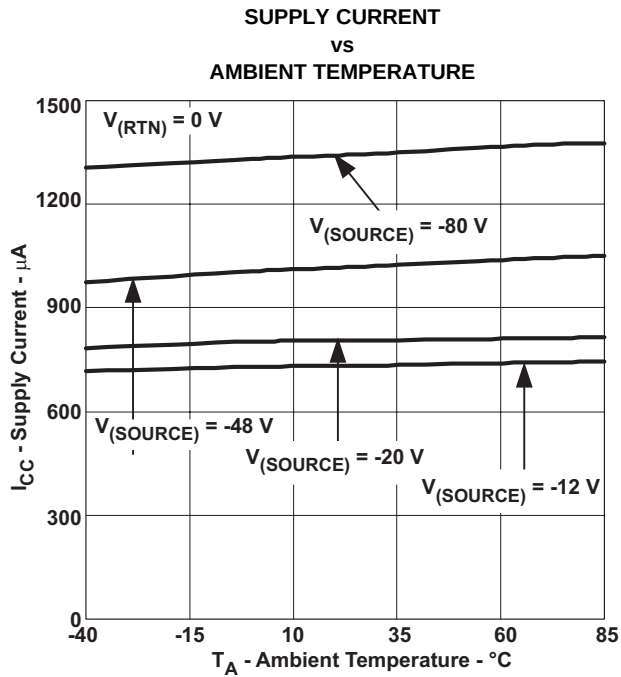


Figure 1.

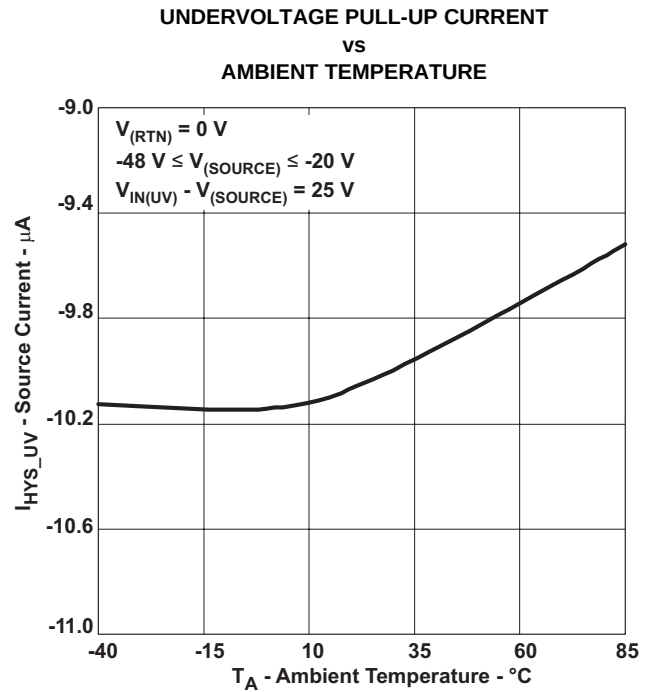


Figure 2.

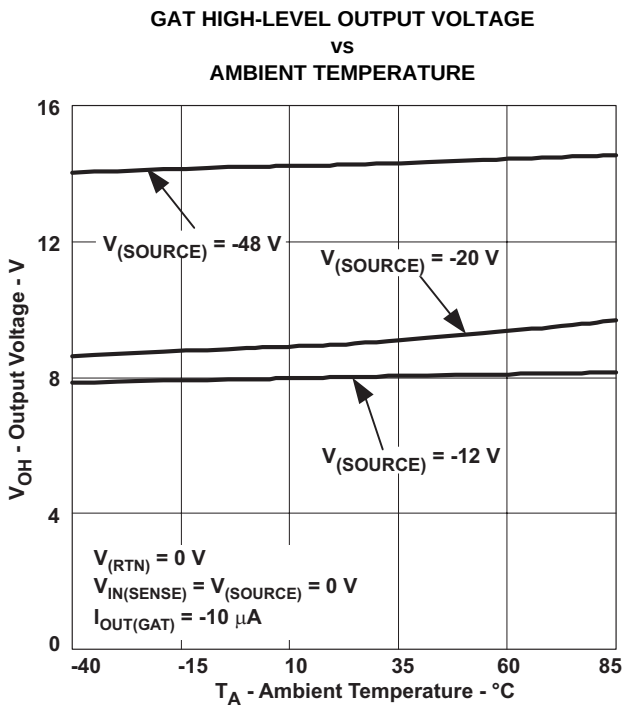


Figure 3.

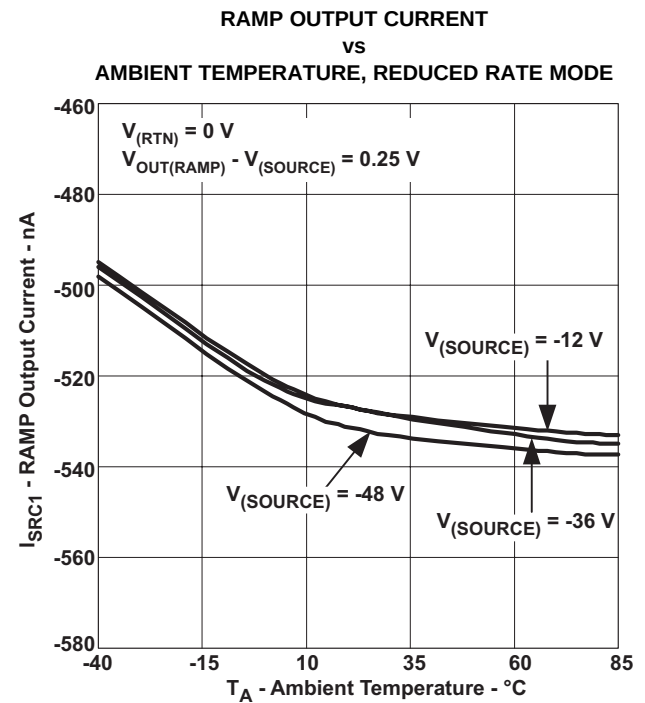


Figure 4.

# TYPICAL CHARACTERISTICS (continued)

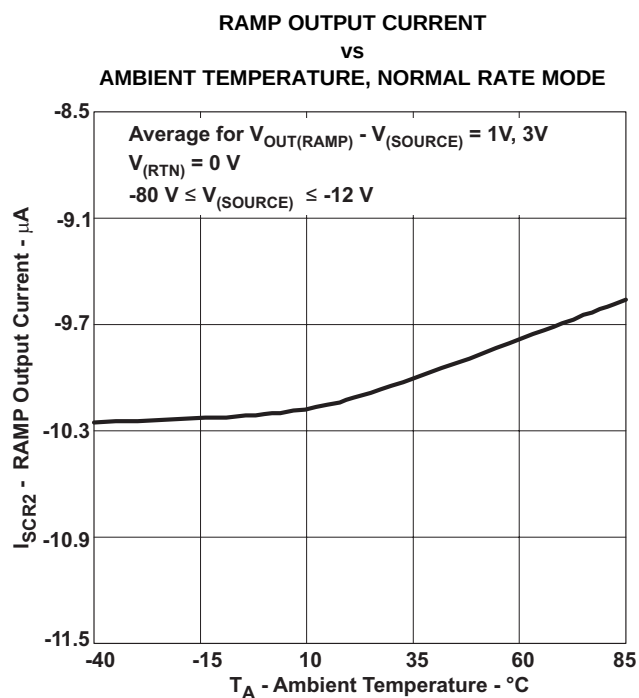


Figure 5.

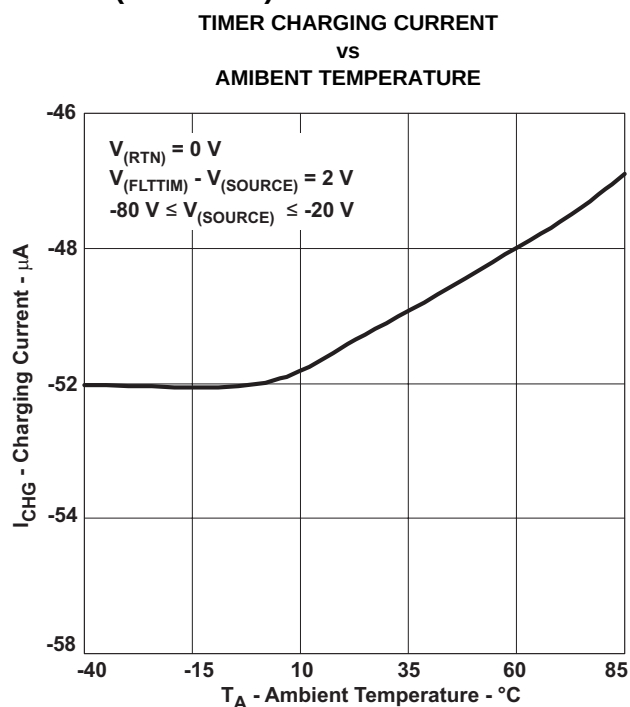


Figure 6.

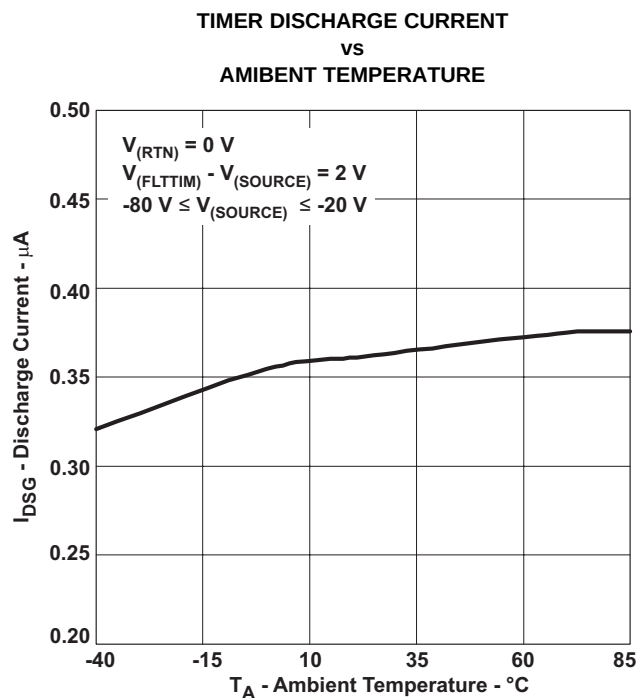


Figure 7.

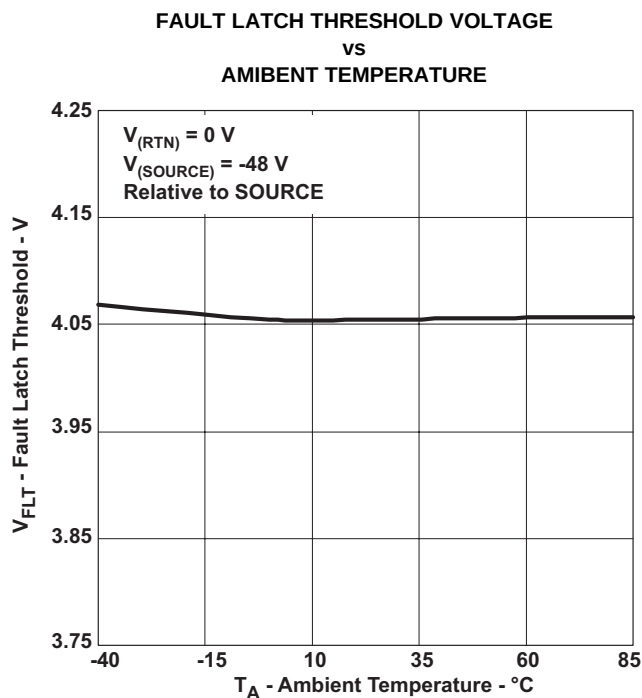
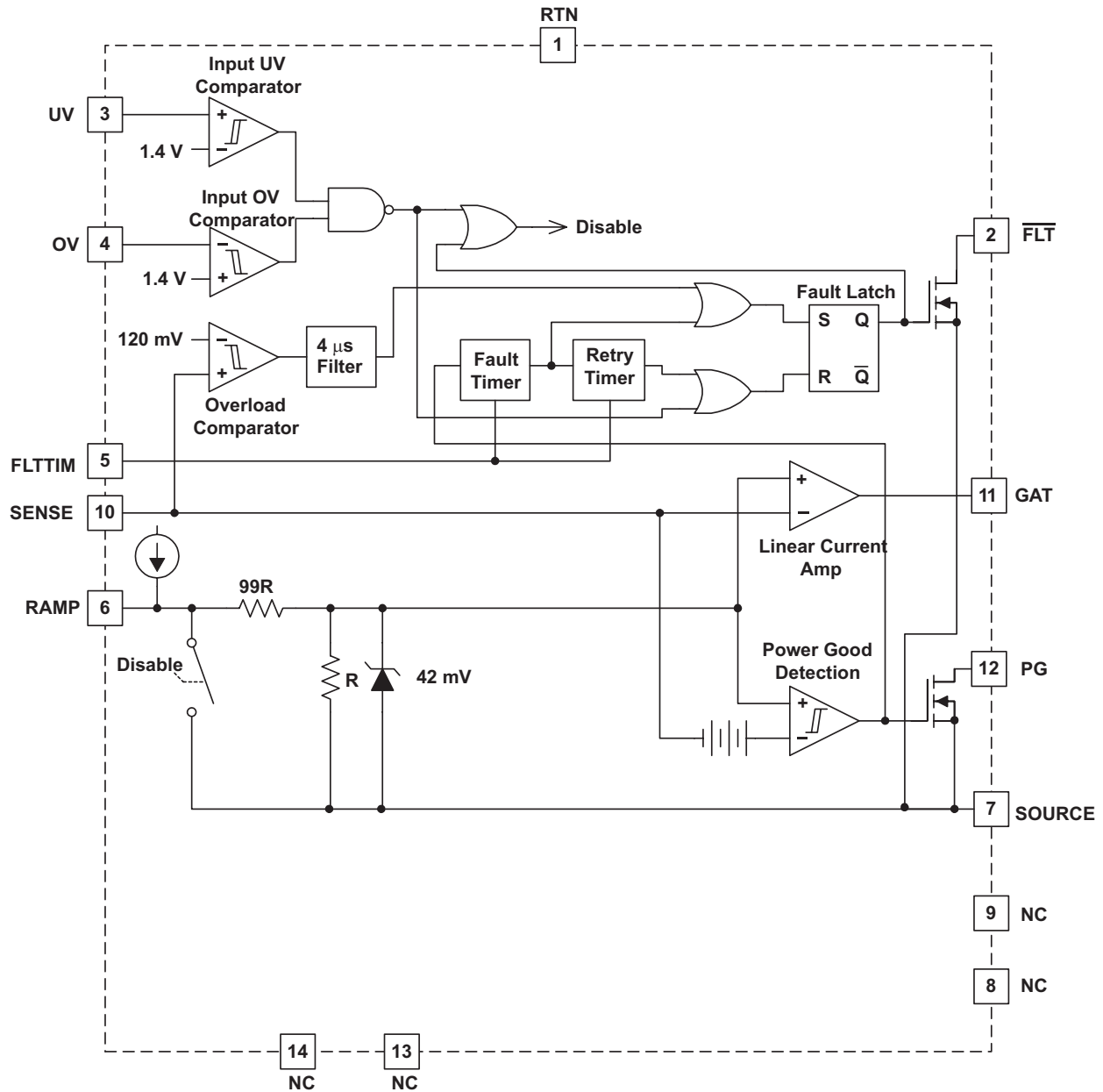


Figure 8.

## FUNCTIONAL BLOCK DIAGRAM



## APPLICATION INFORMATION

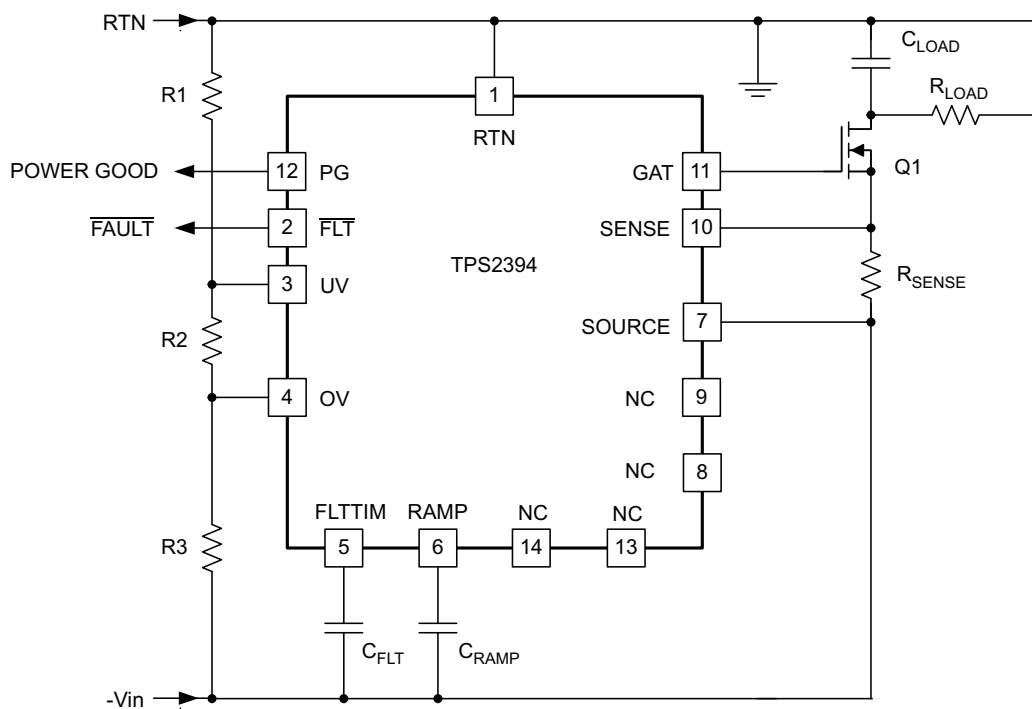


Figure 9. Typical Application

## APPLICATION INFORMATION

### Setting the Sense Resistor Value

Due to the current-limiting action of the internal LCA, the maximum allowable load current for an implementation is easily programmed by selecting the appropriate sense resistor value. The LCA acts to limit the sense voltage  $V(\text{SENSE-SOURCE})$  to its internal reference. Once the voltage at the RAMP pin exceeds approximately 4 V, this limit is the clamp voltage,  $V_{\text{REF\_K}}$ . Therefore; a maximum sense resistor value can be determined from [Equation 1](#).

$$R_{\text{SENSE}} \leq \frac{34 \text{ mV}}{I_{\text{IMAX}}} \quad (1)$$

Where:

$R_{\text{SENSE}}$  is the sensing resistor value

$I_{\text{IMAX}}$  is the minimum desired current limit

When setting the sense resistor value, it is important to consider two factors, the minimum current limit that may be imposed by the TPS2394, and the maximum load under normal operation of the module. For the first factor, the specification minimum clamp value is used, as seen in [Equation 1](#). Second factor is to ensure the peak operating load current is less than  $I_{\text{IMAX}}$ . One example of this is a switching converter which draws higher input current, for a given power output, when the output is at the low end of its voltage range. To avoid current limit operation under normal loading, some margin should be designed in between this maximum anticipated load and the minimum current limit level, or  $I_{\text{IMAX}} > I_{\text{LOAD(max)}}$ , for [Equation 1](#).

For example, using a 10-m $\Omega$  sense resistor for a nominal 2-A load application provides a minimum of 1.4 A of overhead for load variance/margin. Typical bulk capacitor charging current during turn-on is 4.2 A (42 mV/10 m $\Omega$ ).

### Setting the Inrush Slew Rate

The TPS2394 device enables user-programming of the maximum current slew rate during load start-up events. A capacitor tied to the RAMP pin ( $C_{\text{RAMP}}$  in the typical application diagram) controls the  $di/dt$  rate. Once the sense resistor value has been established, a value for  $C_{\text{RAMP}}$ , in microfarads, can be determined from [Equation 2](#).

$$C_{\text{RAMP}} = \frac{11.3}{100 \times R_{\text{SENSE}} \times \left( \frac{di}{dt} \right)_{(\text{max})}} \quad (2)$$

Where:

$R_{\text{SENSE}}$  is the sense resistor value in  $\Omega$

$(di/dt)_{(\text{max})}$  is the desired maximum slew rate in A/s

For example, if the desired slew rate for the typical application shown is 1500 mA/ms, the calculated value for  $C_{\text{RAMP}}$  is about 7500 pF. Selecting the next larger standard value of 8200 pF provides some margin for capacitor and sense resistor tolerances.

### Setting the Fault Timing Capacitor

The fault timeout period is established by the value of the capacitor connected to the FLTTIM pin,  $C_{\text{FLT}}$ . The timeout period permits riding out spurious current glitches and surges that may occur during operation of the system, and prevents indefinite sourcing into faulted loads. However, to ensure smooth voltage ramping under all conditions of load capacitance and input supply potential, the minimum timeout should be set to accommodate these system variables. To do this, a rough estimate of the maximum voltage ramp time for a completely discharged plug-in card provides a good basis for setting the minimum timer delay. This section presents a quick procedure for calculating the timing capacitance requirement. However, for proper operation of the TPS2394, there is an absolute minimum value of 0.01- $\mu$ F for  $C_{\text{FLT}}$ . This minimum requirement overrides any smaller results of [Equation 7](#) and [Equation 8](#).

Due to the three-phase nature of the load current at turn-on, the load voltage ramp has potentially three distinct phases. This profile depends on the relative values of load capacitance, input DC potential, maximum current limit and other factors. The first two phases are characterized by the two different slopes of the current ramp; the third phase, if required to complete load charging, is the constant-current charging at I<sub>MAX</sub>. Considering the two current ramp phases to be one period at an average di/dt simplifies calculation of the required timing capacitor.

For the TPS2394, the typical duration of the soft-start period, t<sub>SS</sub>, is given by Equation 3.

$$t_{SS} = 1260 \times C_{RAMP} \quad (3)$$

Where:

t<sub>SS</sub> is the soft-start period in ms

C<sub>RAMP</sub> is given in μF

During this current ramp period, the load voltage magnitude which is attained is estimated by Equation 4.

$$V_{LSS} = \frac{i_{AVG}}{2 \times C_{LOAD} \times C_{RAMP} \times 100 \times R_{SENSE}} \times (t_{SS})^2 \quad (4)$$

Where:

V<sub>LSS</sub> is the load voltage reached during soft-start

i<sub>AVG</sub> is 3.18 μA for the TPS2394

C<sub>LOAD</sub> is the load capacitance in Farads

t<sub>SS</sub> is the soft-start period in s

The quantity i<sub>AVG</sub> in Equation 4 is a weighted average of the two charge currents applied to C<sub>RAMP</sub> during turn-on, considering the typical output values.

If the result of Equation 4 is larger than the maximum input supply value, then the load can be expected to charge completely during the inrush slewing portion of the insertion event. However, if this voltage is less than the maximum supply input, V<sub>IN(MAX)</sub>, the HSPM transitions to the constant-current charging of the load. The remaining amount of time required at I<sub>MAX</sub> is determined from Equation 5.

$$t_{CC} = \frac{C_{LOAD} \times (V_{IN(MAX)} - V_{LSS})}{\frac{V_{REF\_K(MIN)}}{R_{SENSE}}} \quad (5)$$

Where:

t<sub>CC</sub> is the constant-current voltage ramp time, in seconds

V<sub>REF\_K(MIN)</sub> is the minimum clamp voltage, 34 mV

With this information, the minimum recommended value timing capacitor C<sub>FLT</sub> can be determined. The delay time needed will be either a time t<sub>SS2</sub> or the sum of t<sub>SS2</sub> and t<sub>CC</sub>, according to the estimated time to charge the load. The quantity t<sub>SS2</sub> is the duration of the normal rate current ramp period, and is given by Equation 6.

$$t_{SS2} = 0.35 \times C_{RAMP} \quad (6)$$

Where:

C<sub>RAMP</sub> is given in μF

Since fault timing is generated by the constant-current charging of C<sub>FLT</sub>, the capacitor value is determined from either Equation 7 or Equation 8, as appropriate.

$$C_{FLT(MIN)} = \frac{54 \times t_{SS2}}{3.75} \quad (7)$$

$$C_{FLT(MIN)} = \frac{54 \times (t_{SS2} + t_{CC})}{3.75} \quad (8)$$

Where:

C<sub>FLT(MIN)</sub> is the recommended capacitor value, in μ-Farads

t<sub>SS2</sub> is the result of Equation 6, in seconds

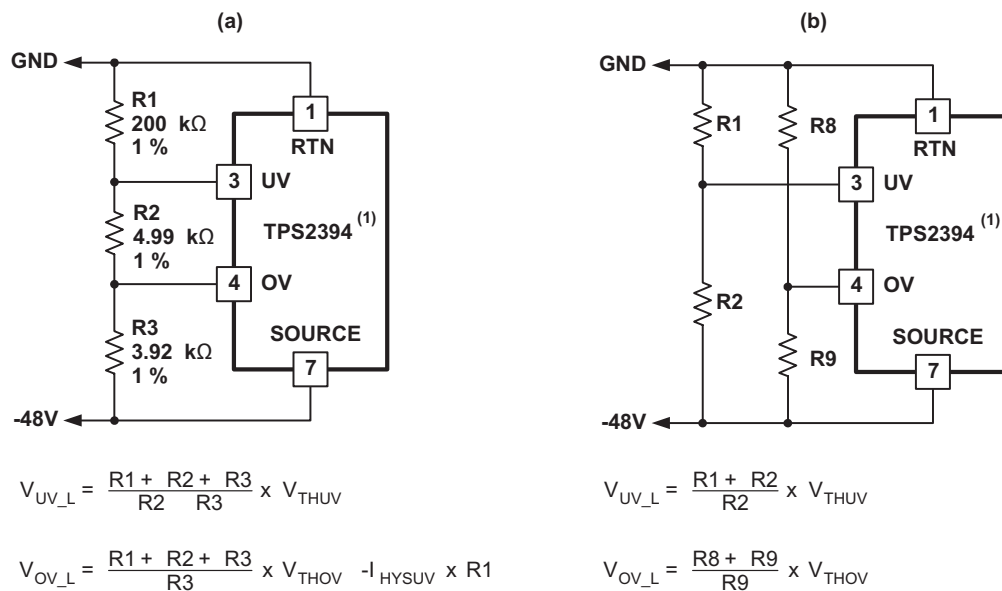
t<sub>CC</sub> is the result of Equation 5, in seconds

Continuing this calculation example, using a 220-μF input capacitor ( $C_{LOAD}$ ), Equation 3 and Equation 4 estimate the load voltage ramping to approximately –45 V during the soft-start period. If the module should operate down to –72-V input supply, approximately another 1.4 ms of constant-current charging may be required. Therefore, Equation 6 and Equation 8 are used to determine  $C_{FLT(MIN)}$ , and the result is approximately 0.039-μF.

## Setting the Undervoltage and Overvoltage Thresholds

The UV and OV pins can be used to set the undervoltage ( $V_{UV}$ ) and overvoltage ( $V_{OV}$ ) thresholds of the hot swap circuit. When the input supply is below  $V_{UV}$  or above  $V_{OV}$ , the GAT pin is held low, disconnecting power from the load, and the PG output is deasserted. When input voltage is within the UV/OV window, the GAT pin drive is enabled, assuming all other input conditions are valid for turn-on.

Threshold hysteresis is provided via two internal sources which are switched to either pin whenever the corresponding input level exceeds the internal 1.4-V reference. The additional bias shifts the pin voltage in proportion to the external resistance connected to it. This small voltage shift at the device pin is gained up by the external divider to input supply levels.



**Figure 10. Programming the Undervoltage and Overvoltage Thresholds**

The UV and OV thresholds can be individually programmed with a three-resistor divider connected to the TPS2394 as shown in the typical application diagram, and again in Figure 10a. When the desired trip voltages and undervoltage hysteresis have been established for the protected board, the resistor values needed can be determined from the following equations. First, select the top leg of the divider (R1 in the diagram) to obtain the threshold hysteresis. This value is calculated using Equation 9.

$$R1 = \frac{V_{HYS\_UV}}{10 \mu A} \quad (9)$$

Where:

$V_{HYS\_UV}$  is the undervoltage hysteresis value

For example, assume the typical application design targets have been set to undervoltage turn-on at 33 V (input supply rising), turn-off at 31 V (input voltage falling), and overvoltage shutdown at 72 V. Then Equation 9 yields  $R1 = 200 \text{ k}\Omega$  for the 2-V hysteresis. Once the value of R1 is selected, it is used to calculate resistors R2 and R3.

$$R2 = \frac{1.4 \times R1}{(V_{UV\_L} - 1.4)} \times \left[ 1 - \frac{V_{UV\_L}}{(V_{OV\_L} + 10^{-5} \times R1)} \right] \quad (10)$$

$$R3 = \frac{1.4 \times R1 \times V_{UV\_L}}{(V_{UV\_L} - 1.4) \times (V_{OV\_L} + 10^{-5} \times R1)} \quad (11)$$

Where:

$V_{UV\_L}$  is the UVLO threshold when the input supply is low; i.e., less than  $V_{UV}$ , and

$V_{OV\_L}$  is the OVLO threshold when the input supply is low; i.e., less than  $V_{OV}$

Referring to [Figure 10a](#), [Equation 10](#) and [Equation 11](#) produce  $R2 = 4.909 \text{ k}\Omega$  (4.99 k $\Omega$  selected) and  $R3 = 3.951 \text{ k}\Omega$  (3.92 k $\Omega$  selected), as shown. For the selected values, the expected nominal supply thresholds are  $V_{UV\_L} = 32.8 \text{ V}$ ,  $V_{UV\_H} = 30.8 \text{ V}$ , and  $V_{OV\_L} = 72.6 \text{ V}$ . The hysteresis of the overvoltage threshold, as seen at the supply inputs, is given by the quantity  $(10 \text{ }\mu\text{A}) \times (R1 + R2)$ . For the majority of applications, this value is almost the same as the UV hysteresis, since typically  $R1 \gg R2$ .

If more independent control is needed for the OVLO hysteresis, there are several options. One option is to use separate dividers for both the UV and OV pins, as shown in [Figure 10b](#). In this case, once  $R1$  and  $R8$  have been selected for the required hysteresis per [Equation 9](#), and values for the bottom resistors in the divider ( $R2$  and  $R9$  in [Figure 10b](#)) can be calculated using [Equation 12](#).

$$R_{XVLO} = \frac{V_{REF}}{(V_{XV\_L} - V_{REF})} \times R_{(TOP)} \quad (12)$$

Where:

$R_{XVLO}$  is  $R2$  or  $R9$

$R_{(TOP)}$  is  $R1$  or  $R8$  as appropriate for the threshold being set

$V_{XV\_L}$  is the under ( $V_{UV\_L}$ ) or overvoltage ( $V_{OV\_L}$ ) threshold at the supply input, and

$V_{REF}$  is either  $V_{THUV}$  or  $V_{THOV}$  from the specification table, as required for the resistor being calculated.

## Reverse Voltage Protection

In some applications, it may be necessary to protect the TPS2394 against reverse polarity supply connections or input transients. If the potential at SOURCE pin rises above that of the RTN pin, device damage may result. If the application environment is such that these conditions are anticipated, a small-signal diode should be inserted between the supply return bus and the TPS2394 RTN pin, as shown in the Typical Application diagram. A 75-V to 100-V rated device (VRRM), such as MMBD4148 or BAV19, is recommended.

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS2394PW</a>  | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TPS2394             |
| <a href="#">TPS2394PWR</a> | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | TPS2394             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2394PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

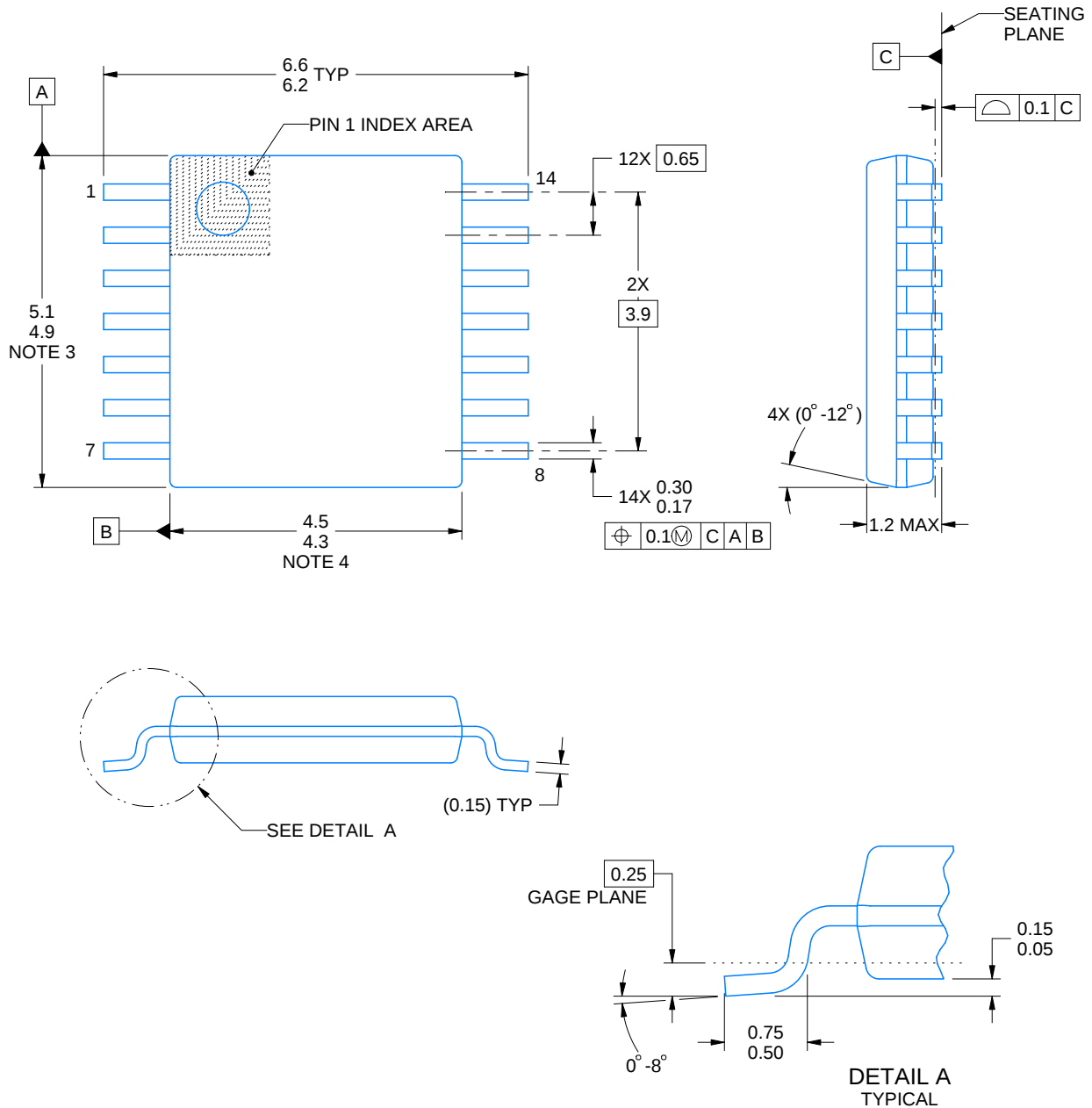
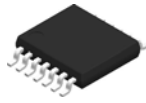
| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2394PWR | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device    | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS2394PW | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |



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## NOTES:

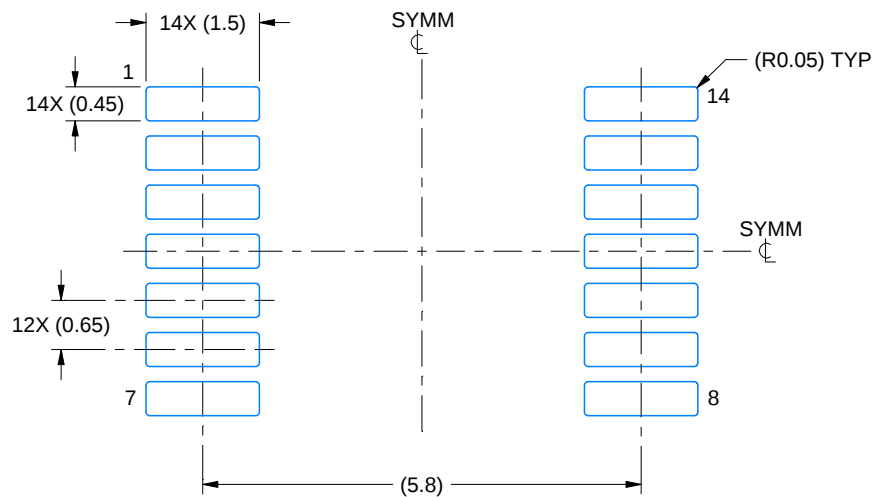
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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