



MX574BBA805M664

Ultra-Low Jitter 805.664062MHz LVPECL XO

ClockWorks® FUSION

General Description

The MX574BBA805M664 is an ultra-low phase jitter XO with LVPECL output optimized for high line rate applications.

Applications

- Optical communications
- Forward error correction (FEC) rates
- FPGA SERDES reference clock

Absolute Maximum Ratings

Supply Voltage (VIN).....+4.6V
Lead Temperature (soldering, 10s).....260°C
Storage Temperature (T_g).....125°C
ESD Rating (HBM).....2kV

Features

- 805.664062MHz LVPECL
- Supports FEC line rate
- Typical phase noise:
 - 103fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

Operating Ratings

Supply Voltage (VIN).....+2.375V to +3.63V
Ambient Temperature (TA).....-40°C to +85°C

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2V.¹

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				120	mA
F0	Center Frequency			805.664062		MHz
	Frequency Stability	Note 2			±50	ppm
Øj	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		142 103		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		85		350	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage	LVPECL output levels	VDD - 1.35	VDD - 1.01	VDD - 0.8	V
VOL	Output Low Voltage	LVPECL output levels	VDD - 2.0	VDD - 1.78	VDD - 1.6	V
Vswing	Peak to Peak Output Voltage Swing		0.65	0.77	0.95	V

Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

ClockWorks is a registered trademark of Microchip Technology Inc.

Microchip Technology Inc.

<http://www.microchip.com>

June 06, 2017
MX574BB1-5329

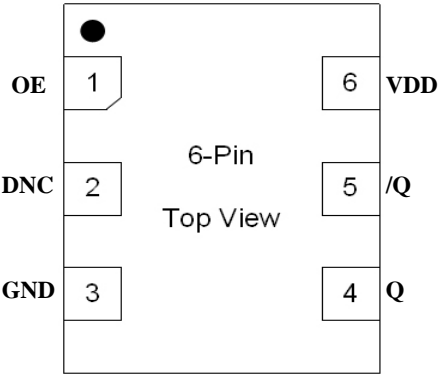
Revision 1.0
tcghelp@microchip.com

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX574BBA805M664	MX574BB	A805M664	Tube	6-Pin 7mm x 5mm LGA
MX574BBA805M664-TR	MX574BB	A805M664	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVPECL	Clock Output Frequency = 805.664062MHz
6	VDD	PWR		Power Supply

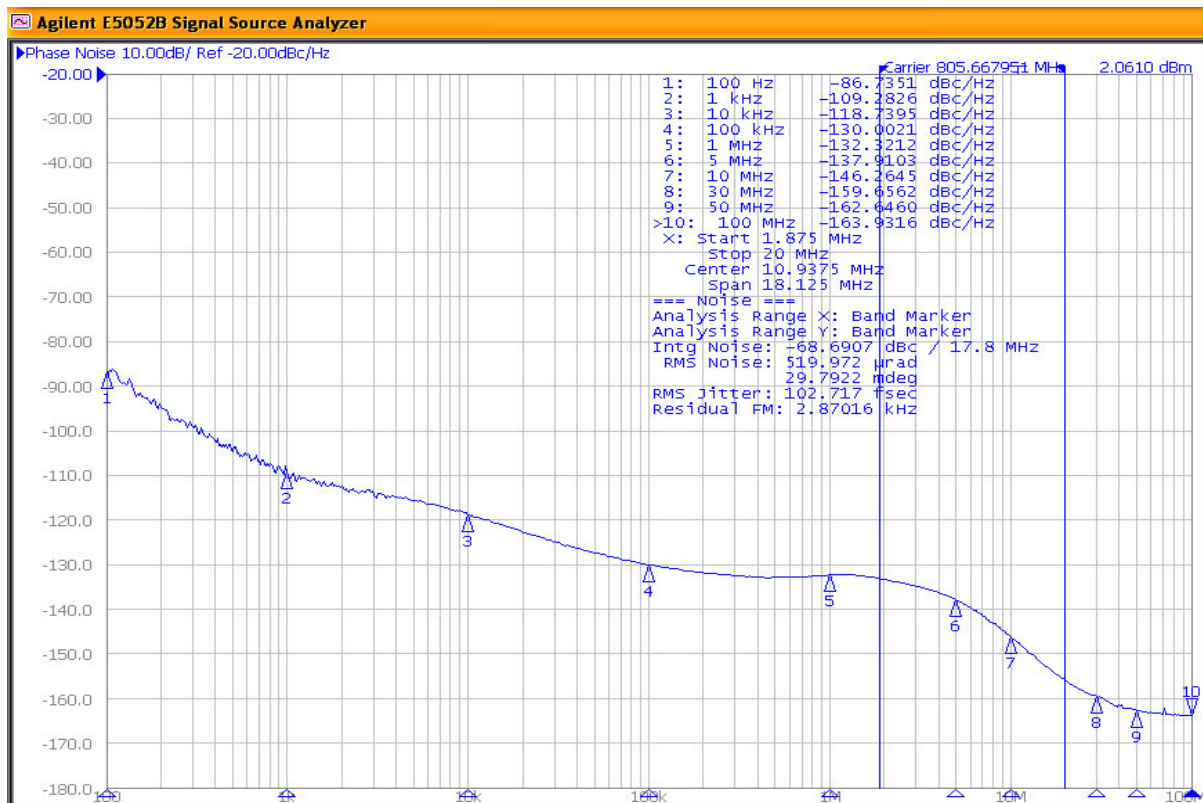


Figure 1. LVPECL Output 805.664062MHz 1.875MHz-20MHz 103fs

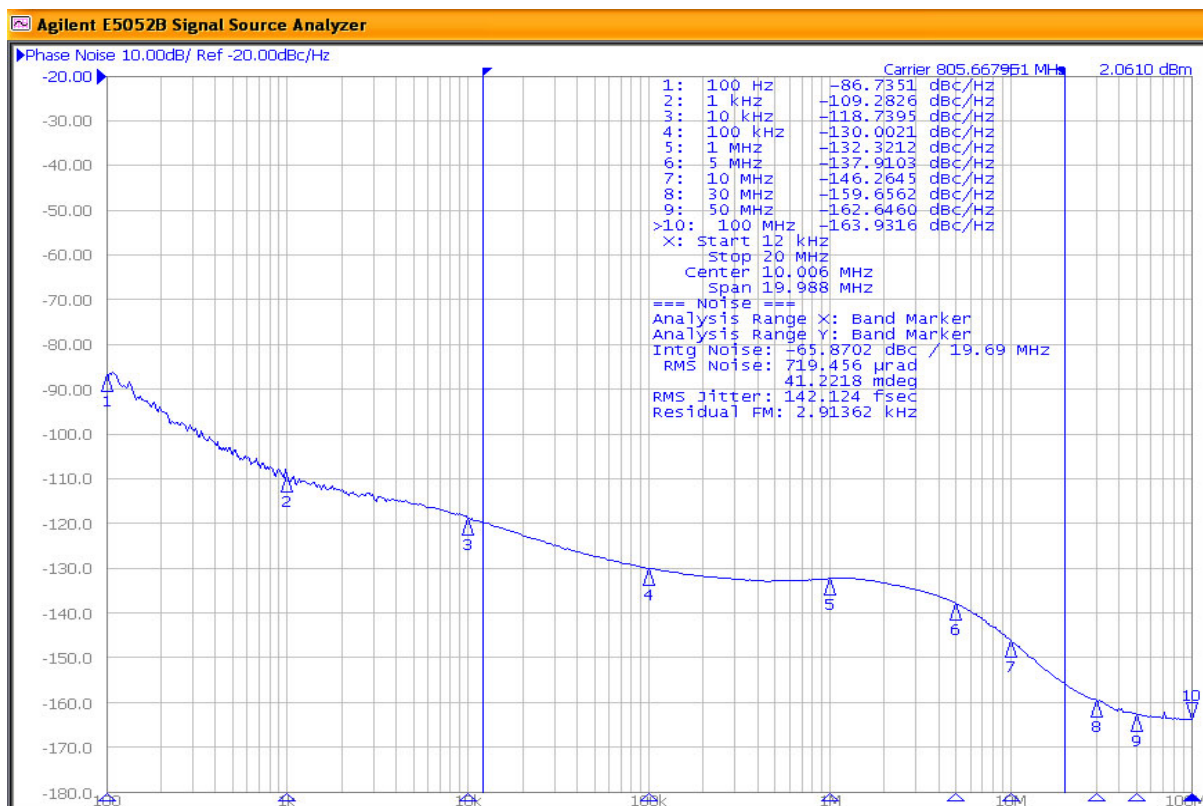


Figure 2. LVPECL Output 805.664062MHz 12kHz-20MHz 142fs

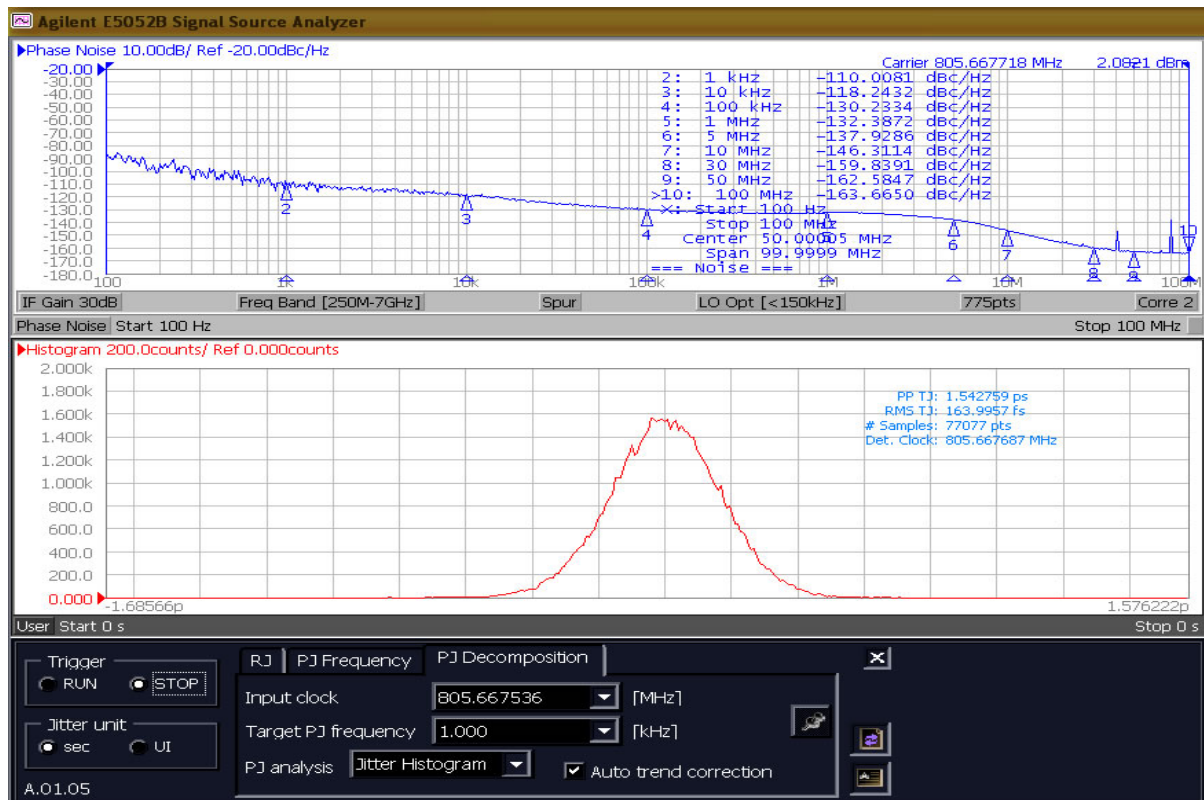
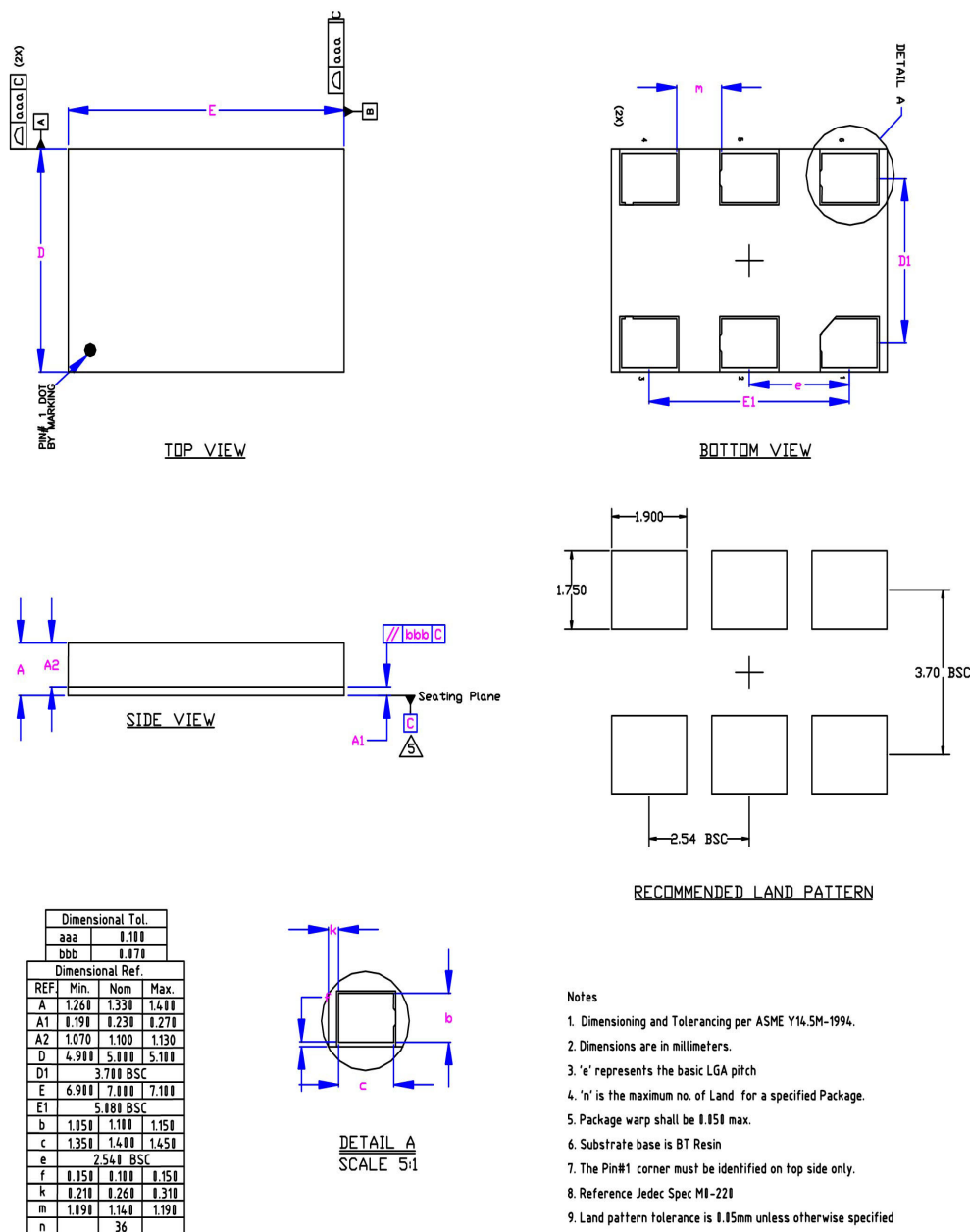


Figure 3. E5001A Period Jitter @ 805.664062MHz LVPECL, RMS TJ: 164fs, Pk-Pk TJ: 1.54ps

Package Information and Recommended Land Pattern for 6-Pin LGA³



6-Pin LGA (7x5mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

Microchip Technology Inc.

<http://www.microchip.com>

Microchip makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet. This information is not intended as a warranty and Microchip does not assume responsibility for its use. Microchip reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Microchip's terms and conditions of sale for such products, Microchip assumes no liability whatsoever, and Microchip disclaims any express or implied warranty relating to the sale and/or use of Microchip products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

© 2017 Microchip Technology Inc.