

SN74LVC1G34 Single Buffer Gate

1 Features

- Available in the Ultra Small 0.64-mm² Package (DPW) with 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Max t_{pd} of 3.5 ns at 3.3 V
- Low Power Consumption, 1- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- DVD Recorder and Player
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

4 Simplified Schematic



3 Description

This single buffer gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G34 device performs the Boolean function Y = A in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} Operating range.

The SN74LVC1G34 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

Device Information⁽¹⁾

DEVICE NAME	PACKAGE (PINS)	BODY SIZE
SN74LVC1G34YFP	DSBGA (4)	0.76 mm × 0.76 mm
SN74LVC1G34YZP	DSBGA (5)	1.38 mm × 0.88 mm
SN74LVC1G34YZV	DSBGA (4)	0.88 mm × 0.88 mm
SN74LVC1G34DPW	X2SON (5)	0.80 mm × 0.80 mm
SN74LVC1G34DBV	SOT-23 (5)	2.90 mm × 2.80 mm
SN74LVC1G34DCK	SC70 (5)	2.00 mm × 2.10 mm
SN74LVC1G34DRL	SOT (5)	1.60 mm × 1.60 mm
SN74LVC1G34DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC1G34DSF	SON(6)	1.00 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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Table of Contents

1	Features	1	9	Detailed Description	11
2	Applications	1	9.1	Overview	11
3	Description	1	9.2	Functional Block Diagram	11
4	Simplified Schematic	1	9.3	Feature Description	11
5	Revision History	2	9.4	Device Functional Modes	11
6	Pin Configuration and Functions	4	10	Application and Implementation	12
7	Specifications	5	10.1	Application Information	12
7.1	Absolute Maximum Ratings	5	10.2	Typical Application	12
7.2	ESD Ratings	5	11	Power Supply Recommendations	13
7.3	Recommended Operating Conditions	6	12	Layout	13
7.4	Thermal Information	6	12.1	Layout Guidelines	13
7.5	Electrical Characteristics	7	12.2	Layout Example	13
7.6	Switching Characteristics, $C_L = 15 \text{ pF}$	8	13	Device and Documentation Support	14
7.7	Switching Characteristics, -40°C to 85°C	8	13.1	Community Resources	14
7.8	Switching Characteristics, -40°C to 125°C	8	13.2	Trademarks	14
7.9	Operating Characteristics	8	13.3	Electrostatic Discharge Caution	14
7.10	Typical Characteristics	8	13.4	Glossary	14
8	Parameter Measurement Information	9	14	Mechanical, Packaging, and Orderable Information	14

5 Revision History

Changes from Revision L (April 2014) to Revision M

	Page
• Changed X2SON from 4 pin to 5 pin on <i>Device Information</i> table	1
• Moved Storage temperature range from <i>ESD Ratings</i> table to <i>Absolute Maximum Ratings</i> table	5
• Added Junction temperature to <i>Absolute Maximum Ratings</i> table	5
• Added package temperature specification for DSBGA package	6

Changes from Revision K (March 2014) to Revision L

	Page
• Added Device Information table	1
• Added Pin Functions table	4
• Updated Handling Ratings table	5
• Updated operating temperature range	6
• Added Thermal Information table	6
• Added Typical Characteristics	8
• Added Detailed Description section	11
• Added Application and Implementation section	12

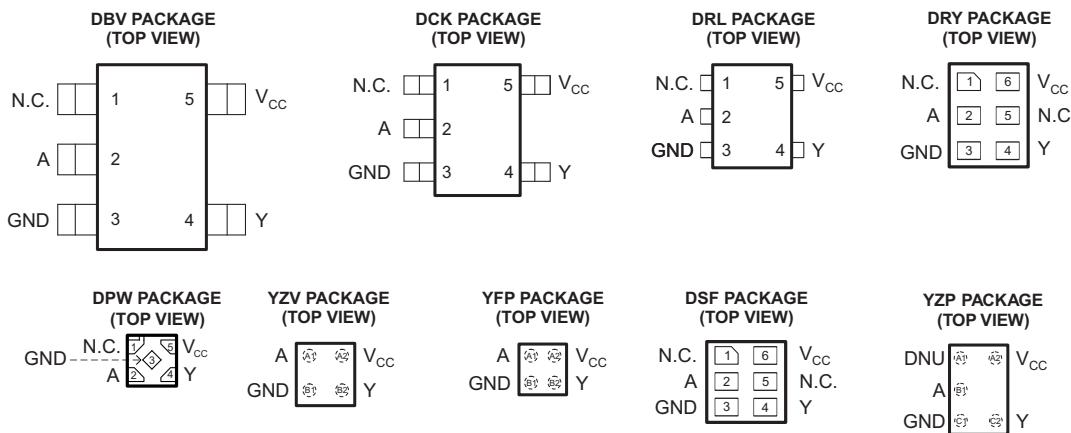
Changes from Revision J (December 2013) to Revision K

	Page
• Added Applications	1
• DPW Package	4
• Moved T_{stg} to Handling Ratings table	5

Changes from Revision I (June2011) to Revision J **Page**

- Updated document to new TI data sheet format. 1
- Removed Ordering Information table. 1

6 Pin Configuration and Functions



See mechanical drawings for dimensions.
N.C. – No internal connection
DNU – Do not use

Pin Functions

PIN						DESCRIPTION
NAME	DRL, DCK, DBV	DPW	DRY, DSF	YZP	YFP, YZV	
NC	1	1	1, 5	A1	–	Not connected
A	2	2	2	B1	A1	Input
GND	3	3	3	C1	B1	Ground
Y	4	4	4	C2	B2	Output
V _{cc}	5	5	6	A2	A2	Power pin

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA
T_{stg}	Storage temperature range	-65	150	°C
T_J	Max Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		± 2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		± 1	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

				MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating		1.65	5.5	V
		Data retention only		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V		1.7		
		V _{CC} = 3 V to 3.6 V		2		
		V _{CC} = 4.5 V to 5.5 V		0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V		0.7		
		V _{CC} = 3 V to 3.6 V		0.8		
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}		
V _I	Input voltage			0	5.5	V
V _O	Output voltage			0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			-4	mA
		V _{CC} = 2.3 V			-8	
		V _{CC} = 3 V			-16	
		V _{CC} = 4.5 V			-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4	mA
		V _{CC} = 2.3 V			8	
		V _{CC} = 3 V			16	
		V _{CC} = 4.5 V			24	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V			20	ns/V
		V _{CC} = 3.3 V ± 0.3 V			10	
		V _{CC} = 5 V ± 0.5 V			10	
T _A	Operating free-air temperature	DSBGA package		-40	85	°C
		All other packages		-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G34						UNIT	
	DBV	DCK	DRL	DRY	YZP	DPW		
	5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	229	278	243	439	130	340	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	164	93	78	277	54	215	
R _{θJB}	Junction-to-board thermal resistance	62	65	78	271	51	294	
Ψ _{JT}	Junction-to-top characterization parameter	44	2	10	84	1	41	
Ψ _{JB}	Junction-to-board characterization parameter	62	64	77	271	50	294	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	-	-	-	-	-	250	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40°C to 85°C			–40°C to 125°C			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = –100 µA	1.65 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
	I _{OH} = –4 mA	1.65 V		1.2			1.2		
	I _{OH} = –8 mA	2.3 V		1.9			1.9		
	I _{OH} = –16 mA	3 V		2.4			2.4		
	I _{OH} = –24 mA			2.3			2.3		
	I _{OH} = –32 mA	4.5 V		3.8			3.8		
V _{OL}	I _{OL} = 100 µA	1.65 V to 5.5 V			0.1			0.1	V
	I _{OL} = 4 mA	1.65 V			0.45			0.45	
	I _{OL} = 8 mA	2.3 V			0.3			0.3	
	I _{OL} = 16 mA	3 V			0.4			0.4	
	I _{OL} = 24 mA				0.55			0.55	
	I _{OL} = 32 mA	4.5 V			0.55			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1			±2	µA
I _{off}	V _I or V _O = 5.5 V	0			±10			±10	µA
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			1			10	µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V			500			500	µA
C _i	V _I = V _{CC} or GND	3.3 V			3.5				pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

7.6 Switching Characteristics, $C_L = 15 \text{ pF}$

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C to 85°C								UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{pd}	A	Y	2	9.9	1.5	6	1	3.5	1	2.9	ns	

7.7 Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C to 85°C								UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{pd}	A	Y	3.2	8.6	1.5	4.4	1.5	4.1	1	3.2	ns	

7.8 Switching Characteristics, -40°C to 125°C

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 4](#))

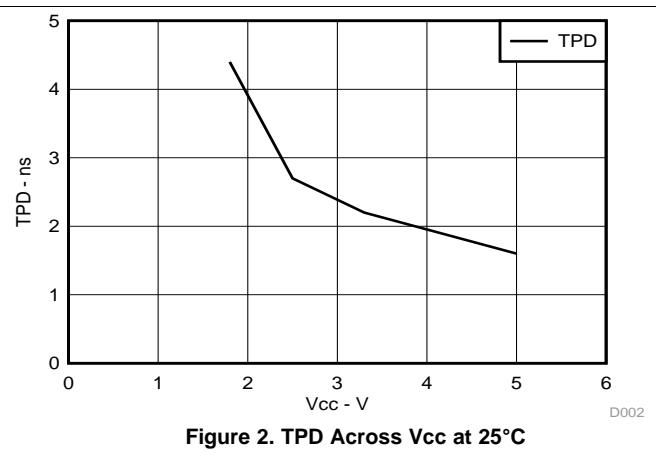
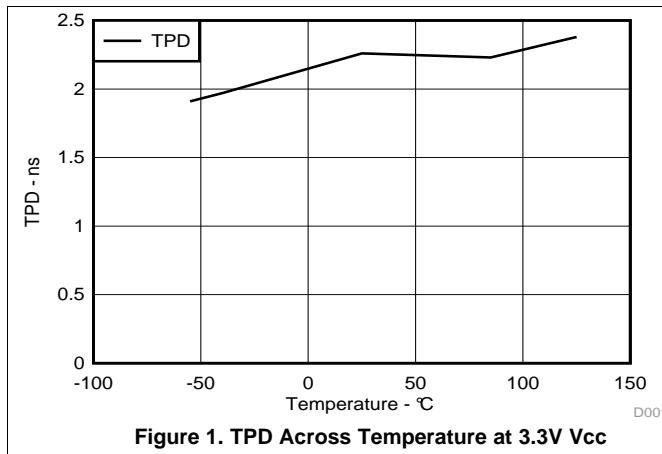
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C to 125°C								UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{pd}	A	Y	3.2	9.5	1.5	5.1	1.5	4.7	1	3.9	ns	

7.9 Operating Characteristics

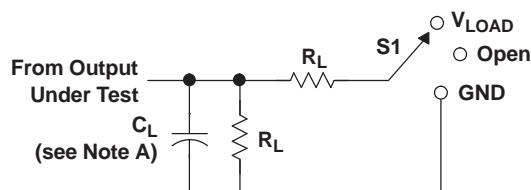
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 \text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	16	16	16	18	pF

7.10 Typical Characteristics



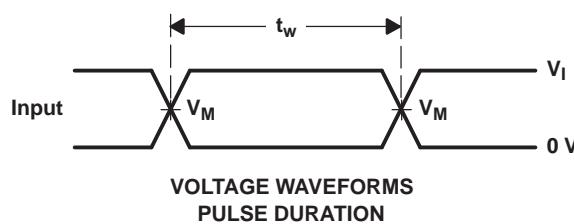
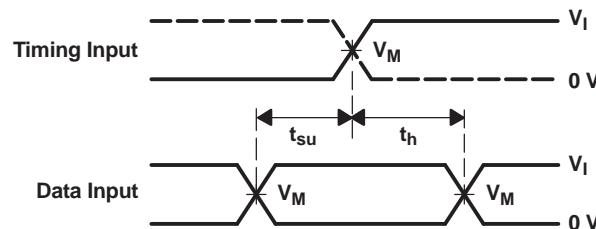
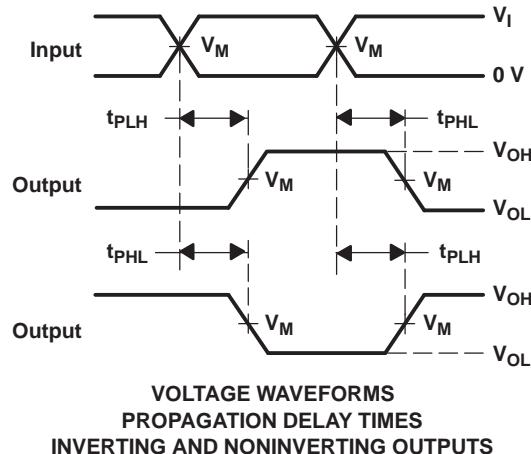
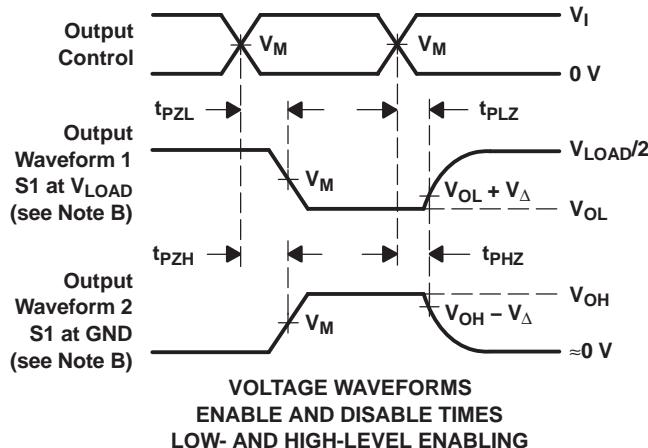
8 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

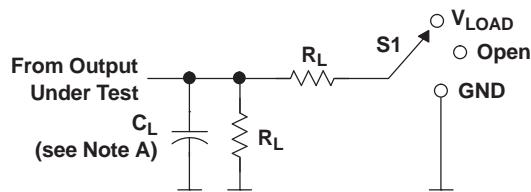
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	15 pF	1 MΩ	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	V_{CC}	$\leq 2.5 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.3 V


**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PZH} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

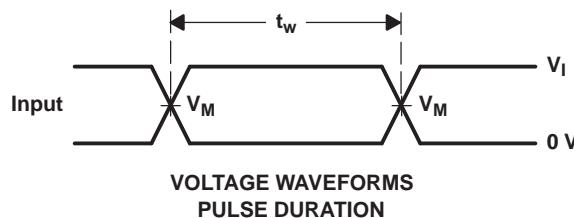
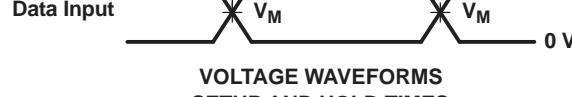
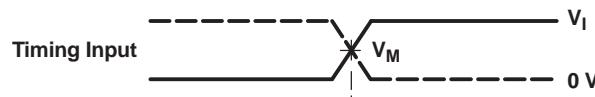
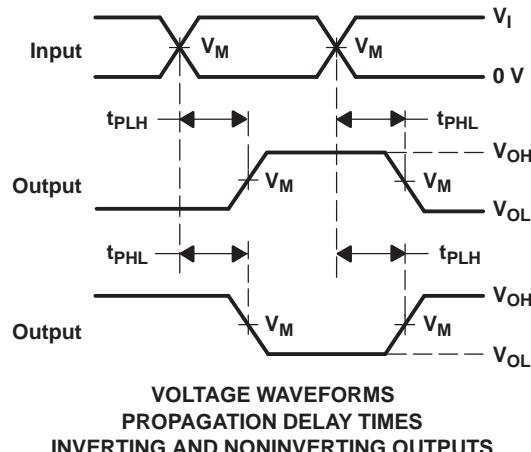
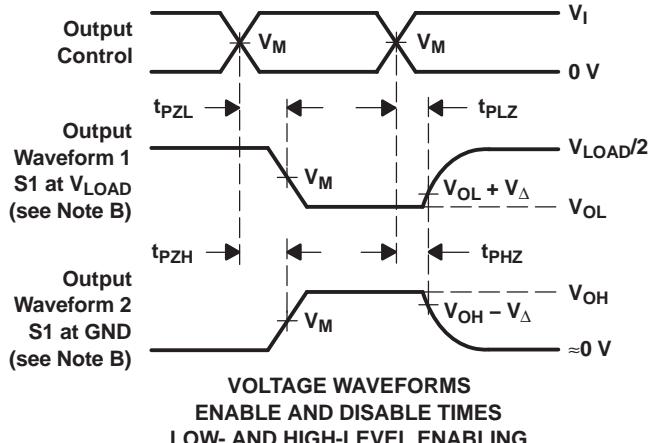
Parameter Measurement Information (continued)



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	V_{CC}	$\leq 2.5 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
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LOW- AND HIGH-LEVEL ENABLING

NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74LVC1G34 device contains one buffer gate device and performs the Boolean function $Y = A$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V.

9.4 Device Functional Modes

Function Table

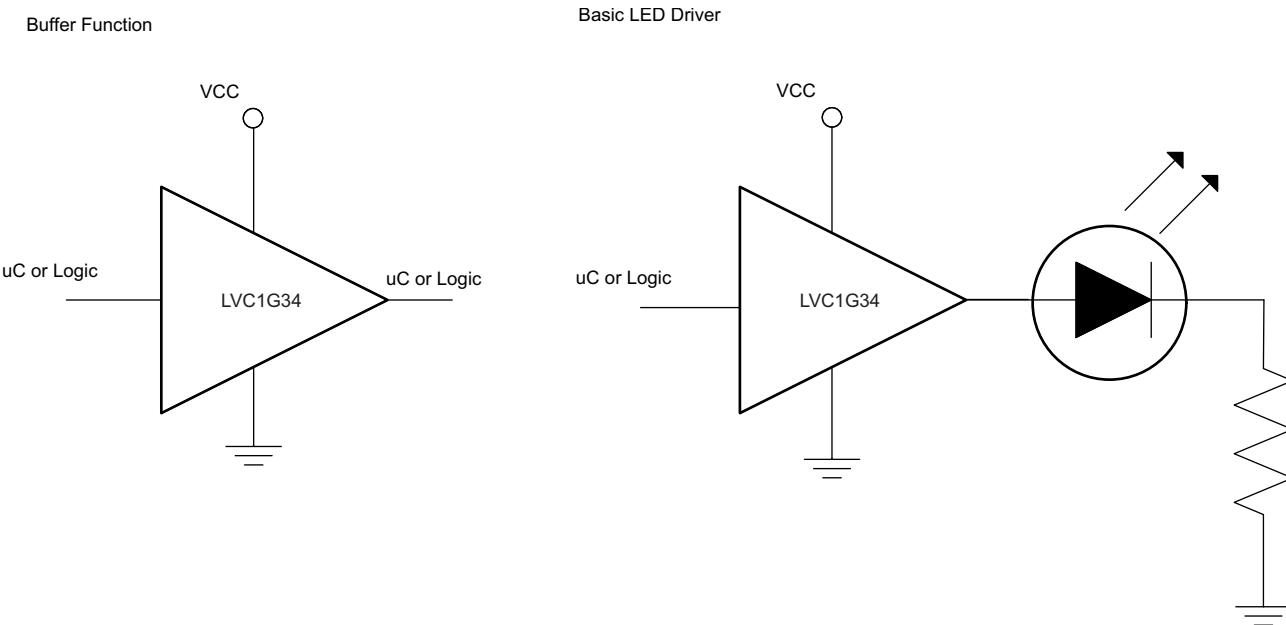
INPUT A	OUTPUT Y
H	H
L	L

10 Application and Implementation

10.1 Application Information

The SN74LVC1G34 is a high drive CMOS device that can be used as a buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC} .

10.2 Typical Application



10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions

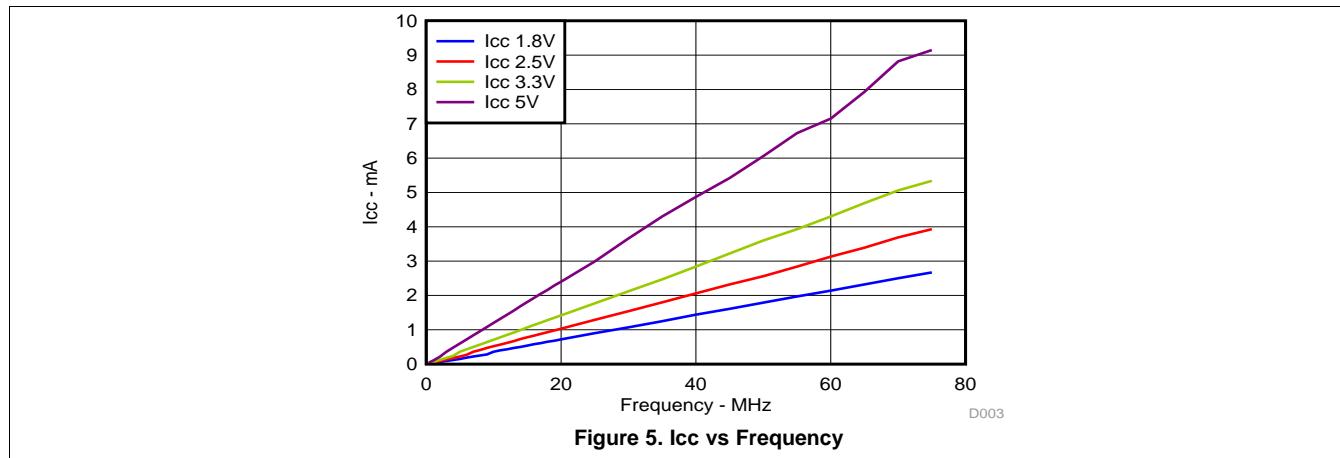
- Rise time and fall time specs. See ($\Delta t/\Delta V$) in the [Recommended Operating Conditions](#) table.
- Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the [Recommended Operating Conditions](#) table at any valid V_{CC} .

2. Recommend Output Conditions

- Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Max Ratings](#) table.
- Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

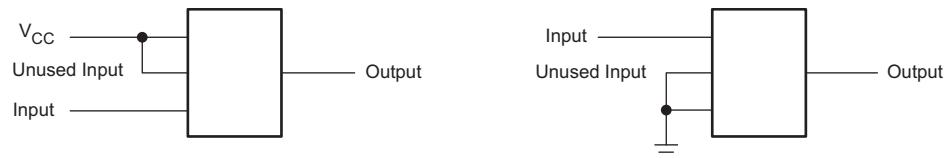
Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1- μ F capacitor is recommended and if there are multiple Vcc pins then a 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or Vcc whichever make more sense or is more convenient.

12.2 Layout Example



13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

 These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G34DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C345 ~ C34F ~ C34K ~ C34R) (C34H ~ C34P ~ C34S)	Samples
SN74LVC1G34DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C345 ~ C34F ~ C34K ~ C34R) (C34H ~ C34P ~ C34S)	Samples
SN74LVC1G34DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C345 ~ C34F ~ C34K ~ C34R) (C34H ~ C34P ~ C34S)	Samples
SN74LVC1G34DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C345 ~ C34K ~ C34R) (C34H ~ C34S)	Samples
SN74LVC1G34DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C345 ~ C34K ~ C34R) (C34H ~ C34S)	Samples
SN74LVC1G34DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C345 ~ C34K ~ C34R) (C34H ~ C34S)	Samples
SN74LVC1G34DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C95 ~ C9F ~ C9K ~ C9R) (C9H ~ C9P ~ C9S)	Samples
SN74LVC1G34DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C95 ~ C9F ~ C9K ~ C9R) (C9H ~ C9P ~ C9S)	Samples
SN74LVC1G34DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C95 ~ C9F ~ C9K ~ C9R) (C9H ~ C9P ~ C9S)	Samples
SN74LVC1G34DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C95 ~ C9K ~ C9R) (C9H ~ C9S)	Samples
SN74LVC1G34DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C95 ~ C9K ~ C9R) (C9H ~ C9S)	Samples
SN74LVC1G34DPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	P4	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G34DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C97 ~ C9R)	Samples
SN74LVC1G34DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C97 ~ C9R)	Samples
SN74LVC1G34DRY2	PREVIEW	SON	DRY	6		TBD	Call TI	Call TI	-40 to 125	C9	
SN74LVC1G34DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C9	Samples
SN74LVC1G34DSF2	PREVIEW	SON	DSF	6		TBD	Call TI	Call TI	-40 to 125	C9	
SN74LVC1G34DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C9	Samples
SN74LVC1G34YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9N	Samples
SN74LVC1G34YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9N	Samples
SN74LVC1G34YZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C9N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

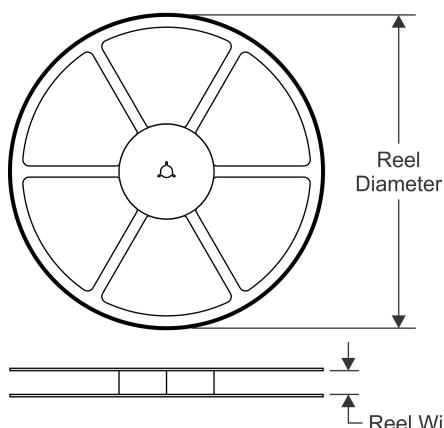
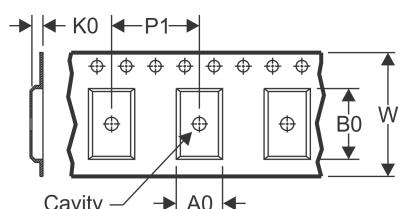
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

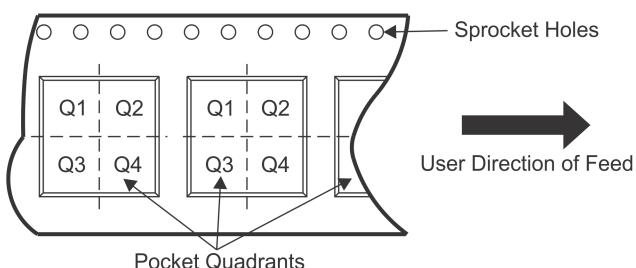
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

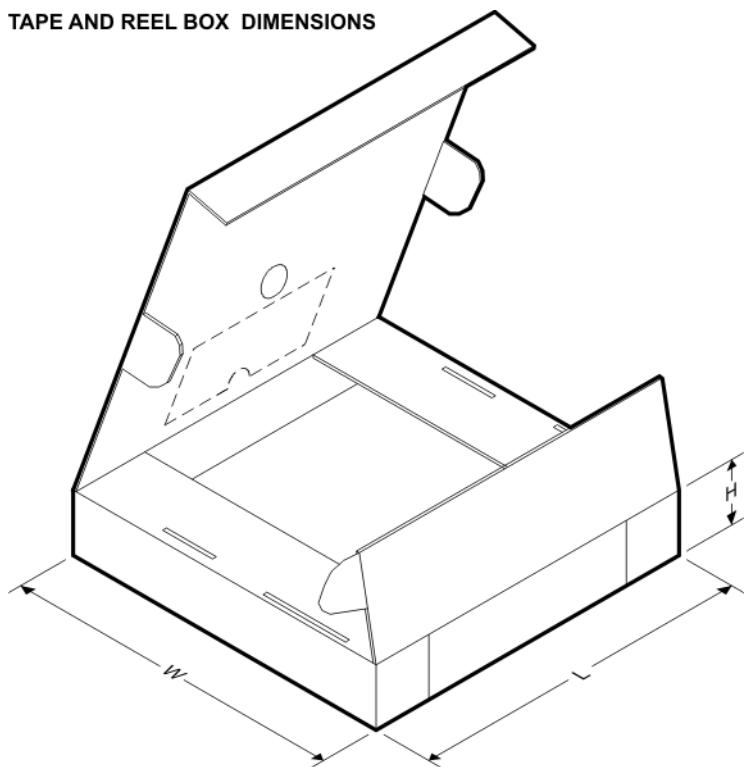
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G34DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G34DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G34DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G34DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G34DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G34DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G34DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G34DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G34DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G34DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G34DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G34YFPR	DSBGA	YFP	4	3000	178.0	9.2	0.89	0.89	0.58	4.0	8.0	Q1
SN74LVC1G34YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G34YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

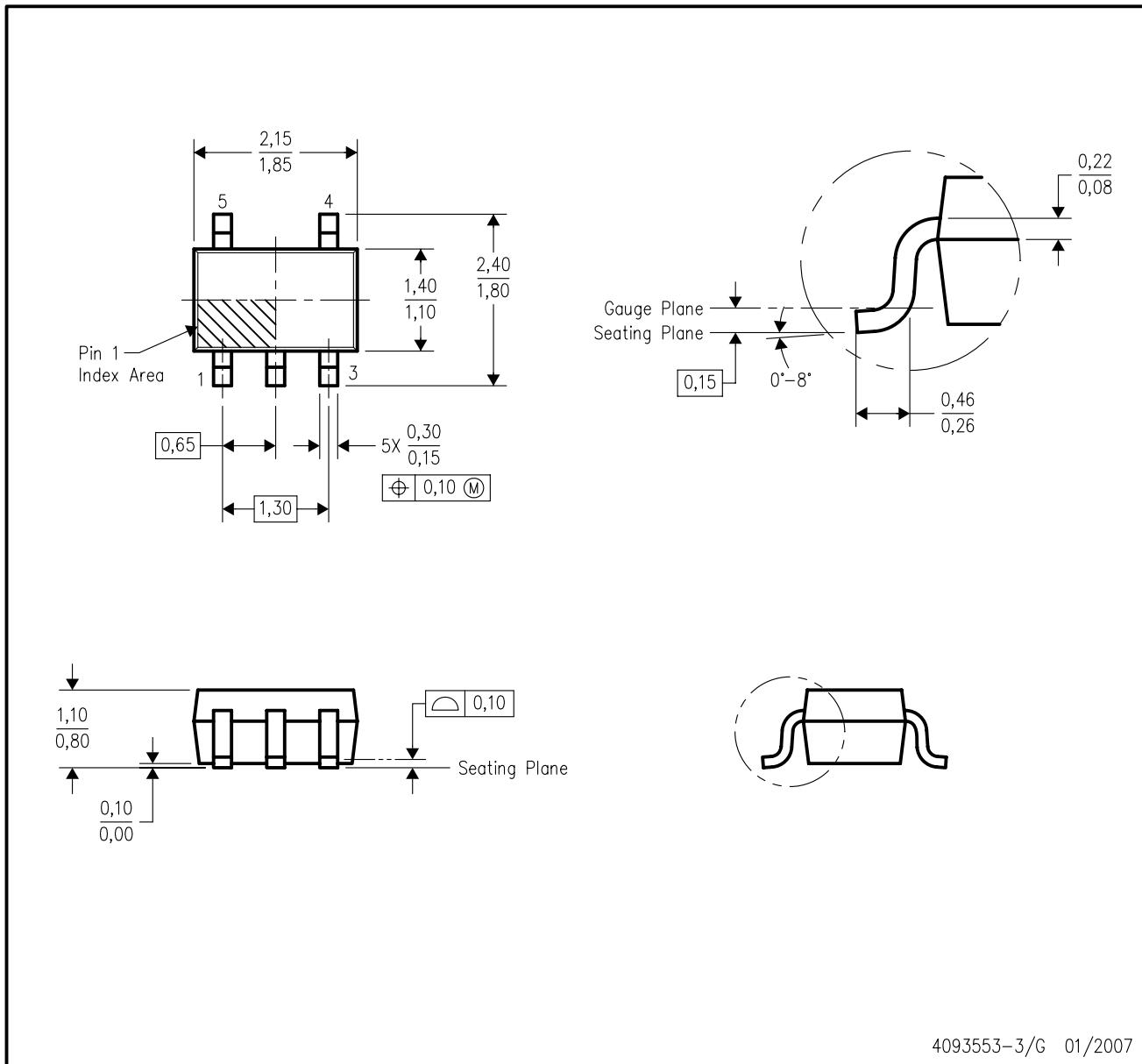
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G34DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G34DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G34DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G34DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G34DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G34DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G34DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G34DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G34DRLR	SOT	DRL	5	4000	184.0	184.0	19.0
SN74LVC1G34DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G34DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G34YFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0
SN74LVC1G34YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G34YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

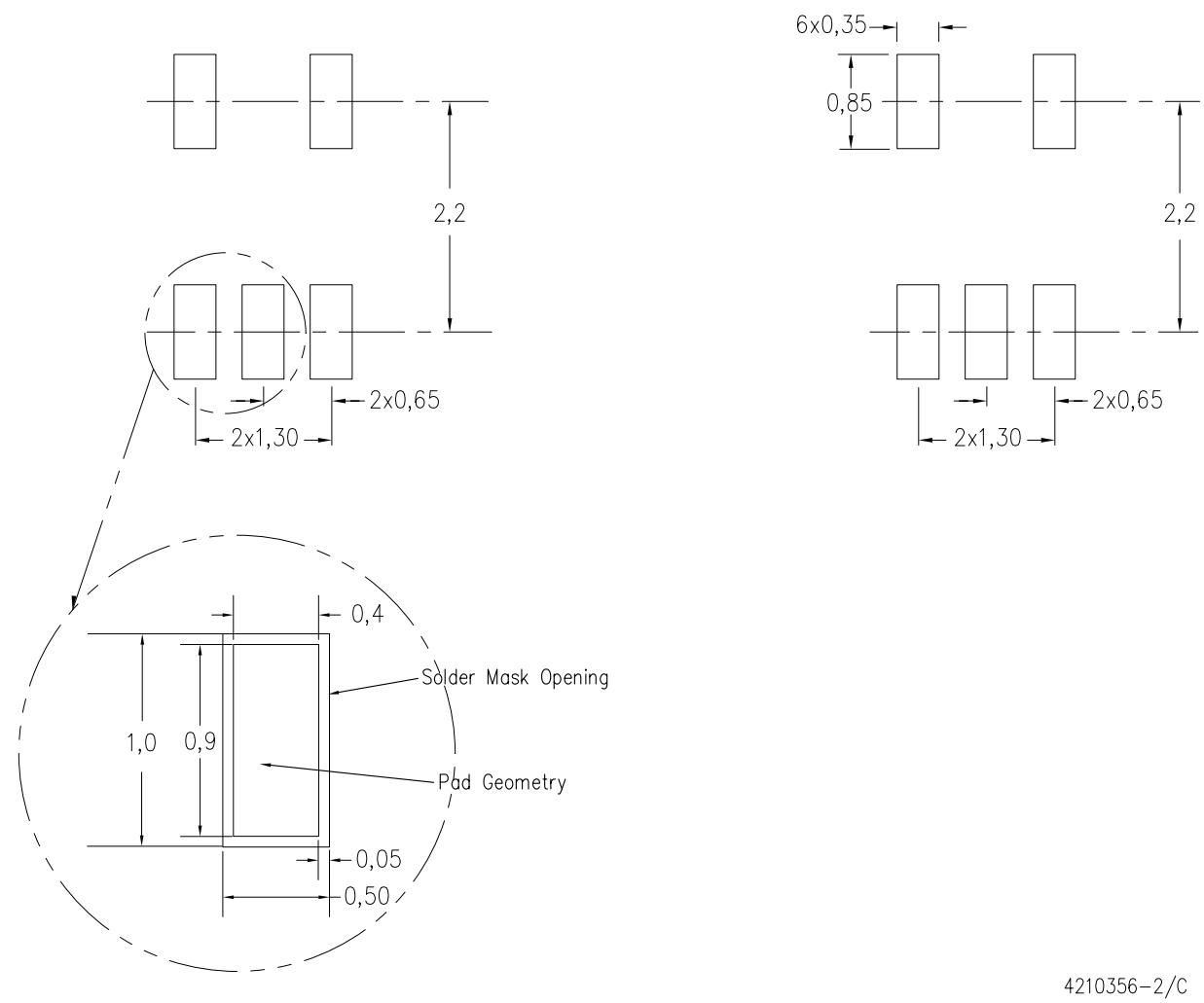
LAND PATTERN DATA

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



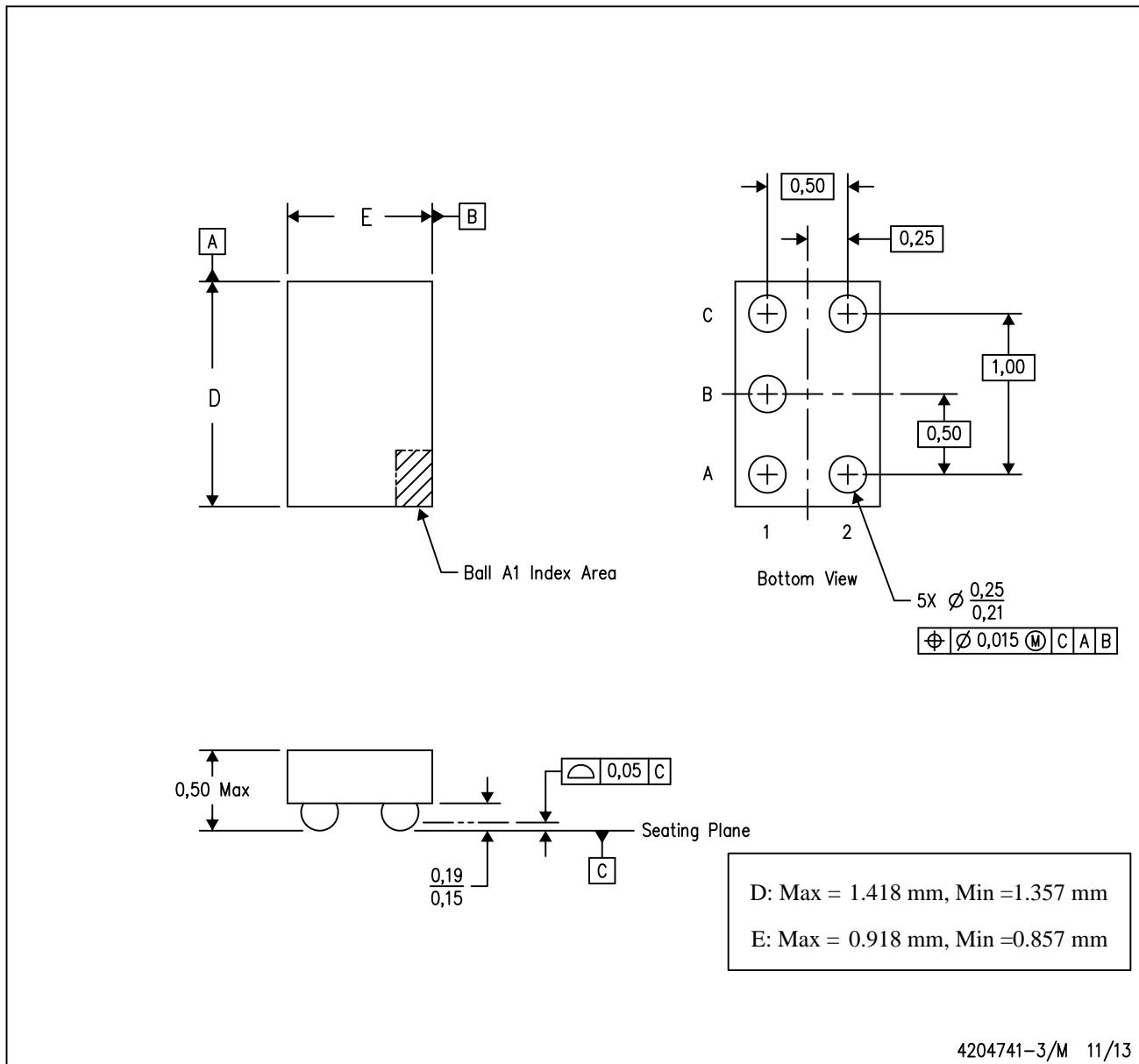
4210356-2/C 07/11

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



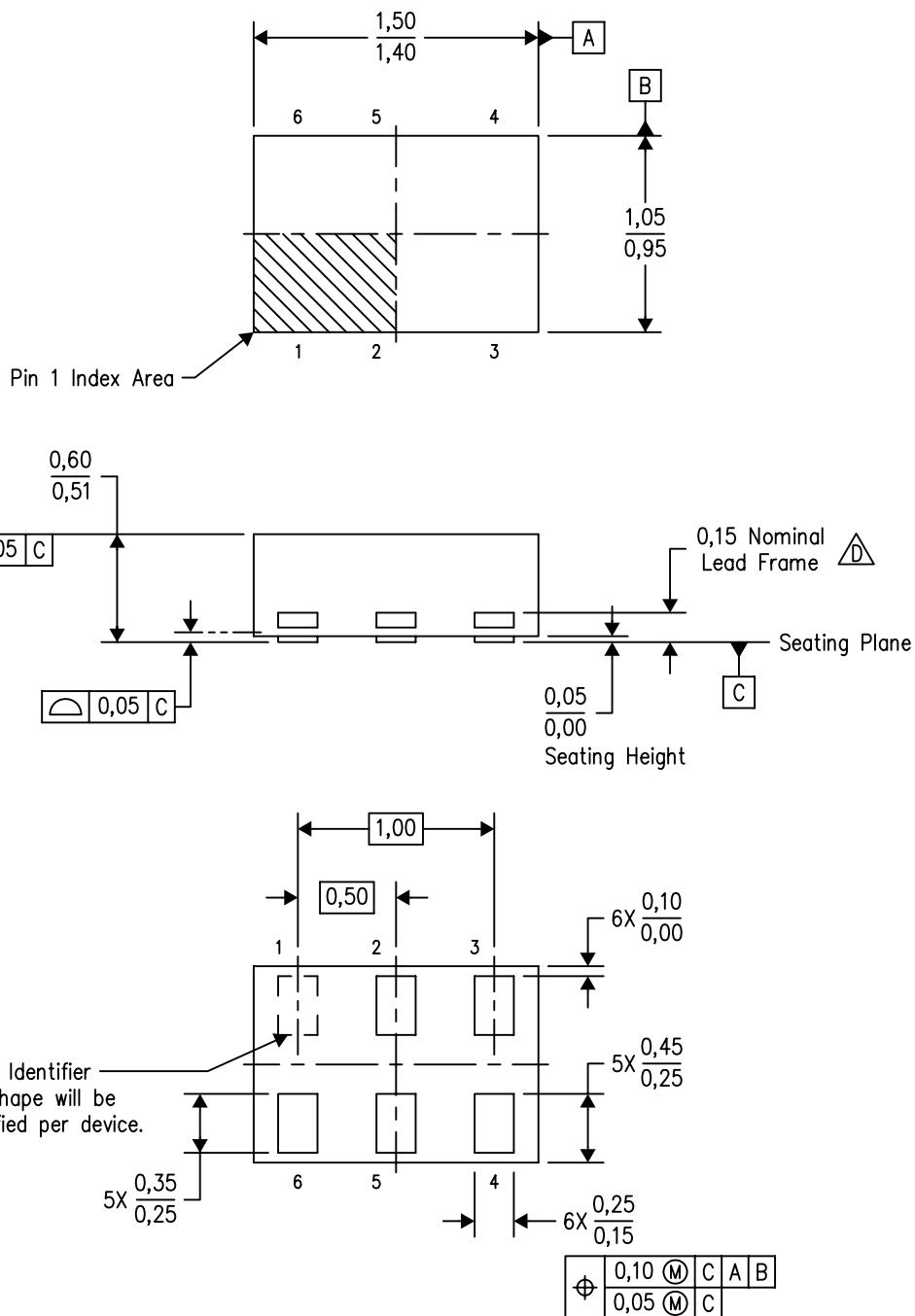
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. NanoFree™ package configuration.

4204741-3/M 11/13

NanoFree is a trademark of Texas Instruments.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. SON (Small Outline No-Lead) package configuration.

D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.

E. This package complies to JEDEC MO-287 variation UFAD.

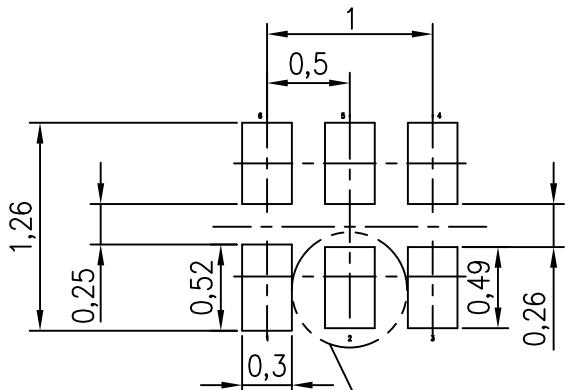
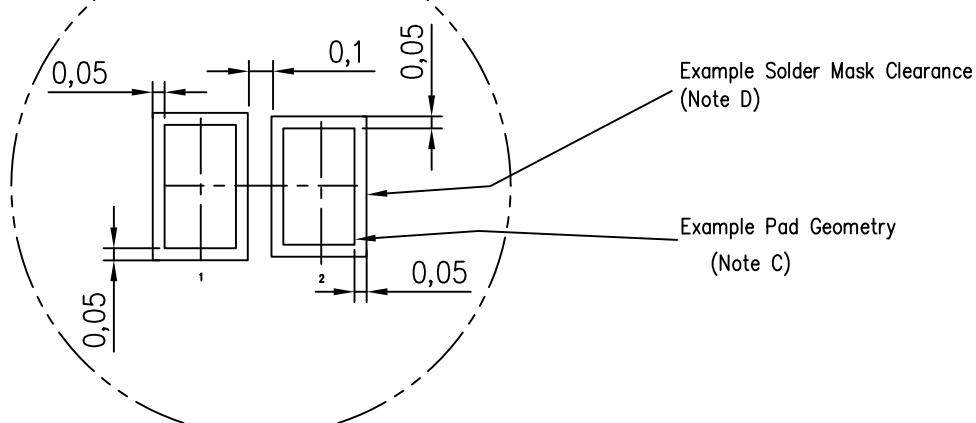
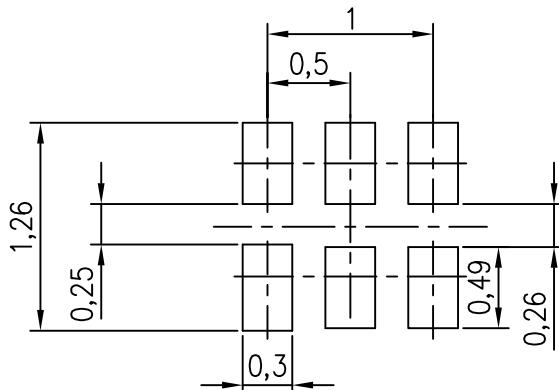
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

4207181/F 12/11

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Example Board Layout

Example Stencil Design
(Note E, F, G)

4208310/E 02/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DPW 5

GENERIC PACKAGE VIEW

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



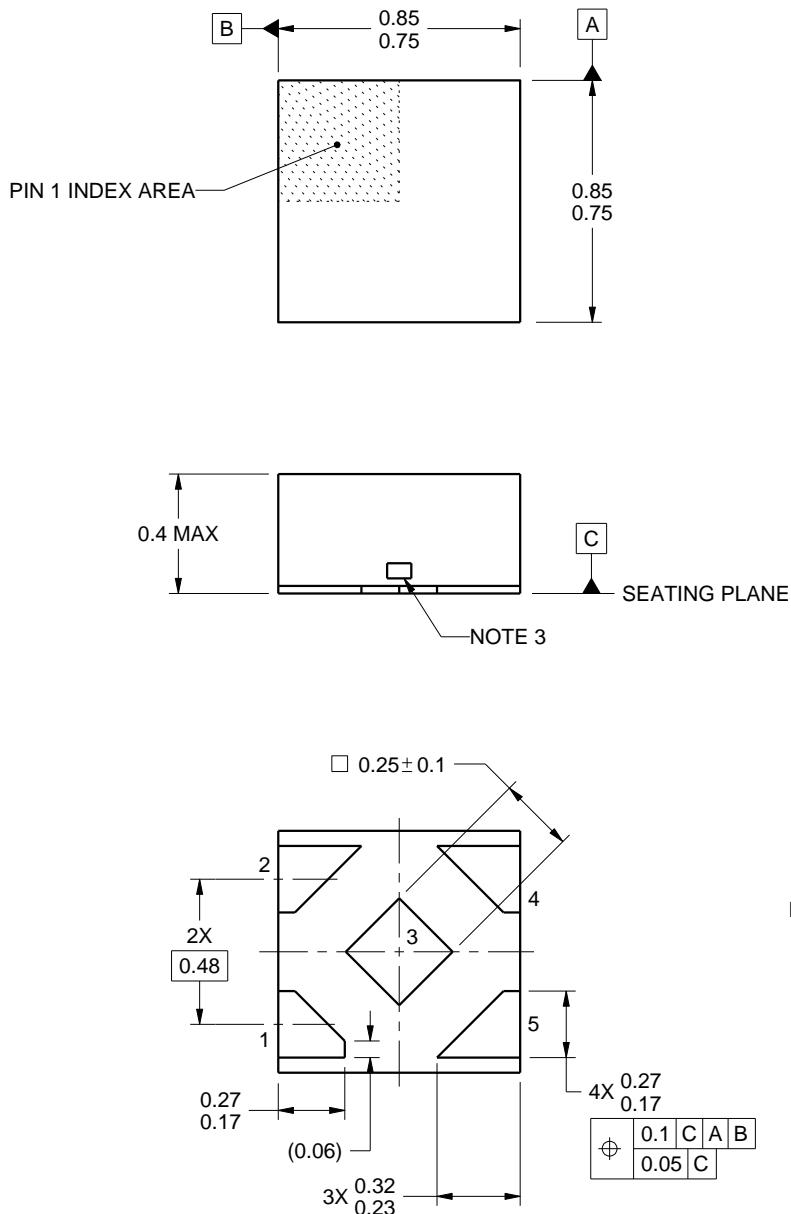
PACKAGE OUTLINE

DPW0005A



X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4223102/A 07/2016

NOTES:

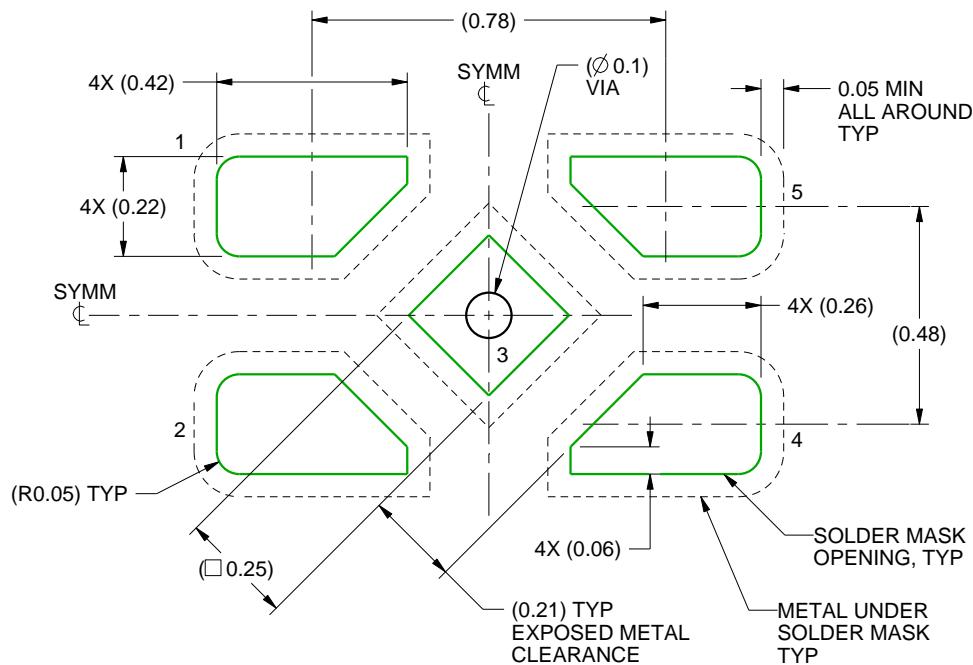
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/A 07/2016

NOTES: (continued)

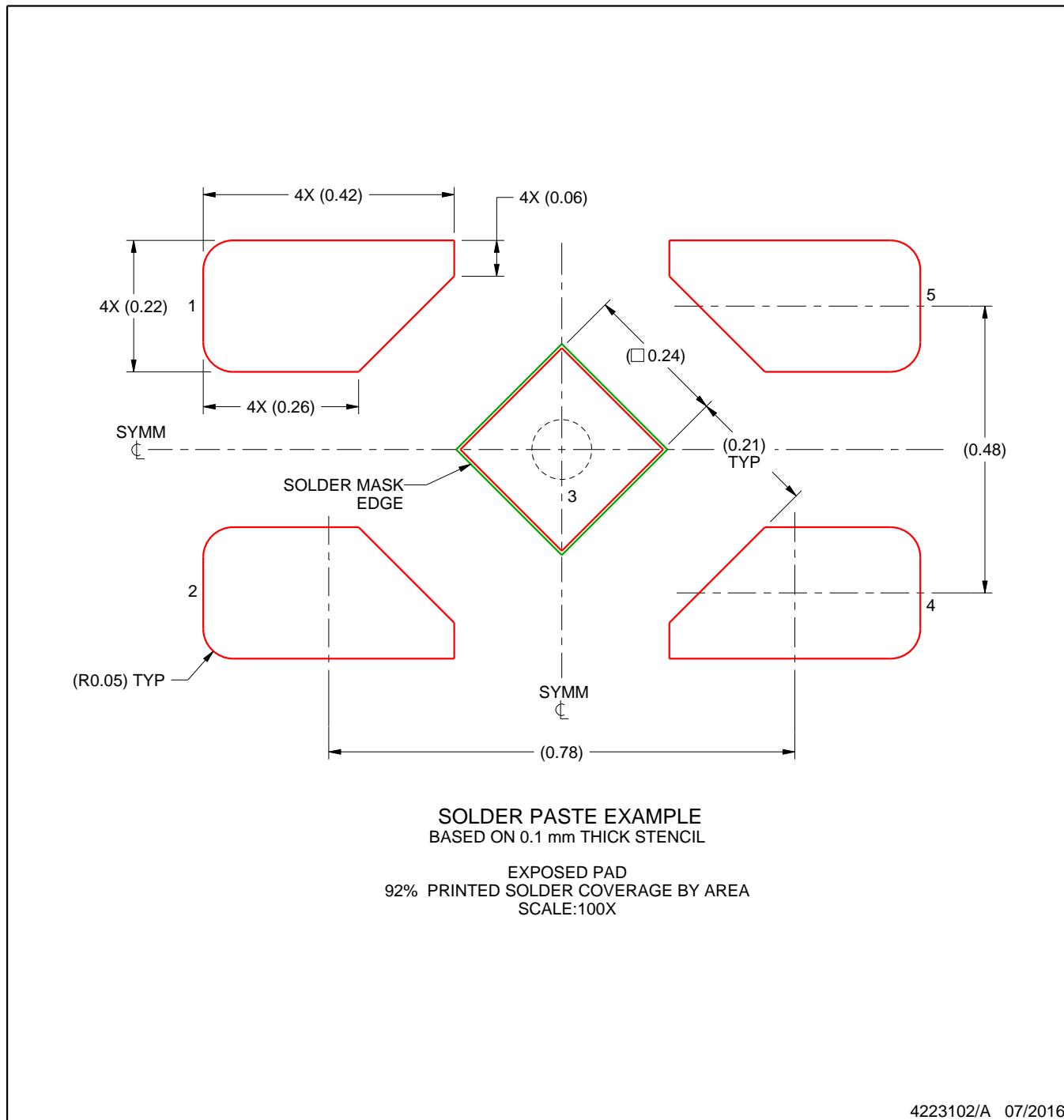
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



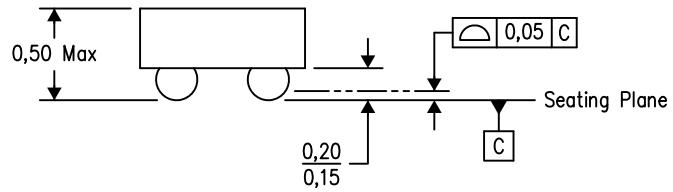
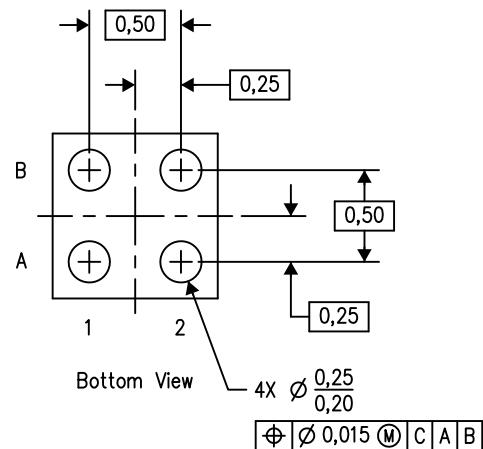
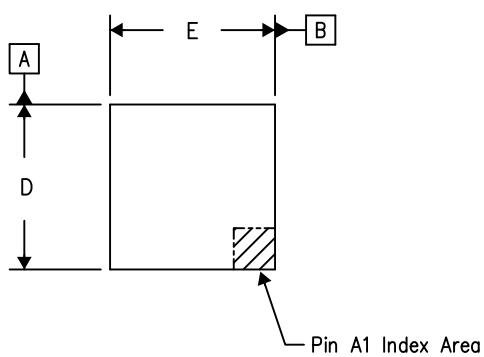
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



D: Max = 0.918 mm, Min = 0.858 mm
E: Max = 0.918 mm, Min = 0.858 mm

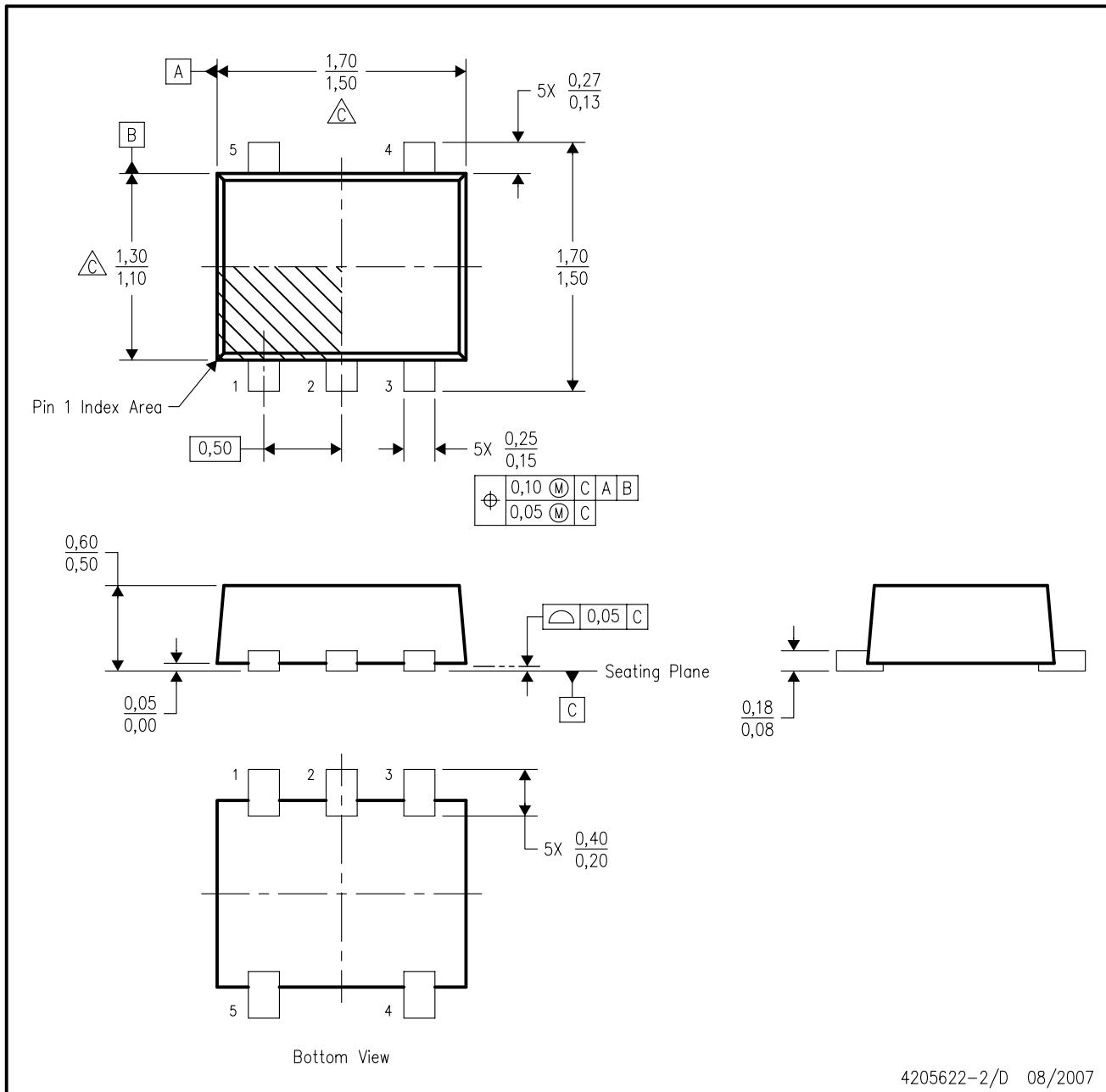
4206083/C 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.

D. JEDEC package registration is pending.

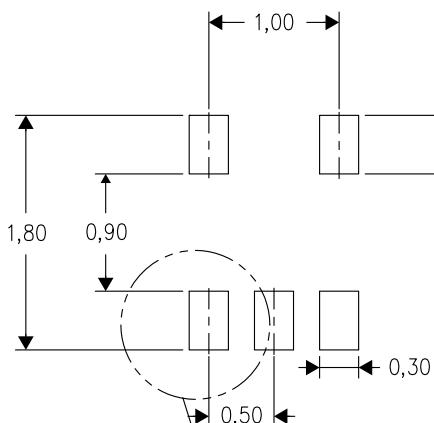
4205622-2/D 08/2007



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

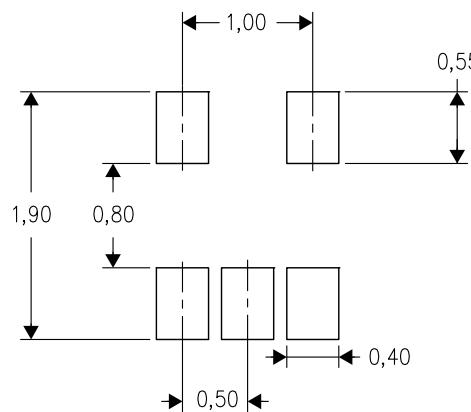
Example Board Layout



Example Non-Soldermask Defined Pad

Example Pad Geometry

Example Non-Soldermask Opening

Example Stencil Design
(Note E)

4208207-2/E 06/12

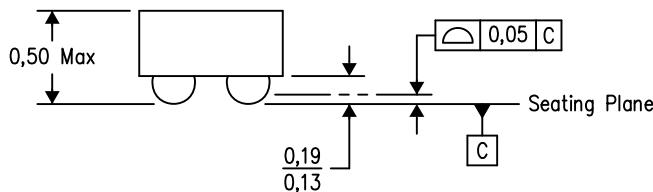
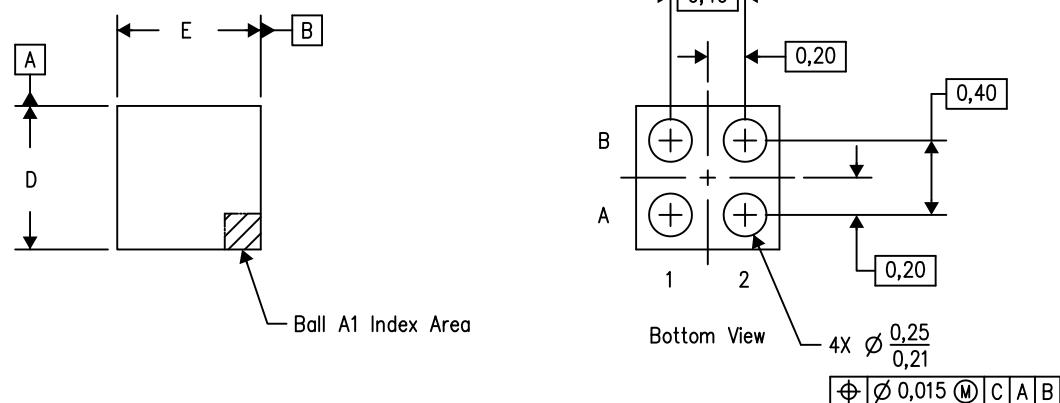
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

MECHANICAL DATA

YFP (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



D: Max = 0.79 mm, Min = 0.73 mm
E: Max = 0.79 mm, Min = 0.73 mm

4206986-2/T 05/13

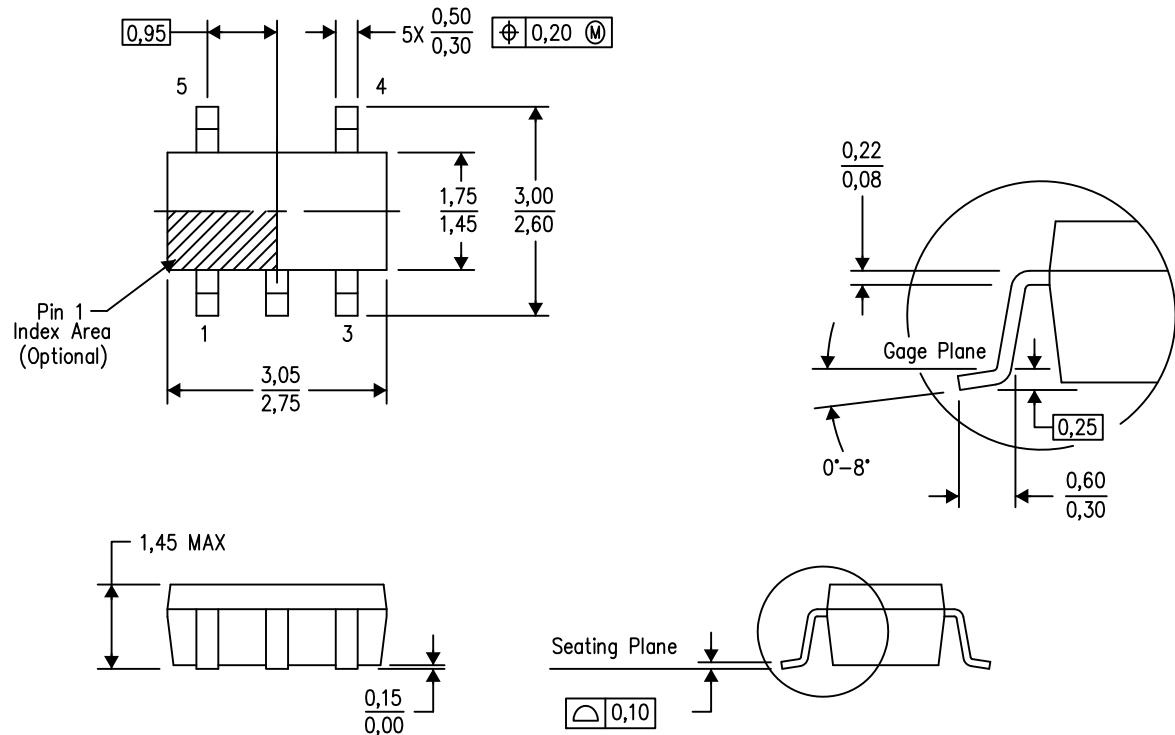
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/N 12/14

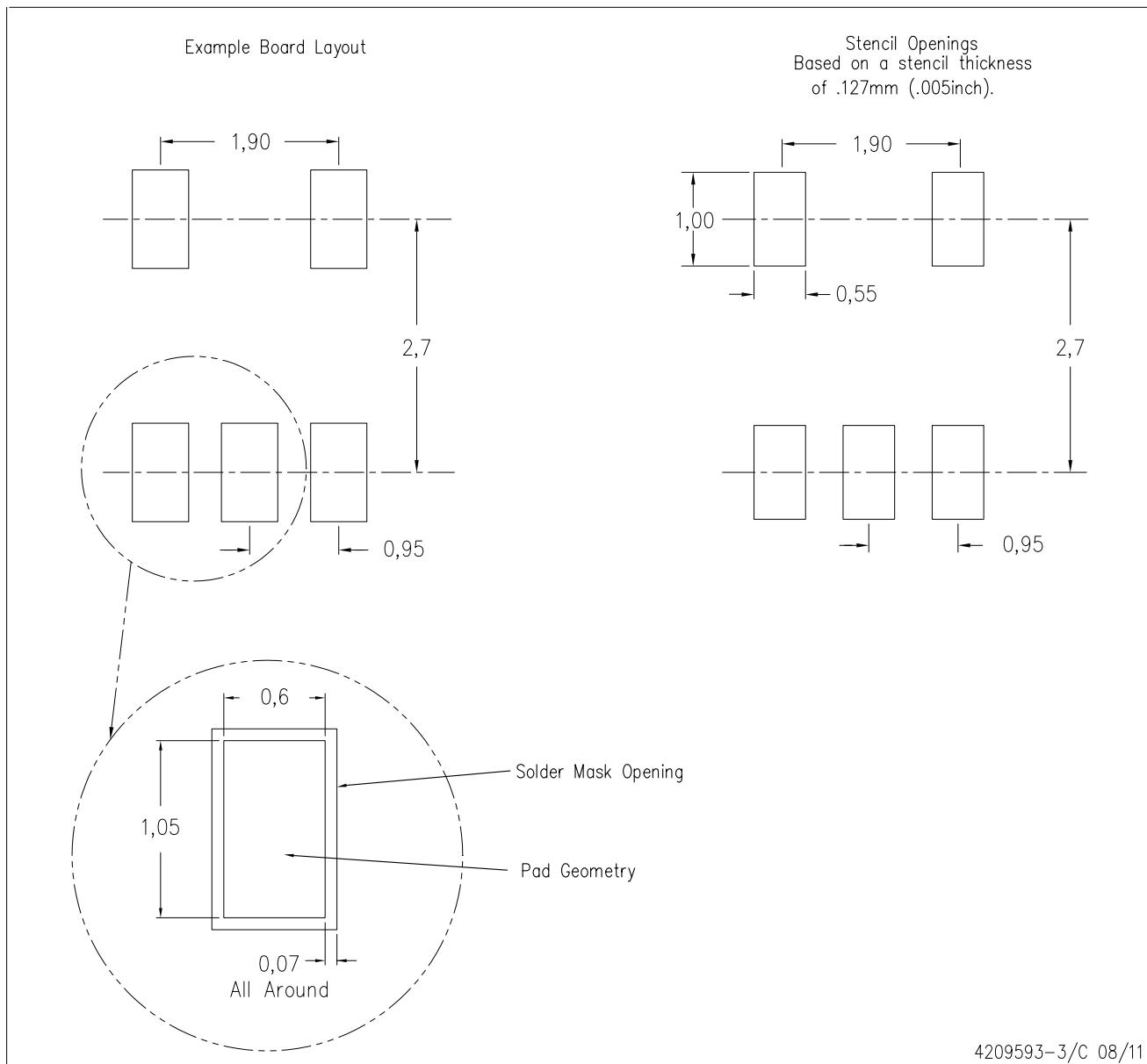
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

LAND PATTERN DATA

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



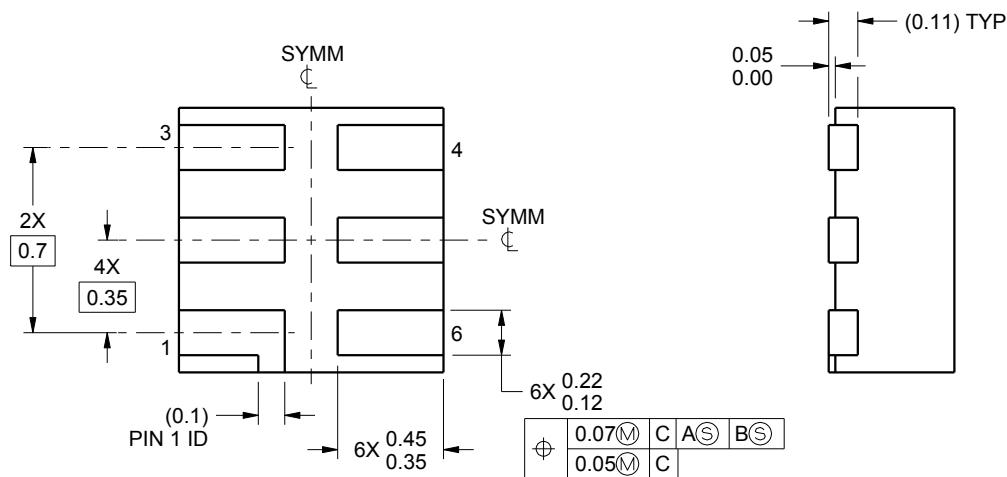
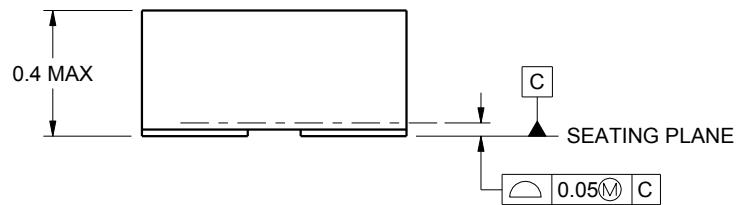
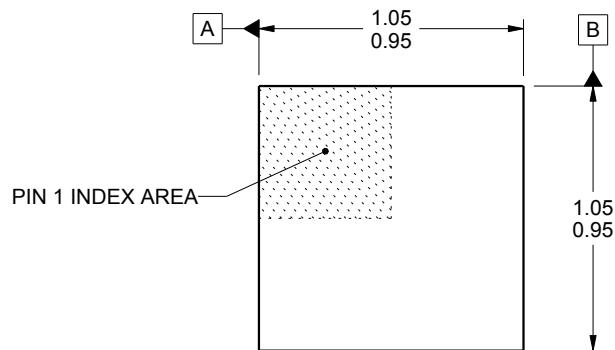
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

MECHANICAL DATA

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4208186/F 10/2014

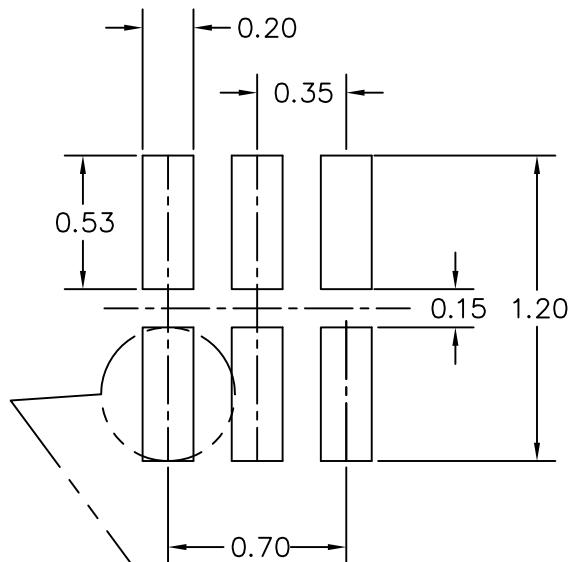
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

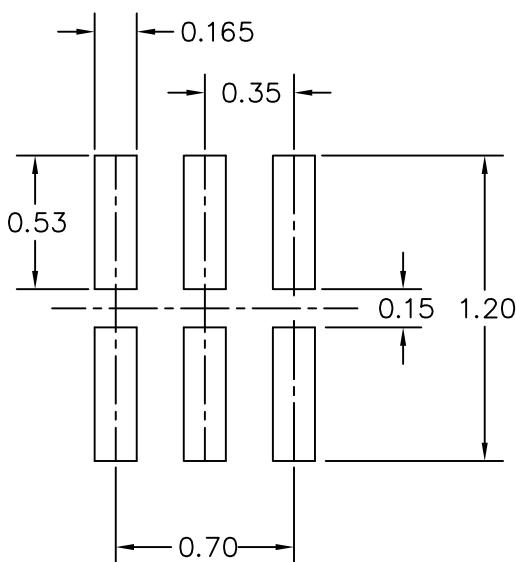
DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern



Stencil Pattern



4210277/D 05/12

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Publication IPC-7351 is recommended for alternate designs.
 D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 H. Component placement force should be minimized to prevent excessive paste block deformation.

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