Automotive PSoC® 4: PSoC 4000 Family Datasheet

Programmable System-on-Chip (PSoC®)

General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an ARM® Cortex™-M0 CPU, while being AEC-Q100 compliant. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC 4000 product family is the smallest member of the PSoC 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CapSense) with best-in-class performance, and general-purpose analog. PSoC 4000 products will be fully upward compatible with members of the PSoC 4 platform for new applications and design needs.

Features

32-bit MCU Subsystem

- 16-MHz ARM Cortex-M0 CPU
- Up to 16 KB of flash with Read Accelerator
- Up to 2 KB of SRAM

Programmable Analog

- Two current DACs (IDACs) for general-purpose or capacitive sensing applications
- One low-power comparator with internal reference

Low Power 1.71-V to 5.5-V operation

- Deep Sleep mode with wake-up on interrupt and I^2C address detect

Capacitive Sensing

- Cypress Capacitive Sigma-Delta (CSD) provides best-in-class signal-to-noise ratio (SNR) and water tolerance
- Cypress-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense™)

Serial Communication

- Multi-master I^2C block with the ability to do address matching during Deep Sleep and generate a wake-up on match

Timing and Pulse-Width Modulation

- One 16-bit Timer/Counter/Pulse-Width Modulator (TCPWM) block
- Center-aligned, Edge, and Pseudo-Random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

Up to 20 Programmable GPIO Pins

- 24-pin QFN and 16-pin SOIC packages
- GPIO pins on Ports 0, 1, and 2 can be CapSense or have other functions
- Drive modes, strengths, and slew rates are programmable

Temperature Ranges

- A Grade: –40 °C to +85 °C
- S-Grade: –40°C to +105 °C
- Automotive Electronics Council (AEC) Q100 qualified

PSoC Creator Design Environment

- Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API) component for all fixed-function and programmable peripherals

Industry-Standard Tool Compatibility

- After schematic entry, development can be done with ARM-based industry-standard development tools

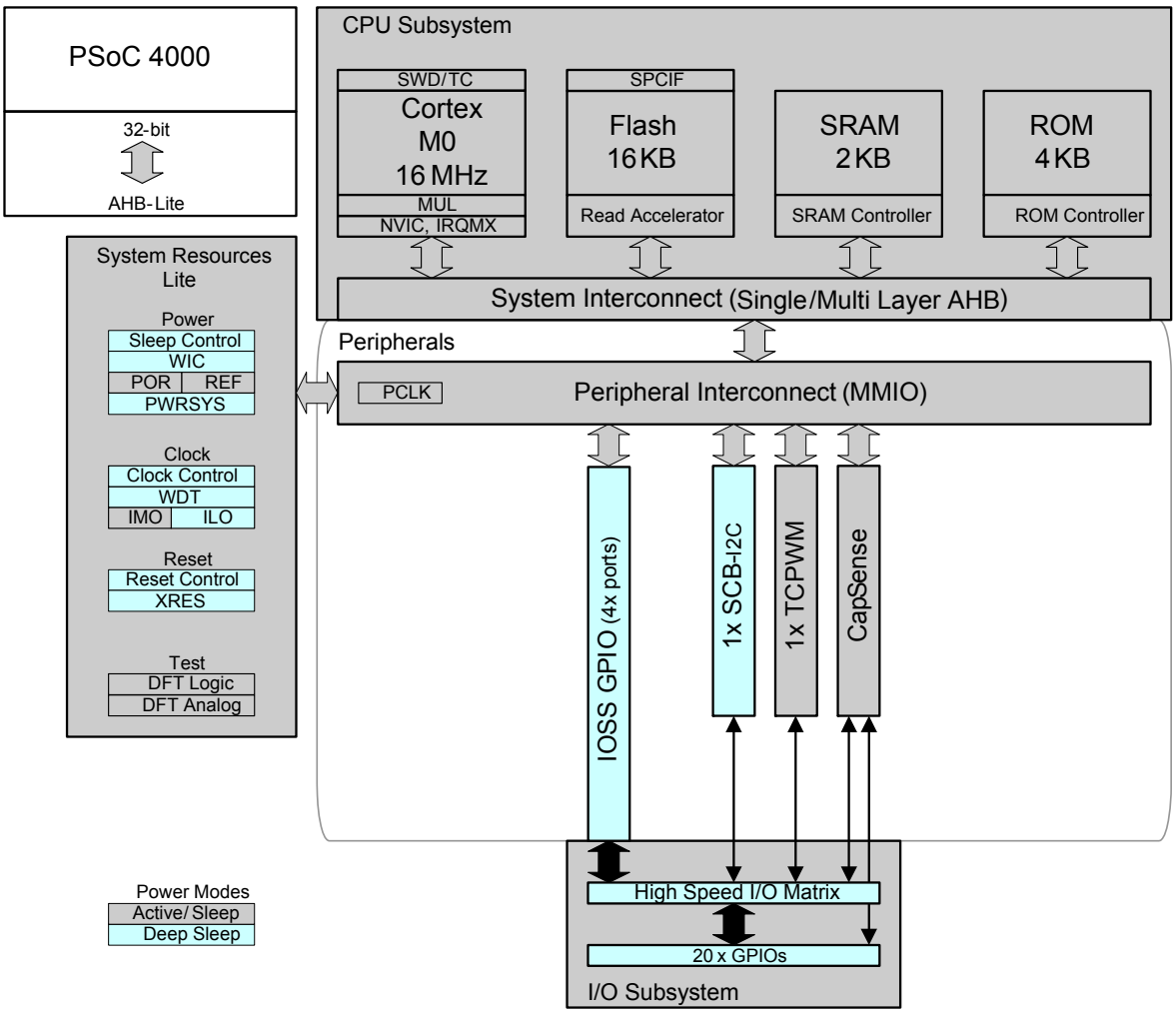
Downloaded from Arrow.com.

Contents

Functional Definition **4**
CPU and Memory Subsystem 4
System Resources 4
Analog Blocks 5
Fixed Function Digital 5
GPIO 5
Special Function Peripherals 5
Pinouts **6**
Power **8**
Unregulated External Supply 8
Regulated External Supply 8
Development Support **9**
Documentation 9
Online 9
Tools 9
Electrical Specifications **10**
Absolute Maximum Ratings 10
Device Level Specifications 11
Analog Peripherals 14
Digital Peripherals 16
Memory 18
System Resources 18
Ordering Information **21**
Part Numbering Conventions 21
Packaging **23**
Package Outline Drawings 24
Acronyms **26**
Document Conventions **28**
Units of Measure 28
Revision History **29**
Sales, Solutions, and Legal Information **31**
Worldwide Sales and Design Support 31
Products 31
PSoC® Solutions 31
Cypress Developer Community 31
Technical Support 31

Downloaded from Arrow.com.

Figure 1. Block Diagram



PSoC 4000 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000 devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000 family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can only be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000, with device security enabled, will have only limited capability for failure analysis. This is a trade-off the PSoC 4000 allows the customer to make.

Downloaded from Arrow.com.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4000 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. This enables fully compatible, binary, upward migration of the code to higher performance processors, such as the Cortex-M3 and M4. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode.

The CPU also includes a debug interface, the SWD interface, which is a 2-wire form of JTAG. The debug configuration used for PSoC 4000 has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4000 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver zero wait-state (WS) access time at 16 MHz. The flash accelerator delivers 85% of the single-cycle SRAM access performance on average.

SRAM

Two KB of SRAM are provided with zero wait-state access at 16 MHz.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section on Power on page 8. It provides an assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000 operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000 provides Active, Sleep, and Deep Sleep low-power modes.

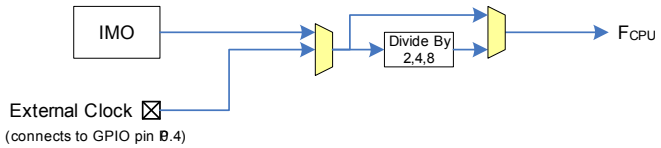
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µS.

Clock System

The PSoC 4000 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000 consists of the internal main oscillator (IMO) and the internal low-frequency oscillator (ILO) and provision for an external clock.

Figure 2. PSoC 4000 MCU Clocking Architecture



The F_{CPU} signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are four clock dividers for the PSoC 4000, each with 16-bit divide capability The 16-bit capability allows flexible generation of fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2% (24 and 32 MHz).

ILO Clock Source

The ILO is a very low power, 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4000 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset on the 24-pin package. An internal POR is provided on the 16-pin package. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4000 reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a ±5% reference.

Downloaded from Arrow.com.

Analog Blocks

Low-power Comparators

The PSoC 4000 has a low-power comparator, which uses the built-in voltage reference. Any one of up to 16 pins can be used as a comparator input and the output of the comparator can be brought out to a pin. The selected comparator input is connected to the minus input of the comparator with the plus input always connected to the 1.2-V voltage reference

Current DACs

The PSoC 4000 has two IDACs, which can drive any of up to 16 pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4000 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on Ports 0, 1, and 2.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention.

Serial Communication Block (SCB)

The PSoC 4000 has a serial communication block, which implements a multi-master I^2C interface.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC 4000 and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode and Fast-mode devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000 is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

GPIO

The PSoC 4000 has up to 20 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (4 for PSoC 4000).

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4000 through a CSD block that can be connected to up to 16 pins through an analog mux bus via an analog switch (pins on Port 3 are not available for CapSense purposes). CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

Downloaded from Arrow.com.

Pinouts

The following is the pin list for PSoC 4000. All Port pins support GPIO. Ports 0, 1, and 2 support CSD CapSense and analog mux bus connections.

Table 1. PSoC 4000 Pin Descriptions

24-QFN		16-SOIC			
Pin	**Name**	**Pin**	**Name**	**TCPWM Signals**	**Alternate Functions**
1	P0.0/TRIN0			TRIN0: Trigger Input 0	
2	P0.1/TRIN1/ CMPO_0	3	P0.1/TRIN1/CMPO_0	TRIN1: Trigger Input 1	CMPO_0: Sense Comp Out
3	P0.2/TRIN2	4	P0.2/TRIN2	TRIN2: Trigger Input 2	
4	P0.3/TRIN3			TRIN3: Trigger Input 3	
5	P0.4/TRIN4/ CMPO_0/EXT_CLK	5	P0.4/TRIN4/CMPO_0 /EXT_CLK	TRIN4: Trigger Input 4	CMPO_0: Sense Comp Out, External Clock, CMOD Cap
6	VCCD	6	VCCD		
7	VDD	7	VDD		
8	VSS	8	VSS		
9	P0.5	9	P0.5		
10	P0.6	10	P0.6		
11	P0.7				
12	P1.0				
13	P1.1/OUT0	11	P1.1/OUT0	OUT0: PWM OUT 0	
14	P1.2/SCL/ SWD_CLK	12	P1.2/SCL/ SWD_CLK		I2C SCL, SWD Clock
15	P1.3/SDA/ SWD_IO	13	P1.3/SDA/ SWD_IO		I2C Data, SWD Data
16	P1.4/UND0			UND0: Underflow Out	
17	P1.5/OVF0			OVF0: Overflow Out	
18	P1.6/OVF0/UND0 /nOUT0/CMPO_0	14	P1.6/OVF0/UND0 /nOUT0/CMPO_0	nOUT0: Complement of OUT0 (not OUT)	CMPO_0: Sense Comp Out, Internal Reset function during POR (must not have load to ground during POR).
19	P1.7/MATCH/EXT_C LK	15	P1.7/MATCH/EXT_C LK	MATCH: Match Out	External Clock
20	P2.0	16	P2.0		
21	P3.0/SDA/ SWD_IO	1	P3.0/SDA/ SWD_IO		I2C Data, SWD IO
22	P3.1/SCL/ SWD_CLK	2	P3.1/SCL/ SWD_CLK		I2C Clock, SWD Clock
23	P3.2			OUT0:PWM OUT 0	
24	XRES				XRES: External Reset

Downloaded from Arrow.com.

Descriptions of the Pin functions are as follows:

VDD: Power supply for both analog and digital sections.

VSS: Ground pin.

VCCD: Regulated digital supply (1.8 V ±5%).

Pins belonging to Ports 0, 1, and 2 can all be used as CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by the firmware.

Pins on Port 3 can be used as GPIO, in addition to their alternate functions listed above.

The following packages are provided: 24-pin QFN and 16-pin SOIC.

Figure 3. 24-pin QFN Pinout

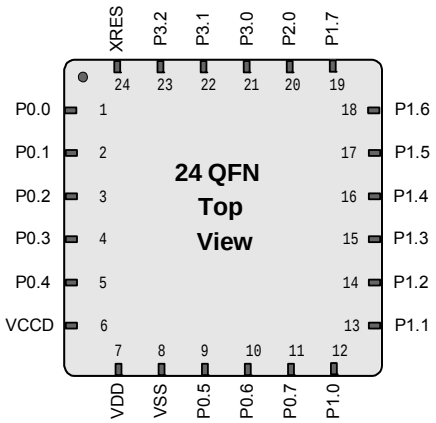
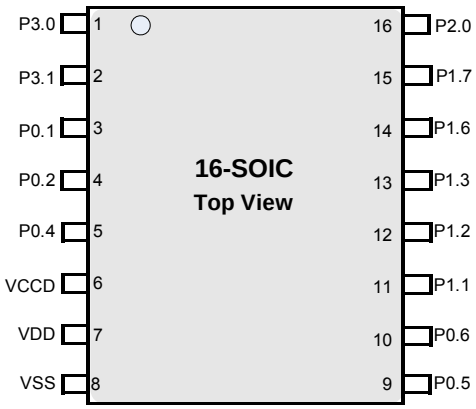


Figure 4. 16-pin SOIC Pinout



Downloaded from Arrow.com.

Power

The following power system diagrams (Figure 5 and Figure 6) show the set of power supply pins as implemented for the PSoC 4000. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input. There is a separate regulator for the Deep Sleep mode. The supply voltage range is either 1.8 V ±5% (externally regulated) or 1.8 V to 5.5 V (unregulated externally; regulated internally) with all functions and circuits operating over that range.

The PSoC 4000 family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply.

Unregulated External Supply

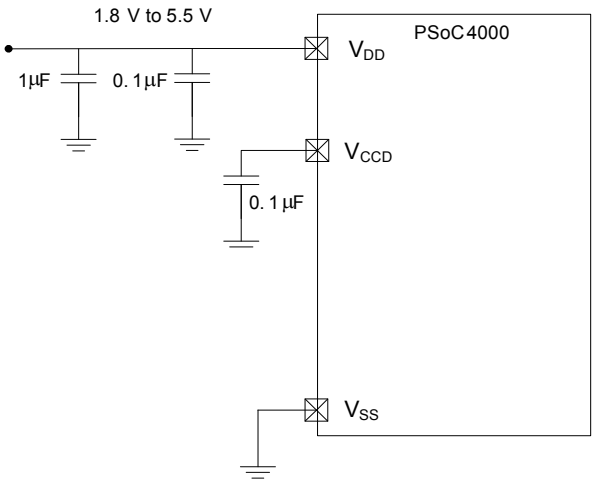
In this mode, the PSoC 4000 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000 supplies the internal logic and the V_{CCD} output of the PSoC 4000 must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better).

Bypass capacitors must be used from V_{DDD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme follows (V_{DDIO} is available on the 16-QFN package).

Figure 5. 24-pin QFN Bypass Scheme Example - Unregulated External Supply

Power supply connections when $1.8 \le V_{DD} \le 5.5$ V



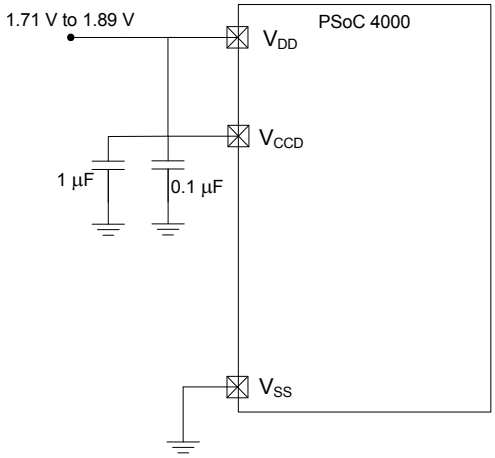
Regulated External Supply

In this mode, the PSoC 4000 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator is disabled in the firmware.

An example of a bypass scheme follows.

Figure 6. 24-pin QFN Bypass Scheme Example - Regulated External Supply

Power supply connections when $1.71 \le V_{DD} \le 1.89$ V



Downloaded from Arrow.com.

Development Support

The PSoC 4000 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4000 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Downloaded from Arrow.com.

Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95	V	
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5	V	
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
SID5	$I_{GPIO_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–140	–	140	mA	

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Downloaded from Arrow.com.

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C for A grade devices and –40 °C ≤ T_A ≤ 105 °C for S grade devices, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max [2]	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
SID255	V_{DD}	Power supply input voltage (V_{CCD} = V_{DD})	1.71	–	1.89	V	Internally unregulated supply
SID54	V_{DDIO}	V_{DDIO} domain supply	1.71	–	V_{DD}	V	
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.8 to 5.5 V							
SID9	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.0	2.85	mA	
SID12	I_{DD8}	Execute from flash; CPU at 12 MHz	–	3.2	3.75	mA	
SID16	I_{DD11}	Execute from flash; CPU at 16 MHz	–	4.0	4.5	mA	
Sleep Mode, V_{DDD} = 1.71 to 5.5 V							
SID25	I_{DD20}	I^2C wakeup, WDT on. 6 MHz	–	1.1	–	mA	
SID25A	I_{DD20A}	I^2C wakeup, WDT on. 12 MHz	–	1.4	–	mA	
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	8.2	µA	
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	12	µA	
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	9.2	µA	
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Note
2. Maximum values corresponds to values at higher temperature (105 °C).

Downloaded from Arrow.com.

Table 4. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	16	MHz	$1.71 \le V_{DD} \le 5.5$
SID49[3]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	
SID50[3]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	µs	

GPIO

Table 5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[4]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID241	V_{IH}[4]	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	
SID243	V_{IH}[4]	LVTTL input, $V_{DDD} \ge 2.7$ V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, $V_{DDD} \ge 2.7$ V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	3	7	pF	
SID67[5]	V_{HYSTTL}	Input hysteresis LVTTL	15	40	–	mV	$V_{DDD} \ge 2.7$ V
SID68[5]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	V_{DD} < 4.5 V
SID68A[5]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–	mV	V_{DD} > 4.5 V
SID69[5]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	
SID69A[5]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	85	mA	

Notes
3. Guaranteed by characterization.
4. V_{IH} must not exceed V_{DDD} + 0.2 V.
5. Guaranteed by characterization.

Downloaded from Arrow.com.

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	16	MHz	90/10% V_{IO}

XRES

Table 7. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	7	pF	
SID81[6]	$V_{HYSXRES}$	Input voltage hysteresis	–	05*V_{DD}	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5V

Table 8. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83[6]	$T_{RESETWIDTH}$	Reset pulse width	5	–	–	µs	
BID#194[6]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	3	ms	

Note
6. Guaranteed by characterization.

Downloaded from Arrow.com.

Analog Peripherals

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID330[6]	I_{CMP1}	Block current, High Bandwidth mode	–	–	110	µA	
SID331[6]	I_{CMP2}	Block current, Low Power mode	–	–	85	µA	
SID332[6]	$V_{OFFSET1}$	Offset voltage, High Bandwidth mode	–	10	30	mV	
SID333[6]	$V_{OFFSET2}$	Offset voltage, Low Power mode	–	10	30	V	
SID334[6]	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	
SID338[6]	VINP_COMP	Comparator input range	0	–	3.6	V	Max input voltage is lower of 3.6 V or V_{DD}

Table 10. Comparator AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID336[6]	T_{COMP1}	Response Time High Bandwidth mode, 50-mV overdrive	–	–	90	ns	
SID337[6]	T_{COMP2}	Response Time Low Power mode, 50-mV overdrive	–	–	110	ns	

Downloaded from Arrow.com.

CSD

Table 11. CSD and IDAC Block Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD and IDAC Specifications							
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	VDD > 2V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	VDD > 1.75V (with ripple), 25 C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD#15	VREF	Voltage reference for CSD and Comparator	1.1	1.2	1.3	V	
SID.CSD#16	IDAC1IDD	IDAC1 (8-bits) block current	–	–	1125	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1125	µA	
SID308	V_{CSD}	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.8	–	V_{DD} –0.8	V	
SID309	$IDAC1_{DNL}$	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	$IDAC1_{INL}$	INL for 8-bit resolution	–3	–	3	LSB	
SID311	$IDAC2_{DNL}$	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	$IDAC2_{INL}$	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	$IDAC1_{CRT1}$	Output current of IDAC1 (8 bits) in high range	–	612	–	µA	
SID314A	$IDAC1_{CRT2}$	Output current of IDAC1(8 bits) in low range	–	306	–	µA	
SID315	$IDAC2_{CRT1}$	Output current of IDAC2 (7 bits) in high range	–	304.8	–	µA	
SID315A	$IDAC2_{CRT2}$	Output current of IDAC2 (7 bits) in low range	–	152.4	–	µA	
SID320	$IDAC_{OFFSET}$	All zeroes input	–	–	±1	LSB	
SID321	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±10	%	
SID322	$IDAC_{MISMATCH}$	Mismatch between IDACs	–	–	7	LSB	
SID323	$IDAC_{SET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$IDAC_{SET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Downloaded from Arrow.com.

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 12. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 8 MHz	–	–	145	µA	All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 16 MHz	–	–	160	µA	All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 16 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[7]
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

Note
7. Guaranteed by characterization.

Downloaded from Arrow.com.

I²C

Table 13. Fixed I²C DC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	25	µA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	2.5	µA	

Table 14. Fixed I²C AC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	400	Kbps	

Note
8. Guaranteed by characterization.

Downloaded from Arrow.com.

Memory

Table 15. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 16. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[9]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$[9]	Row erase time	–	–	13	ms	
SID176	$T_{ROWPROGRAM}$[9]	Row program time after erase	–	–	7	ms	
SID178	$T_{BULKERASE}$[9]	Bulk erase time (16 KB)	–	–	15	ms	
SID180[10]	$T_{DEVPROG}$[9]	Total device program time	–	–	7.5	seconds	
SID181[10]	F_{END}	Flash endurance	100 K	–	–	cycles	
SID182[10]	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20 [11]	–	–	years	
SID182A[10]		Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10 [12]	–	–	years	

System Resources

Power-on Reset (POR)

Table 17. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185[10]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	
SID186[10]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4	V	

Table 18. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190[10]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	
SID192[10]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5	V	

Notes

9. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
10. Guaranteed by characterization.
11. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customercare@cypress.com.
12. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact customercare@cypress.com.

Downloaded from Arrow.com.

SWD Interface

Table 19. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215[13]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	
SID216[13]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	
SID217[13]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	
SID217A[13]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	

Internal Main Oscillator

Table 20. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	

Table 21. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24 and 32 MHz (trimmed)	–	–	±2	%	2 V ≤ V_{DD} ≤ 5.5 V, and –25 °C ≤ T_A ≤ 85 °C for A grade devices and –25 °C ≤ T_A ≤ 105°C for S grade devices
SID223A	$F_{IMOTOLVCCD}$	Frequency variation (trimmed)	–	–	±4	%	All
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	

Internal Low-Speed Oscillator

Table 22. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231[13]	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	
SID233[13]	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	

Table 23. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234[13]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	
SID236[13]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	

Note
13. Guaranteed by characterization.

Downloaded from Arrow.com.

Table 24. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305[14]	ExtClkFreq	External clock input frequency	0	–	16	MHz	
SID306[14]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	

Table 25. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262[14]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	

Note
14. Guaranteed by characterization.

Downloaded from Arrow.com.

Ordering Information

The PSoC 4000 part numbers and features are listed in the following table.

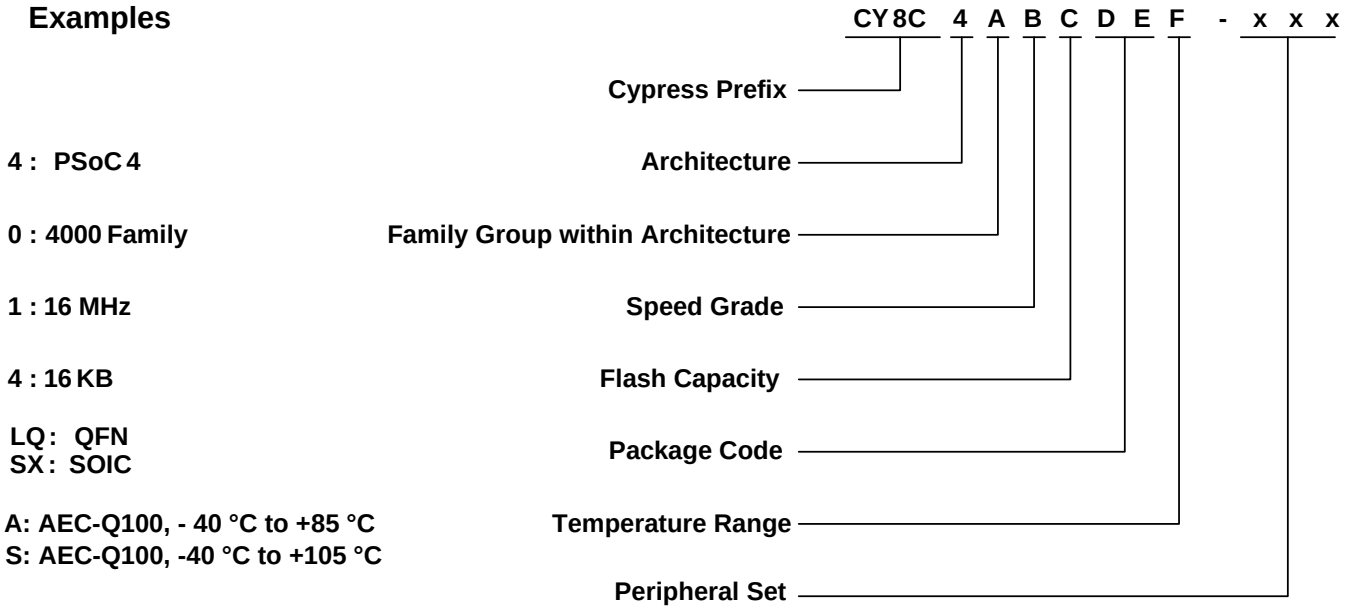
MPN	Features									Package		Operating Temperature	
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	CapSense	7-bit IDAC	8-bit IDAC	Comparators	TCPWM Blocks	SCB (I2C)	16-SOIC	24-QFN	–40 to +85 °C	–40 to +105 °C
CY8C4014SXA-421	16	16	2	✔	1	1	1	1	1	✔	–	✔	–
CY8C4014LQA-422	16	16	2	✔	1	1	1	1	1	–	✔	✔	–
CY8C4014SXS-421	16	16	2	✔	1	1	1	1	1	✔	–	–	✔
CY8C4014LQS-422	16	16	2	✔	1	1	1	1	1	–	✔	–	✔

Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.

Examples



Downloaded from Arrow.com.

The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress prefix		
4	Architecture	4	PSoC 4
A	Family	0	4000 Family
B	CPU speed	1	16 MHz
		4	48 MHz
C	Flash capacity	3	8 KB
		4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	SX	SOIC
		LQ	QFN
F	Temperature range	A/S	Automotive
XYZ	Attributes code	000-999	Code of feature set in specific family

Downloaded from Arrow.com.

Packaging

Table 26. Package List

Spec ID#	Package	Description
BID#26	24-pin QFN	24-pin 4 x 4 x 0.6 mm QFN with 0.5-mm pitch
BID#40	16-pin SOIC	16-pin (150 Mil) SOIC

Table 27. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	For A grade devices	–40	25.00	85	°C
T_A	Operating ambient temperature	For S grade devices	–40	25.00	105	°C
T_J	Operating junction temperature	For A grade devices	–40	–	100	°C
T_J	Operating junction temperature	For S grade devices	–40	–	120	°C
T_{JA}	Package θ_{JA} (24-pin QFN)		–	38.01	–	°C/Watt
T_{JA}	Package θ_{JA} (16-pin SOIC)		–	142.14	–	°C/Watt

Table 28. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

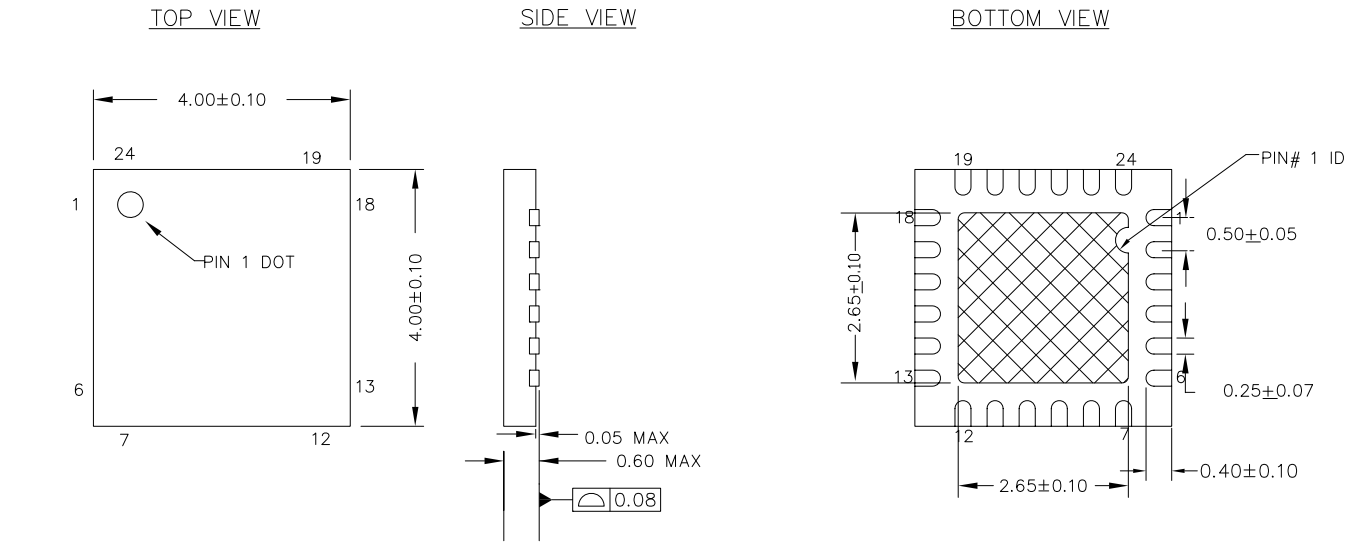
Table 29. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

Downloaded from Arrow.com.

Package Outline Drawings

Figure 7. 24-pin QFN EPAD (Sawn) Package Outline



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

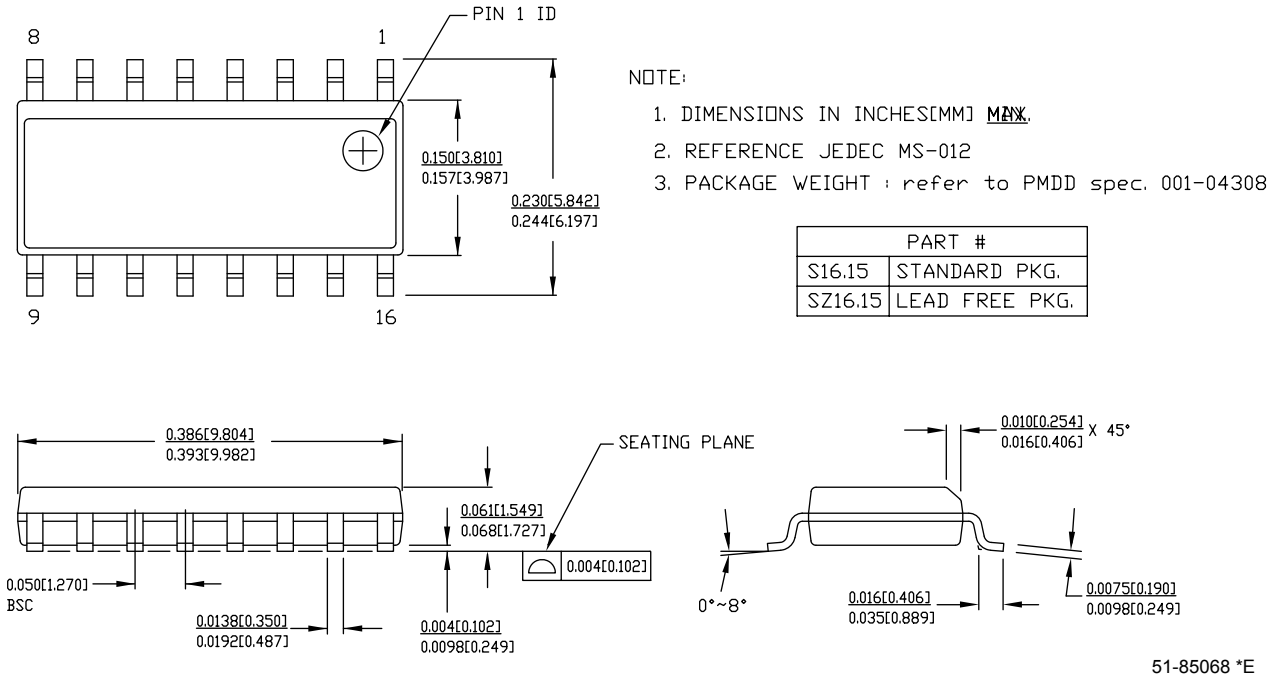
001-13937 *E

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Note
15. Dimensions of the QFN package drawings are in millimeters.

Downloaded from Arrow.com.

Figure 8. 16-pin SOIC (150 Mils) Package Outline



Downloaded from Arrow.com.

Acronyms

Table 30. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 30. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Downloaded from Arrow.com.

Table 30. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

Table 30. Acronyms Used in this Document *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Downloaded from Arrow.com.

Document Conventions

Units of Measure

Table 31. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Downloaded from Arrow.com.

Revision History

Description Title: Automotive PSoC® 4: PSoC 4000 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-92145				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4388517	SNPR	05/23/2014	New datasheet for new device family.
*A	4425292	SNPR	07/23/2014	Changed status from Advance to Preliminary. Updated Electrical Specifications: Updated Device Level Specifications: Updated description above Table 3. Updated Memory: Updated Table 16: Added Note 11 and referred the same note in minimum value of SID182 spec. Added Note 12 and referred the same note in minimum value of SID182A spec.
*B	4594824	JICG	12/12/2014	Updated Electrical Specifications: Updated Device Level Specifications: Updated Table 3: Updated entire table. Updated Analog Peripherals: Updated Comparator: Updated Table 9: Added maximum value of I_{CMP1} parameter as 110 µA. Added maximum value of I_{CMP2} parameter as 85 µA. Updated Table 10: Changed maximum value of T_{COMP1} parameter from 50 ns to 90 ns. Changed maximum value of T_{COMP2} parameter from 100 ns to 110 ns. Updated Digital Peripherals: Removed Timer. Added Timer Counter Pulse-Width Modulator (TCPWM). Removed Counter. Removed Pulse Width Modulation (PWM). Updated I^2C: Updated Table 13: Changed maximum value of I_{I2C1} parameter from 10.5 µA to 25 µA. Added maximum value of I_{I2C4} parameter as 2.5 µA. Updated Power-on Reset (POR): Updated Table 17: Updated entire table. Updated Memory: Updated Table 16: Added maximum value of $T_{BULKERASE}$ parameter as 15 ms. Added maximum value of $T_{DEVPROG}$ parameter as 7.5 seconds. Updated System Resources: Updated Power-on Reset (POR): Updated Table 18: Added maximum value of $V_{FALLPPOR}$ parameter as 1.62 V. Changed minimum value of $V_{FALLDPSLP}$ parameter from 1.14 V to 1.11 V. Updated Internal Main Oscillator: Updated Table 20: Changed maximum value of I_{IMO1} parameter from 1000 µA to 250 µA. Changed maximum value of I_{IMO2} parameter from 325 µA to 180 µA. Updated Table 21: Added maximum value of $T_{STARTIMO}$ parameter as 7 µs.

Downloaded from Arrow.com.

Revision History *(continued)*

Description Title: Automotive PSoC® 4: PSoC 4000 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-92145				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B (cont.)	4594824	JICG	12/12/2014	Updated Packaging: Updated Table 27: Added values for T_J parameter corresponding to Condition “For A grade devices”. Changed maximum value of T_J parameter corresponding to Condition “For S grade devices” from 100 °C to 120 °C. Removed T_{JC} parameter and its details.
*C	4615131	SNPR	01/06/2015	Changed status from Preliminary to Final.
*D	4669514	KUK	02/24/2015	Updated Ordering Information: No change in part numbers. Updated Part Numbering Conventions.

Downloaded from Arrow.com.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2014-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

All products and company names mentioned in this document may be the trademarks of their respective holders.

Downloaded from Arrow.com.