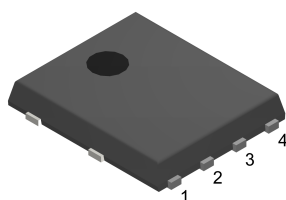
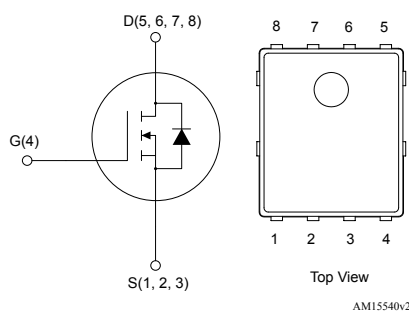


N-channel 30 V, 7.6 mΩ typ., 56 A STripFET H5 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL56N3LLH5	30 V	9 mΩ	56 A

- Low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.



Product status link

[STL56N3LLH5](#)

Product summary

Order code	STL56N3LLH5
Marking	56N3LLH5
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	+22 / -20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	56	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	37	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	15	A
	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	10	A
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	224	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	60	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ °C}$	62.5	W
$P_{TOT}^{(2)}$	Total power dissipation at $T_{pcb} = 25\text{ °C}$	4	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	150	mJ
T_{stg}	Storage temperature range	- 55 to 150	°C
T_J	Operating junction temperature range		°C

1. This value is rated according to R_{thj-c} .
2. This value is rated according to $R_{thj-pcb}$.
3. Pulse width is limited by safe operating area.
4. Starting $T_J = 25\text{ °C}$, $I_D = 56\text{ A}$, $V_{DD} = 50\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

1. When mounted on a 1-inch² FR-4 board, 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = +22 / -20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 7.5\text{ A}$		7.6	9	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 7.5\text{ A}$		9.9	11.2	

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	950		pF
C_{oss}	Output capacitance		-	193		pF
C_{rss}	Reverse transfer capacitance		-	27		pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 4.5\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	6.5	10	nC
Q_{gs}	Gate-source charge		-	3.3		nC
Q_{gd}	Gate-drain charge		-	2.4		nC
R_g	Gate input resistance	$f = 1\text{ MHz}$, gate DC Bias = 0 V , test signal level = 20 mV , $I_D = 0\text{ A}$	-	1.7	2.5	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 7.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	10.8	-	ns
t_r	Rise time		-	15.6	-	ns
$t_{d(off)}$	Turn-off-delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	14.2	-	ns
t_f	Fall time		-	6	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		56	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		224	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 15\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	20	36	ns
Q_{rr}	Reverse recovery charge		-	10	18	nC
I_{RRM}	Reverse recovery current		-	1		A

1. Pulse width limited by safe operating area.

2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

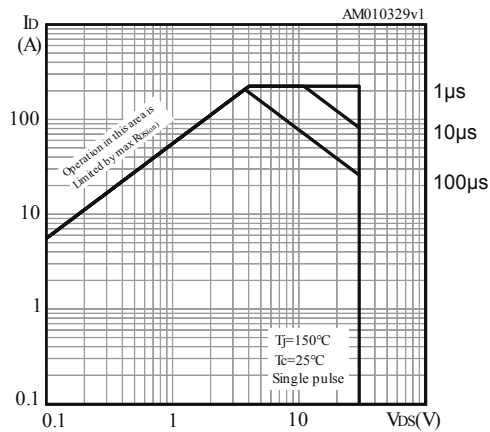
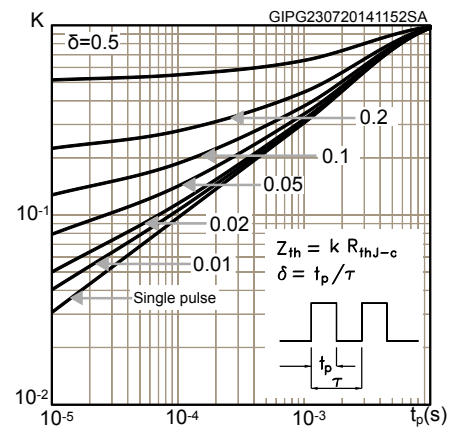
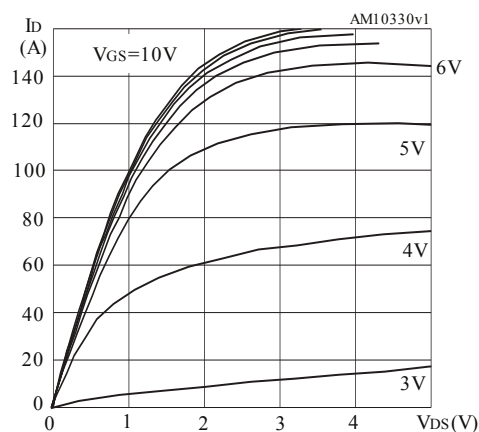
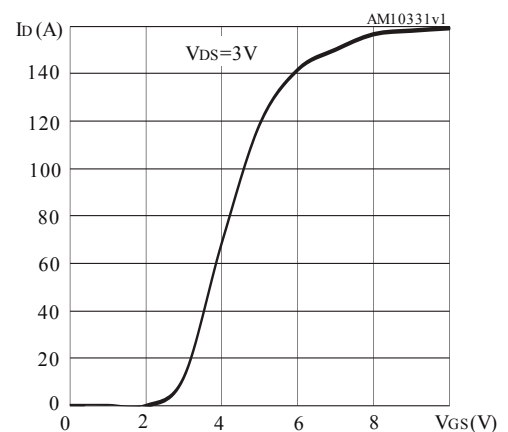
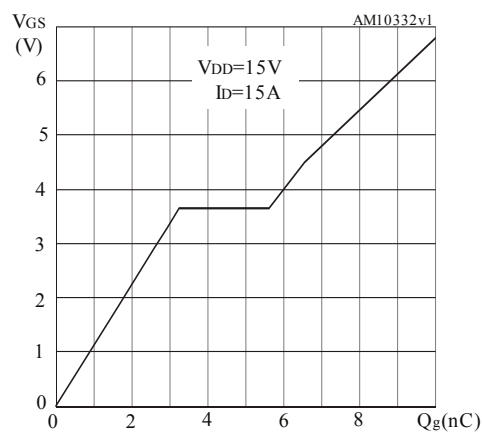
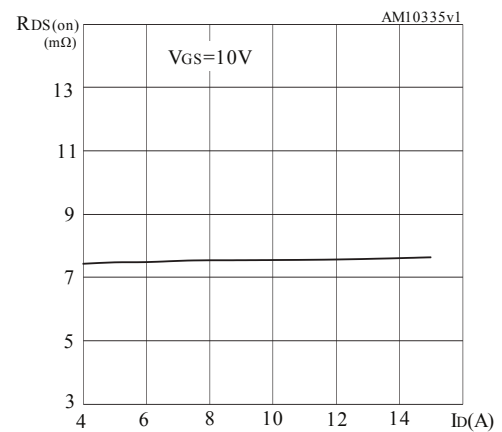
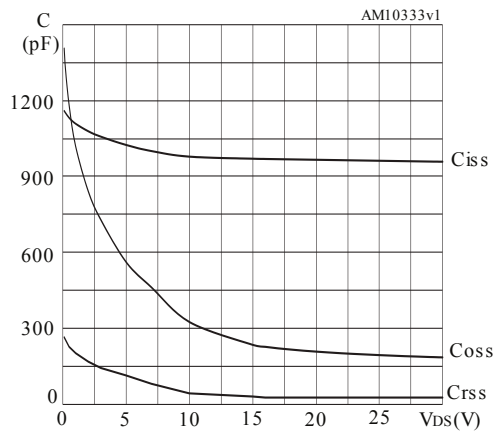
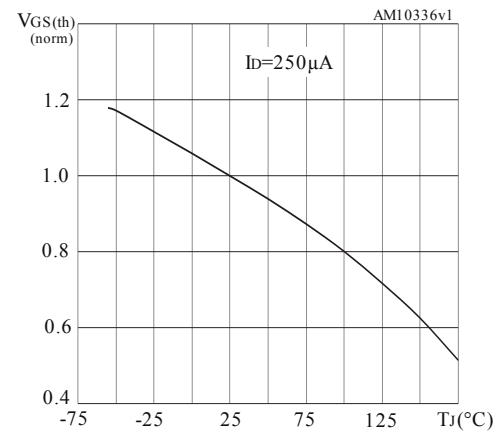
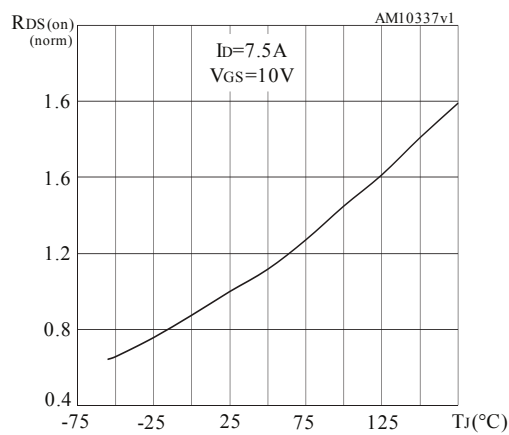
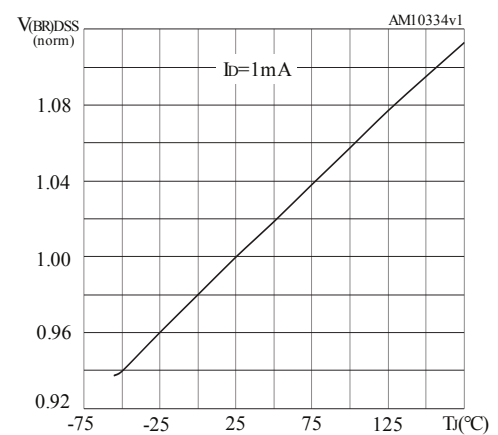
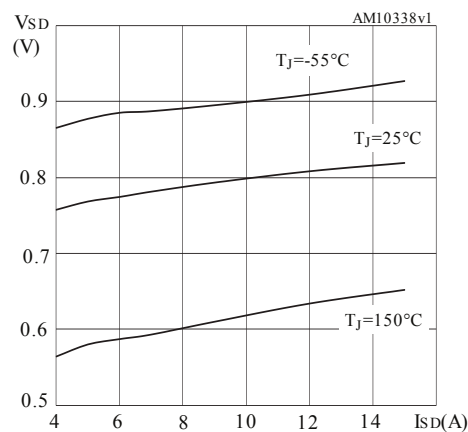
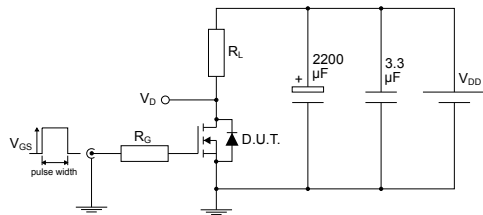
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


Figure 7. Capacitance variations

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

Figure 11. Source-drain diode forward characteristics


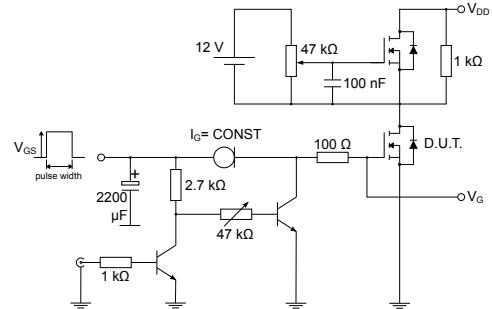
3 Test circuits

Figure 12. Test circuit for resistive load switching times



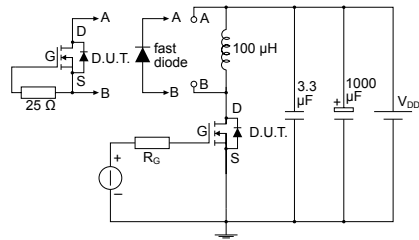
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Figure 13. Test circuit for gate charge behavior



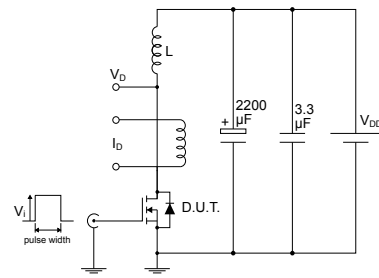
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Figure 14. Test circuit for inductive load switching and diode recovery times



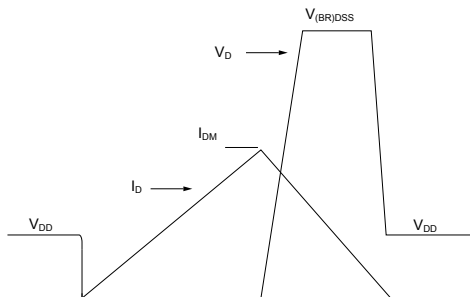
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Figure 15. Unclamped inductive load test circuit



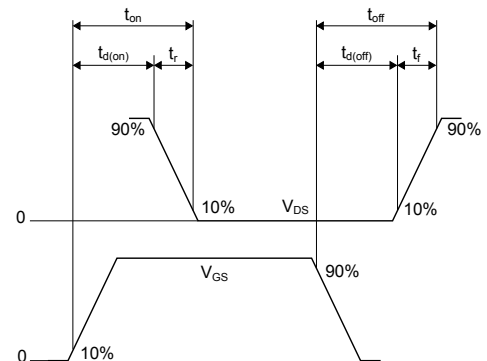
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Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



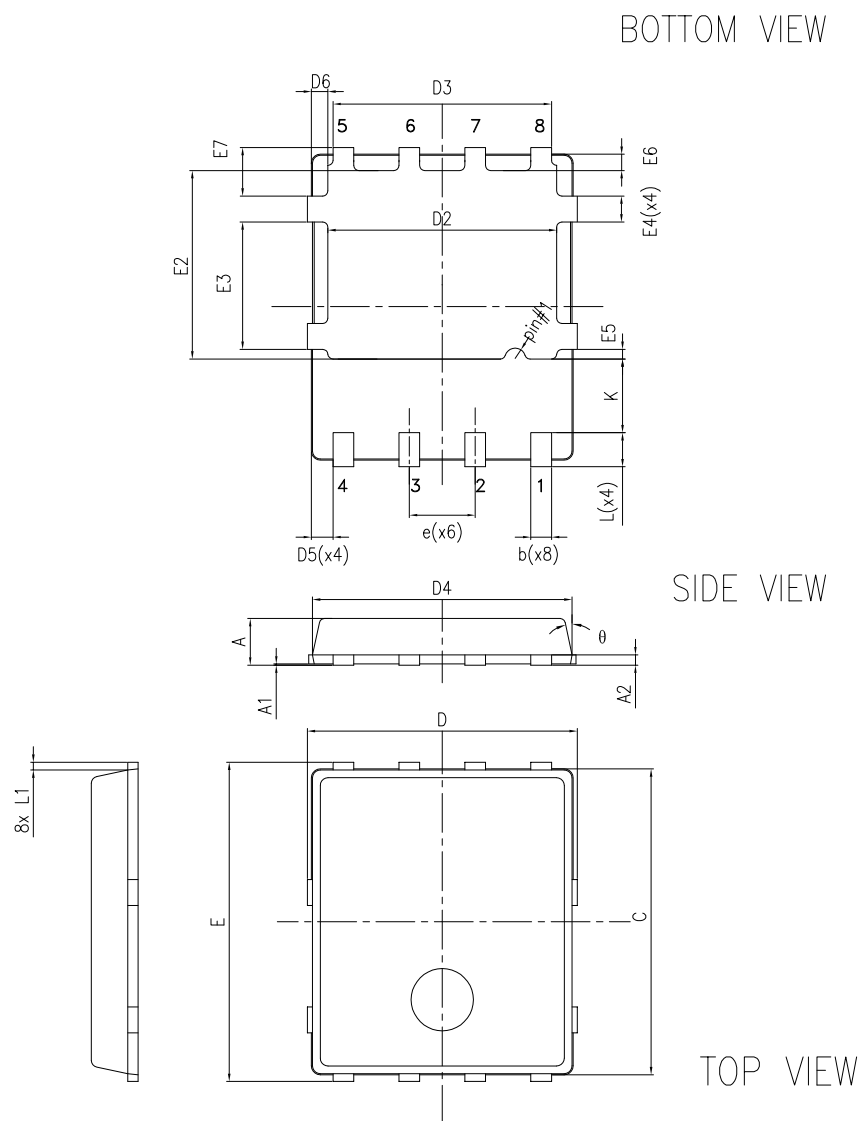
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type R package information

Figure 18. PowerFLAT 5x6 type R package outline



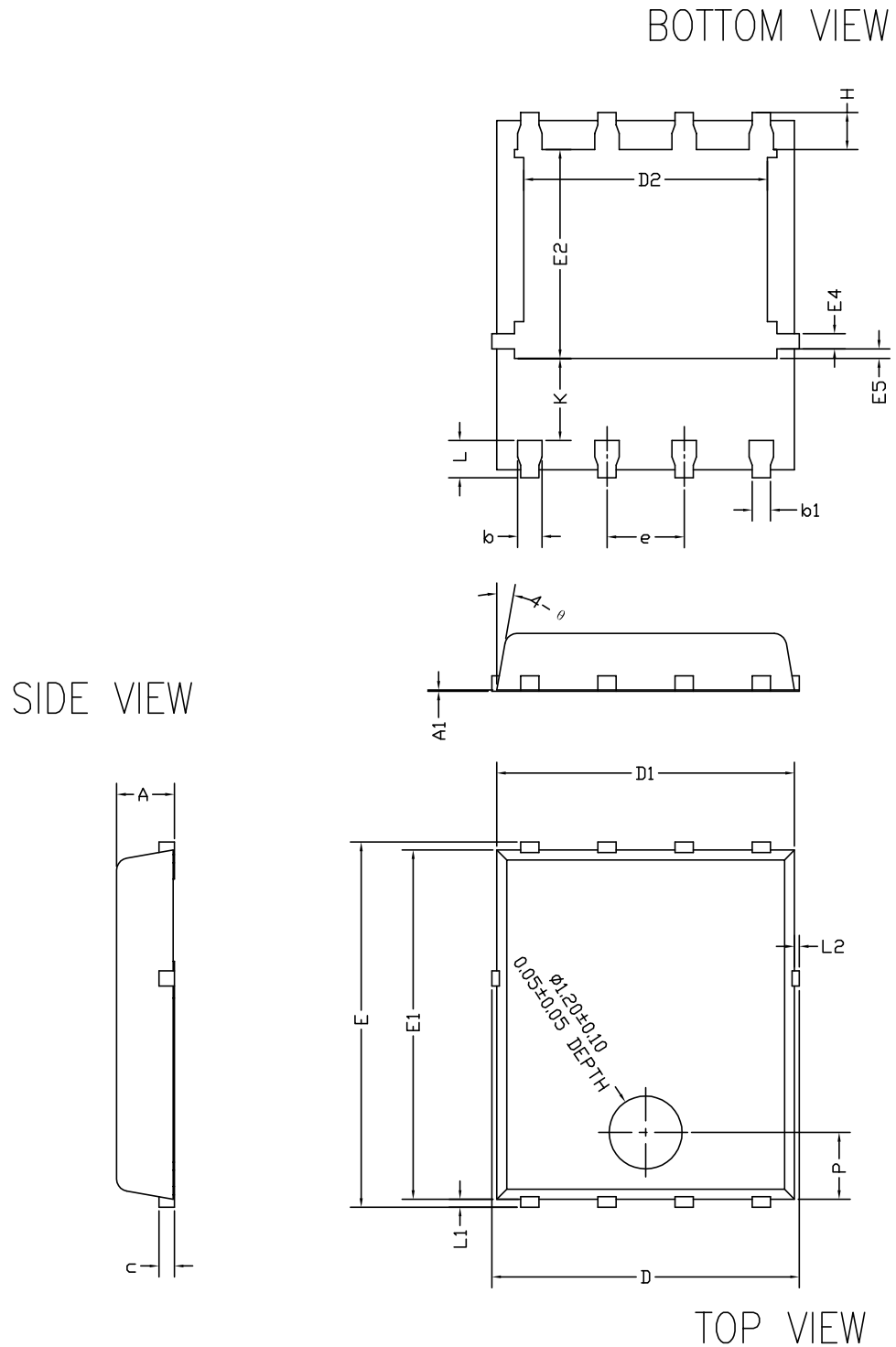
A0ER_8231817_Rev20

Table 7. PowerFLAT 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

4.2 PowerFLAT 5x6 type R SUBCON package information

Figure 19. PowerFLAT 5x6 type R SUBCON package outline

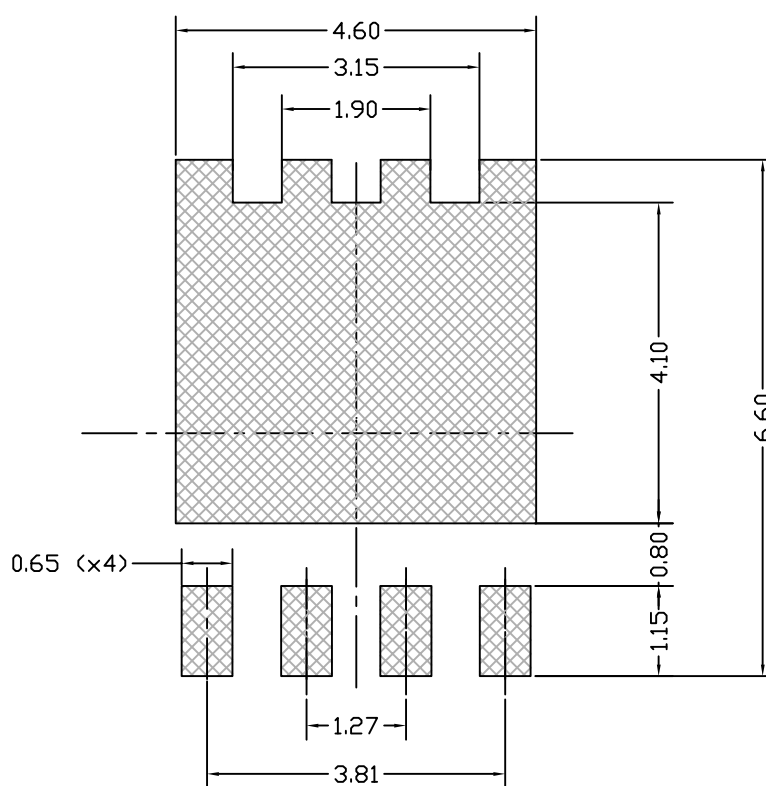


8472137_SUBCON_998G_Type_R_REV4

Table 8. PowerFLAT 5x6 type R SUBCON package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
E4	0.15	0.25	0.35
E5	0.06	0.16	0.26
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

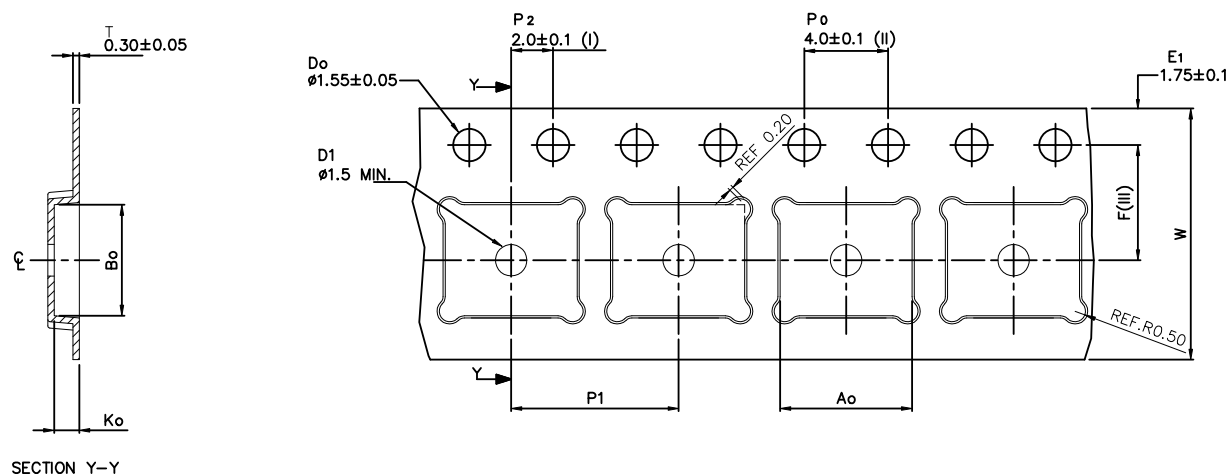
Figure 20. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_simp_Rev_20

4.3 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



Ao	6.30	+/-	0.1
Bo	5.30	+/-	0.1
Ko	1.20	+/-	0.1
F	5.50	+/-	0.1
P1	8.00	+/-	0.1
W	12.00	+/-	0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
 All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape

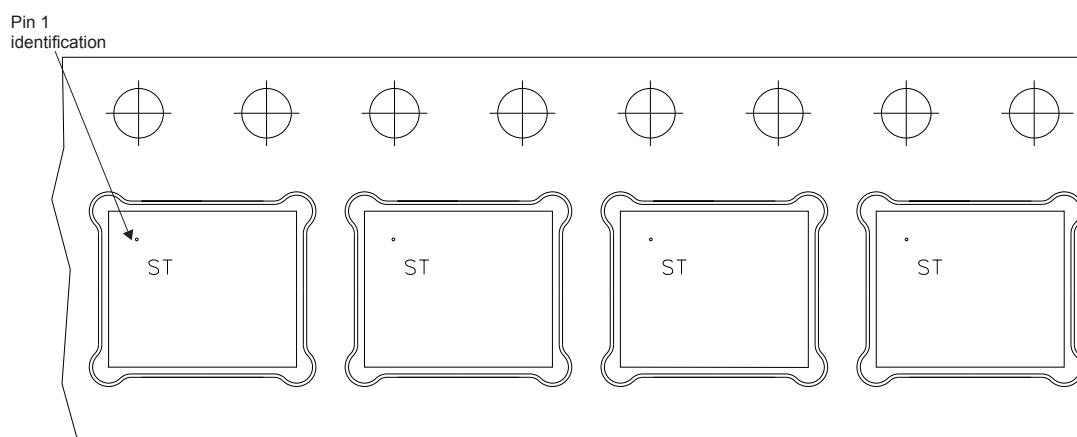
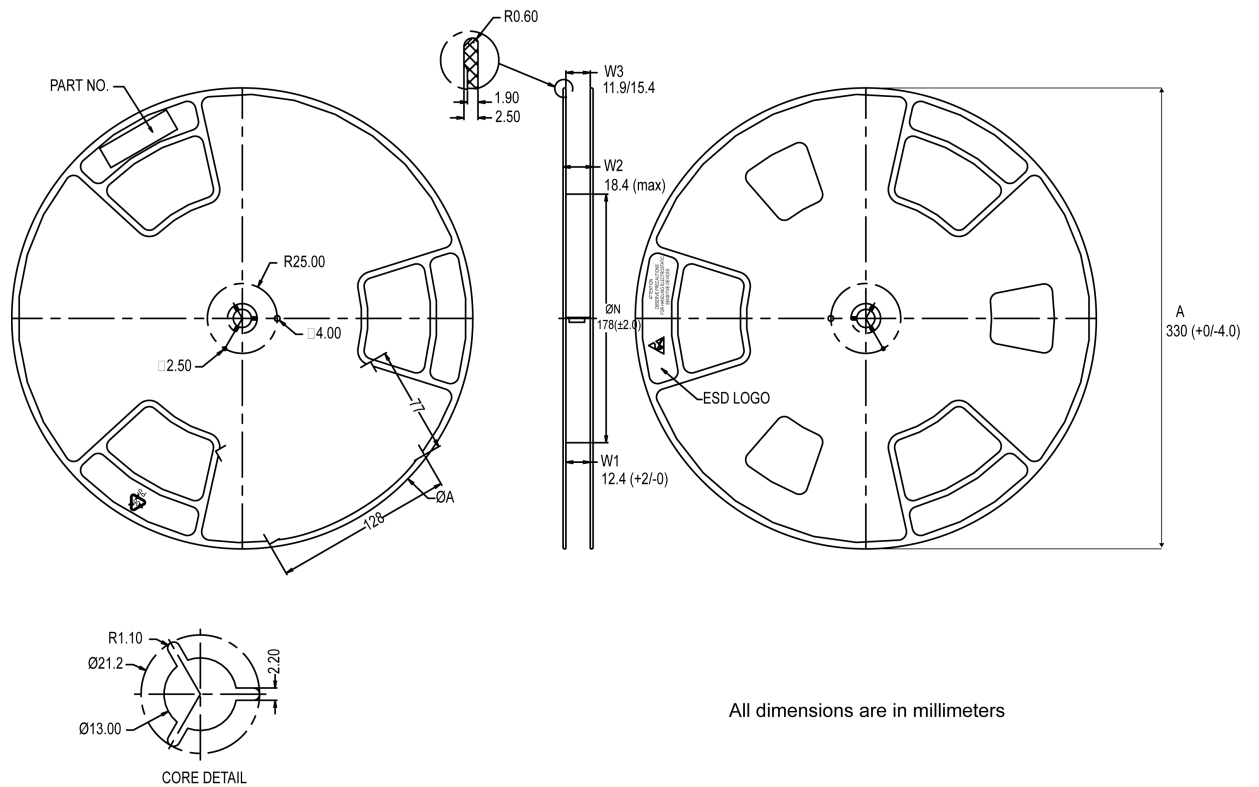


Figure 23. PowerFLAT 5x6 reel



8234350_Reel_rev_C

Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Jan-2011	1	First release.
01-Jul-2011	2	Document status promoted from preliminary data to datasheet.
27-Apr-2012	3	Added E_{AS} value in <i>Table 2: Absolute maximum ratings</i> . Updated <i>Table 3: Thermal resistance</i> , <i>Table 4: On/off states</i> , <i>Table 5: Dynamic</i> and <i>Table 7: Source drain diode</i> . Minor text changes.
13-Feb-2013	4	– Added: <i>Section 5: Packaging mechanical data</i> . – Updated <i>Section 4: Package mechanical data</i> .
25-Jul-2014	5	– Modified: title, features and description in cover page – Modified: I_{SD} and I_{SDM} max values in <i>Table 7</i> – Updated: <i>Figure 2</i> and <i>3</i> – Updated: <i>Figure 13, 14, 15</i> and <i>16</i> – Updated: <i>Section 4: Package mechanical data</i> – Minor text changes
19-Feb-2020	6	Updated <i>Section 4 Package information..</i> Minor text changes.
20-May-2021	7	Updated marking in cover page.

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