

# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

**80 V, 6.5 mΩ , 48 A**

**FDMC86340**

## Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

## Features

- Shielded Gate MOSFET Technology
- Max  $R_{DS(on)}$  = 6.5 mΩ at  $V_{GS} = 10$  V,  $I_D = 14$  A
- Max  $R_{DS(on)}$  = 8.5 mΩ at  $V_{GS} = 8$  V,  $I_D = 12$  A
- High Performance Technology for Extremely Low  $R_{DS(on)}$
- Termination is Lead-Free
- RoHS Compliant

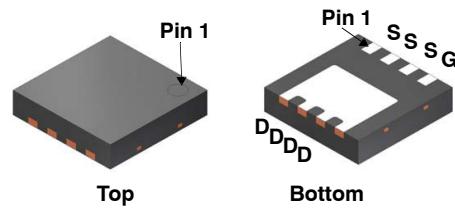
## Applications

- DC-DC Conversion

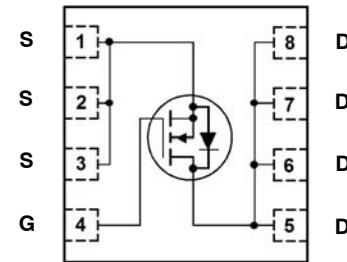
## MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Ratings	Unit
V <sub>DS</sub>	Drain-to-Source Voltage	80	V
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V
I <sub>D</sub>	Drain Current – Continuous T <sub>C</sub> = 25°C T <sub>A</sub> = 25°C (Note 1a)	48 14	A
	– Pulsed (Note 4)	200	
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 3)	216	mJ
P <sub>D</sub>	Power Dissipation T <sub>C</sub> = 25°C T <sub>A</sub> = 25°C (Note 1a)	54 2.3	W
	Operating and Storage Junction Temperature Range	–55 to +150	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



WDFN8  
CASE 483AW



## MARKING DIAGRAM

\$YZXYYKK  
FDMC  
86340

\$Y = onsemi Logo  
 Z = Assembly Plant Code  
 XYY = Date Code (Year & Week)  
 KK = Lot Traceability Code  
 FDMC86340 = Specific Device Code

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
FDMC86340	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMC86340

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta,JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.3	°C/W
$R_{\theta,JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	53	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$\text{BV}_{\text{DSS}}$	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	80	—	—	V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	—	46	—	mV/°C
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(\text{th})}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	3.4	4.0	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	—	-10	—	mV/°C
$R_{DS(\text{on})}$	Static Drain-to-Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 14 \text{ A}$	—	5.0	6.5	mΩ
		$V_{GS} = 8 \text{ V}, I_D = 12 \text{ A}$	—	6.0	8.5	
		$V_{GS} = 10 \text{ V}, I_D = 14 \text{ A}, T_J = 125^\circ\text{C}$	—	8.5	11	
$g_{\text{FS}}$	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 14 \text{ A}$	—	36	—	S

### DYNAMIC CHARACTERISTICS

$C_{\text{iss}}$	Input Capacitance	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	2775	3885	pF
$C_{\text{oss}}$	Output Capacitance		—	468	655	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		—	15	25	pF
$R_g$	Gate Resistance		0.1	0.7	2.1	Ω

### SWITCHING CHARACTERISTICS

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 40 \text{ V}, I_D = 14 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$	—	20	32	ns
$t_r$	Rise Time		—	7.9	16	
$t_{d(\text{off})}$	Turn-Off Delay Time		—	23	37	
$t_f$	Fall Time		—	5.1	10	
$Q_{g(\text{tot})}$	Total Gate Charge	$V_{GS} = 0 \text{ V} \text{ to } 10 \text{ V}, V_{DD} = 40 \text{ V}, I_D = 14 \text{ A}$		38	53	nC
$Q_{g(\text{tot})}$	Total Gate Charge	$V_{GS} = 0 \text{ V} \text{ to } 8 \text{ V}, V_{DD} = 40 \text{ V}, I_D = 14 \text{ A}$		31	44	
$Q_{gs}$	Gate-to-Source Charge	$V_{DD} = 40 \text{ V}, I_D = 14 \text{ A}$		14	—	
$Q_{gd}$	Gate-to-Drain "Miller" Charge	$V_{DD} = 40 \text{ V}, I_D = 14 \text{ A}$		8.0	—	
$Q_{oss}$	Output Charge	$V_{DD} = 40 \text{ V}, I_D = 0 \text{ V}$		42	—	

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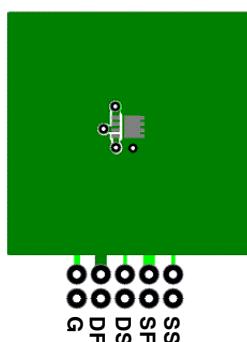
ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$V_{SD}$	Source-to-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = 14 \text{ A}$ (Note 2)	–	0.80	1.3	V
		$V_{GS} = 0 \text{ V}$ , $I_S = 1.9 \text{ A}$ (Note 2)	–	0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 14 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$	–	41	66	ns
			–	25	40	nC

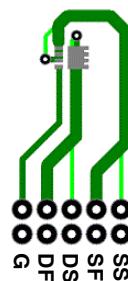
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1 \text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5 \text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $53^\circ\text{C}/\text{W}$  when mounted on a  $1 \text{ in}^2$  pad of 2 oz copper

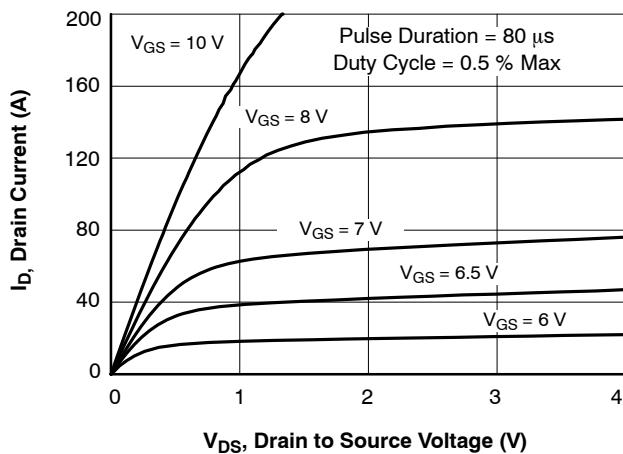


b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

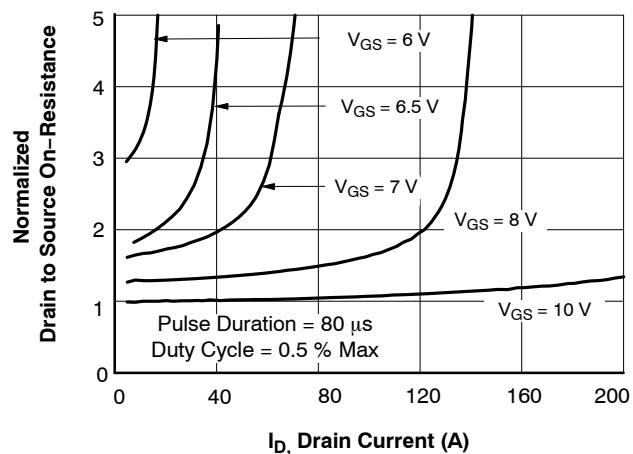
- Pulse Test: Pulse Width  $< 300 \mu\text{s}$ , Duty cycle  $< 2.0\%$ .
- $E_{AS}$  of 216 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3 \text{ mH}$ ,  $I_{AS} = 12 \text{ A}$ ,  $V_{DD} = 80 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ . 100% test at  $L = 0.1 \text{ mH}$ ,  $I_{AS} = 37 \text{ A}$ .
- Pulsed  $I_d$  limited by junction temperature,  $t_d \leq 100 \mu\text{s}$ , please refer to SOA curve for more details.

**TYPICAL CHARACTERISTICS**

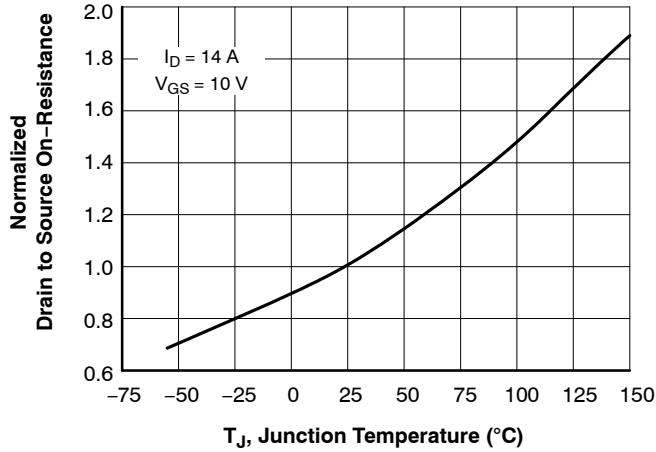
( $T_J = 25^\circ\text{C}$  unless otherwise noted)



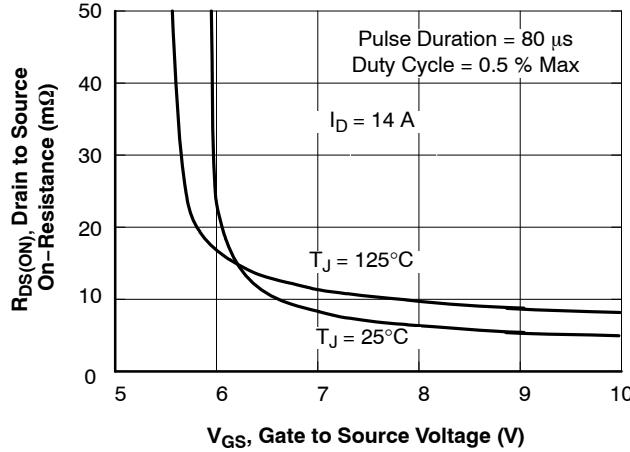
**Figure 1. On-Region Characteristics**



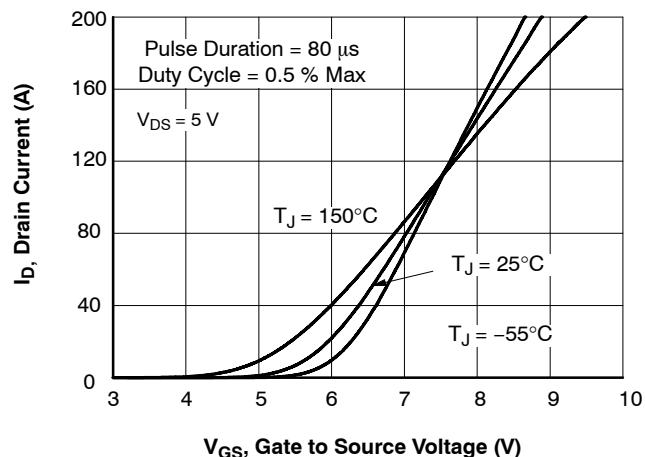
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



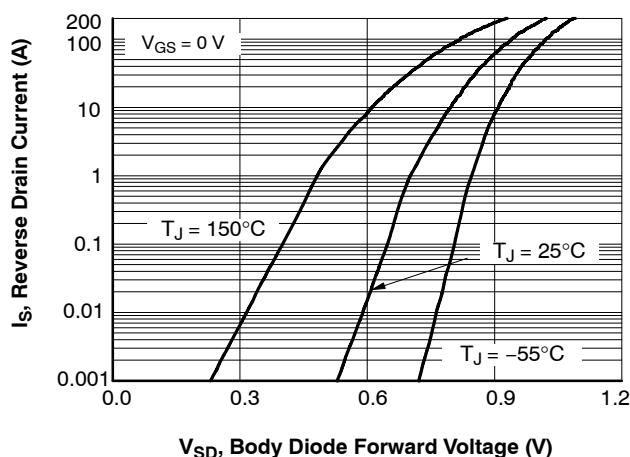
**Figure 3. Normalized On-Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**



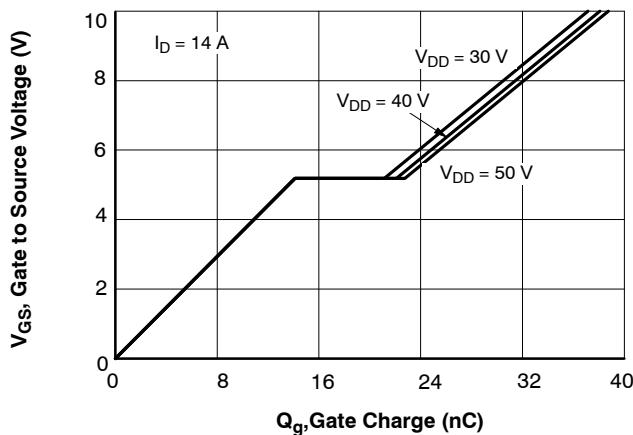
**Figure 5. Transfer Characteristics**



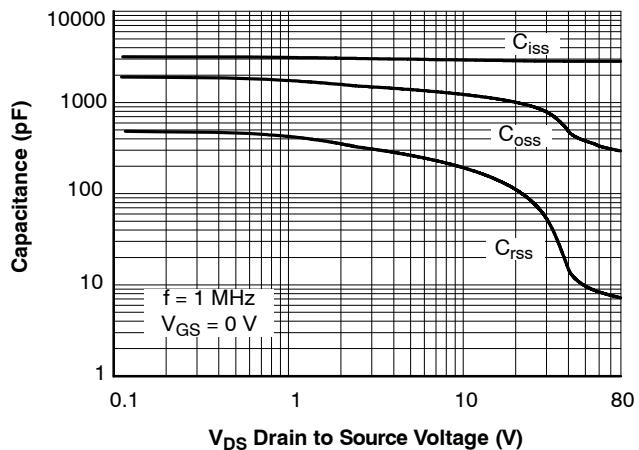
**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

**TYPICAL CHARACTERISTICS** (continued)

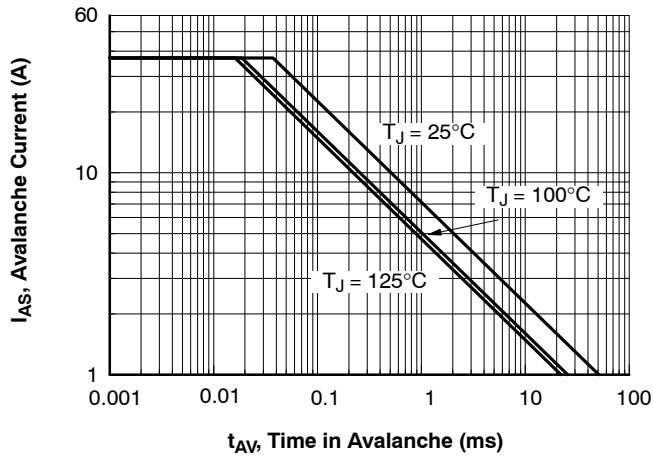
( $T_J = 25^\circ\text{C}$  unless otherwise noted)



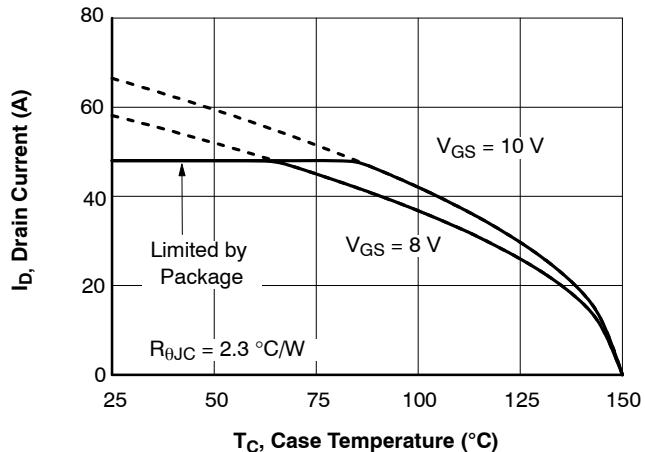
**Figure 7. Gate Charge Characteristics**



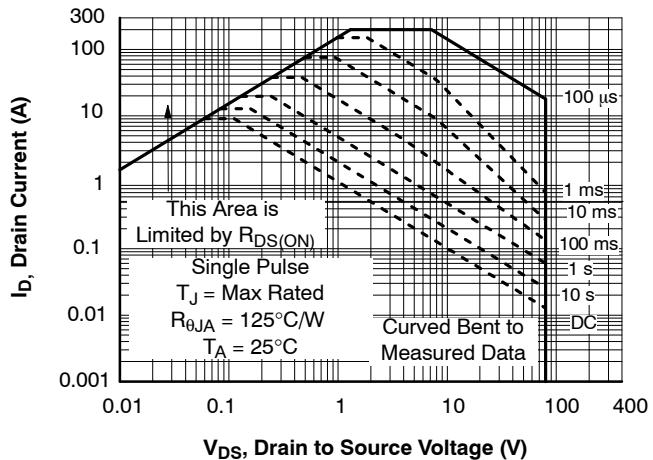
**Figure 8. Capacitance vs Drain to Source Voltage**



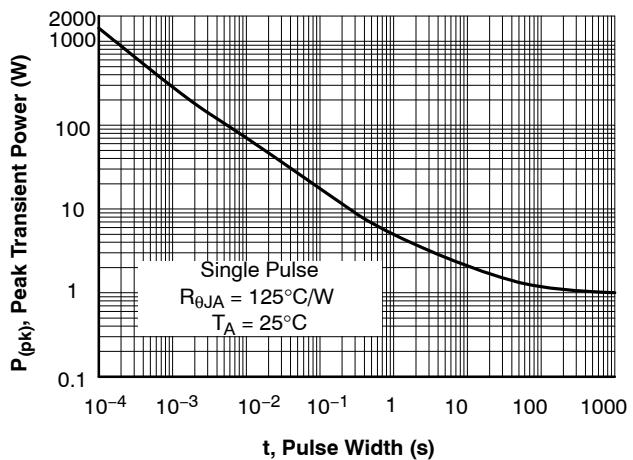
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

## TYPICAL CHARACTERISTICS (continued)

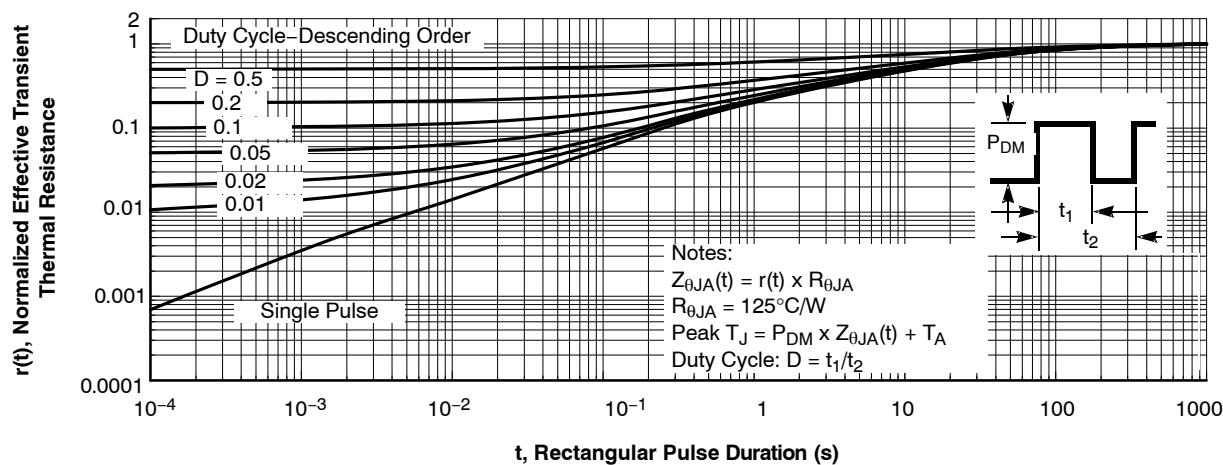
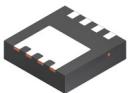
(T<sub>J</sub> = 25°C unless otherwise noted)

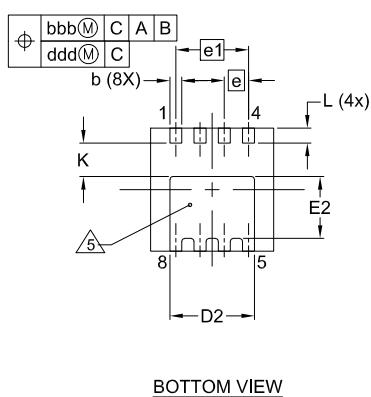
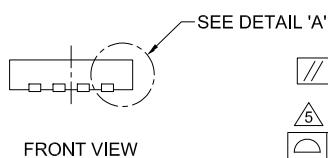
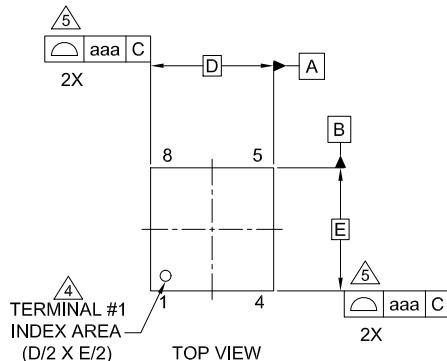
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

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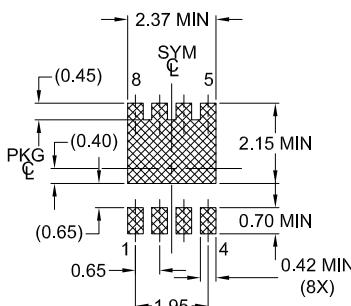


**WDFN8 3.30x3.30x0.75, 0.65P  
CASE 483AW  
ISSUE B**

DATE 22 MAR 2024



## LAND PATTERN RECOMMENDATION



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SODERRM.D.

## GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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