

## SNx4AHC245 Octal Bus Transceivers With 3-State Outputs

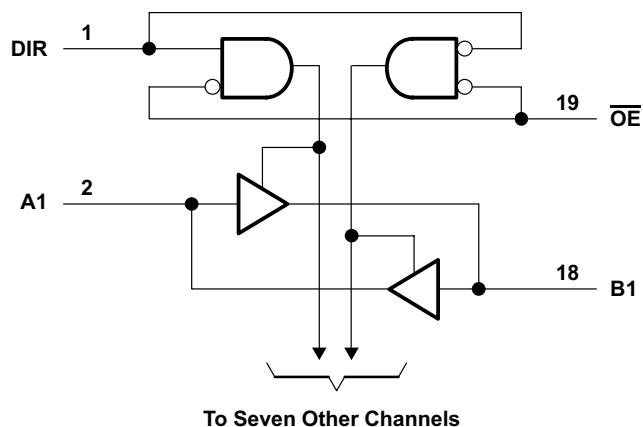
### 1 Features

- Operating Range 2-V to 5.5-V  $V_{CC}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Fitness Devices
- Telecom Infrastructures
- Electronic Points of Sale

### 4 Simplified Schematic



### 3 Description

The SNx4AHC245 octal bus transceivers are designed for asynchronous two-way communication between data buses. This part operates from 4.5 V to 5.5 V.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC245	PDIP (20)	25.40 mm x 6.35 mm
	SSOP (20)	7.50 mm x 5.30 mm
	TSSOP (20)	6.50 mm x 4.40 mm
	TVSOP (20)	5.00 mm x 4.40 mm
	SOIC (20)	12.80 mm x 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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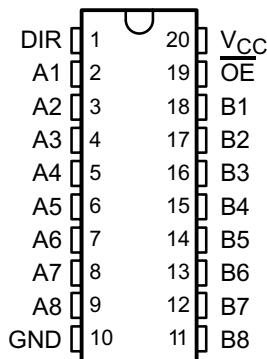
## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

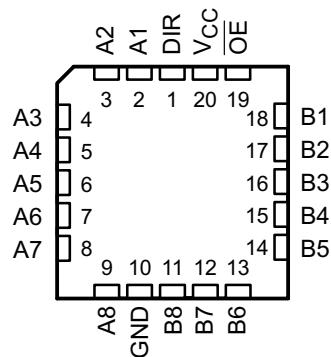
Changes from Revision I (July 2003) to Revision J	Page
• Updated document to new TI data sheet format.	1
• Removed Ordering Information table.	1
• Added Military Disclaimer to Features list.	1
• Added Applications.	1
• Added Device Information table.	1
• Added Handling Ratings table.	4
• Changed MAX ambient temperature to 125°C in Recommended Operating Conditions.	5
• Added Typical Characteristics.	8
• Added Detailed Description section.	10
• Added Application and Implementation section.	11
• Added Power Supply Recommendations and Layout sections.	12

## 6 Pin Configuration and Functions

**SN54AHC245 . . . J OR W PACKAGE  
SN74AHC245 . . . DB, DGV, DW, N, OR PW PACKAGE  
(TOP VIEW)**



**SN54AHC245 . . . FK PACKAGE  
(TOP VIEW)**



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DIR	I/O	Direction Pin
2	A1	I/O	A1 Input/Output
3	A2	I/O	Y4 Input/Output
4	A3	I/O	A2 Input/Output
5	A4	I/O	Y3 Input/Output
6	A5	I/O	A3 Input/Output
7	A6	I/O	Y2 Input/Output
8	A7	I/O	A4 Input/Output
9	A8	I/O	Y1 Input/Output
10	GND	—	Ground Pin
11	B8	I/O	A1 Input/Output
12	B7	I/O	Y4 Input/Output
13	B6	I/O	A2 Input/Output
14	B5	I/O	Y3 Input/Output
15	B4	I/O	A3 Input/Output
16	B	I/O	Y2 Input/Output
17	B2	I/O	A4 Input/Output
18	B2	I/O	Y1 Input/Output
19	B1	I/O	Output Enable
20	V <sub>CC</sub>	—	Power Pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	Control inputs	-0.5	7	V
$V_O$	I/O, Output voltage range		-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	Control inputs	-20	mA
$I_{OK}$	I/O, Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		$\pm 20$	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		$\pm 25$	mA
	Continuous current through $V_{CC}$ or GND			$\pm 75$	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 Handling Ratings

			MIN	MAX	UNIT
$T_{stg}$	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHC245		SN74AHC245		UNIT	
		MIN	MAX	MIN	MAX		
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5	1.5	V	
		V <sub>CC</sub> = 3 V	2.1	2.1	2.1		
		V <sub>CC</sub> = 5.5 V	3.85	3.85	3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	0.5	0.5	V	
		V <sub>CC</sub> = 3 V	0.9	0.9	0.9		
		V <sub>CC</sub> = 5.5 V	1.65	1.65	1.65		
V <sub>I</sub>	Input voltage	OE or DIR	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	A or B	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	–50	–50	–50	μA	
		V <sub>CC</sub> = 3.3 V ± 0.3 V	–4	–4	–4	mA	
		V <sub>CC</sub> = 5 V ± 0.5 V	–8	–8	–8		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	50	50	μA	
		V <sub>CC</sub> = 3.3 V ± 0.3 V	4	4	4	mA	
		V <sub>CC</sub> = 5 V ± 0.5 V	8	8	8		
Δt/ΔV	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	100	100	100	ns/V	
		V <sub>CC</sub> = 5 V ± 0.5 V	20	20	20		
T <sub>A</sub>	Operating free-air temperature	–55	125	–40	125	°C	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	DB	DGV	DW	N	NS	PW	RGY	UNIT
	20 PINS							
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	96.0	116.1	79.8	51.5	77.1	102.8	35.1
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	57.7	31.3	45.8	38.2	43.6	36.8	43.3
R <sub>θJB</sub>	Junction-to-board thermal resistance	51.2	57.6	47.4	32.4	44.6	53.8	12.9
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	19.4	1.0	18.5	24.6	17.2	2.5	0.9
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	50.8	56.9	47.0	32.3	44.2	53.3	12.9
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	7.9

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC245		SN74AHC245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2	1.9	1.9	1.9	1.9	1.9	V
		3 V	2.9	3	2.9	2.9	2.9	2.9	2.9	
		4.5 V	4.4	4.5	4.4	4.4	4.4	4.4	4.4	
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48	2.48			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V		0.1		0.1	0.1	0.1	0.1	V
		3 V		0.1		0.1	0.1	0.1	0.1	
		4.5 V		0.1		0.1	0.1	0.1	0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.36	0.5	0.5	0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.36	0.5	0.5	0.44	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND OE or DIR	5.5 V		±0.1		±1	±1	±1	µA
			0 V to 5.5 V		±0.1		±1 <sup>(1)</sup>	±1	±1	
I <sub>OZ</sub> <sup>(2)</sup>		V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V		±0.25		±2.5	±2.5	±2.5	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4	40	40	40	µA
C <sub>I</sub>	OE or DIR	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10			10	pF
C <sub>IO</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4					pF

 (1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

 (2) The parameter I<sub>OZ</sub> includes the input leakage current.

## 7.6 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC245		SN74AHC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 15 pF		5.8 <sup>(1)</sup>	8.4 <sup>(1)</sup>	1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10	ns
t <sub>PHL</sub>					5.8 <sup>(1)</sup>	8.4 <sup>(1)</sup>	1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10	
t <sub>PZH</sub>	OE	A or B	C <sub>L</sub> = 15 pF		8.5 <sup>(1)</sup>	13.2 <sup>(1)</sup>	1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	ns
t <sub>PZL</sub>					8.5 <sup>(1)</sup>	13.2 <sup>(1)</sup>	1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	
t <sub>PHZ</sub>	OE	A or B	C <sub>L</sub> = 15 pF		8.9 <sup>(1)</sup>	12.5 <sup>(1)</sup>	1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	ns
t <sub>PLZ</sub>					8.9 <sup>(1)</sup>	12.5 <sup>(1)</sup>	1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 50 pF		8.3	11.9	1	13.5	1	13.5	ns
t <sub>PHL</sub>					8.3	11.9	1	13.5	1	13.5	
t <sub>PZH</sub>	OE	A or B	C <sub>L</sub> = 50 pF		11	16.7	1	19	1	19	ns
t <sub>PZL</sub>					11	16.7	1	19	1	19	
t <sub>PHZ</sub>	OE	A or B	C <sub>L</sub> = 50 pF		11.5	15.8	1	18	1	18	ns
t <sub>PLZ</sub>					11.5	15.8	1	18	1	18	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			1.5 <sup>(2)</sup>				1.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 7.7 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC245		SN74AHC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	$C_L = 15 \text{ pF}$	4 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	ns
$t_{PHL}$				4 <sup>(1)</sup>	5.5 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 15 \text{ pF}$	5.8 <sup>(1)</sup>	8.5 <sup>(1)</sup>	1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10	1	ns
$t_{PZL}$				5.8 <sup>(1)</sup>	8.5 <sup>(1)</sup>	1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10	1	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 15 \text{ pF}$	5.6 <sup>(1)</sup>	7.8 <sup>(1)</sup>	1 <sup>(1)</sup>	9.2 <sup>(1)</sup>	1	9.2	1	ns
$t_{PLZ}$				5.6 <sup>(1)</sup>	7.8 <sup>(1)</sup>	1 <sup>(1)</sup>	9.2 <sup>(1)</sup>	1	9.2	1	
$t_{PLH}$	A or B	B or A	$C_L = 50 \text{ pF}$	5.5	7.5	1	8.5	1	8.5	1	ns
$t_{PHL}$				5.5	7.5	1	8.5	1	8.5	1	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 50 \text{ pF}$	7.3	10.6	1	12	1	12	1	ns
$t_{PZL}$				7.3	10.6	1	12	1	12	1	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 50 \text{ pF}$	7	9.7	1	11	1	11	1	ns
$t_{PLZ}$				7	9.7	1	11	1	11	1	
$t_{SK(0)}$			$C_L = 50 \text{ pF}$			1 <sup>(2)</sup>				1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.  
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 7.8 Noise Characteristics<sup>(1)</sup>

$V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	SN74AHC245			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.9		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.9		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.3		V
$V_{IH(D)}$ High-level dynamic input voltage		3.5		V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

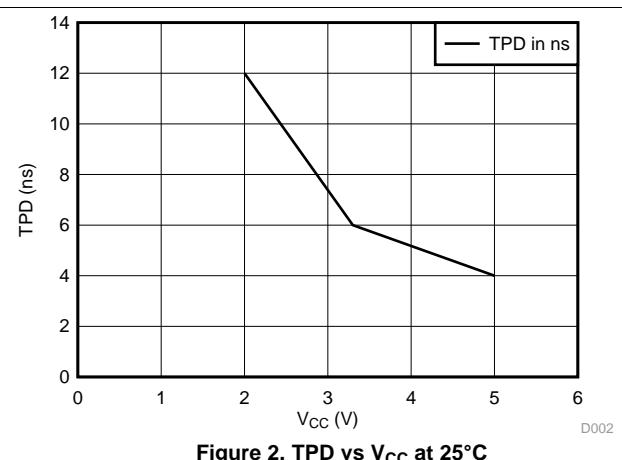
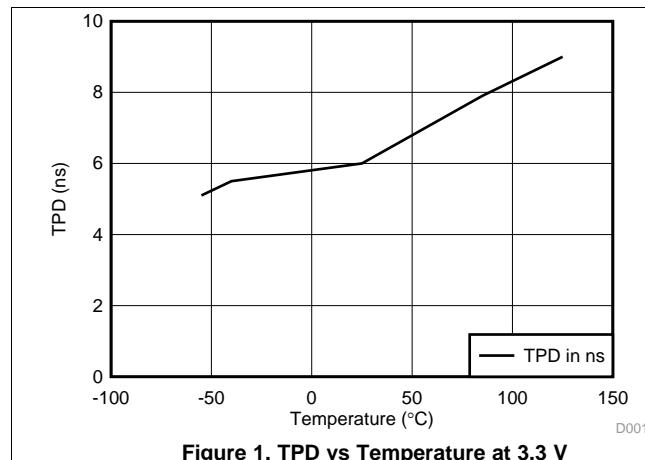
(1) Characteristics are for surface-mount packages only.

## 7.9 Operating Characteristics

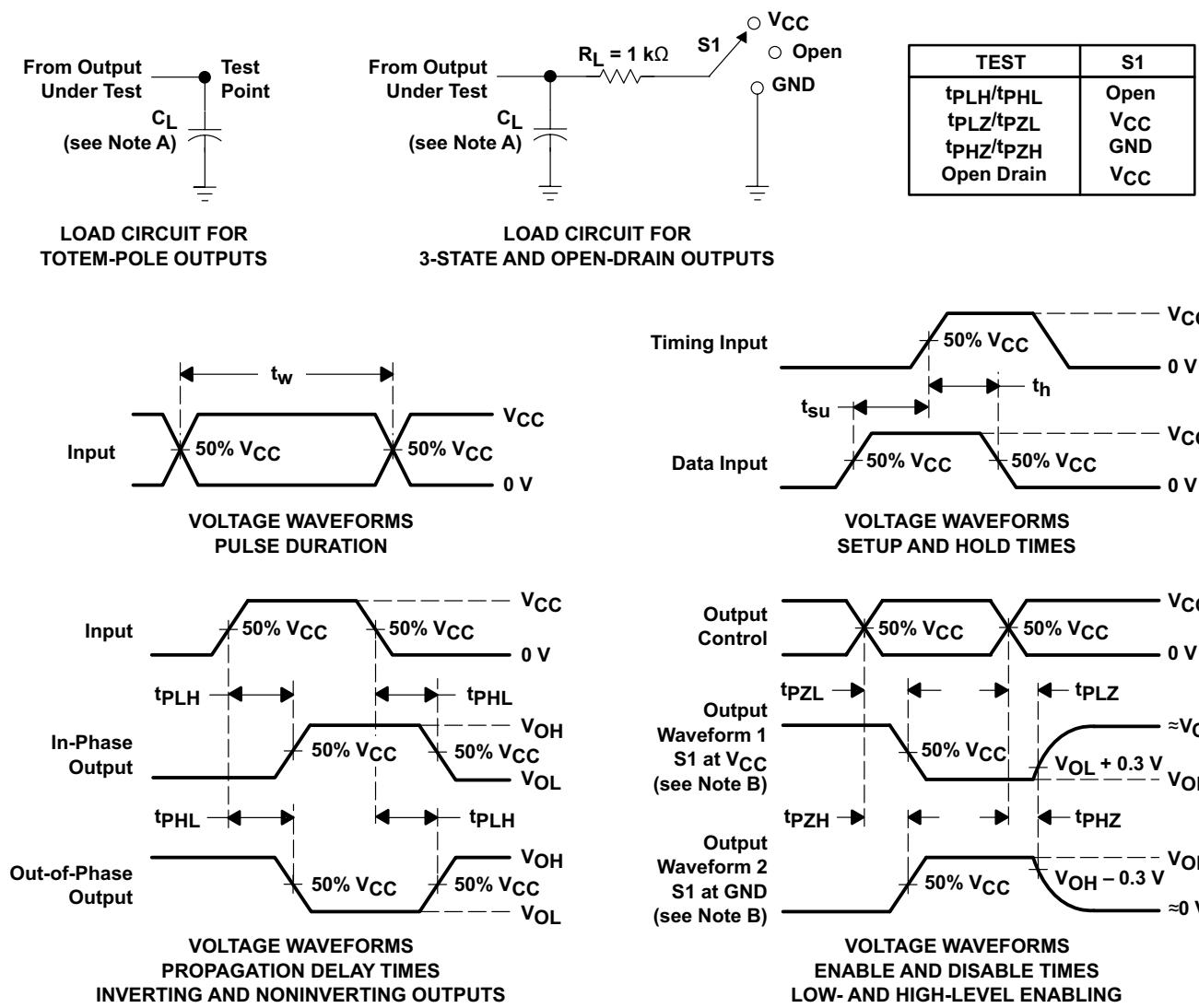
$V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load $f = 1 \text{ MHz}$	14	pF

## 7.10 Typical Characteristics



## 8 Parameter Measurement Information



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

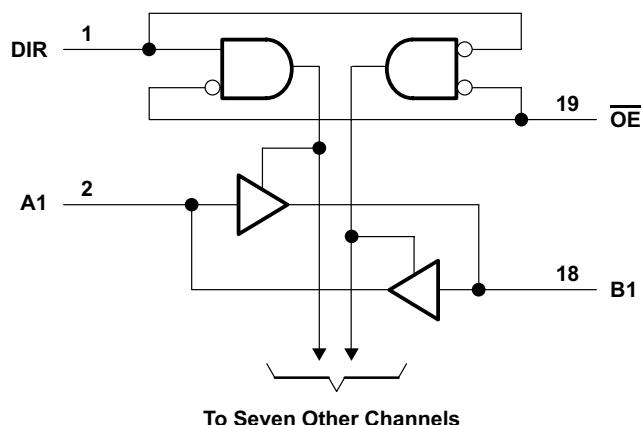
**Figure 3. Load Circuit and Voltage Waveforms**

## 9 Detailed Description

### 9.1 Overview

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SNx4AHC245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- $V_{CC}$  is optimized at 5 V
- Allows down voltage translation from 5 V to 3.3 V
  - Inputs accept voltage levels up to 5.5 V
- Slow edge rates minimize output ringing

### 9.4 Device Functional Modes

**Table 1. Function Table  
(Each Transceiver)**

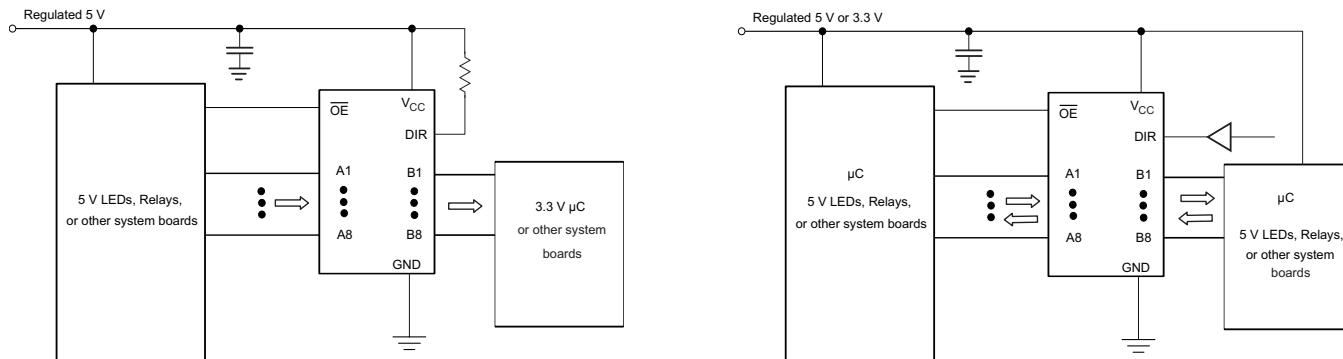
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## 10 Application and Implementation

### 10.1 Application Information

The SNx4AHC245A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making it ideal for down translation.

### 10.2 Typical Application



**Figure 4. Typical Application Schematic**

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 75 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves

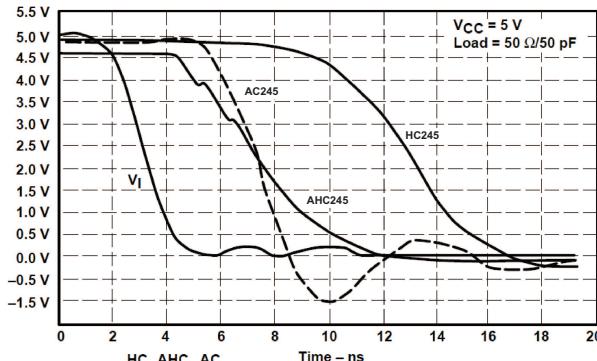


Figure 5. Switching Characteristics Comparison

## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and a 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 6 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

### 12.2 Layout Example

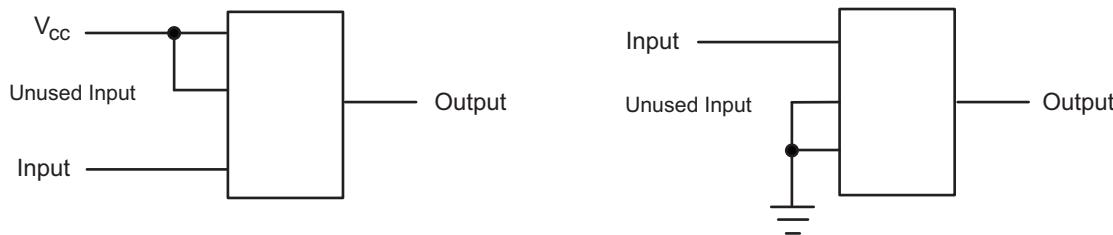


Figure 6. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC245	<a href="#">Click here</a>				
SN74AHC245	<a href="#">Click here</a>				

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

#### [SLYZ022 — TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9681801Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9681801Q2A SNJ54AHC 245FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9681801QRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801QR A SNJ54AHC245J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9681801QSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801QS A SNJ54AHC245W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9681801VSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801VS A SNV54AHC245W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245DWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC245N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HA245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74AHC245PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA245	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHC245FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9681801Q2A SNJ54AHC 245FK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHC245J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801QR A SNJ54AHC245J	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54AHC245W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9681801QS A SNJ54AHC245W	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHC245, SN54AHC245-SP, SN74AHC245 :**

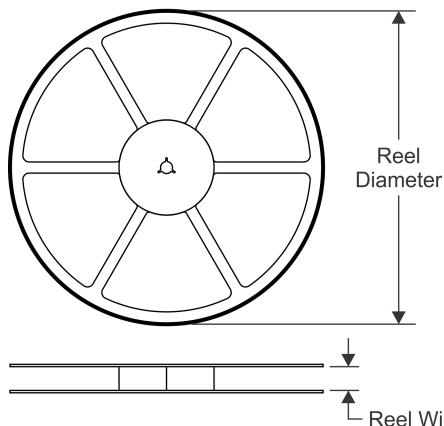
- Catalog : [SN74AHC245](#), [SN54AHC245](#)
- Automotive : [SN74AHC245-Q1](#), [SN74AHC245-Q1](#)
- Enhanced Product : [SN74AHC245-EP](#), [SN74AHC245-EP](#)
- Military : [SN54AHC245](#)
- Space : [SN54AHC245-SP](#)

**NOTE: Qualified Version Definitions:**

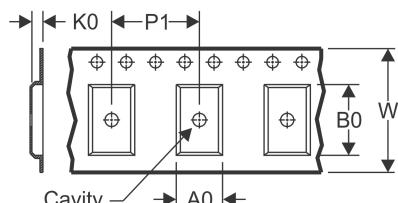
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

## REEL DIMENSIONS

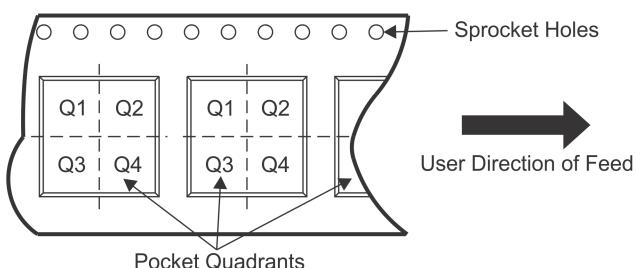


## TAPE DIMENSIONS



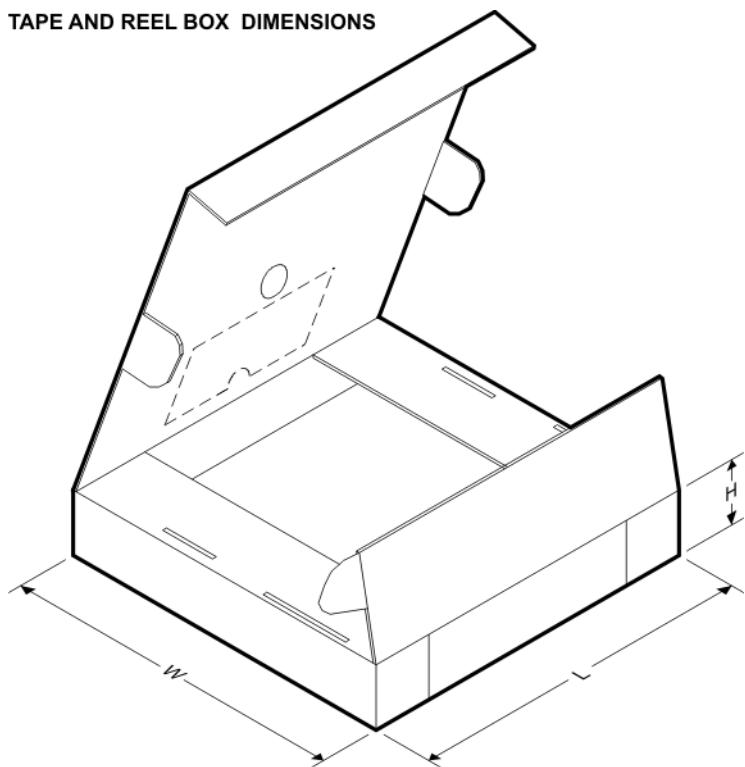
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



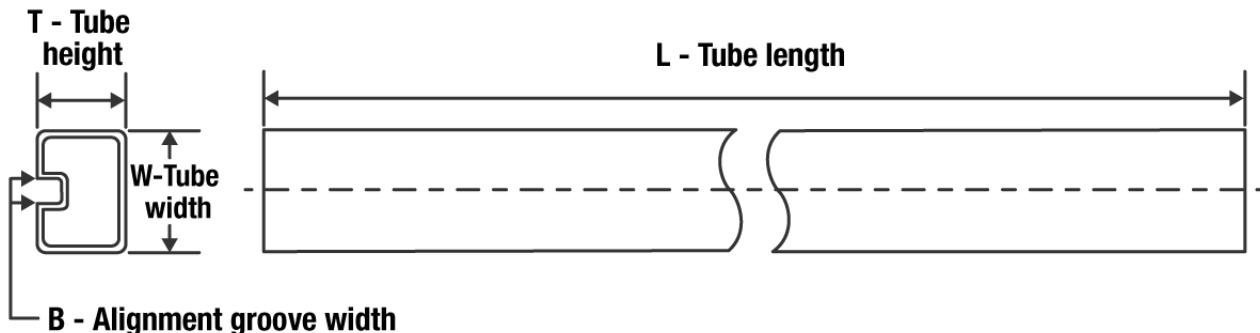
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC245NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC245DBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74AHC245DGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
SN74AHC245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC245NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHC245PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74AHC245PWR	TSSOP	PW	20	2000	853.0	449.0	35.0
SN74AHC245PWRG4	TSSOP	PW	20	2000	853.0	449.0	35.0

**TUBE**


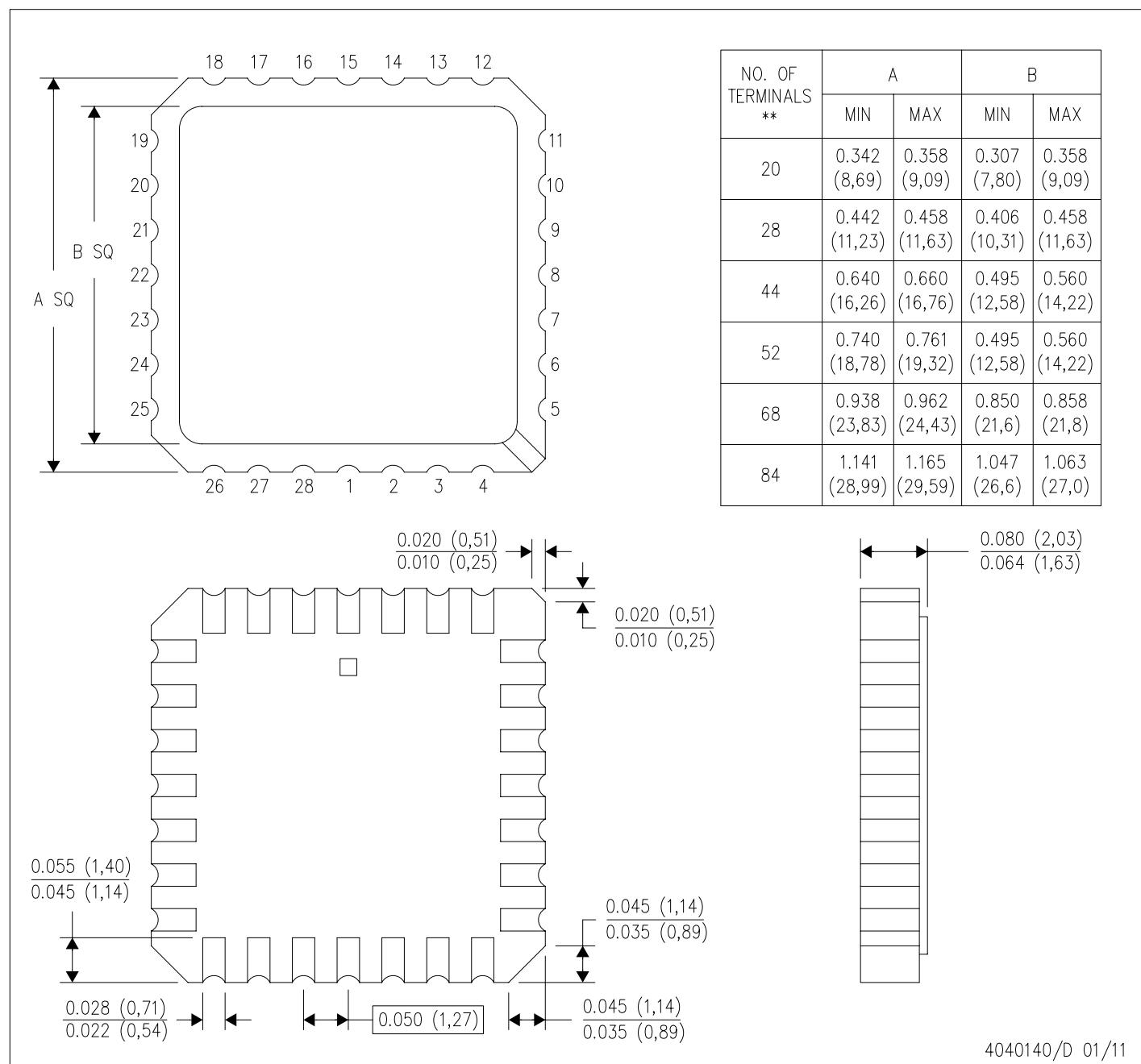
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9681801Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9681801VSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AHC245DWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74AHC245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC245PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54AHC245FK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a metal lid.
- Falls within JEDEC MS-004

4040140/D 01/11

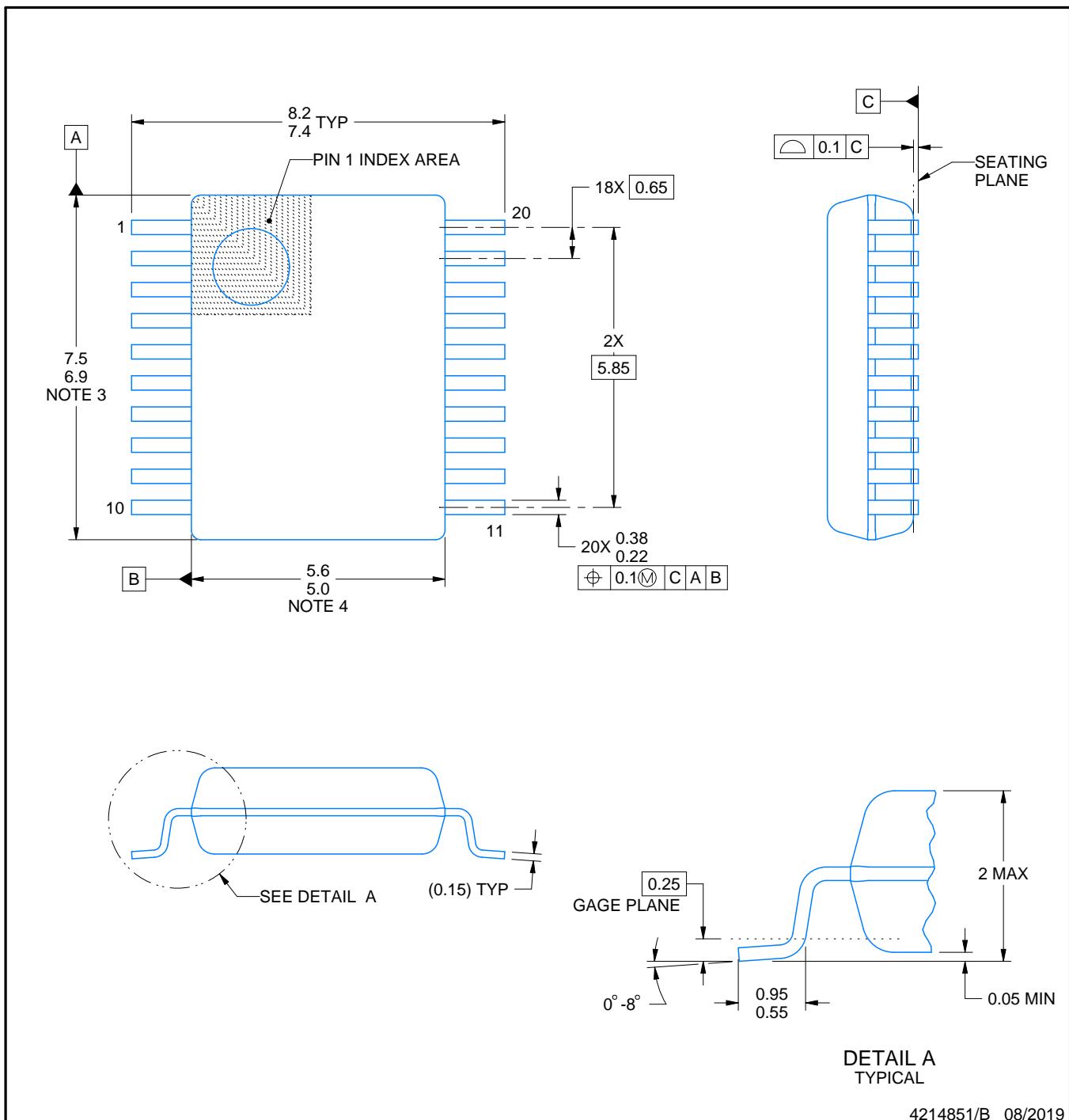
# PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

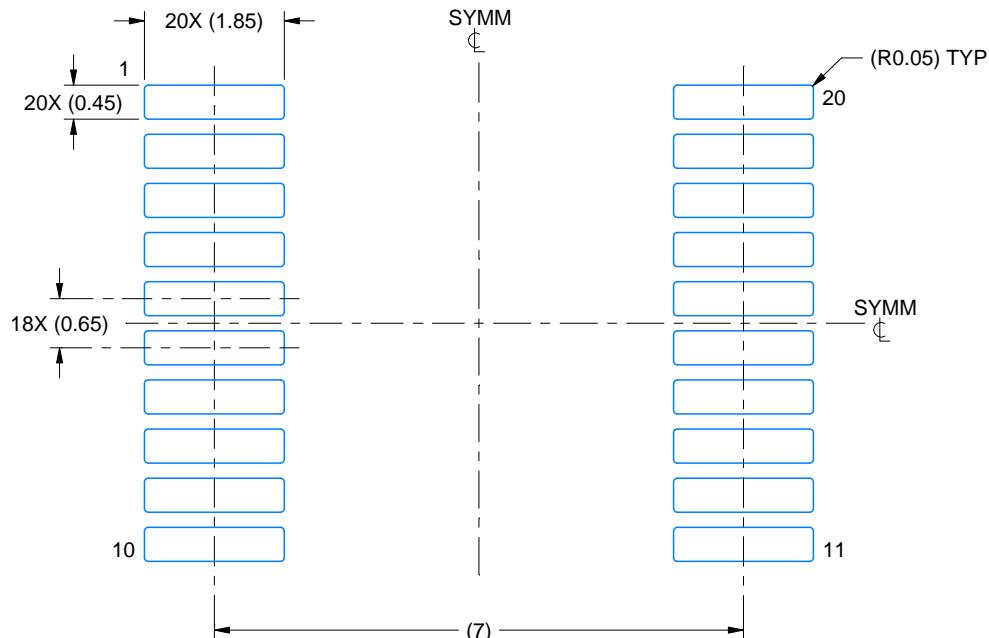
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

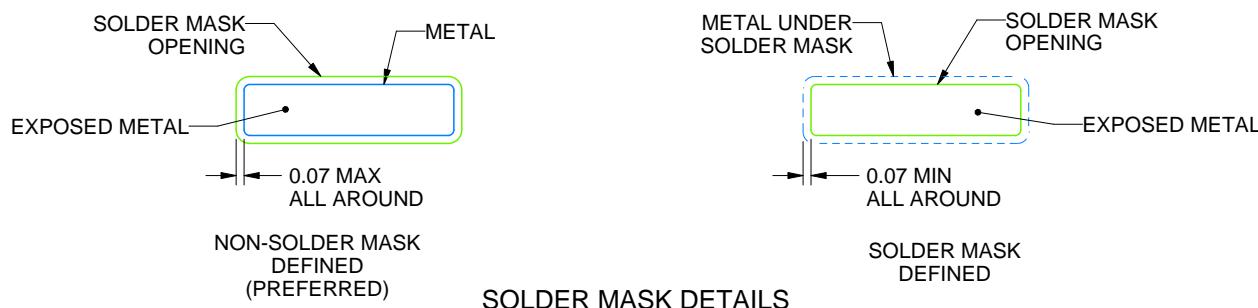
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

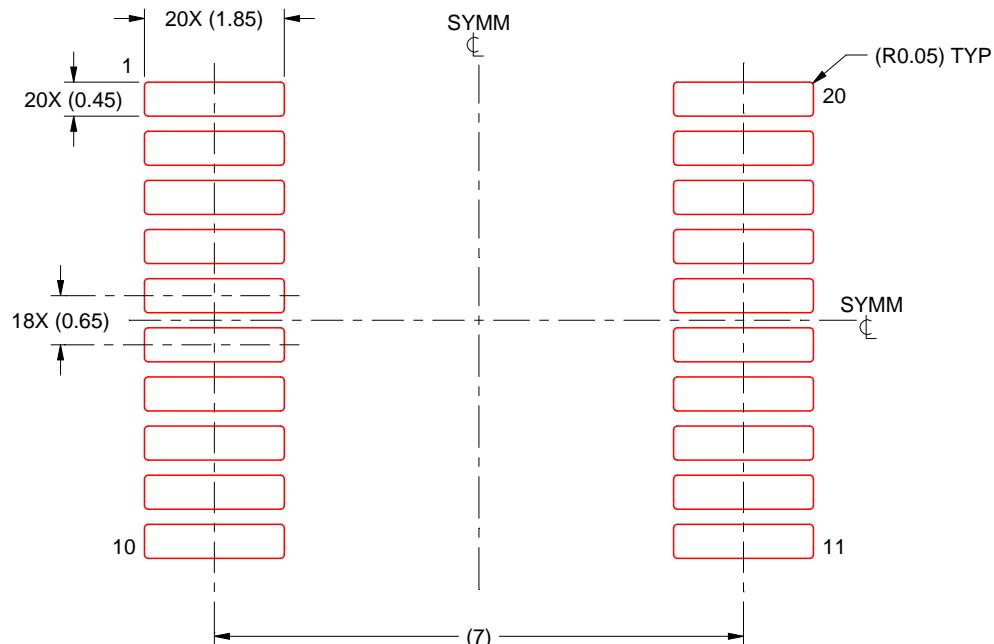
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

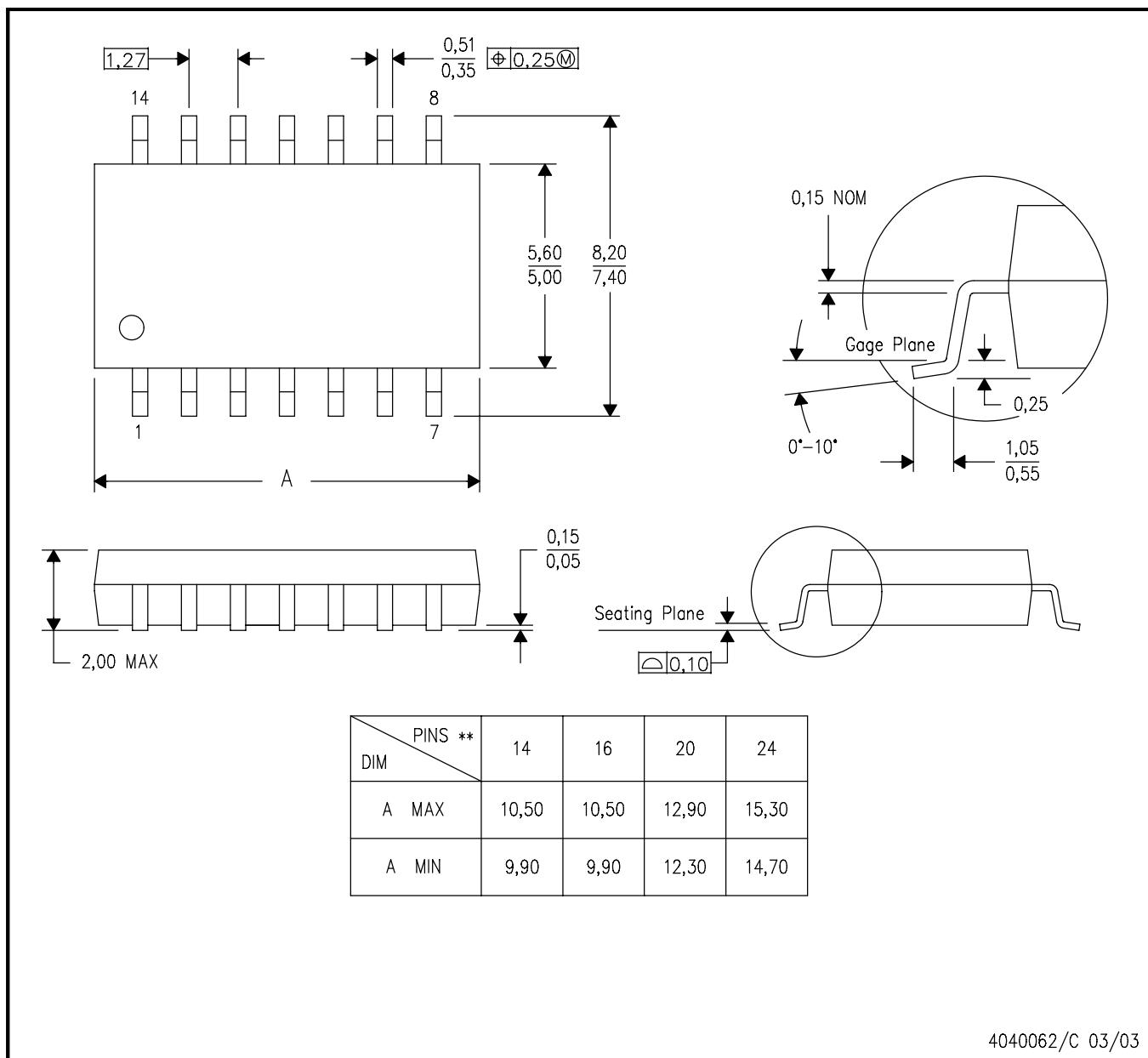
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



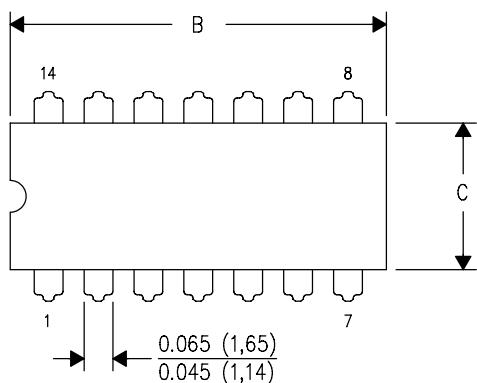
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

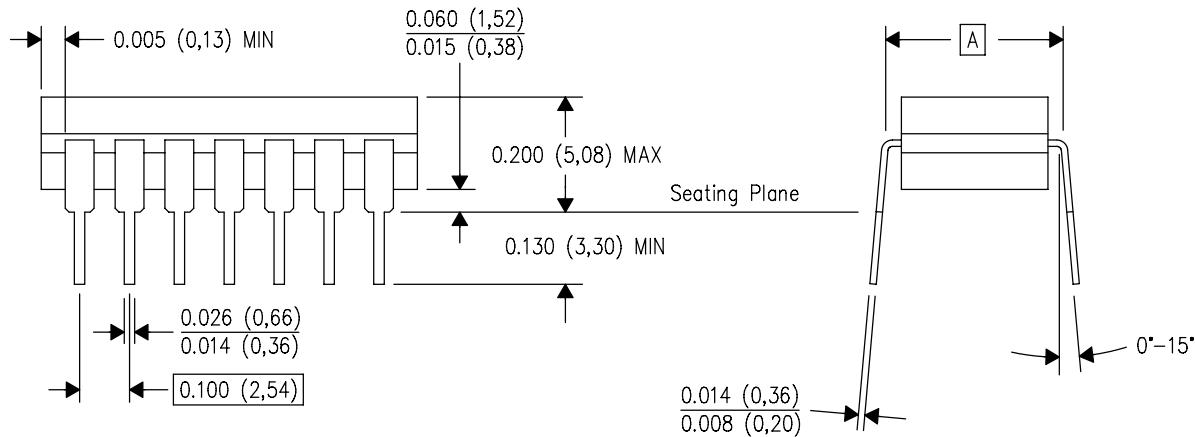
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

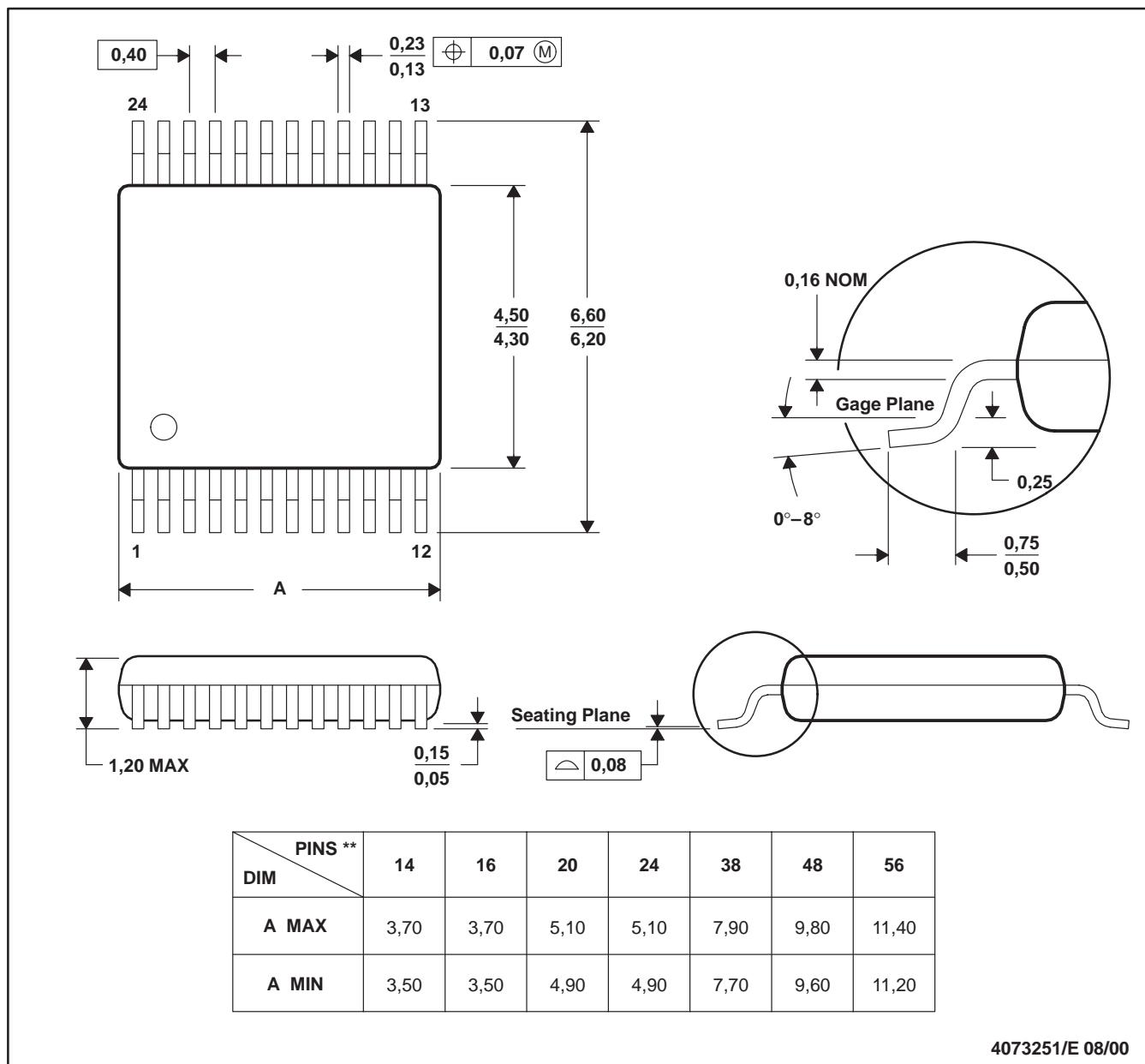
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN

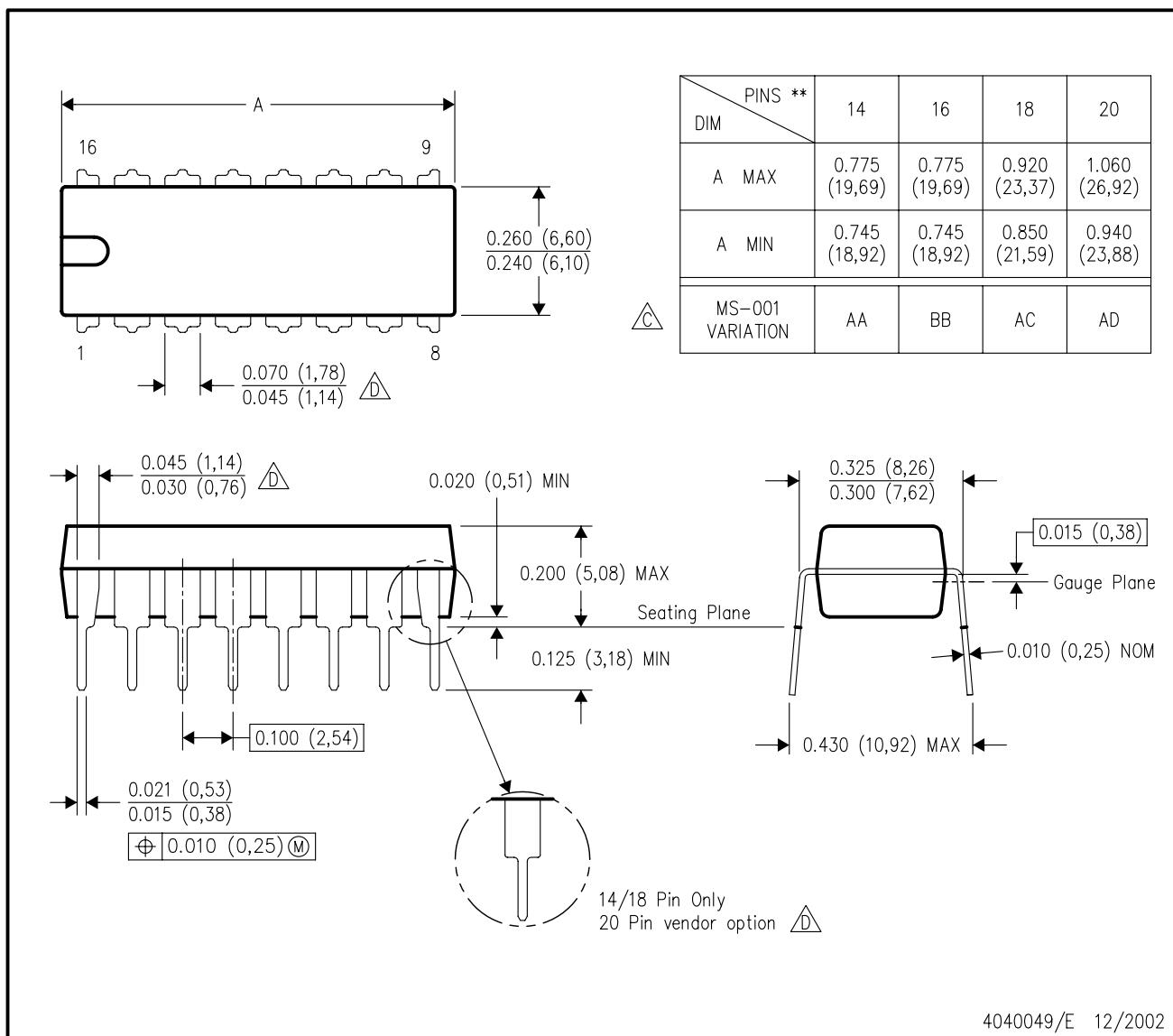


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

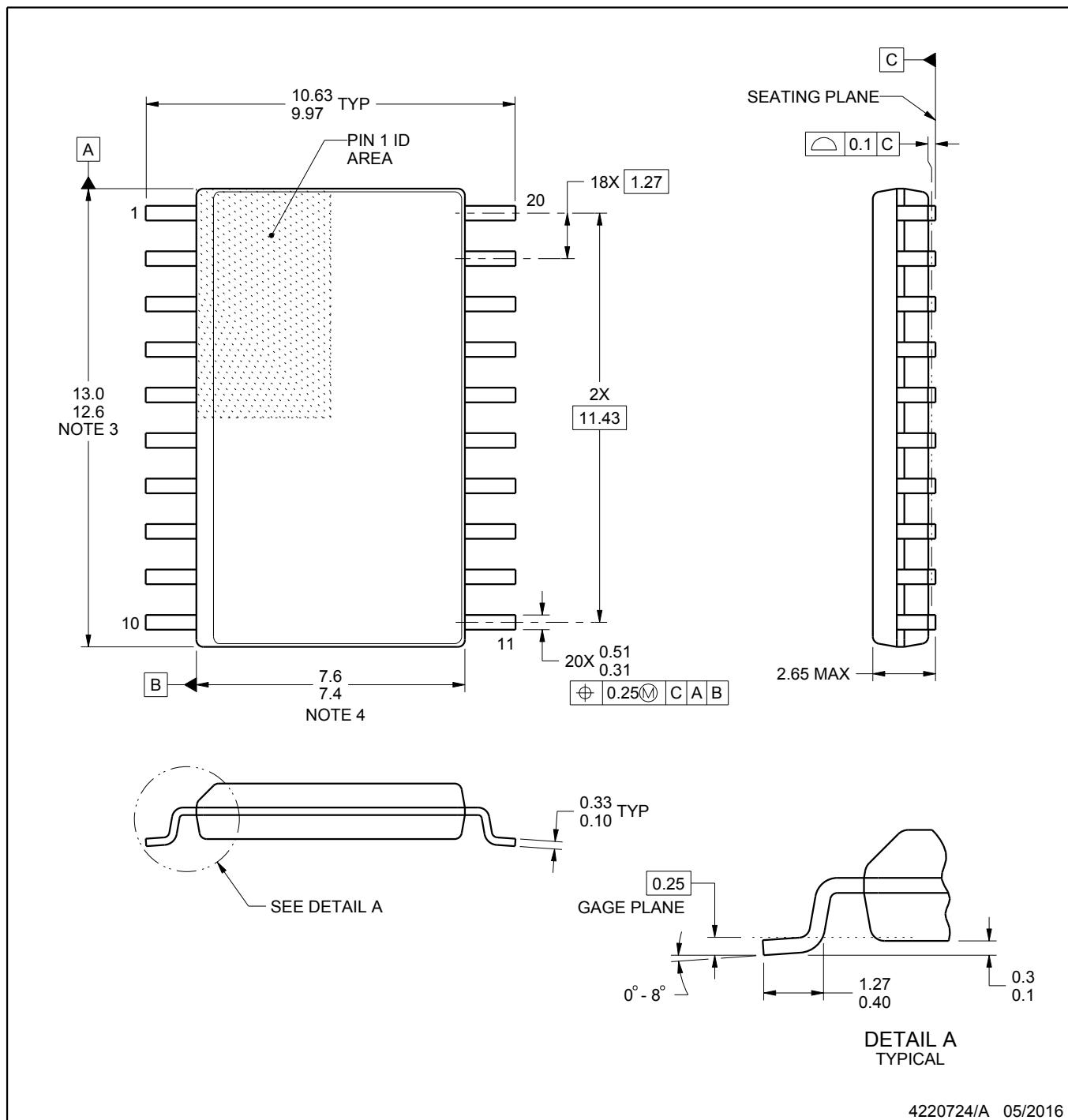


## PACKAGE OUTLINE

**DW0020A**

## **SOIC - 2.65 mm max height**

SOIC



## NOTES:

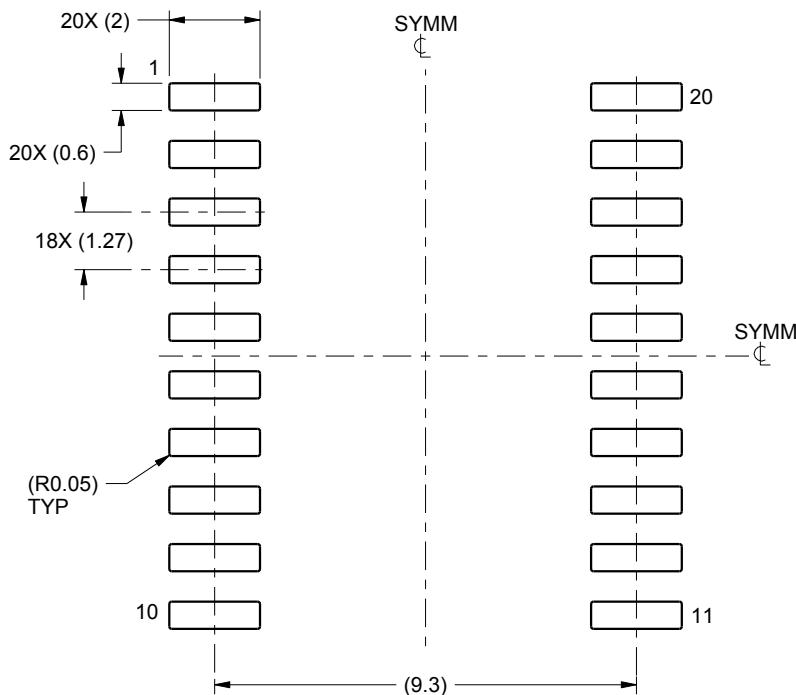
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

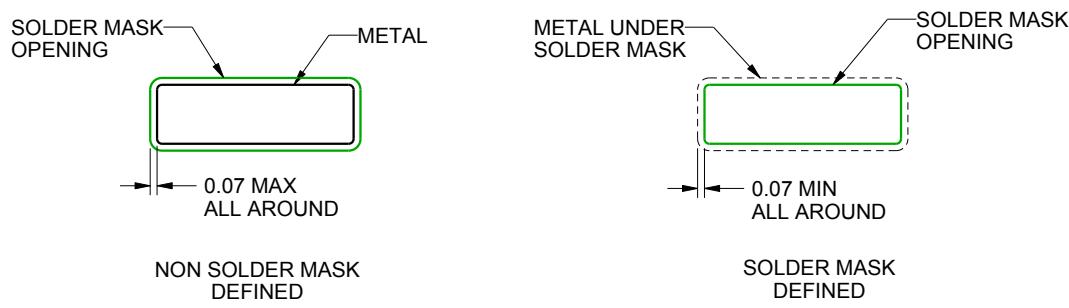
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

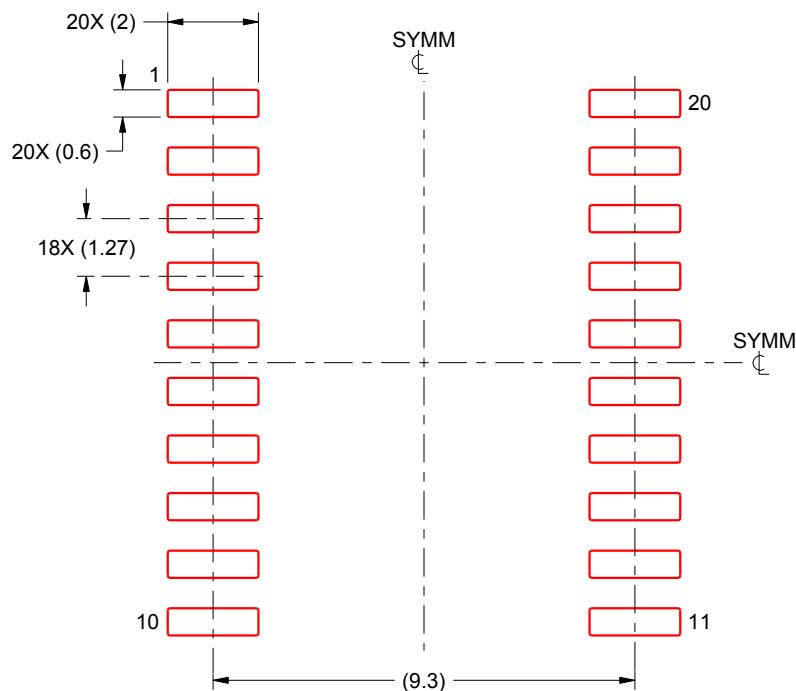
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

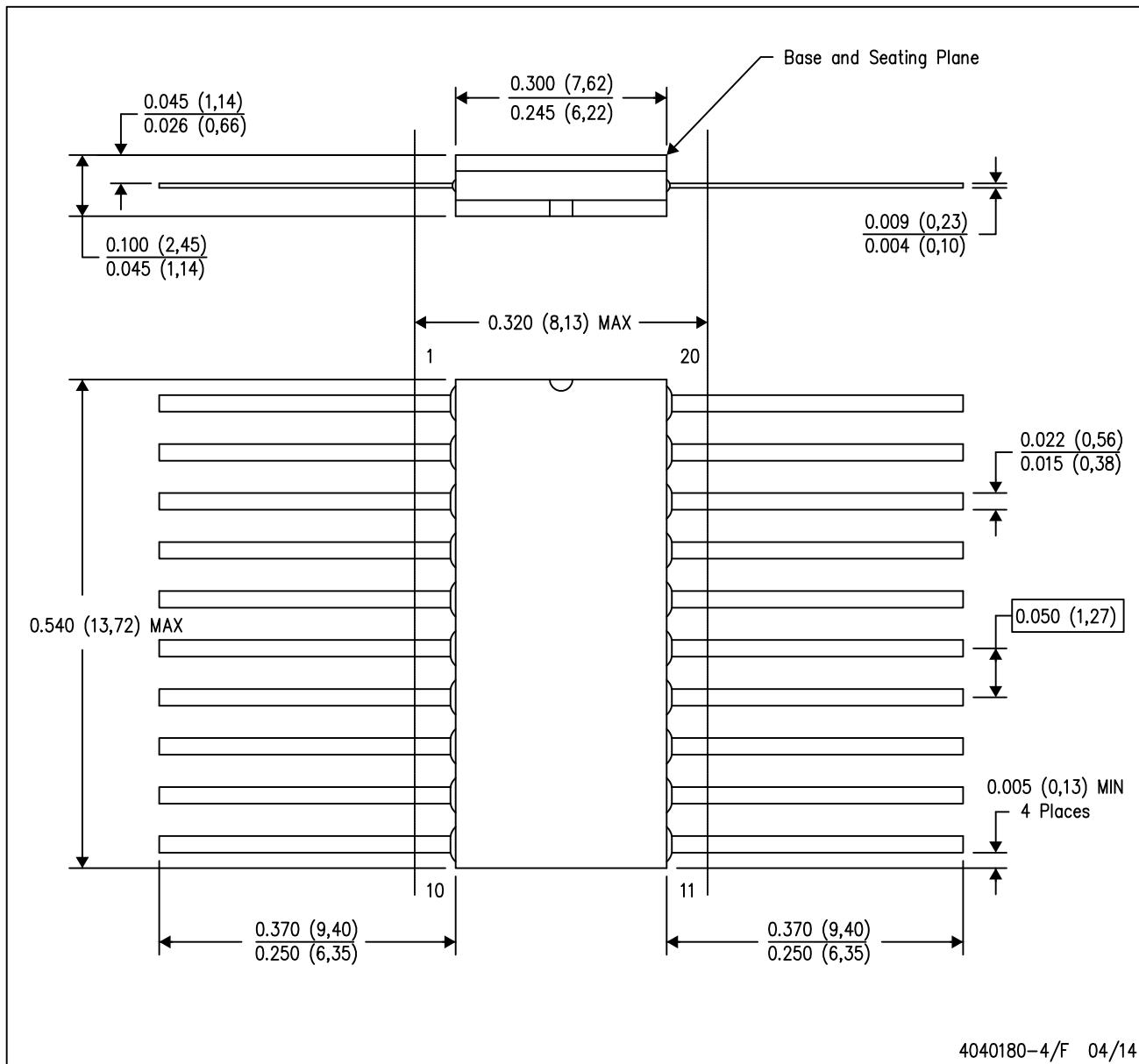
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

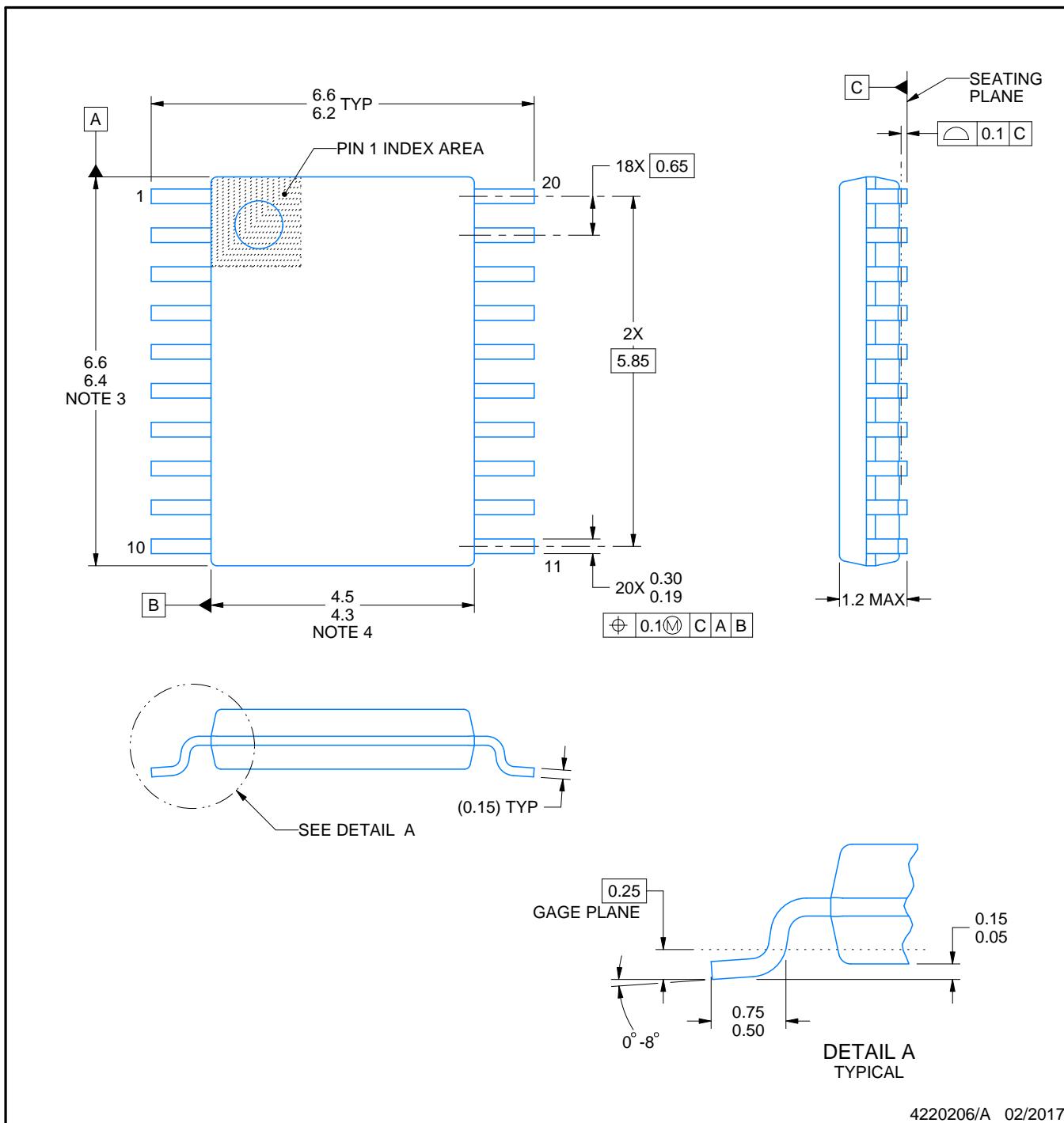
## PACKAGE OUTLINE

**PW0020A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

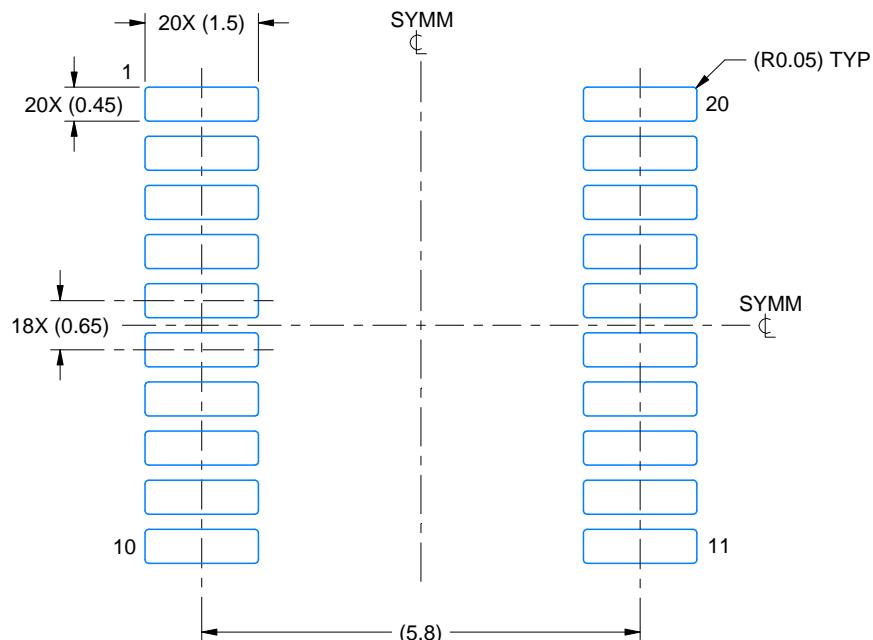
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

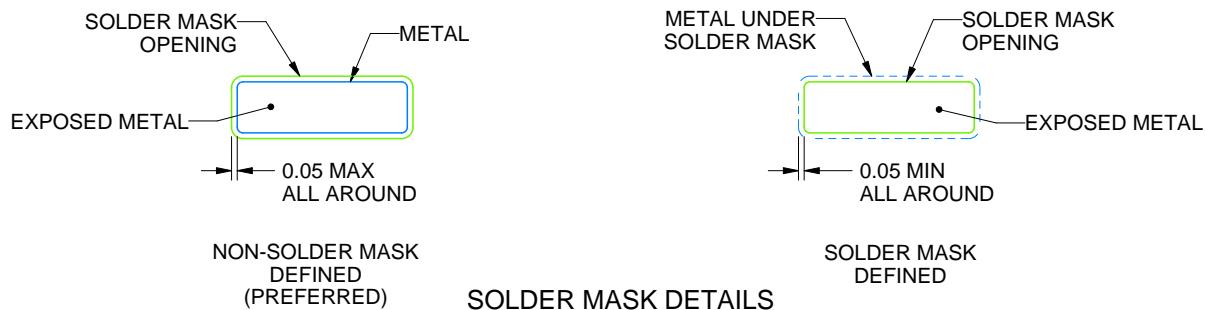
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

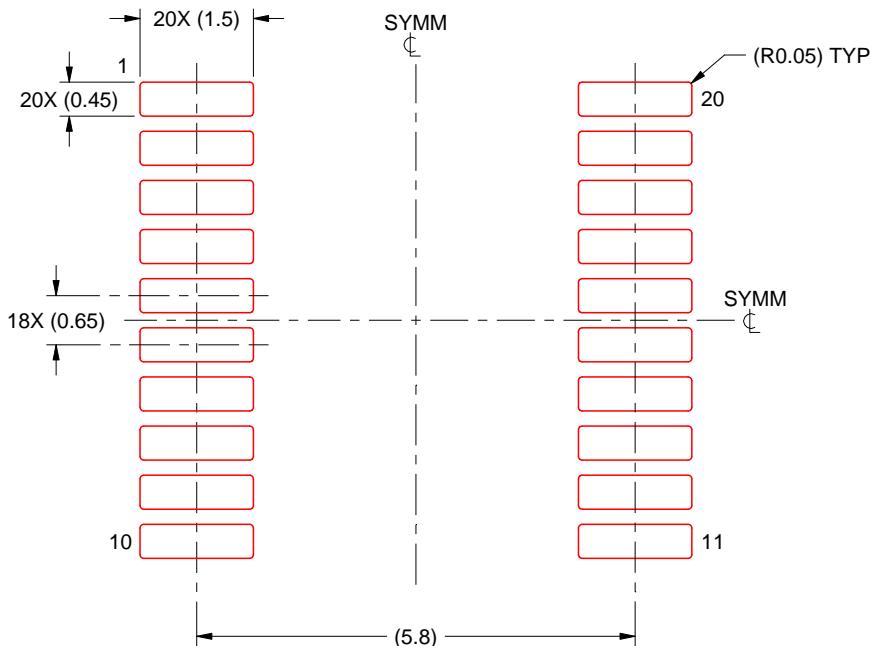
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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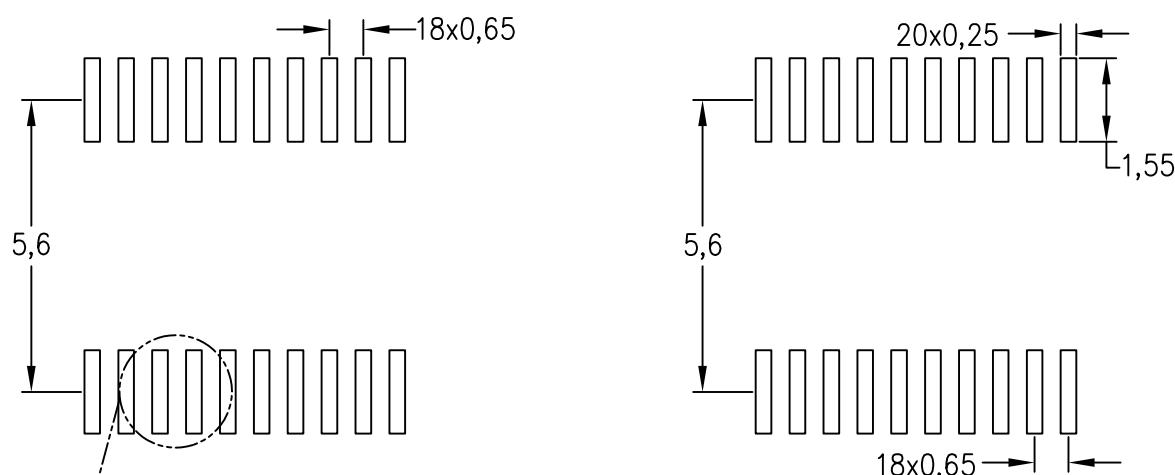
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).Example  
Non Soldermask Defined PadExample  
Solder Mask Opening  
(See Note E)

Pad Geometry

0,3  
1,6  
0,07  
All Around

4211284-5/G 08/15

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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