2ED4820-EM EB2 2HSV48

About this document

Scope and purpose

This document describes how to use the evaluation board 2ED4820-EM EB2 2HSV48.

Intended audience

Engineers who want to evaluate the capabilities of the 2ED4820-EM 48V high side gate driver in an easy and flexible way, at medium current levels (up to 20A DC).

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1 Introduction to the 2ED4820-EM EB2 2HSV48

1.1 Overview

The 2ED4820-EM EB2 2HSV48 from Infineon Technologies is a flexible evaluation board designed to showcase the capabilities of the 2ED4820-EM. This board includes Infineon's XMC1100 XMC2Go daughter board to interface to a PC over a USB cable.
A graphical user interface (GUI), called Config Wizard for 2ED4820 EB, is provided via Infineon Development center. It running on a Windows PC, to control, configure and diagnoze the 2ED4820-EM.

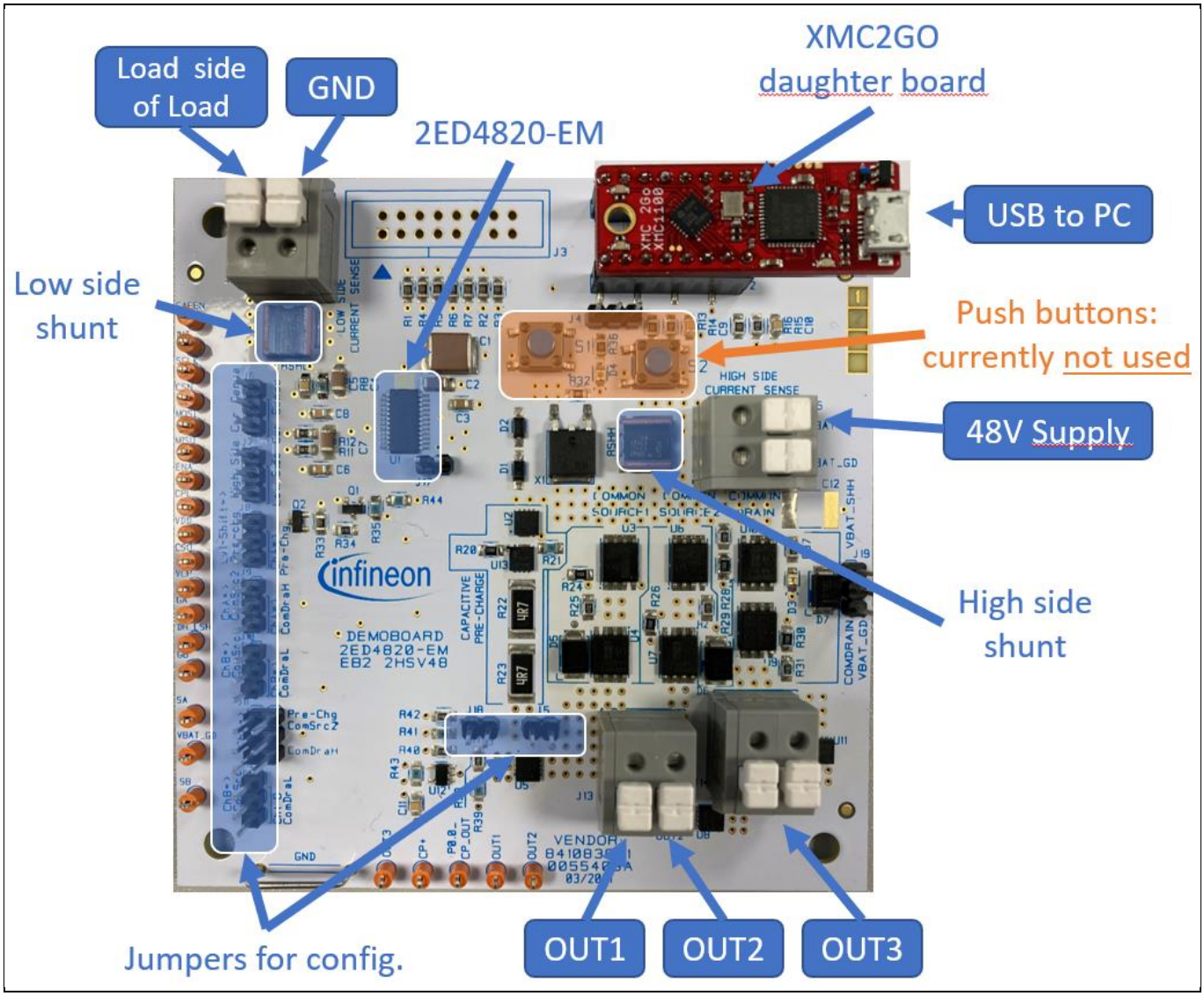


Figure 1 Board overview

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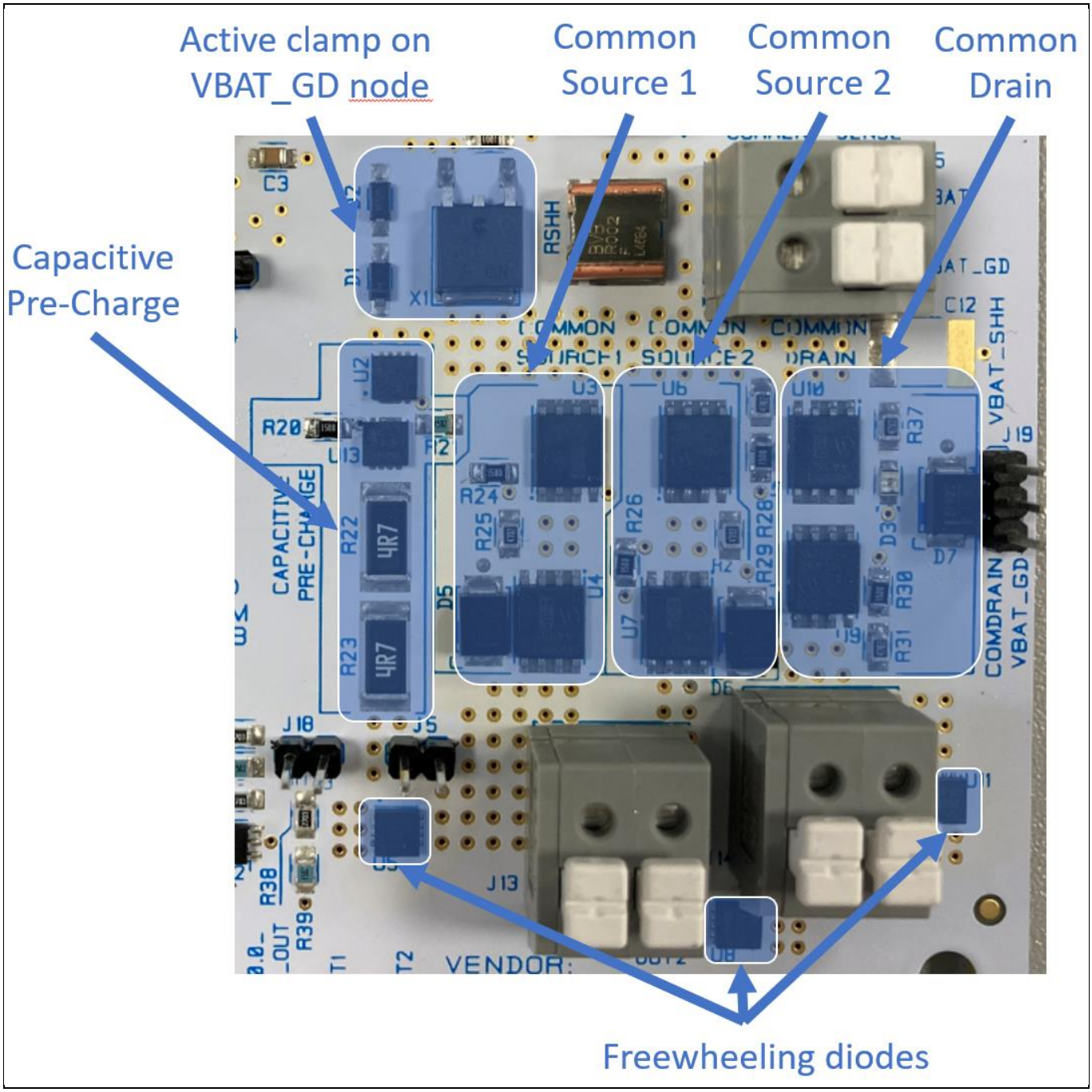


Figure 2 Power section overview

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1.2 Key features

- The evaluation board is able to deliver a continuous DC current up to 20A per channel

It comes with a jumper-based configurability, to test various topologies.

Warning: make sure to completely configure the jumpers before turning ON the power supply!!

The various configurations include:

- Power MOSFETs configured either in common drain or common source topologies
- High side or low side current sense
- Optional capacitor pre-charge resistive channel, driven either by one channel of the 2ED4820-EM or by a discrete level shifter supplied by the charge-pump of 2ED4820-EM.

Warning: the power resistors (R22 and R23) are sized to pre-charge a capacitance of max 1mF (one millifarad).

- The board comes with any test points on the edges of the board to easily check signals with an oscilloscope.
- A USB interface (XMC2GO) is provided, to drive the SPI serial interface of 2ED4820-EM from a PC
- A graphical user interface running on a PC allows to control, configure and diagnose the 2ED4820-EM

1.2.1 Typical connection with a PC and a power supply (Common source + High side current sense)

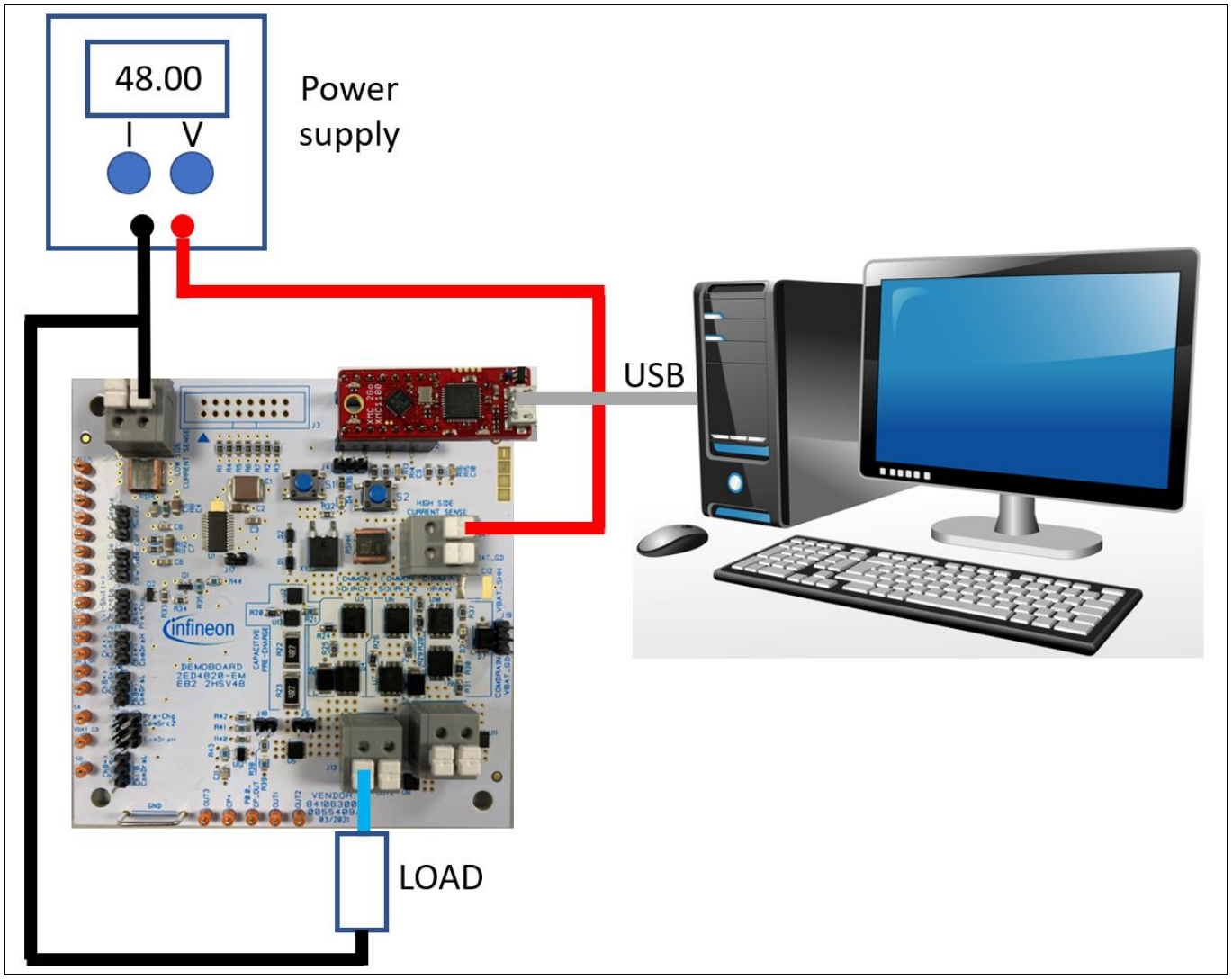


Figure 3 Conection with a PC and a power supply

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1.3 Mandatory jumpers

The 2ED4820-EM EB2 2HSV48 comes with two jumpers: J4 for supply selection and J17 for GND connection. Both jumpers have to be kept on the board for proper operation:

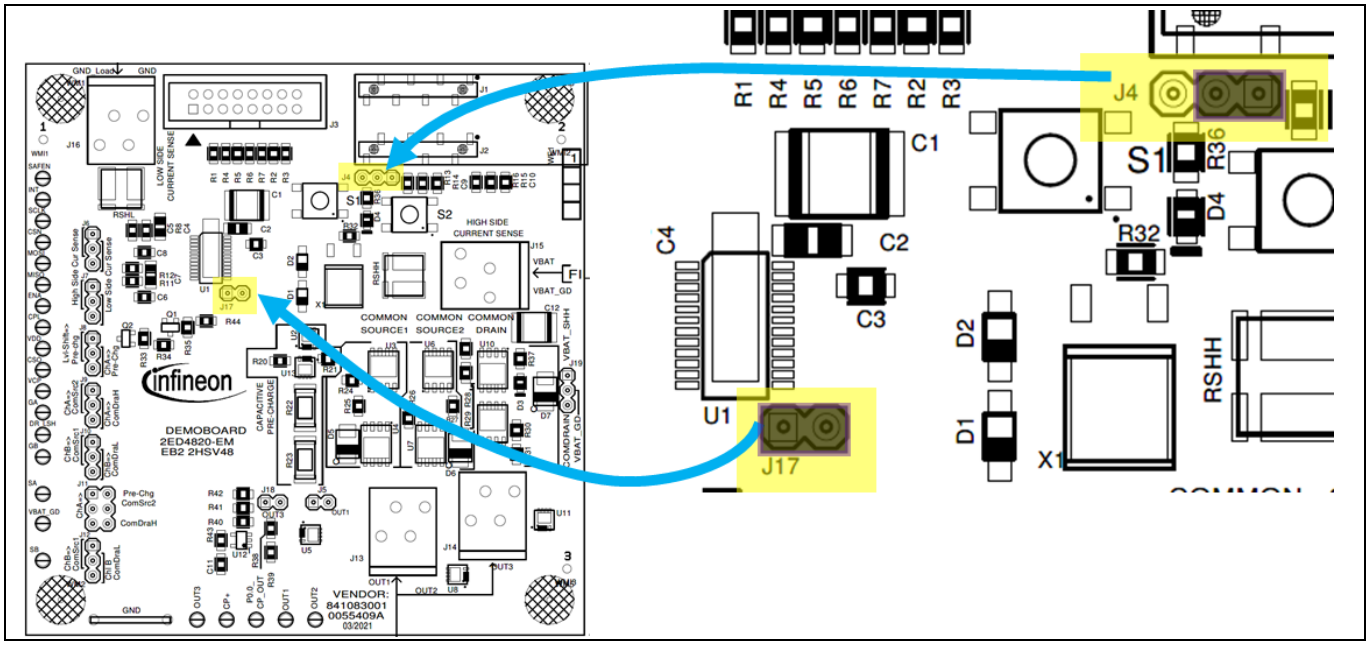


Figure 4 Mandatory jumpers.

1.4 Configuring the current sense position

1.4.1 Low side current sense:

This configuration is used to sense the current thanks to a low ohmic shunt connected to the ground node:

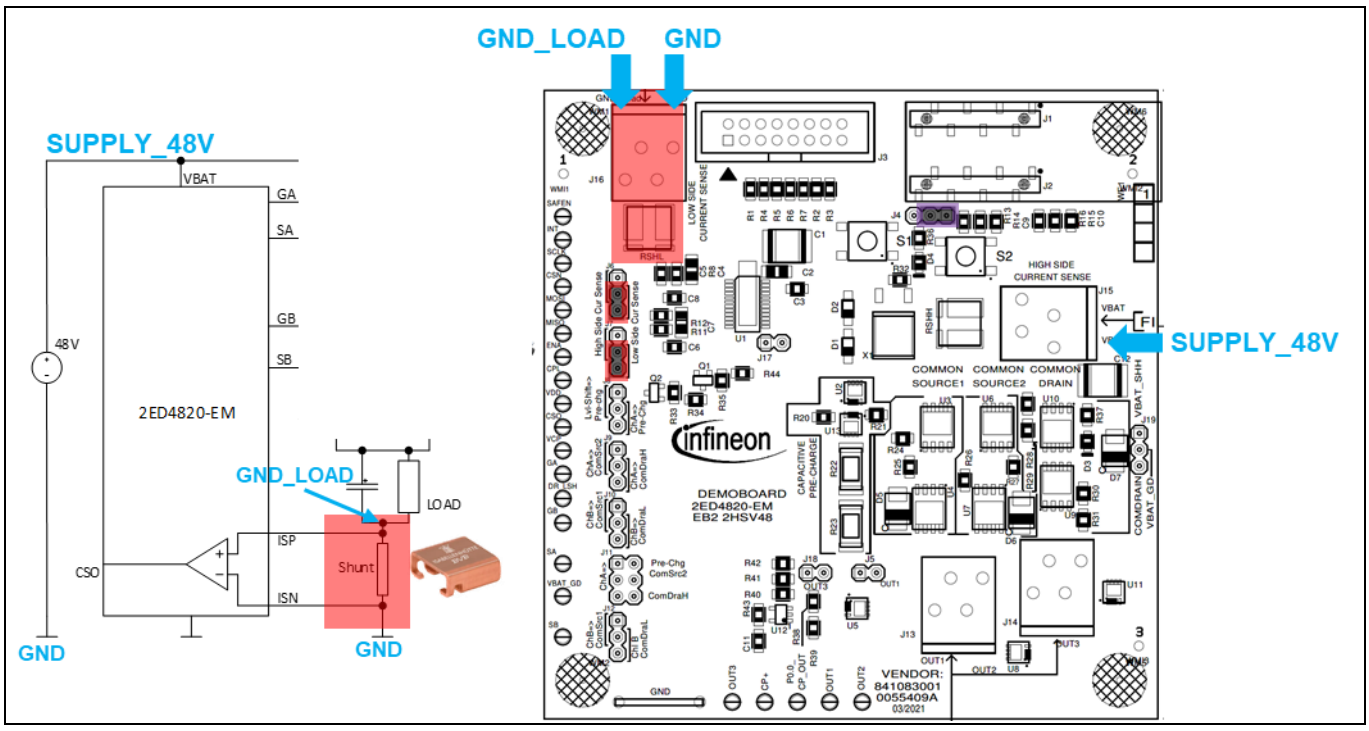


Figure 5 Configuration for low side current sense.

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1.4.2 High side current sense:

This configuration is used to sense the current thanks to a low ohmic shunt connected to the supply node:

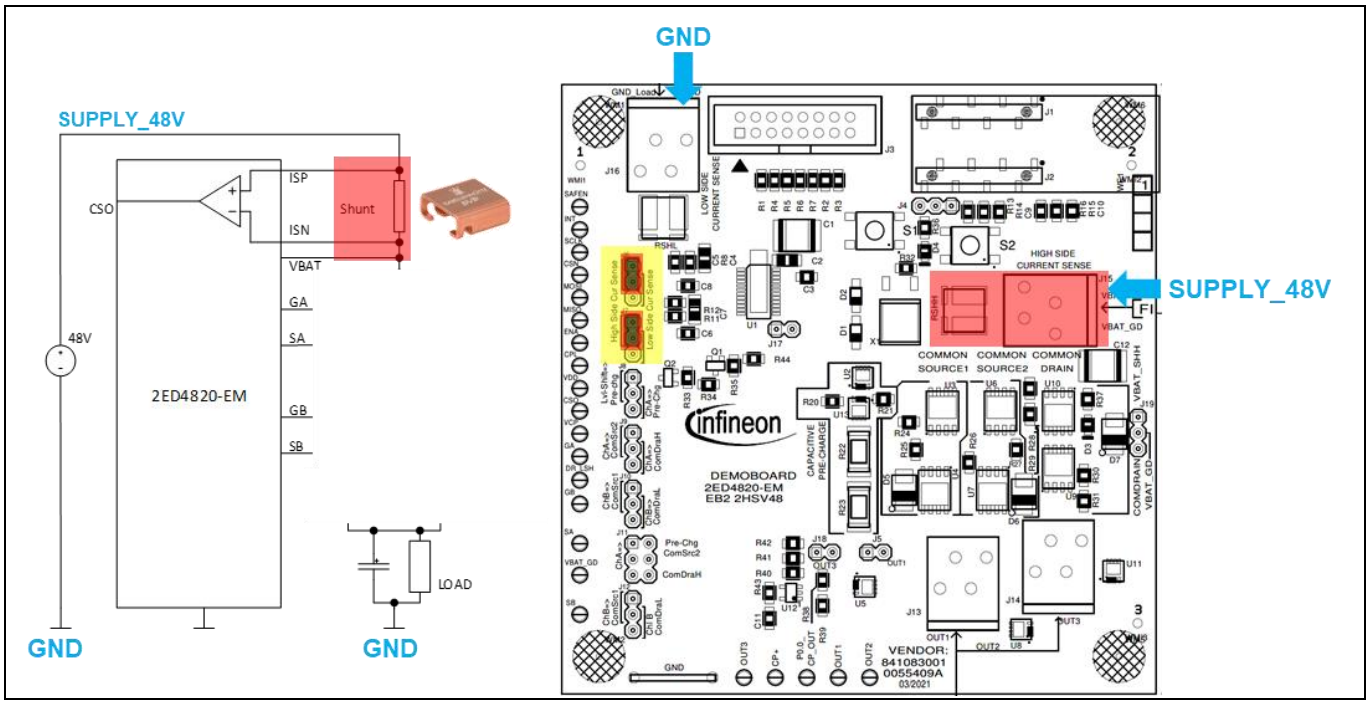


Figure 6 Configuration for low side current sense.

1.5 Overview of the power configurations which can be tested

There are at least three different power configurations which can be tested.

1.5.1 Common drain power configuration (1 single load):

- Channel A drives the high side MOS of low-ohmic path on **OUT3**
- Channel B drives the low side MOS of low-ohmic path on **OUT3**
- Optional capacitive pre-charge with discrete level shifter, connected thanks to a jumper on **J8**

This configuration can be used either with low side (Config 1) or with high side current sense (Config 2):

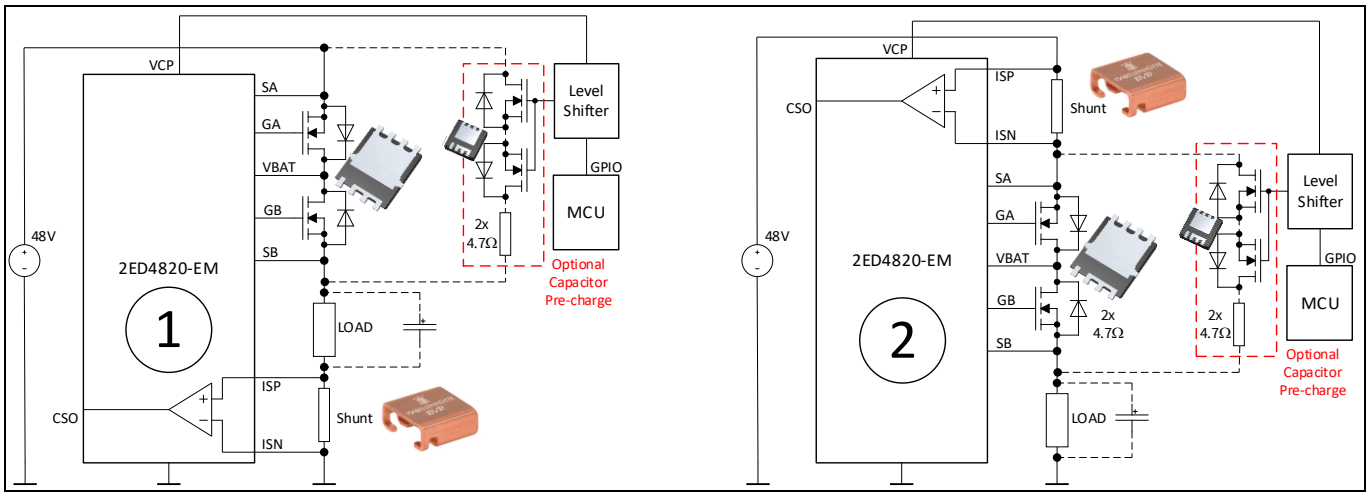


Figure 7 Common drain.

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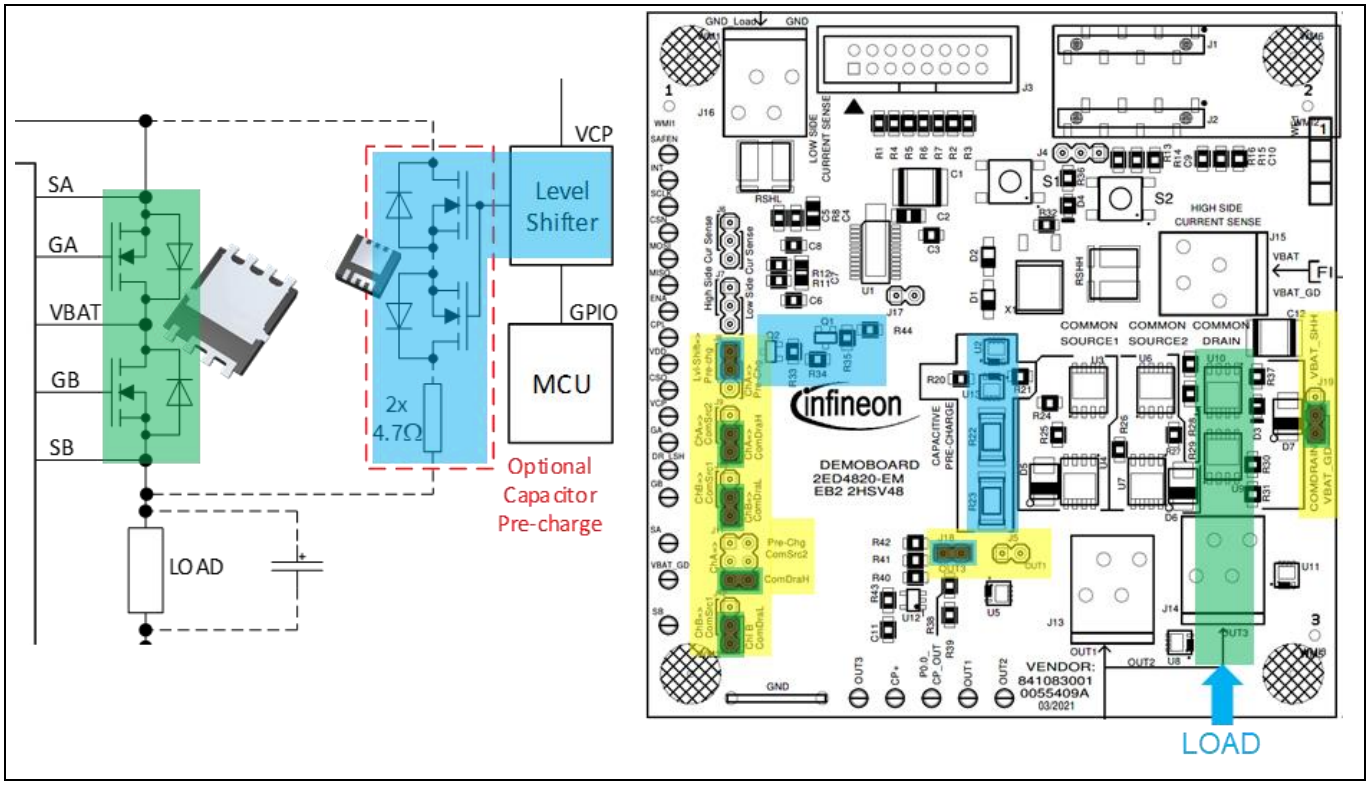


Figure 8 Configuring the jumpers & connecting the load.

1.5.2 Common source power configuration, 1 single load:

- Channel A drives the ohmic path to pre-charge capacitor(s), connected thanks to a jumper on **J7**
- Channel B drives the low-ohmic path on **OUT1**

This configuration can be used either with Low Side (Config 3) or with High Side current sense (Config 4):

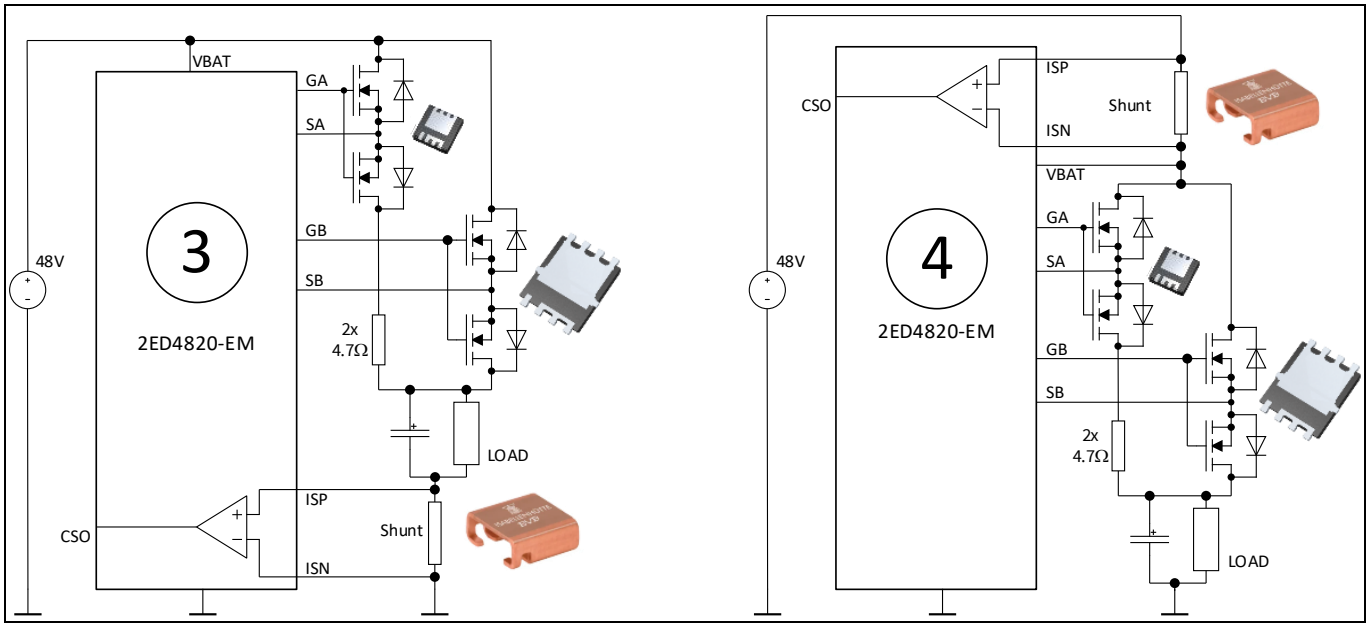


Figure 9 Common source, 1 single load.

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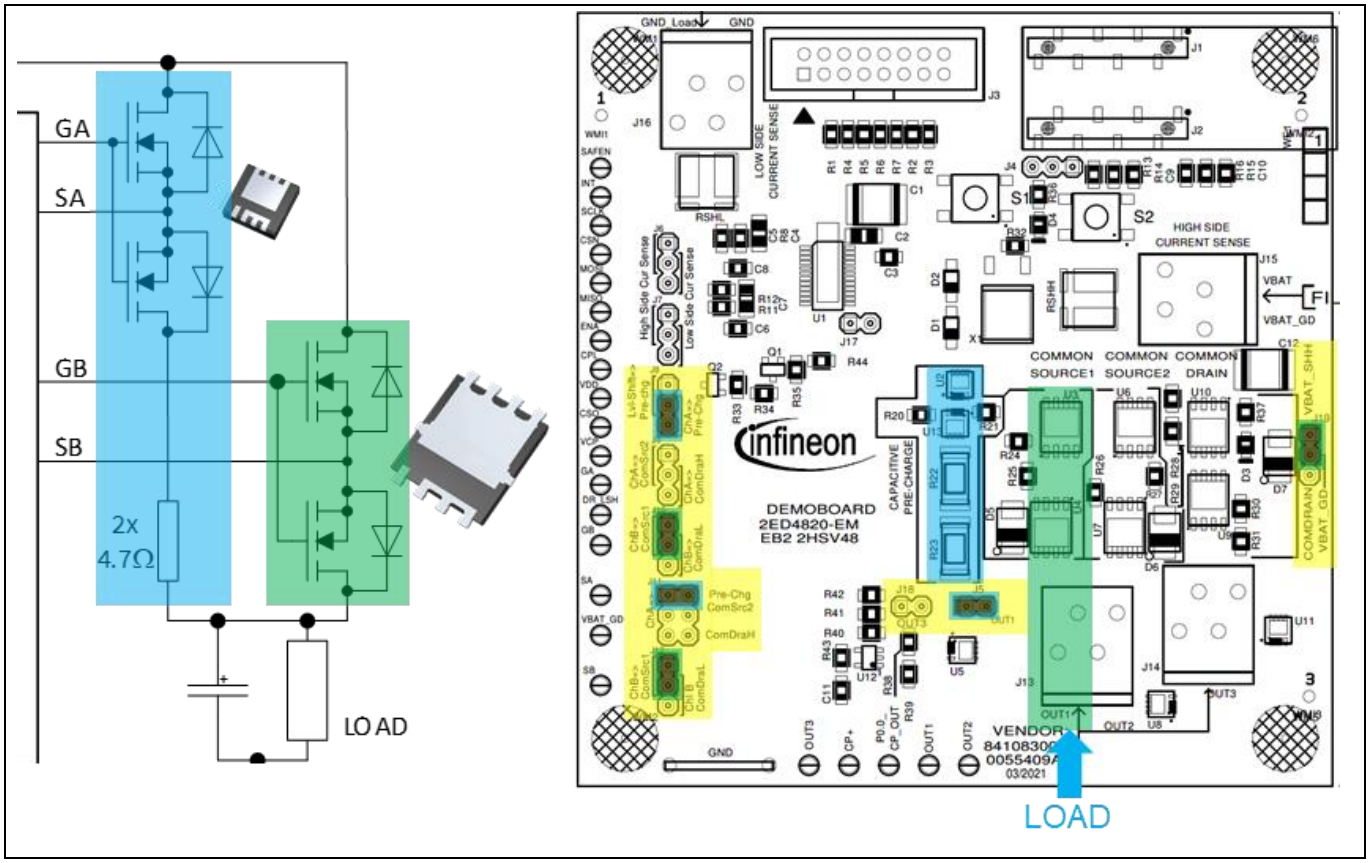


Figure 10 Configuring the jumpers & connecting the load.

1.5.3 Common source power configuration, 2 loads:

- Channel A drives the low-ohmic path on **OUT2**
- Channel B drives the low-ohmic path on **OUT1**
- Optional capacitive pre-charge with discrete level shifter, connected thanks to a jumper on **J8**

This configuration can be used either with Low Side (Config 5) or with High Side current sense (Config 6)

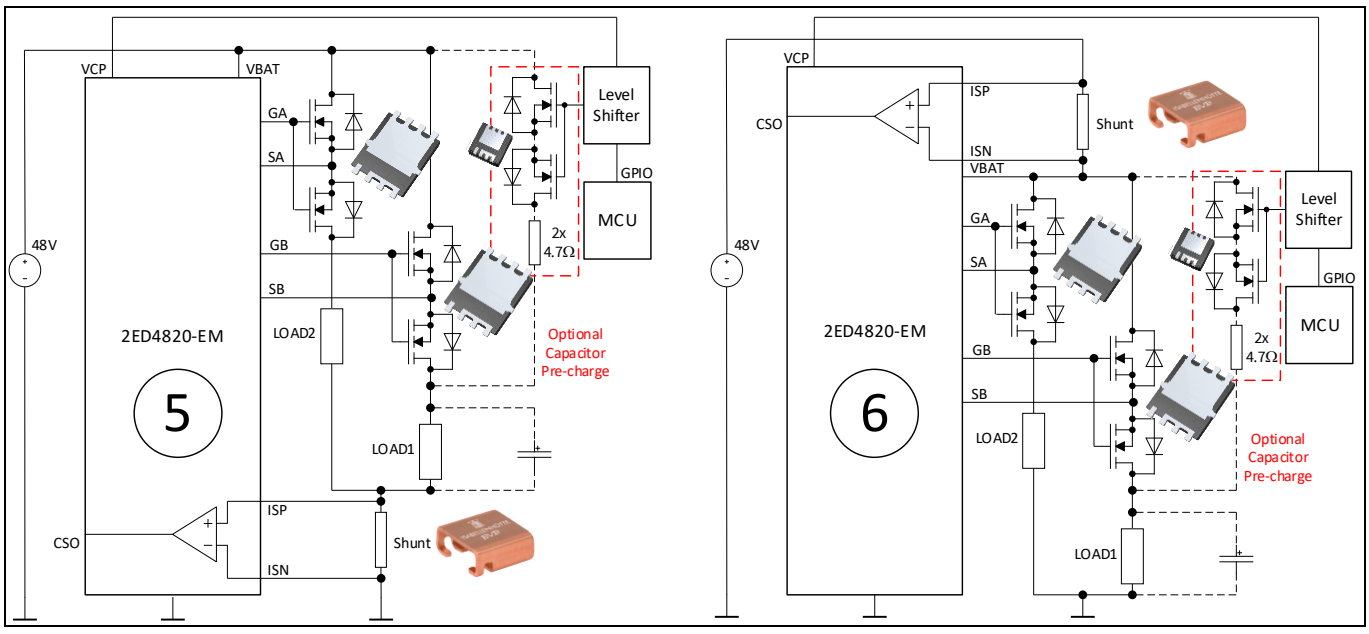


Figure 11 Common source, 2 loads.

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Introduction to the 2ED4820-EM EB2 2HSV48

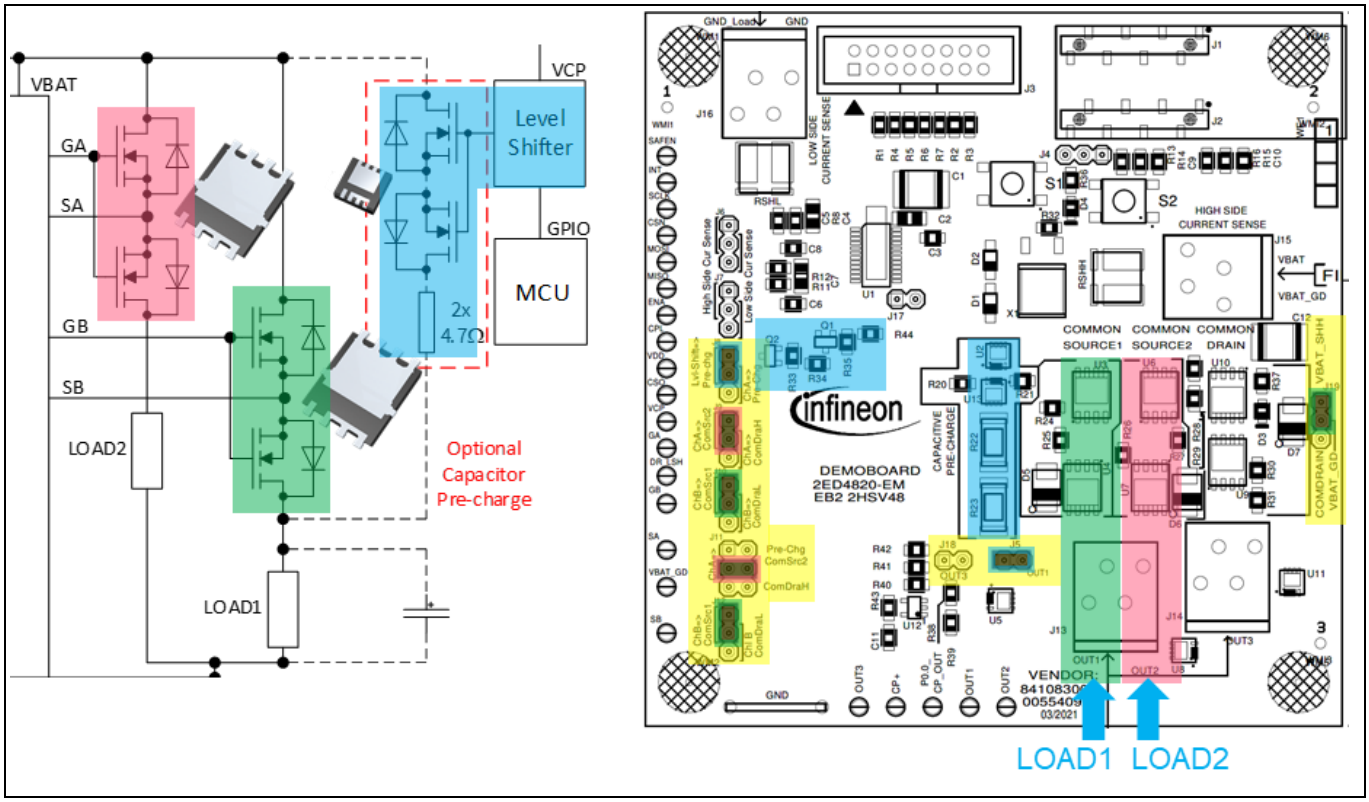


Figure 12 Configuring the jumpers & connecting the load.

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1.6 Level shifter and end-of-charge detector

The 2ED4820-EM 2HSV48 EB comes with two features external to 2ED4820-EM:

1. **High voltage level shifter**, to optionally drive the resistive path for capacitor pre-charge either from an MCU GPIO (**P0.14_LSh**) or from an external waveform generator (using **TP23**)

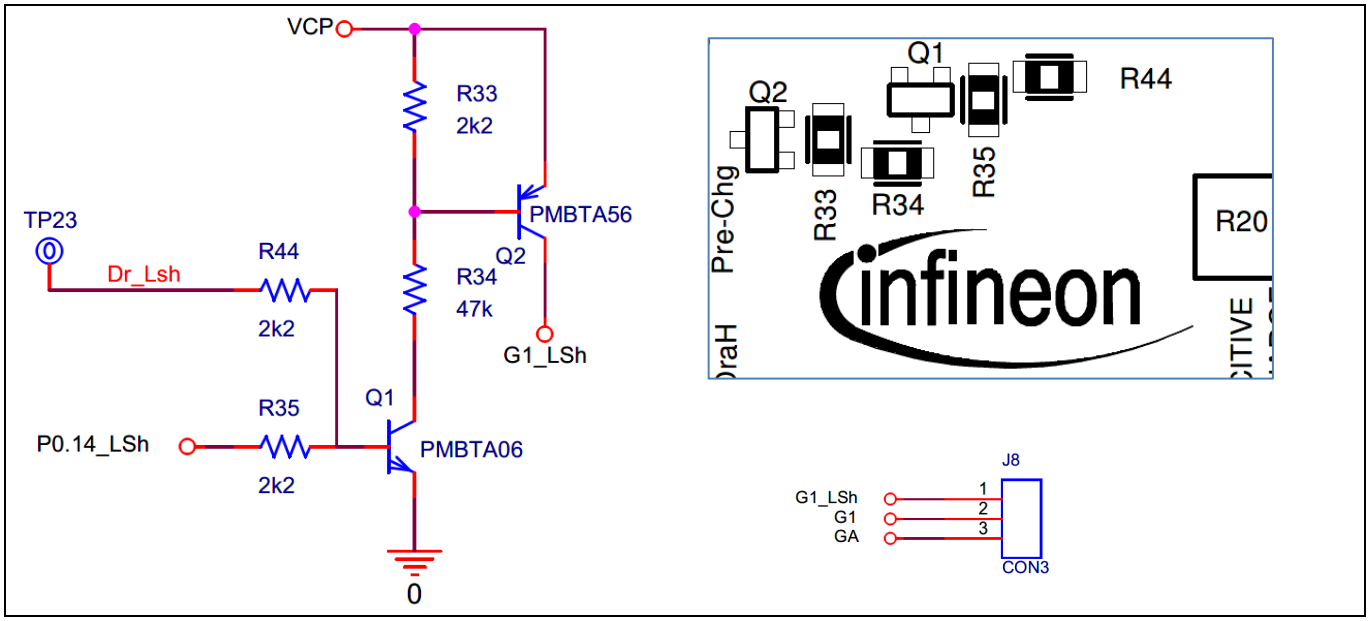


Figure 13 High voltage level shifter.

The level shifter is powered from the Charge pump (**VCP**) in 2ED4820-EM, which generates a supply 15V above the 48V supply connected to J15. The charge pump can deliver up to 10mA for such an external circuitry.

J8 allows to select how the resistive path made by U2, U13, R22 and R23 is driven:

- Using a jumper on pins 1 & 2, the level shifter drives the resistive path
- Using a jumper on pins 2 & 3, 2ED4820-EM drives the resistive path from channel A (GA pin)

J11 also has to be configured properly, to connect the SA pin of 2ED4820-EM when it is driving the resistive path: put the jumper on pins 1 & 2.

2. **End-of-charge detector**, based on a comparator, to detect when the capacitor(s) are sufficiently charged to switch ON the low-ohmic path.

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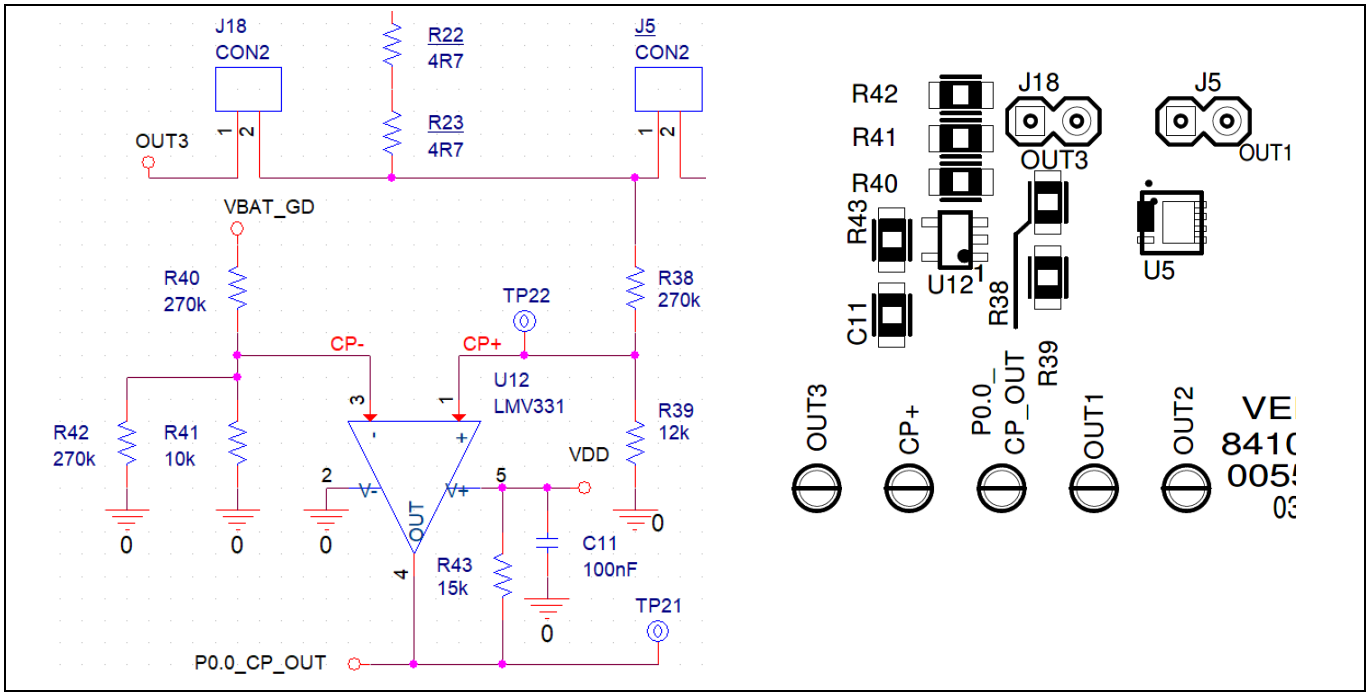


Figure 14 End of charge detector.

The voltage out of the resistive path, which is charging the capacitor, is compared to a reference voltage generated from the supply voltage supplying the board.

- R38 & R39 divide the voltage on the capacitor: CP+ is biased to 12/(270+12) = 4.255 % of OUT1 voltage.
- R40, R41 & R42 divide the voltage of the supply: R41 // R42 is : (10*270)/(10+270) = 9.64 kΩ, so CP- is biased to (9.64) / (270+9.64) = 3.448 % of the supply voltage applied on VBAT_GD.

The comparator output is triggered when CP+ = CP-, which means:
[4.25 % x V(OUT1)] = [3.448 % x V(VBAT_GD)] → V(OUT1) = 0.03448/0.04255 x V(VBAT_GD)

→ V(OUT1) = 81% V(VBAT_GD).

The comparator output is triggered when the voltage on the capacitor has reached 81 % of the supply rail.

The value of R42 can be modified to change this percentage if required:

Table 1 Percentage of VBAT_GD for which the comparator triggers

Value of R42 (kΩ)	**none**	**270**	**120**	**56**	**39**	**27**
Percentage of VBAT_GD	87 %	81 %	77.7 %	71.6 %	67.3 %	61.8 %

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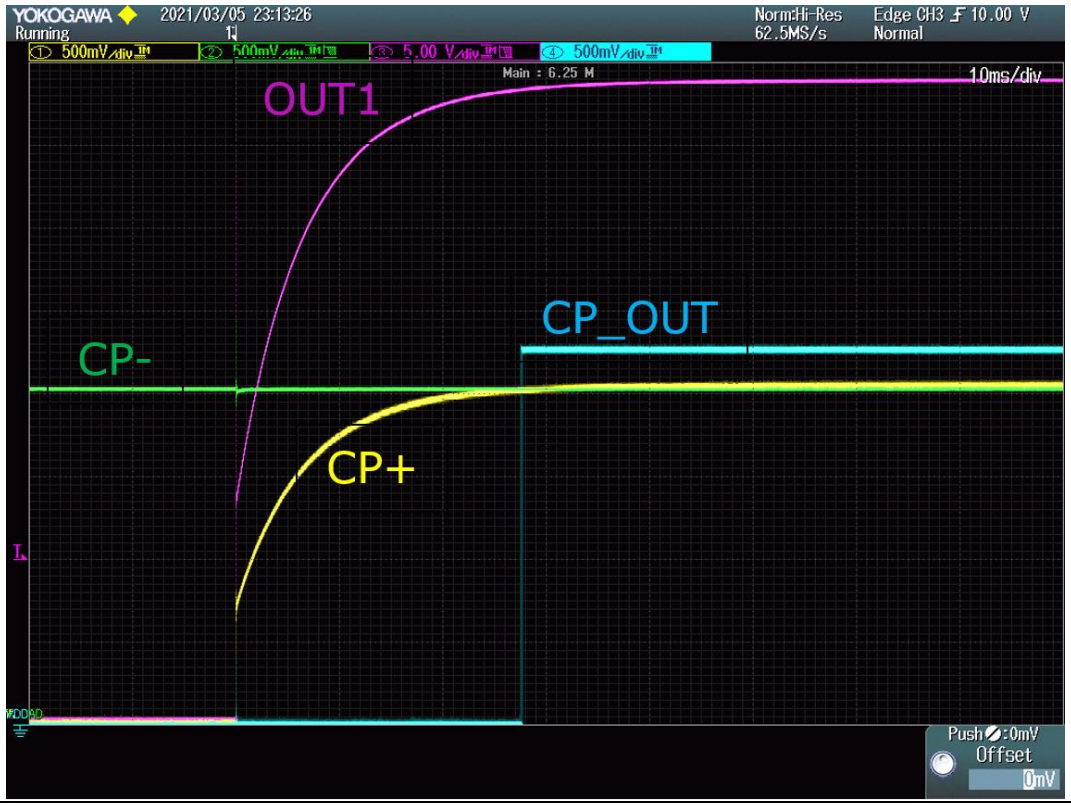


Figure 15 End of charge detector: scope capture.

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2 Software user manual

In order to interact with the SPI interface of the 2ED4820-EM, an XMC2Go daughter board is assembled on top of the EB2 2HSV48 board. A firmware has been developed for the XMC MCU to drive the 2ED4820-EM over SPI.

To enable easy testing, a Graphical User Interface has also been developed, which runs on a PC and interacts with the XMC2Go daughter board by sending/receiving messages over USB: **Config Wizard for 2ED4820 EB.**

2.1 Prerequiresites

2.1.1 Installing the Config Wizard for 2ED4820 EB

For your PC to interact with the XMC2Go over USB, install the **Infineon Developer Center launcher** from this link: Infineon Developer Center Launcher, using a web browser:

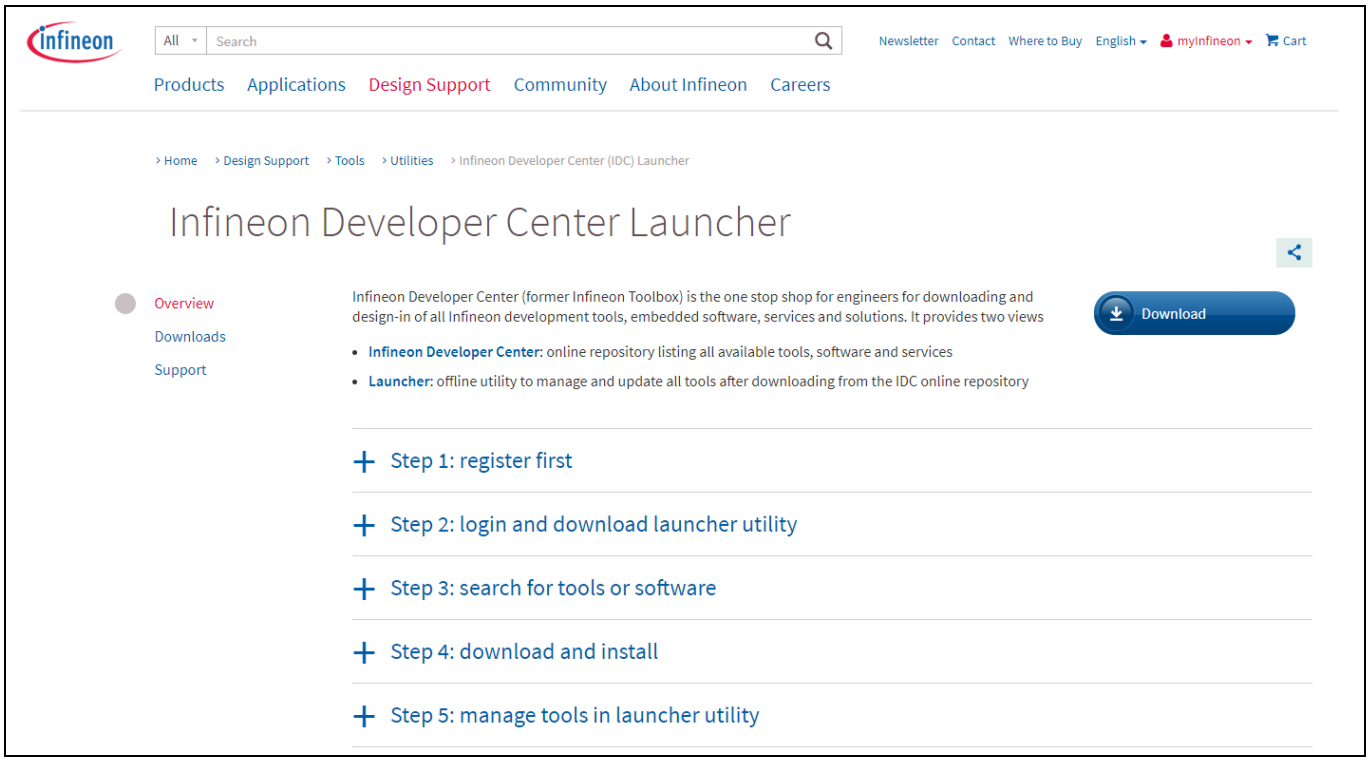


Figure 16 Installing the Infineon Developper Center.

Follow Step 1 + Step 2 to install the launcher.

In Step 3, search for the **Config Wizard for 2ED4820 EB** in the “Tools” menu, download and install it (Step 4):

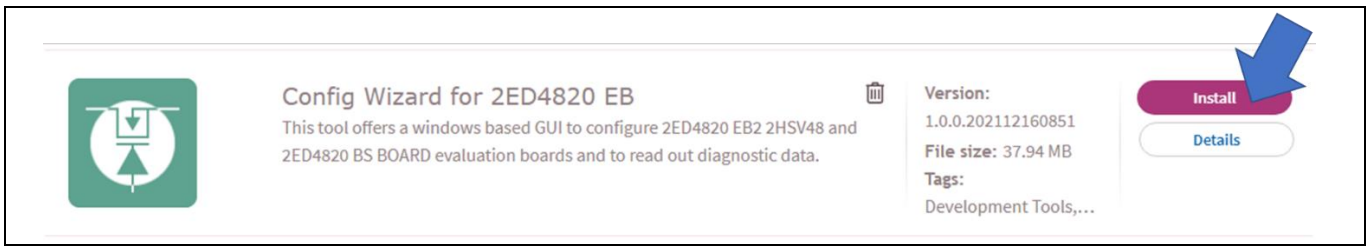


Figure 17 Installing the Config Wizard for 2ED4820 EB.

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2.1.2 Flashing the XMC2Go

Once the **Config Wizard for 2ED4820 EB** software is installed on the PC, the XMC2Go can be connected to the PC thanks to a micro USB cable. To ensure consistency with the **Config Wizard for 2ED4820 EB** software running on the PC, it is necessary to flash the firmware of the XMC microcontroller.

1st step: launch the **Config Wizard for 2ED4820 EB** software on the PC, from the Infineon Developer Center:



Figure 18 Launching the program.

The window shown in the next figure should pop-up on your PC:

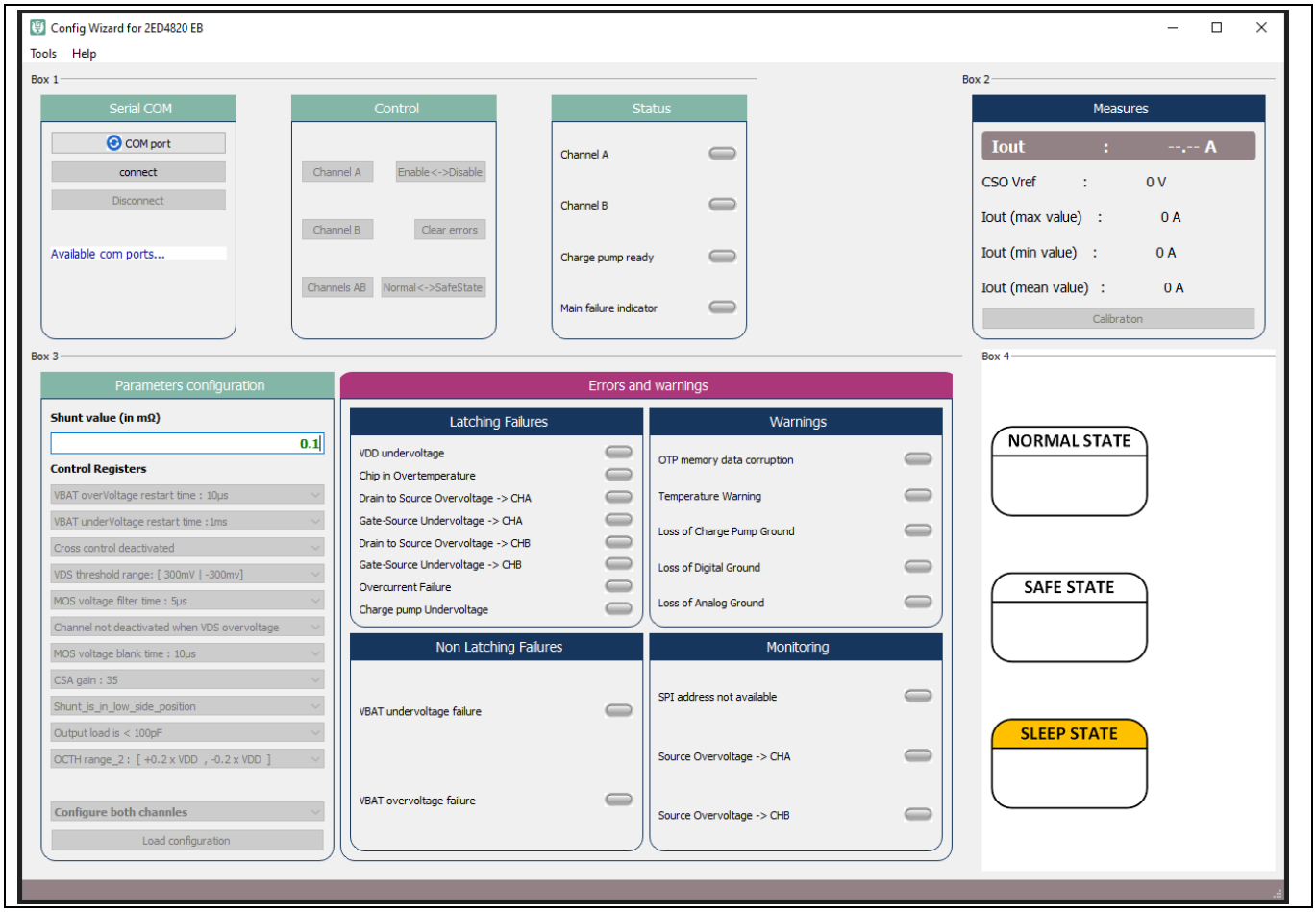


Figure 19 Welcome page.

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2nd step: establish the connection with the XMC2Go board:

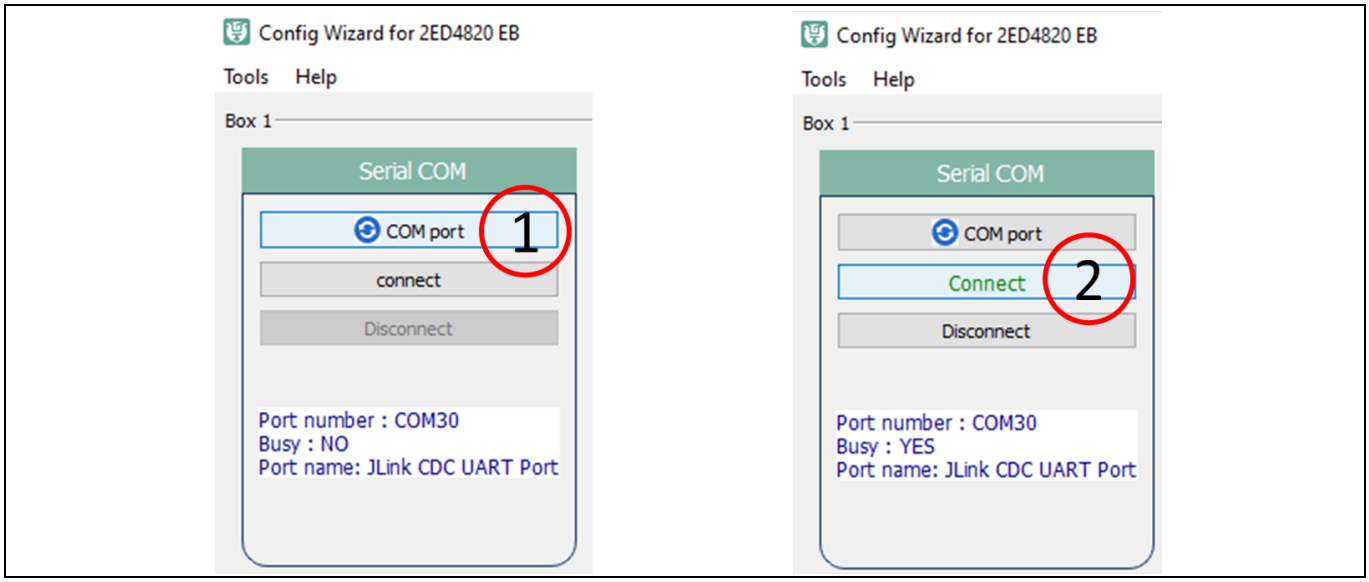


Figure 20 Selecting the Com Port & activating the connection.

3rd step: flash the firmware in the XMC MCU memory

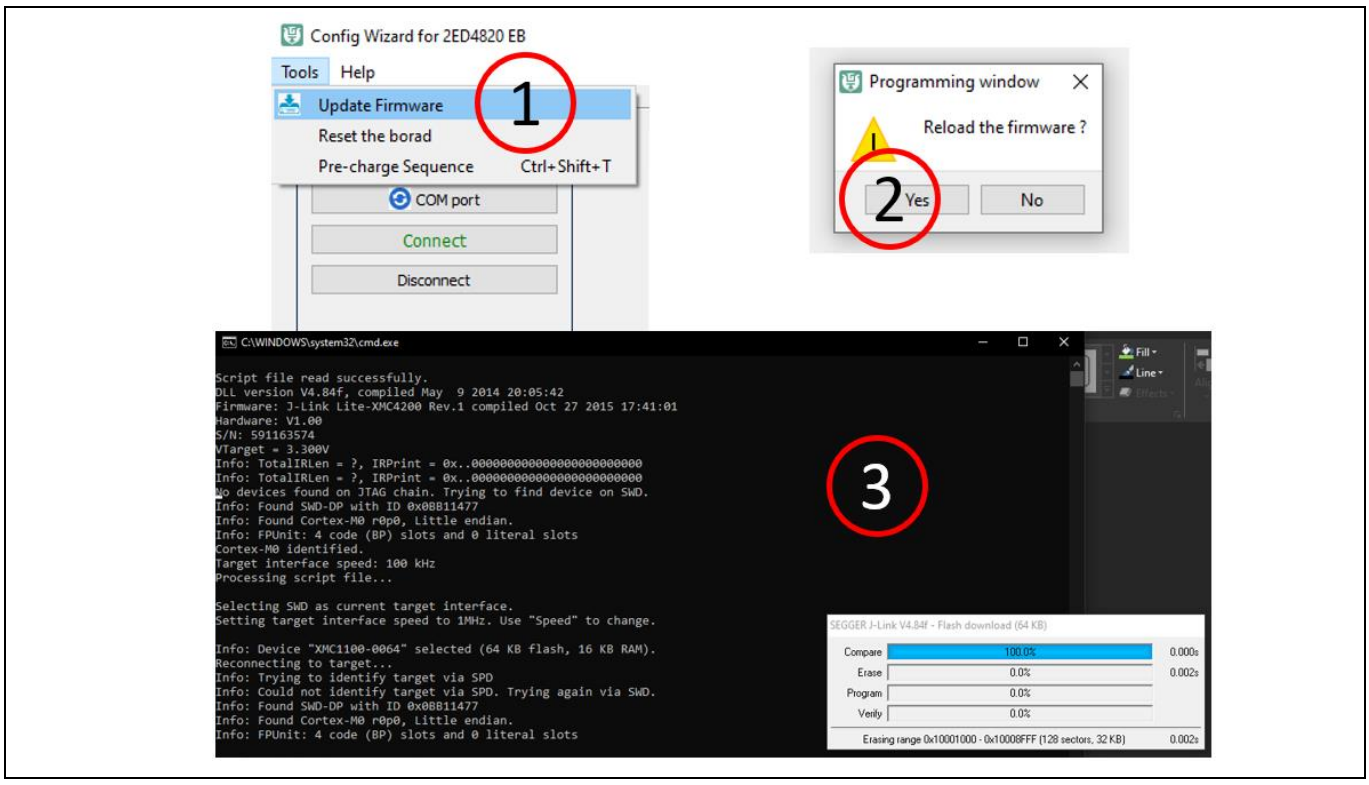


Figure 21 Flash the XMC MCU code.

The XMC firmware is now updated to be in sync with **Config Wizard for 2ED4820 EB** version.

This update of the XMC firmware has to be performed every time a new version of the Config Wizard for 2ED4820 EB is downloaded and installed!!

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2.2 Accessing the user guide in the ‘Help’ menu

Access the help menu to discover the functionality of the **Config Wizard for 2ED4820 EB** software (the help opens in a web browser, as an html file):

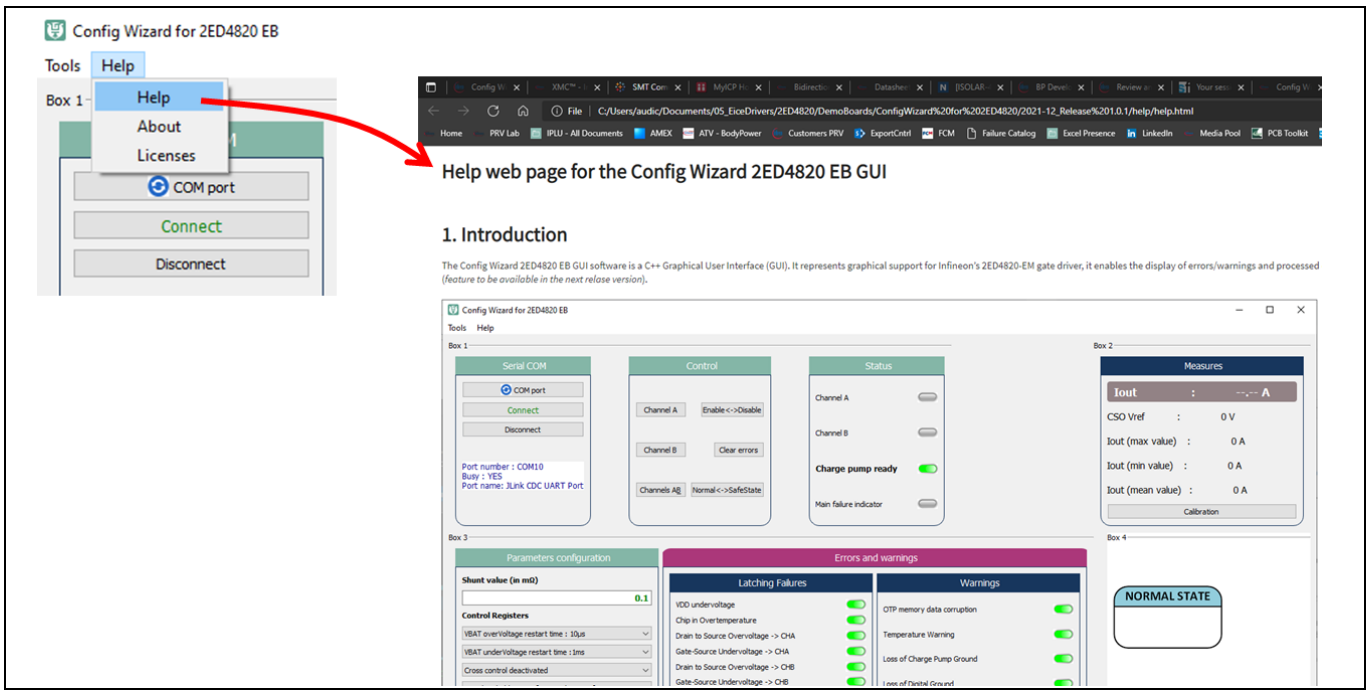


Figure 22 On-line user guide.

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3 Board connectors description

3.1 Power connectors

Name	Connector	Type	Description
VBAT	J15/1	Power supply	Positive power supply 48V
GND	J16/2	Ground power	Ground
GND_Load	J16/1	Ground power	Ground connection for the load, in low side current sense configuration
OUT1	J13/1	Power output	Output 1 for a load, up to 20 A DC
OUT2	J13/2	Power output	Output 2 for a load, up to 20 A DC
OUT3	J14/1 and J14/2	Power output	Output 3 for a load, up to 20 A DC

3.2 Interface connectors

3.2.1 Connector J1

Name	Pin	Type	Description
P2.7_OFF	1	Digital Input	Connects to switch S2
P2.9_CSO	2	Analog Input	Connects to CSO output on 2ED4820-EM through 12kΩ series resistor (R8)
P2.10_ON	3	Digital Input	Connects to switch S1
P2.11_MOSI	4	Digital Output	Connects to MOSI input on 2ED4820-EM through 1kΩ series resistor (R5)
GND	5	Ground	Ground
+3V3_XMC	6	Supply	3V3 supply, connects to VDD pin of 2ED4820-EM if a jumper is positioned on pins 1 & 2 of J4 (default config)
P0.0_CP_OUT	7	Digital Input	Connects to U12 comparator output to detect end of capacitor charge
NC	8	No connected	-

3.2.2 Connector J2

Name	Pin	Type	Description
P2.6_MISO	1	Digital Input	Connects to MISO output on 2ED4820-EM through 1kΩ series resistor (R4)
P2.0_INT	2	Digital Output	Connects to INTERRUPT input on 2ED4820-EM through 1kΩ series resistor (R2)
NC	3	No connected	-
P0.14_LSh	4	Digital Output	Connects to the input of the discrete level shifter
P0.9_CSN	5	Digital Output	Connects to CSN input on 2ED4820-EM through 1kΩ series resistor (R6)
P0.8_SCLK	6	Digital Output	Connects to SCLK input on 2ED4820-EM through 1kΩ series resistor (R7)
P0.7_ENA	7	Digital Output	Connects to ENABLE input on 2ED4820-EM through 1kΩ series resistor (R1)
P0.6_SAFEN	8	Digital Output	Connects to SAFESTATEN input on 2ED4820-EM through 1kΩ series resistor (R3)

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3.2.1 Connector J3

Note: J3 is not assembled, reference = 09195166324 from Harting or compatible connector

Name	Pin	Type	Description
NC	1	No connected	-
GND	2	Ground	Ground
NC	3	No connected	-
P0.14_LSh	4	Supply	5V supply, connects to VDD pin of 2ED4820-EM if a jumper is positioned on pins 2 & 3 of J4
NC	5	No connected	-
NC	6	No connected	-
NC	7	No connected	-
P2.0_INT	8	Digital Output	Connects to INTERRUPT input on 2ED4820-EM through 1kΩ series resistor (R2)
P0.9_CSN	9	Digital Output	Connects to CSN input on 2ED4820-EM through 1kΩ series resistor (R6)
P0.6_SAFEN	10	Digital Output	Connects to SAFESTATEN input on 2ED4820-EM through 1kΩ series resistor (R3)
P0.8_SCLK	11	Digital Output	Connects to SCLK input on 2ED4820-EM through 1kΩ series resistor (R7)
P0.7_ENA	12	Digital Output	Connects to ENABLE input on 2ED4820-EM through 1kΩ series resistor (R1)
P2.6_MISO	13	Digital Input	Connects to MISO output on 2ED4820-EM through 1kΩ series resistor (R4)
P2.10_ON	14	Digital Input	Connects to switch S1
P2.11_MOSI	15	Digital Output	Connects to MOSI input on 2ED4820-EM through 1kΩ series resistor (R5)
P2.9_CSO	16	Analog Input	Connects to CSO output on 2ED4820-EM through 12kΩ series resistor (R8)

3.3 Test points

Name	Signal name	Type	Description
TP1	SCLK	Digital Input	Directly connects to input pin SCLK on 2ED4820-EM
TP2	CSN	Digital Input	Directly connects to input pin CSN on 2ED4820-EM
TP3	MOSI	Digital Input	Directly connects to input pin MOSI on 2ED4820-EM
TP4	MISO	Digital output	Directly connects to input pin MISO on 2ED4820-EM
TP5	SAFESTATEN	Digital Input	Directly connects to input pin SAFESTATEN on 2ED4820-EM
TP6	INTERRUPT	Digital Input	Directly connects to input pin INTERRUPT on 2ED4820-EM
TP7	ENABLE	Digital Input	Directly connects to input pin ENABLE on 2ED4820-EM
TP8	CSO	Analog output	Directly connects to output pin CSO on 2ED4820-EM
TP9	VBAT_GD	Analog supply	Directly connects to supply pin VBAT on 2ED4820-EM
TP10	GA	Analog output	Directly connects to output pin GA on 2ED4820-EM
TP11	GB	Analog output	Directly connects to output pin GB on 2ED4820-EM
TP12	SA	Analog input	Directly connects to input pin SA on 2ED4820-
TP13	SB	Analog input	Directly connects to input pin SB on 2ED4820-
TP14	OUT1	Power output	Connects to power signal OUT1
TP15	OUT2	Power output	Connects to power signal OUT2
TP16	OUT3	Power output	Connects to power signal OUT3
TP17	GND	Ground	Connects to board ground plane
TP18	VDD	Supply	Directly connects to supply pin VDD on 2ED4820-EM
TP19	VCP	Supply	Directly connects to supply pin VCP on 2ED4820-EM
TP20	CPL	Analog output	Directly connects to output pin CPL on 2ED4820-EM
TP21	P0.0_CP_OUT	Digital output	Connects to U12 comparator output to detect end of capacitor charge
TP22	CP+	Analog output	Connects to U12 comparator positive input
TP23	Dr_Lsh	Digital input	Connects to Level shifter input

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4 Schematic

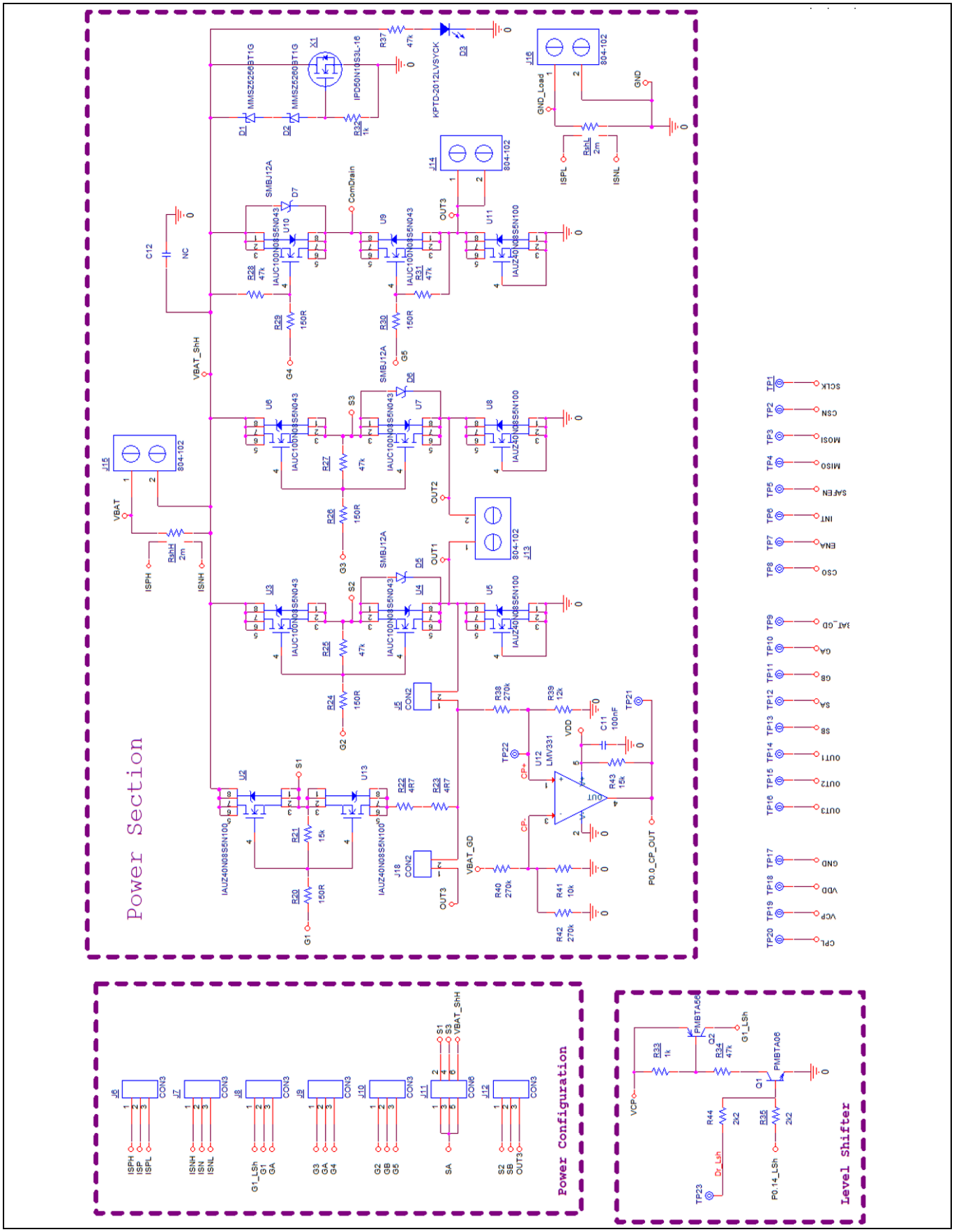


Figure 23 Schematic: power section

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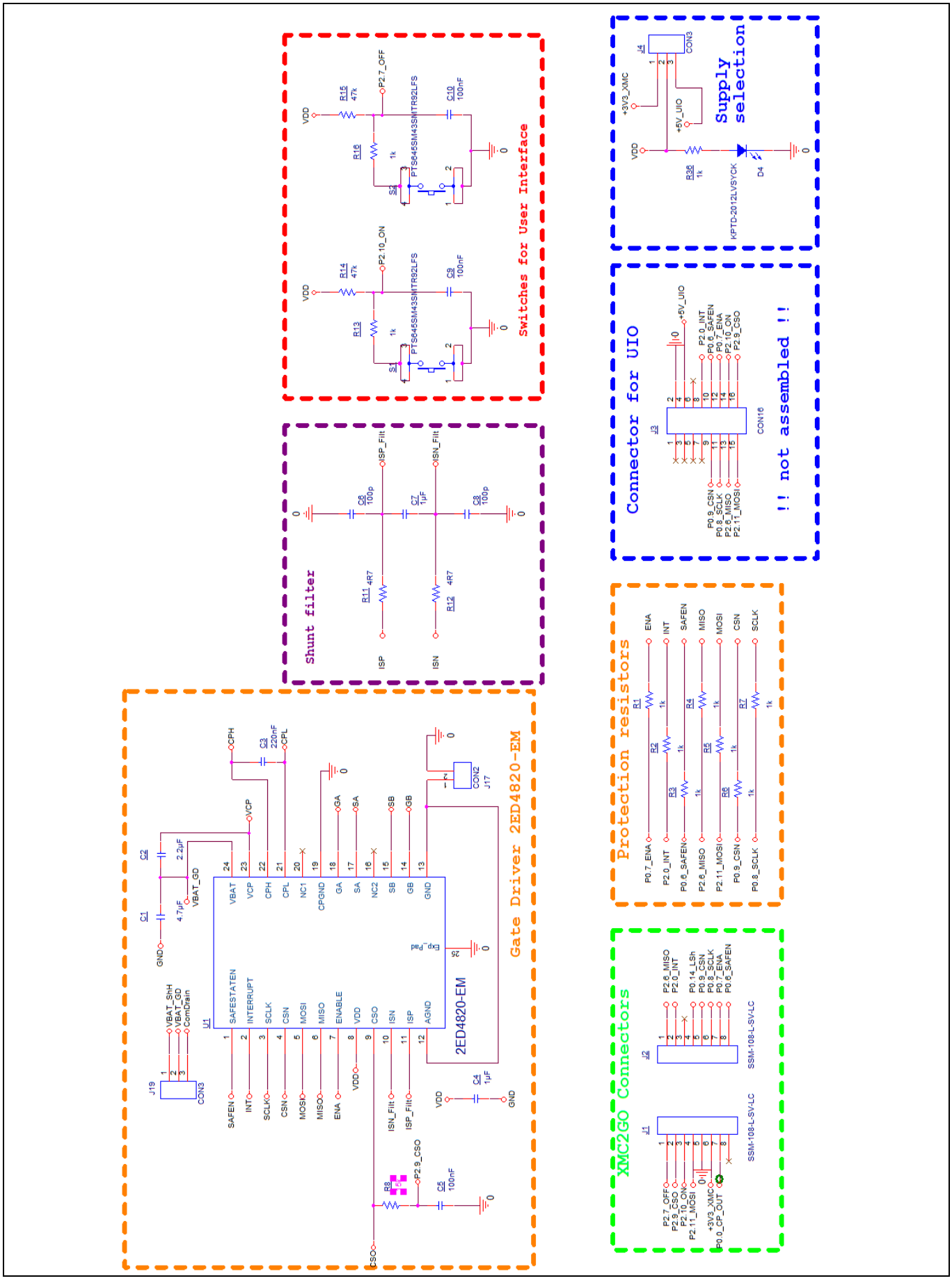


Figure 24 Schematic: gate driver section

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5 Bill of Material

Item	Qty	Identifier	Value	Charact.	Footprint
1	1	C1	4.7µF	100V/X7R	2220
2	1	C2	2.2µF	25V/X7R	1206
3	1	C3	220nF	100V/X7R	805
4	2	C4, C7	1µF	16V/X7R	1206
5	4	C5, C9, C10, C11	100nF	16V/X7R	805
6	2	C6, C8	100p	16V/X7R	805
7	1	C12	TbD	TbD	2220
8	1	D1	MMSZ5256BT1G	Zener 30V	SOD123
9	1	D2	MMSZ5260BT1G	Zener 43V	SOD123
10	2	D3, D4	KPTD-2012LVSYCK	LED	805
11	3	D5, D6, D7	SMBJ12A	TVS 14V	SMB
12	2	J1, J2	SSM-108-L-SV-LC		
13	0	J3	CON16	09195166324	HE10 16pts
14	8	J4, J6, J7, J8, J9, J10, J12, J19	CON3		
15	3	J5, J17, J18	CON2		
16	1	J11	CON6		
17	4	J13, J14, J15, J16	804-102		
18	1	Q1	PMBTA06	NPN 80V	SOT23
19	1	Q2	PMBTA56	PNP 80V	SOT23
20	2	RshL, RshH	2m	4-pin shunt	BVB
21	12	R1, R2, R3, R4, R5, R6, R7, R13, R16, R32, R33, R36	1k		805
22	1	R39	12k		805
23	1	R41	10k		805
24	3	R8, R21, R43	15k		805
25	2	R11, R12	4R7		805
26	8	R14, R15, R25, R27, R28, R31, R34, R37	47k		805
27	5	R20, R24, R26, R29, R30	150R		805
28	2	R22, R23	4R7		2512
29	2	R35, R43	2k2		805
30	3	R38, R40, R42	270k		805
31	2	S1, S2	PTS645SM43SMTR92LFS	switch	
32	23	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16,	Test Point		

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		TP17, TP18, TP19, TP20, TP21, TP22, TP23			
33	1	U1	2ED4820-EM	SPI gate driver	TSDSO24
34	5	U2, U5, U8, U11, U13	IAUZ40N08S5N100	10mΩ NMOS 80V	S3O8
35	6	U3, U4, U6, U7, U9, U10	IAUC100N08S5N043	4.3mΩ NMOS 80V	SSO8
36	1	X1	IPD50N10S3L-16	15mΩ NMOS 100V	DPAK
37	1	U12	LMV331	Low voltage comparator	SOT23-5

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1 PCB: layers

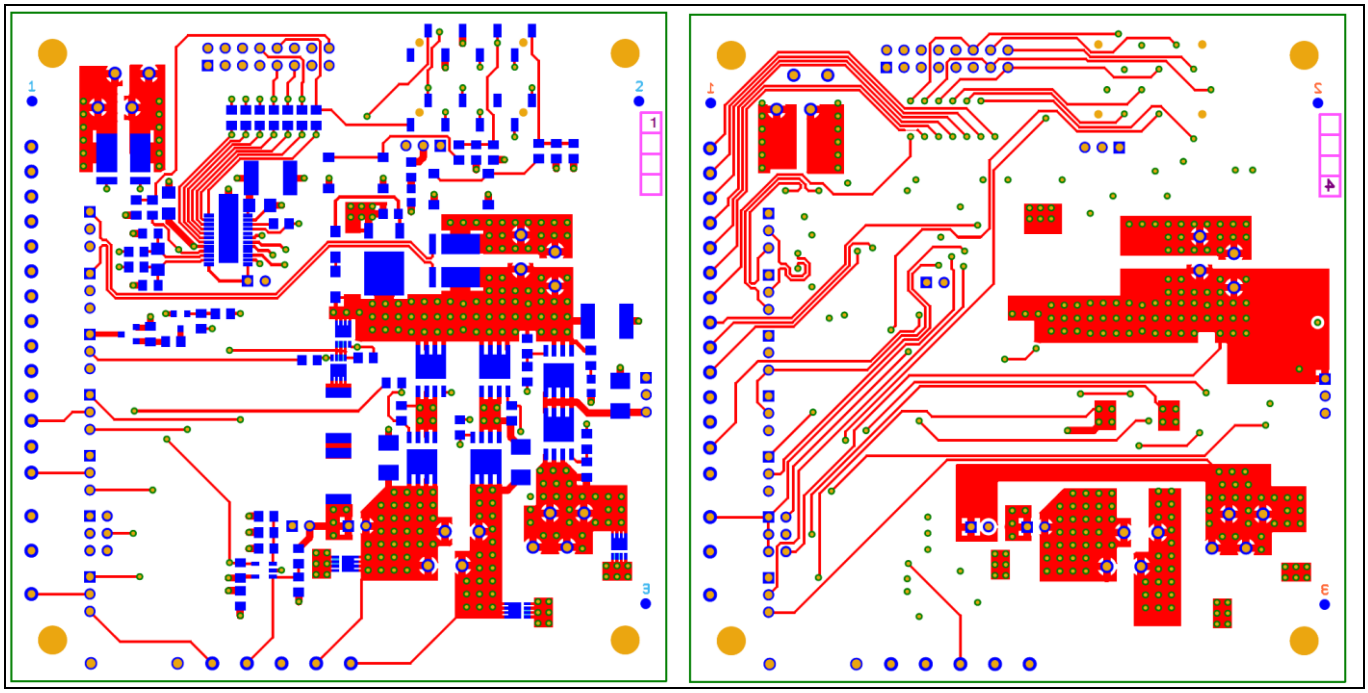


Figure 25 Top and bottom layers

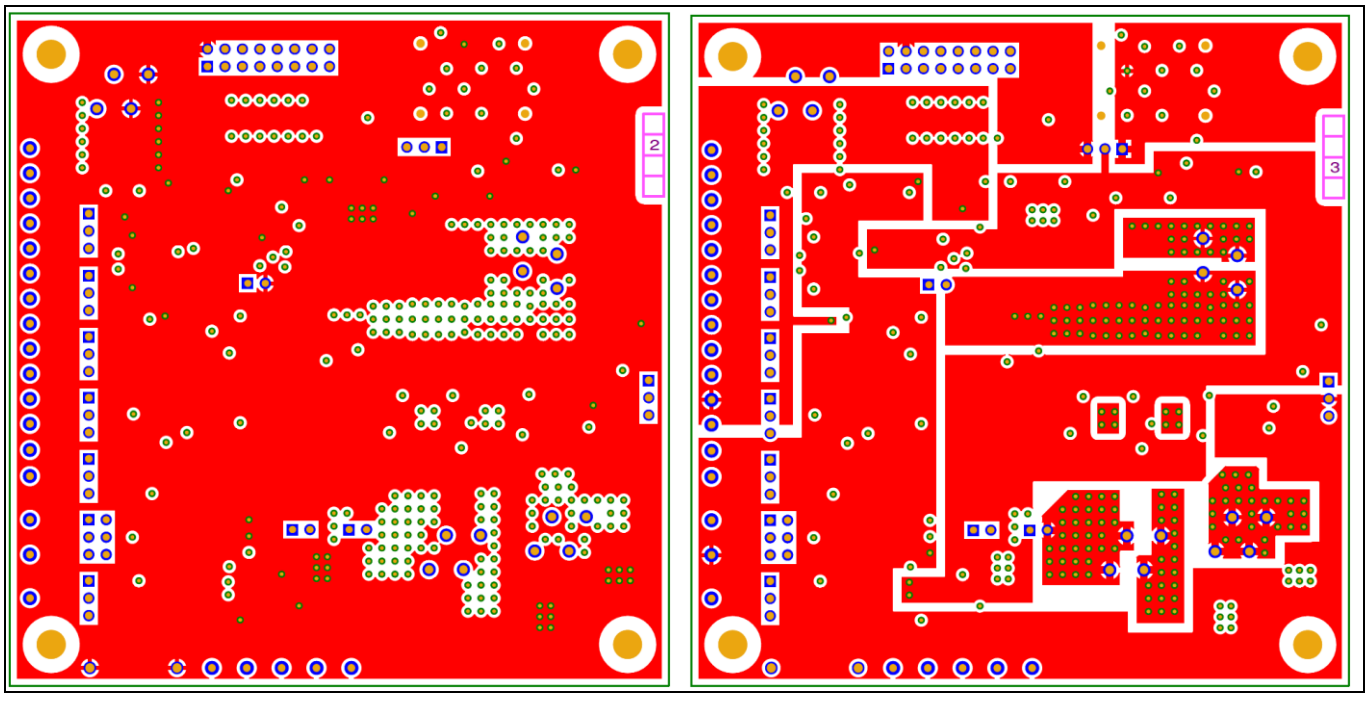


Figure 26 Inner planes

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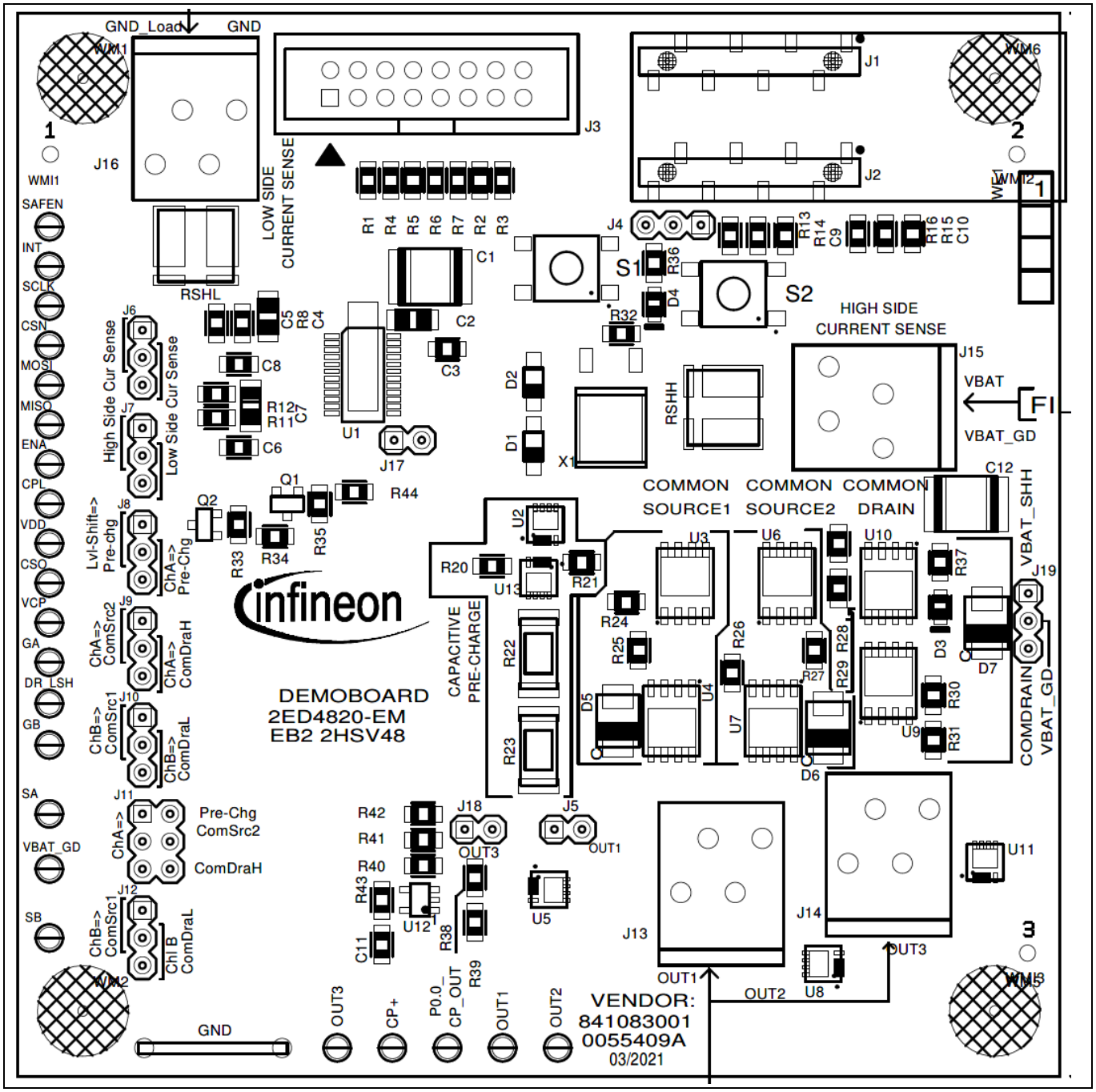


Figure 27 Top assembly

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Revision history

Document version	Date of release	Description of changes
Rev 1.0	2022-01-20	Initial version

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