To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1251GR-9LG, μPC1251MP-KAA, μPC358GR-9LG

SINGLE POWER SUPPLY DUAL OPERATIONAL AMPLIFIERS

<R> DESCRIPTION

The μPC1251GR-9LG, μPC1251MP-KAA, μPC358GR-9LG are dual operational amplifiers which are designed to operate for a single power supply. It includes features of low-voltage operation, a common-mode input voltage that range from V^- (GND) level, an output from a V^- (GND) level that is determined by the output stage of class C push-pull circuit and a 50 μA(TYP.) constant current, and a low current consumption.

In addition, this can operate at both positive and negative power supply and it can be extensively used in various amplifier circuits.

The μPC1251GR-9LG, μPC1251MP-KAA which expands temperature type is suited for wide operating ambient temperature use, and μPC358GR-9LG is used for general purposes.

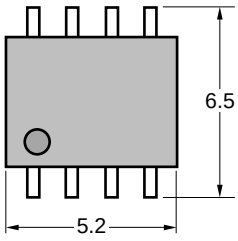
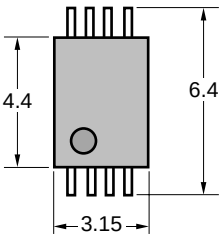
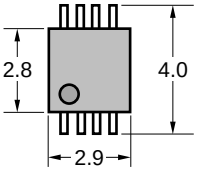
A DC parameter selection that is compatible to operational amplifiers is also available.

μPC451GR-9LG, μPC324GR-9LG which are quad types with the same circuit configuration are also available as series of operational amplifiers.

<R> FEATURES

- Input Offset Voltage ±2 mV (TYP.)
- Input Offset Current ±5 nA (TYP.)
- Large Signal Voltage Gain 100000 (TYP.)
- Internal frequency compensation
- Output short-circuit protection
- Small Package

  The mounting area is reduced to 40% or 66% compared to the conventional 8-pin plastic SOP as shown in the following diagram.

Package	Standard SOP	TSSOP	TSSOP (2.8 x 2.9)
Subject part number	μPC1251G2, μPC358G2	μPC1251GR-9LG, μPC358GR-9LG	μPC1251MP-KAA
Outline comparison			
(Mounting area ratio)	(100%)	(60%)	(34%)

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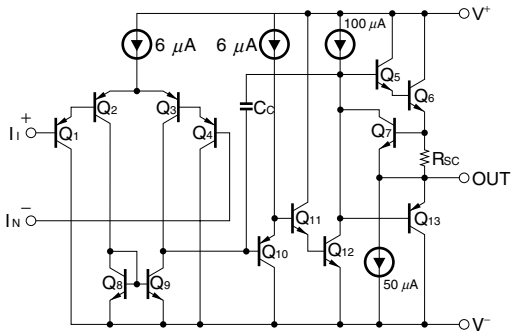
<R> ORDERING INFORMATION

Part Number	Selected Grade	Package	Package Type
μPC1251GR-9LG-E1-A Note	Standard	8-pin plastic TSSOP (5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 on draw-out side
μPC1251GR-9LG-E2-A Note	Standard	8-pin plastic TSSOP (5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 at take-up side
μPC1251GR(5)-9LG-E1-A Note	DC parameter selection	8-pin plastic TSSOP (5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 on draw-out side
μPC1251GR(5)-9LG-E2-A Note	DC parameter selection	8-pin plastic TSSOP (5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 at take-up side
μPC1251MP-KAA-E1-A Note	Standard	8-pin plastic TSSOP (2.8 x 2.9)	• 12 mm wide embossed taping • Pin 1 on draw-out side
μPC1251MP-KAA-E2-A Note	Standard	8-pin plastic TSSOP (2.8 x 2.9)	• 12 mm wide embossed taping • Pin 1 at take-up side
μPC1251MP(5)-KAA-E1-A Note	DC parameter selection	8-pin plastic TSSOP (2.8 x 2.9)	• 12 mm wide embossed taping • Pin 1 on draw-out side
μPC1251MP(5)-KAA-E2-A Note	DC parameter selection	8-pin plastic TSSOP (2.8 x 2.9)	• 12 mm wide embossed taping • Pin 1 at take-up side
μPC358GR-9LG-E1-A Note	Standard	8-pin plastic TSSOP(5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 on draw-out side
μPC358GR-9LG-E2-A Note	Standard	8-pin plastic TSSOP(5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 at take-up side
μPC358GR(5)-9LG-E1-A Note	DC parameter selection	8-pin plastic TSSOP(5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 on draw-out side
μPC358GR(5)-9LG-E2-A Note	DC parameter selection	8-pin plastic TSSOP(5.72 mm(225))	• 12 mm wide embossed taping • Pin 1 at take-up side

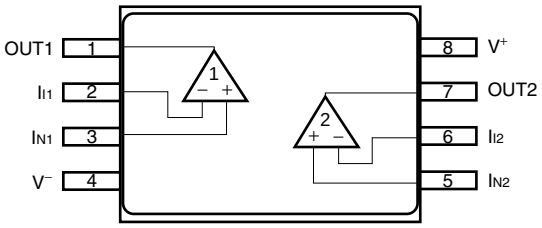
Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

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EQUIVALENT CIRCUIT (1/2 Circuit)



<R> PIN CONFIGURATION (Marking side)



<R> ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Parameter	Symbol	μPC1251GR-9LG, μPC1251GR(5)-9LG	μPC1251MP-KAA, μPC1251MP(5)-KAA	μPC358GR-9LG, μPC358GR(5)-9LG	Unit
Voltage between V^+ and V^- Note1	$V^+ - V^-$	−0.3 to +32			V
Differential Input Voltage	V_{ID}	±32			V
Input Voltage Note2	V_I	V^- − 0.3 to V^- + 32			V
Output applied Voltage Note3	V_O	V^- − 0.3 to V^+ + 0.3			V
Total Power Dissipation Note4	P_T	440			mW
Output Short Circuit Duration Note5	t_S	Indefinite			s
Operating Ambient Temperature	T_A	−40 to +125		−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150		−55 to +125	°C

Note1. Note that reverse connections of the power supply may damage ICs.

2. The input voltage is allowed to input without damage or destruction independent of the magnitude of V^+. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.

3. A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.

4. This is the value of when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

μPC1251GR-9LG: Derate at −5.5 mW/°C when T_A > 69°C.

(Junction − ambient thermal resistance $R_{th(J-A)}$ = 183°C/W)

μPC1251MP-KAA: Derate at −4.8 mW/°C when T_A > 58°C.

(Junction − ambient thermal resistance $R_{th(J-A)}$ = 208°C/W)

μPC358GR-9LG: Derate at −5.5 mW/°C when T_A > 44°C.

(Junction − ambient thermal resistance $R_{th(J-A)}$ = 183°C/W)

5. Short circuits from the output to V^+ can cause destruction. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, **Note 4**.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Split)	$V^{\pm}$	±1.5		±15	V
Power Supply Voltage (V^- = GND)	V^+	+3		+30	V

<R> ELECTRICAL CHARACTERISTICS

μPC1251GR-9LG, μPC1251MP-KAA, μPC358GR-9LG (T_A = 25°C, V^+ = +5 V, V^- = GND)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	R_S = 0 Ω		±2	±7	mV
Input Offset Current	I_{IO}			±5	±50	nA
Input Bias Current Note1	I_B			14	250	nA
Large Signal Voltage Gain	A_V	R_L ≥ 2 kΩ	25000	100000		
Circuit Current Note2	I_{CC}	R_L = ∞, I_O = 0 A		0.7	1.2	mA
Common Mode Rejection Ratio	CMR		65	70		dB
Supply Voltage Rejection Ratio	SVR		65	100		dB
Output Voltage Swing	V_O	R_L = 2 kΩ (Connect to GND)	0		V^+ – 1.5	V
Common Mode Input Voltage Range	V_{ICM}		0		V^+ – 1.5	V
Output Source Current	$I_{O\ SOURCE}$	$V_{IN(+)}$ = +1 V, $V_{IN(-)}$ = 0 V	20	40		mA
Output Sink Current	$I_{O\ SINK1}$	$V_{IN(-)}$ = +1 V, $V_{IN(+)}$ = 0 V	10	20		mA
	$I_{O\ SINK2}$	$V_{IN(-)}$ = +1 V, $V_{IN(+)}$ = 0 V, V_O = 200 mV	12	50		μA
Channel Separation		f = 1 to 20 kHz		120		dB

μPC1251GR(5)-9LG, μPC1251MP(5)-KAA, μPC358GR(5)-9LG (T_A = 25°C, V^+ = +5 V, V^- = GND)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	R_S = 0 Ω		±2	±3	mV
Input Offset Current	I_{IO}			±5	±50	nA
Input Bias Current Note1	I_B			14	60	nA
Large Signal Voltage Gain	A_V	R_L ≥ 2 kΩ	50000	100000		
Circuit Current Note2	I_{CC}	R_L = ∞, I_O = 0 A		0.7	0.9	mA
Common Mode Rejection Ratio	CMR		65	70		dB
Supply Voltage Rejection Ratio	SVR		65	100		dB
Output Voltage Swing	V_O	R_L = 2 kΩ (Connect to GND)	0		V^+ – 1.5	V
Common Mode Input Voltage Range	V_{ICM}		0		V^+ – 1.4	V
Output Source Current	$I_{O\ SOURCE}$	$V_{IN(+)}$ = +1 V, $V_{IN(-)}$ = 0 V	30	40		mA
Output Sink Current	$I_{O\ SINK1}$	$V_{IN(-)}$ = +1 V, $V_{IN(+)}$ = 0 V	15	20		mA
	$I_{O\ SINK2}$	$V_{IN(-)}$ = +1 V, $V_{IN(+)}$ = 0 V, V_O = 200 mV	30	50	70	μA
Channel Separation		f = 1 to 20 kHz		120		dB

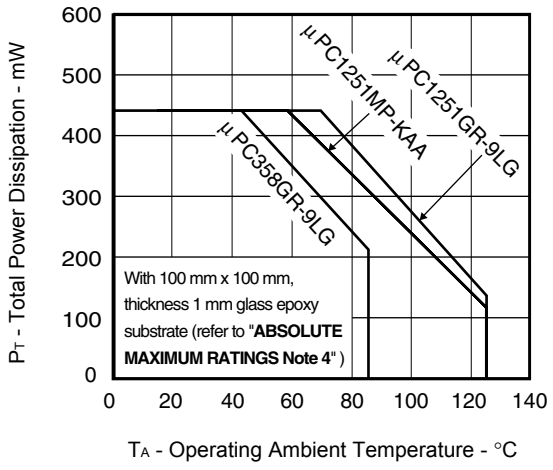
Notes1. The input bias current flows in the direction where the IC flows out because the first stage is configured with a PNP transistor.

2. This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.

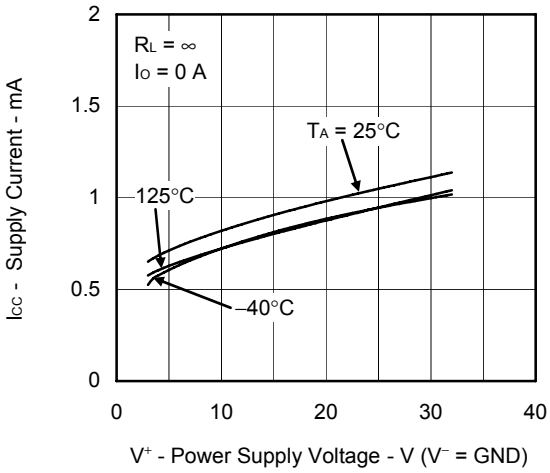
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<R> TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, TYP.) (Reference value)

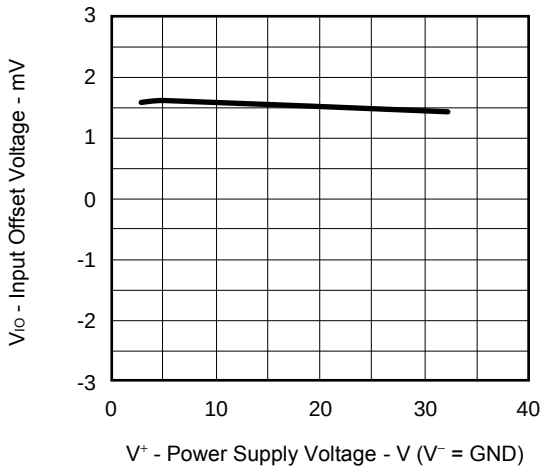
P_T vs. T_A



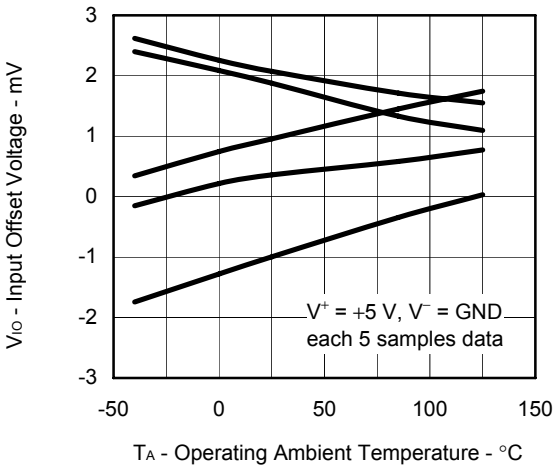
I_{CC} vs. V^+



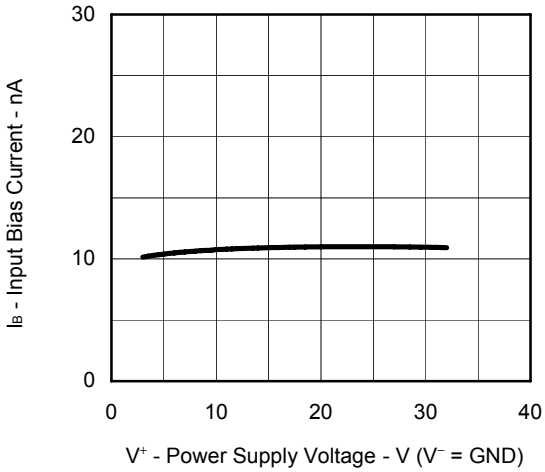
V_{IO} vs. V^+



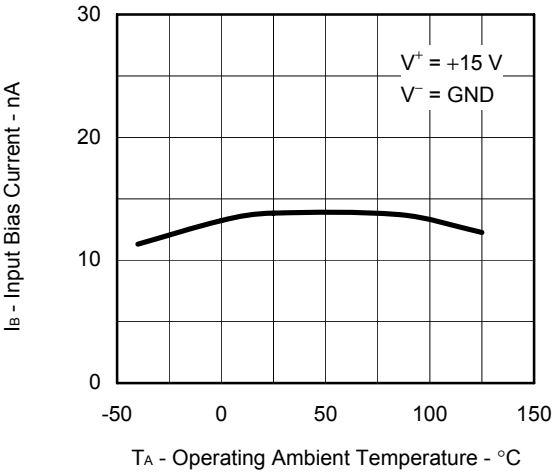
V_{IO} vs. T_A



I_B vs. V^+

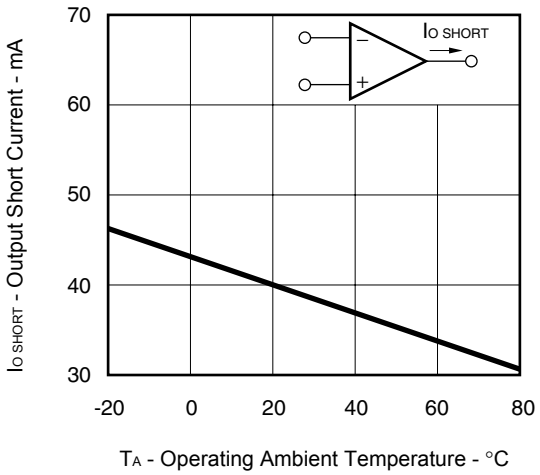


I_B vs. T_A

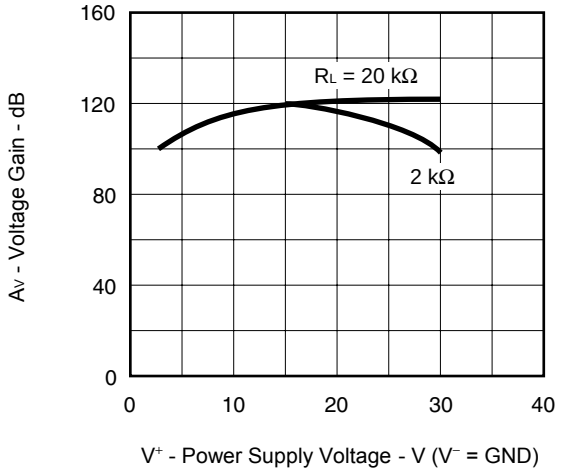


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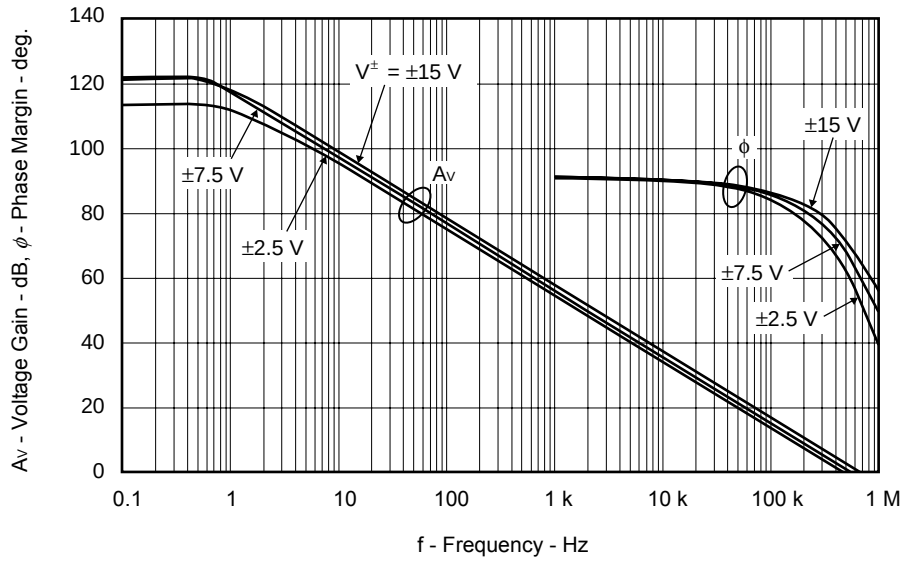
$I_{O\ SHORT}$ vs. T_A



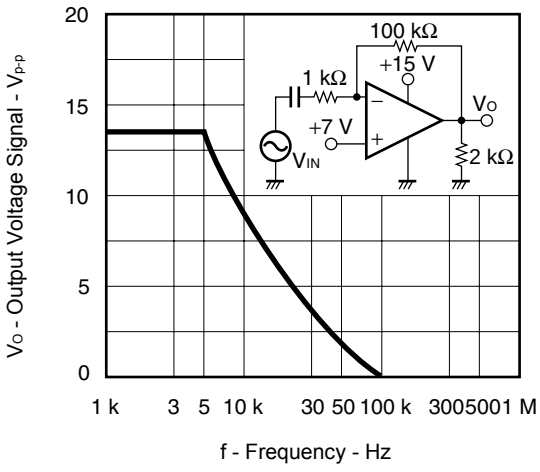
A_V vs. V^+



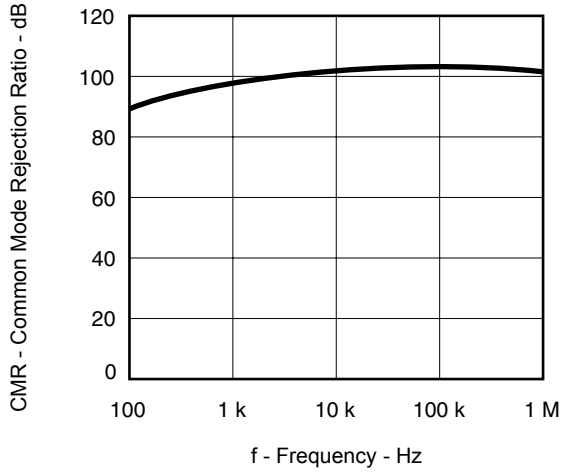
A_V, ϕ vs. f



V_O vs. f

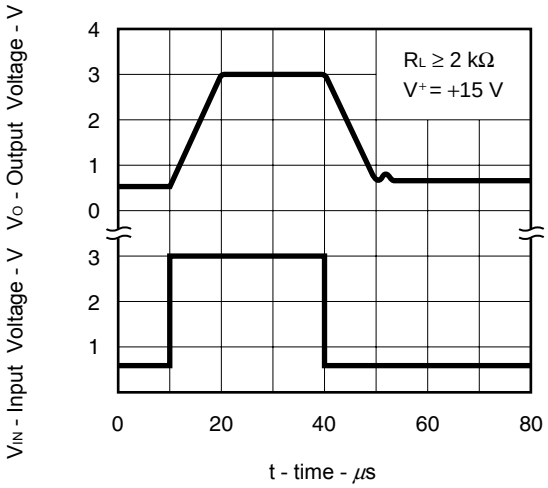


CMR vs. f

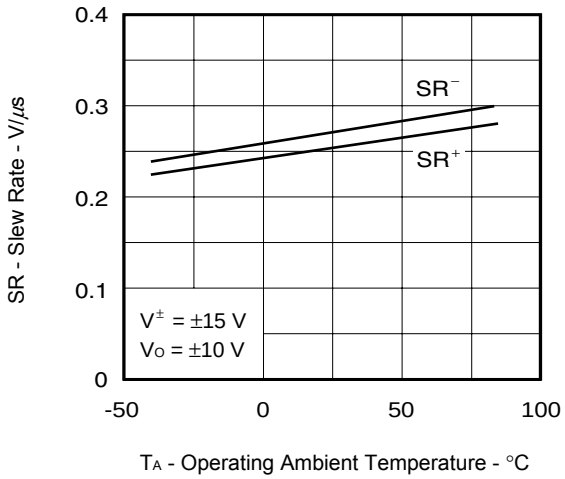


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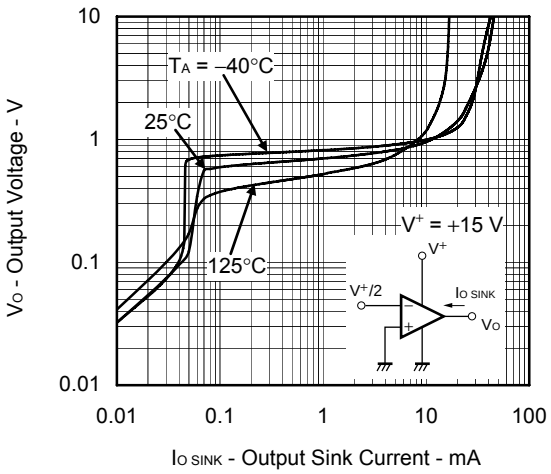
PULSE RESPONSE



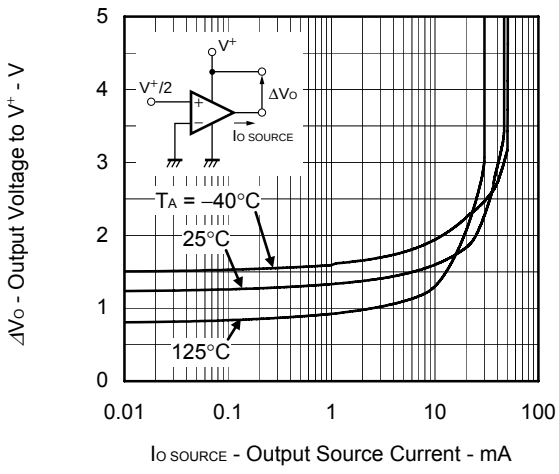
SR - TA



VO vs. IO SINK



ΔVO vs. IO SOURCE



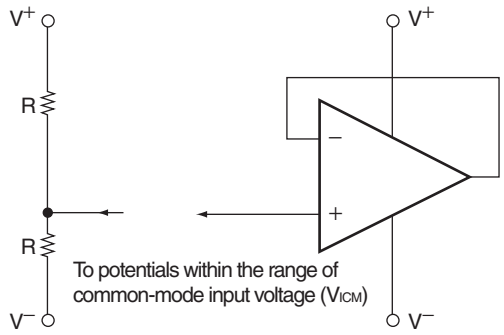
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<R> PRECAUTIONS FOR USE

O The process of unused circuits

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark A midpoint potential of V^+ and V^- is applied to this example.

O Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damages, by a conduction of a parasitic diode within an IC. In addition, when the input pin may be lower than V^-, or the output pin may exceed the power supply voltage, it is recommended to make a clump circuit by a diode whose forward voltage is low (e.g.: Schottky diode) for protection.

O Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

V_{ICM} (TYP.): V^- to $V^+ - 1.5$ (V) (T_A = 25°C)

During designing, temperature characteristics for use with allowance.

O The maximum output voltage

The range of the TYP. value of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

V_{Om}^+ (TYP.): $V^+ - 1.5$ (V) (T_A = 25°C), V_{Om}^- (TYP.) ($I_{O\ SINK} \leq 50\ \mu A$): Approx. V^- (V) (T_A = 25°C)

During designing, consider variations in characteristics and temperature characteristics for use with allowance.

In addition, also note that the output voltage range ($V_{Om}^+ - V_{Om}^-$) becomes narrow when an output current increases.

O Operation of output

This IC consist an output level of a class C push-pull. Therefore, when a load resistance is connected to the midpoint potential of V^+, V^-, a crossover distortion occurs at the transition state of output current flow direction (source, sink).

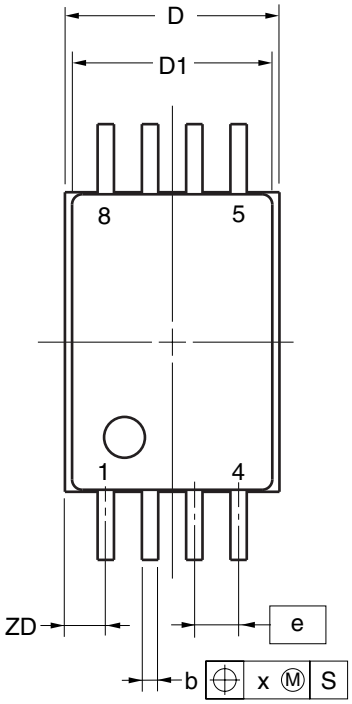
O Handling of ICs

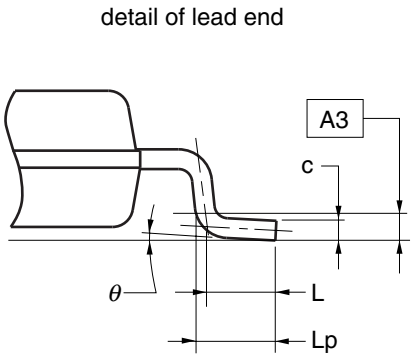
When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

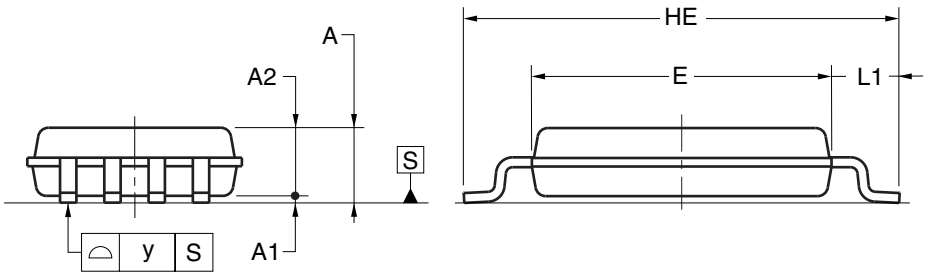
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PACKAGE DRAWINGS (Unit: mm)

8-PIN PLASTIC TSSOP (5.72mm (225))







(UNIT:mm)

ITEM	DIMENSIONS
D	3.15±0.15
D1	3.00±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	$0.24^{+0.06}_{-0.05}$
c	0.145±0.055
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.10
y	0.10
ZD	0.60

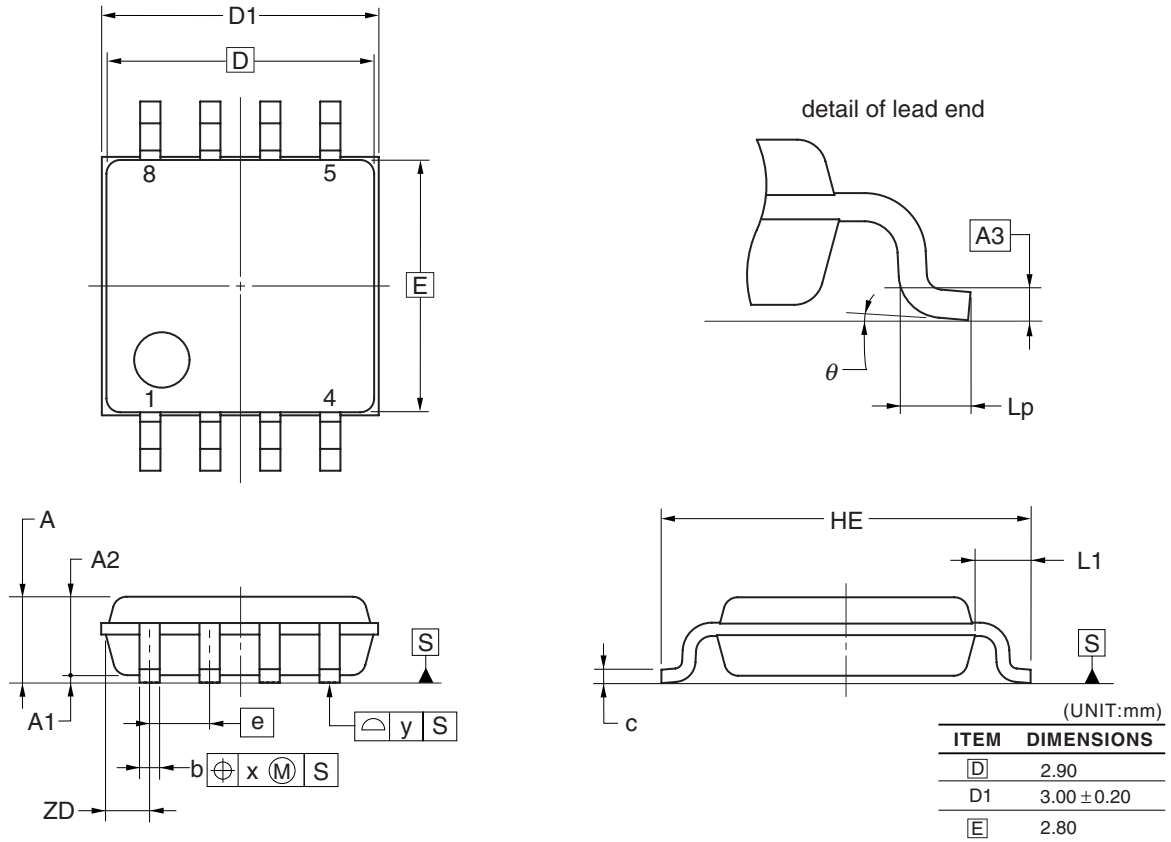
P8GR-65-9LG

NOTE
Each lead centerline is located within 0.10mm of its true position at maximum material condition.

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<R> 8-PIN PLASTIC TSSOP(2.8x2.9)



(UNIT:mm)

ITEM	DIMENSIONS
D	2.90
D1	3.00 ±0.20
E	2.80
HE	4.00 ±0.20
e	0.65
b	0.22 ±0.05
A	1.03 MAX.
A1	0.08 ±0.05
A2	0.85 ±0.05
A3	0.25
L1	0.60 ±0.20
c	$0.145^{+0.05}_{-0.03}$
Lp	0.37 ±0.10
x	0.10
y	0.10
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
ZD	0.525

P8MP-65-KAA

NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

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<R> RECOMMENDED SOLDERING CONDITIONS

The μPC1251GR-9LG, μPC1251MP-KAA, μPC358GR-9LG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPC1251GR-9LG-A Note, μPC1251GR(5)-9LG-A Note,
μPC358GR-9LG-A Note, μPC358GR(5)-9LG-A Note: 8-pin plastic TSSOP (5.72 mm (225))
μPC1251MP-KAA-A Note, μPC1251MP(5)-KAA-A Note: 8-pin plastic TSSOP (2.8 x 2.9)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 260°C, Reflow time: 60 seconds or less (at 220°C or higher), Maximum number of reflow processes: 3 times.	IR60-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120°C or below (Package surface temperature).	WS60-00-1
Partial heating method	Pin temperature: 350°C or below, Heat time: 3 seconds or less (Per each side of the device).	P350

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Remark Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended.

<R> REFERENCE DOCUMENTS

Document Name	Document No.
QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES	C11531E
SEMICONDUCTOR DEVICE MOUNT MANUAL	http://www.necel.com/pkg/en/mount/index.html
NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM-STANDARD LINEAR IC	IEI-1212
REVIEW OF QUALITY AND RELIABILITY HANDBOOK	C12769E
NEC SEMICONDUCTOR DEVICE RELIBIALITY/QUALITY CONTROL SYSTEM	C10983E

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