

LOW VOLTAGE CMOS QUAD 2-INPUT AND GATE WITH 5V TOLERANT INPUTS

- HIGH SPEED:
 $t_{PD} = 4.8ns$ (TYP.) at $V_{CC} = 3.3V$
- 5V TOLERANT INPUTS
- INPUT VOLTAGE LEVEL:
 $V_{IL}=0.8V$, $V_{IH}=2V$ AT $V_{CC}=3V$
- LOW POWER DISSIPATION:
 $I_{CC} = 2 \mu A$ (MAX.) at $T_A=25^\circ C$
- LOW NOISE:
 $V_{OLP} = 0.3V$ (TYP.) at $V_{CC} = 3.3V$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4mA$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \equiv t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(OPR) = 2V$ to $3.6V$ (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 08
- IMPROVED LATCH-UP IMMUNITY
- POWER DOWN PROTECTION ON INPUTS

DESCRIPTION

The 74LVX08 is a low voltage CMOS QUAD 2-INPUT AND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.

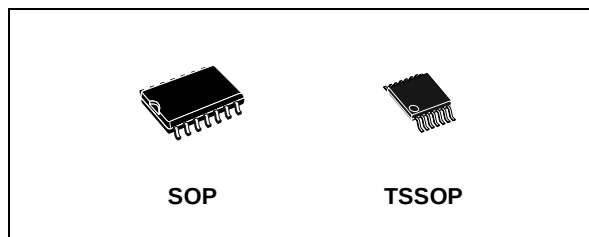


Table 1: Order Codes

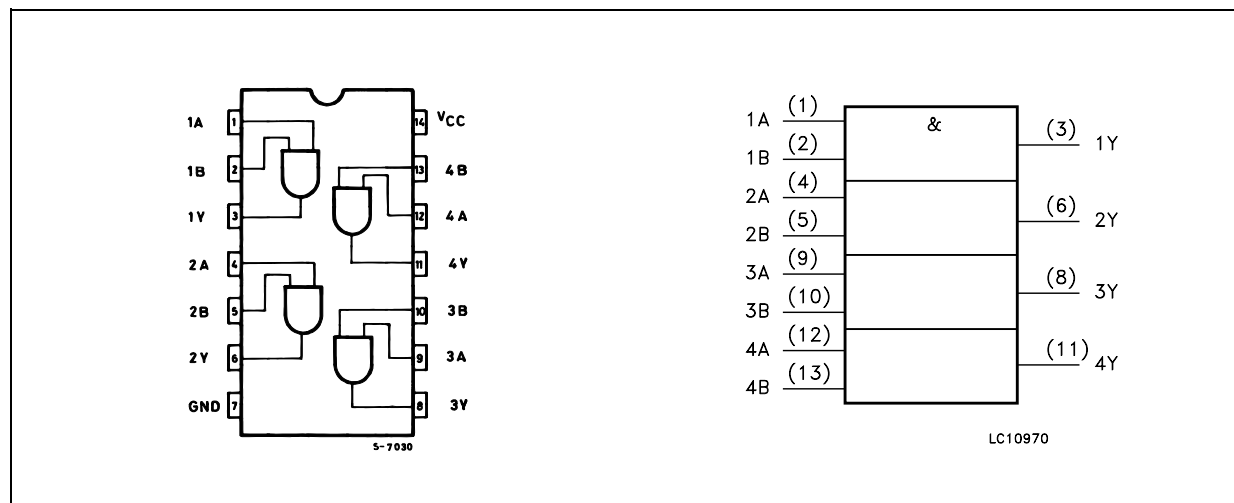
PACKAGE	T & R
SOP	74LVX08MTR
TSSOP	74LVX08TTR

The internal circuit is composed of 2 stages including buffer output, which provides high noise immunity and stable output.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

This device can be used to interface 5V to 3V system. It combines high speed performance with the true CMOS low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols



The diagram shows an input signal line labeled "INPUT" entering from the left. The signal line has four connection points marked with black dots. At the first dot, a vertical line connects to a rectangular block labeled "ESD PROTEC.". This block is connected to ground (GND) at the bottom. At the second dot, a vertical line connects to the anode of a diode. The cathode of this diode is connected to ground (GND). At the third dot, a horizontal line connects to the left side of a rectangular component, likely a resistor. At the fourth dot, a vertical line connects to the anode of a second diode. The cathode of this diode is connected to ground (GND). A dashed horizontal line connects the cathodes of the two diodes. The signal line continues to the right after the fourth dot. The label "SC11940" is located at the bottom right of the diagram.

PIN N°	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2) ($V_{CC} = 3.3V$)	0 to 100	ns/V

2) V_{IN} from 0.8V to 2.0V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		3.0	I _O =-4 mA	2.58			2.48		2.4		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
I _I	Input Leakage Current	3.6	V _I = 5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND			2		20		20	μA

Table 7: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C _L = 50 pF		0.3	0.5					V
V _{OLV}				-0.5	-0.3						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2							
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3					0.8				

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Table 8: AC Electrical Characteristics (Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time	2.7	15			6.3	11.4	1.0	12.5	1.0	13.5	ns
		2.7	50			8.8	14.9	1.0	17.0	1.0	18.0	
		3.3 ^(*)	15			4.8	7.1	1.0	8.5	1.0	9.5	
		3.3 ^(*)	50			7.3	10.6	1.0	12.0	1.0	13.0	
t _{OSLH} t _{OSHL}	Output To Output Skew Time (note1, 2)	2.7	50			0.5	1.0		1.5		1.5	ns
		3.3 ^(*)	50			0.5	1.0		1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

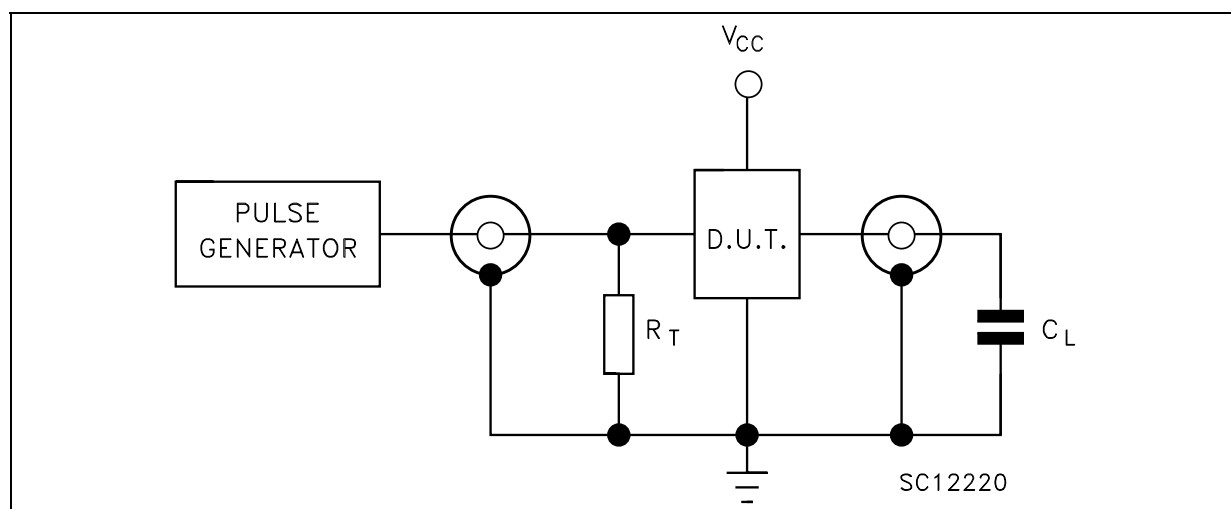
2) Parameter guaranteed by design

(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$

Table 9: Capacitive Characteristics

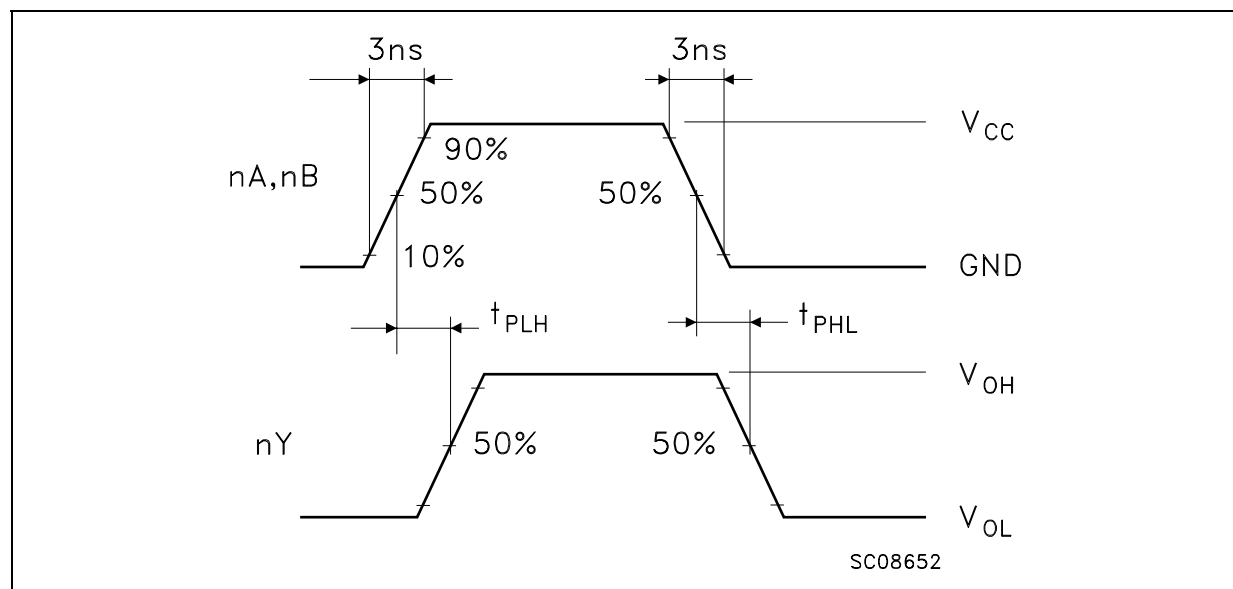
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	3.3			4	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3			18						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per gate)

Figure 3: Test Circuit

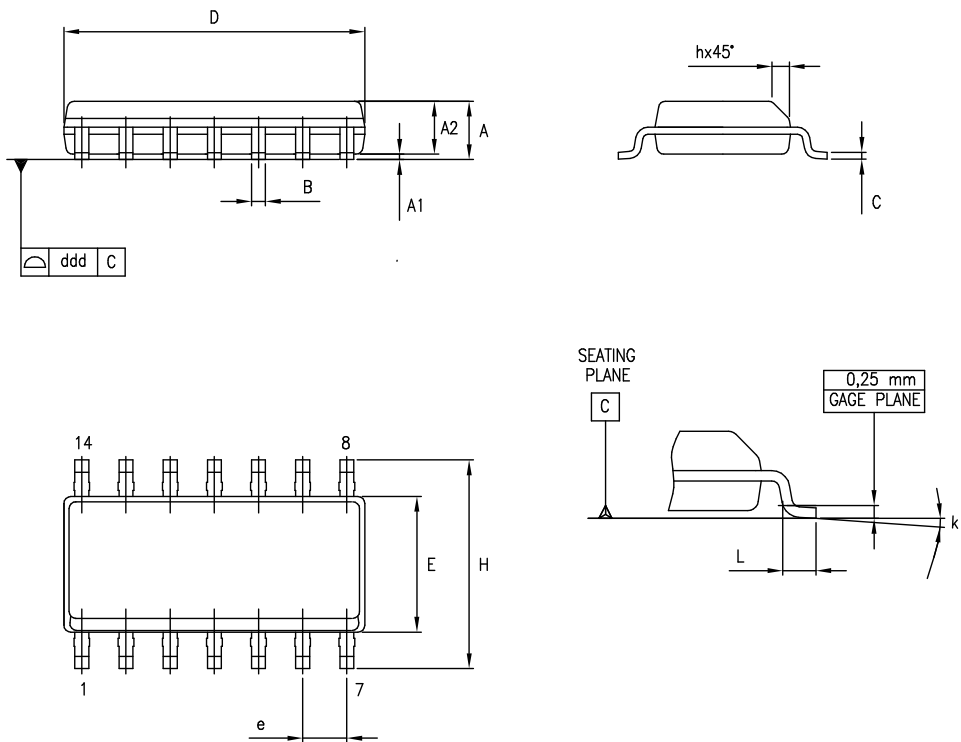
$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 4: Waveform - Propagation Delays ($f=1\text{MHz}$; 50% duty cycle)

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.1		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	8.55		8.75	0.337		0.344
E	3.8		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.2	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004



0016019D

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0080337D

Tape & Reel SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	0.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Tape & Reel TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Table 10: Revision History

Date	Revision	Description of Changes
27-Aug-2004	4	Ordering Codes Revision - pag. 1.

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