REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements. Editorial changes throughout. - gap	02-04-18	Raymond Monnin
B	Boilerplate update, part of 5 year review. ksr	08-07-09	Robert M. Heber

REV																				
SHEET																				
REV	B	B	B																	
SHEET	15	16	17																	

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
94-12-21

REVISION LEVEL
B

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ELECTRICALLY ERASABLE PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-94762**

SHEET 1 OF 17

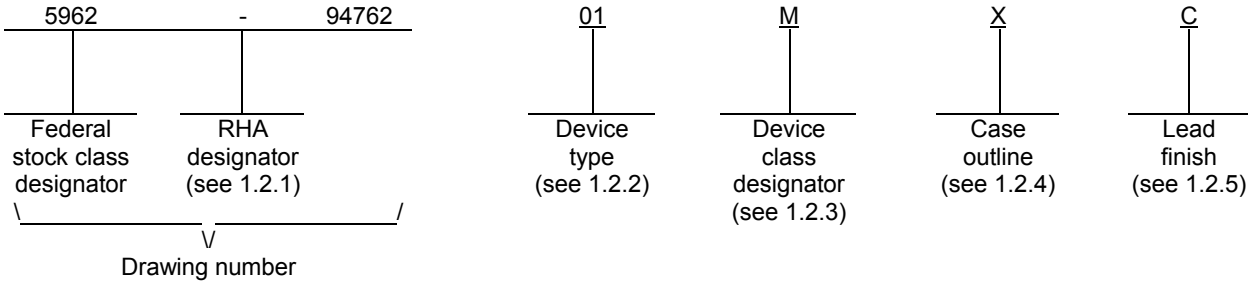
DSCC FORM 2233
APR 97

5962-E399-08

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Maximum clock frequency
01	ispLSI1016	EECMOS 2,000 gate in-system programmable logic device	60 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC2-J44	44	J-Leaded chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range (applied)	-2.5 V dc to V_{CC} + 1.0 V dc
Off-state output voltage range applied.	-2.5 V dc to V_{CC} + 1.0 V dc
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Maximum power dissipation (P_D) 2/	1.9 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds max)	+300°C
Data retention (at +55°C)	20 years (minimum)
Endurance	1,000 erase/write cycles (minimum)

1.4 Recommended operating conditions.

Supply voltage range, V_{CC}	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH})	2.0 V dc to V_{CC} + 1.0 V dc
Low Level input voltage range (V_{IL})	0.0 V dc to 0.8 V dc
Case operating temperature range, T_C	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein), or qualification conformance inspection groups A, B, C, or D (see 4.3 herein), the devices shall be programmed by the manufacturer prior to test.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
Low level output voltage	V_{OL}	I_{OL} = 8.0 mA, V_{IL} = 0.8 V, V_{CC} = 4.5 V	1, 2, 3		0.4	V
High level output voltage	V_{OH}	I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{CC} = 4.5 V	1, 2, 3	2.4		V
High level input voltage	V_{IH}	1/	1, 2, 3	2.0		V
Low level input voltage	V_{IL}	1/	1, 2, 3		0.8	V
Input or I/O low leakage current	I_{IL}	$0\ V \le V_{IN} \le 0.8\ V$	1, 2, 3		-10	µA
Input or I/O high leakage current	I_{IH}	$3.5\ V \le V_{IN} \le V_{CC}$	1, 2, 3		10	µA
I/O active pull-up current 2/	I_{PU}	$0\ V \le V_{IN} \le V_{IL}$	1, 2, 3		-150	µA
Output short circuit current 3/	I_{OS}	V_{OUT} = 0.5 V, V_{CC} = 5.0 V, T_A = +25°C, see 4.4.1f	1	-60	-200	mA
Operating power supply current 4/	I_{CC}	V_{IL} = 0.5 V, V_{IH} = 3.0 V, f = 1.0 MHz	1, 2, 3		170	mA
Dedicated input capacitance	C_{IN}	V_{IN} = 2.0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1.0 MHz, see 4.4.1e	4		10	pF
I/O and clock capacitance	$C_{I/O}$, C_Y	$V_{I/O}$, V_Y = 2.0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1.0 MHz, see 4.4.1e	4		10	pF
Functional tests		See 4.4.1c	7, 8A, 8B			
Data propagation delay, 4PT bypass, ORB bypass	t_{PD1}	V_{CC} = 4.5 V, see figure 4 5/ 6/	9, 10, 11		20	ns
Data propagation delay, worst case path	t_{PD2}		9, 10, 11		25	ns
Clock frequency with internal feedback 7/	f_{MAX1}		9, 10, 11	60		MHz
Clock frequency with external feedback 8/	f_{MAX2}		9, 10, 11	38		MHz
Clock frequency, maximum toggle 9/	f_{MAX3}		9, 10, 11	83		MHz
GLB register setup time before clock, 4PT bypass	t_{SU1}		9, 10, 11	9		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
GLB register clock to delay, ORP bypass	t_{CO1}	V_{CC} = 4.5 V, see figure 4 5/ 6/	9, 10, 11		13	ns
GLB register hold time after clock, 4PT bypass	t_{H1}		9, 10, 11	0		ns
GLB register setup time before clock	t_{SU2}		9, 10, 11	13		ns
GLB register clock to output delay	t_{CO2}		9, 10, 11		16	ns
GLB register hold time after clock	t_{H2}		9, 10, 11	0		ns
External reset pin to output delay	t_R		9, 10, 11		22.5	ns
External reset pulse duration	t_{RPW}		9, 10, 11	13		ns
Input to output enable	t_{PZH}, t_{PZL}		9, 10, 11		24	ns
Input to output disable	t_{PHZ}, t_{PLZ}		9, 10, 11		24	ns
External synchronous clock pulse duration, high	t_{PWH}		9, 10, 11	6		ns
External synchronous clock pulse duration, low	t_{PWL}		9, 10, 11	6		ns
I/O register setup time before external synchronous clock (Y2, Y3)	t_{SU5}		9, 10, 11	2.5		ns
I/O register hold time after external synchronous clock (Y2, Y3)	t_{H5}		9, 10, 11	8.5		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ Pull-up circuitry is programmable.
3/ One output at a time for a maximum duration of one second. V_{OUT} = 0.5 V was selected to avoid test problems by tester ground degradation. If not tested, shall be guaranteed to the limits specified in table I.
4/ Measured using six 16-bit counters.
5/ AC tests are performed with input rise and fall times (10% to 90%) of 3.0 ns, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V, and the output load of figure 4. Input pulse levels are absolute values with respect to device ground and all overshoots due to system or tester noise are included. Unless otherwise specified, all parameters use a GRP load of 4 GLB's, 20 PTXOR path, ORP and Y0 clock.
6/ May not be tested directly but shall be guaranteed to the values specified in table I.
7/ Standard 16-bit loadable counter using GRP feedback.
8/ Calculated value; $1/t_{SU2} + t_{CO1}$.
9/ f_{MAX3} may be less than $1/(t_{PWH} + t_{PWL})$. This is to allow for a clock duty cycle of other than 50%.

Device type	All	Device type	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	30	I/O13
2	IN3	31	I/O14
3	I/O24	32	I/O15
4	I/O25	33	Y2/SCLK*
5	I/O26	34	V_{CC}
6	I/O27	35	Y1/$\overline{\text{RESET}}$
7	I/O28	36	IN2/MODE*
8	I/O29	37	I/O16
9	I/O30	38	I/O17
10	I/O31	39	I/O18
11	Y0	40	I/O19
12	V_{CC}	41	I/O20
13	* $\overline{\text{ispEN}}$	42	I/O21
14	*SDI/IN0	43	I/O22
15	I/O0	44	I/O23
16	I/O1		
17	I/O2		
18	I/O3		
19	I/O4		
20	I/O5		
21	I/O6		
22	I/O7		
23	GND		
24	*SDO/IN1		
25	I/O8		
26	I/O9		
27	I/O10		
28	I/O11		
29	I/O12		

* Pins have dual function capability for the in-system-programmable devices listed on this drawing.

FIGURE 1. Terminal connections.

INPUTS				INPUTS/OUTPUTS
I	Y	$\overline{\text{RESET}}$	isp $\overline{\text{EN}}$	I/O
X	X	X	H or NC 1/	Z

X = Don't care
Z = High impedance state
NC = Not connected
H = Logic high voltage level
L = Logic low voltage level

1/ If logic L, certain outputs become undefined.

FIGURE 2. Truth table (unprogrammed).

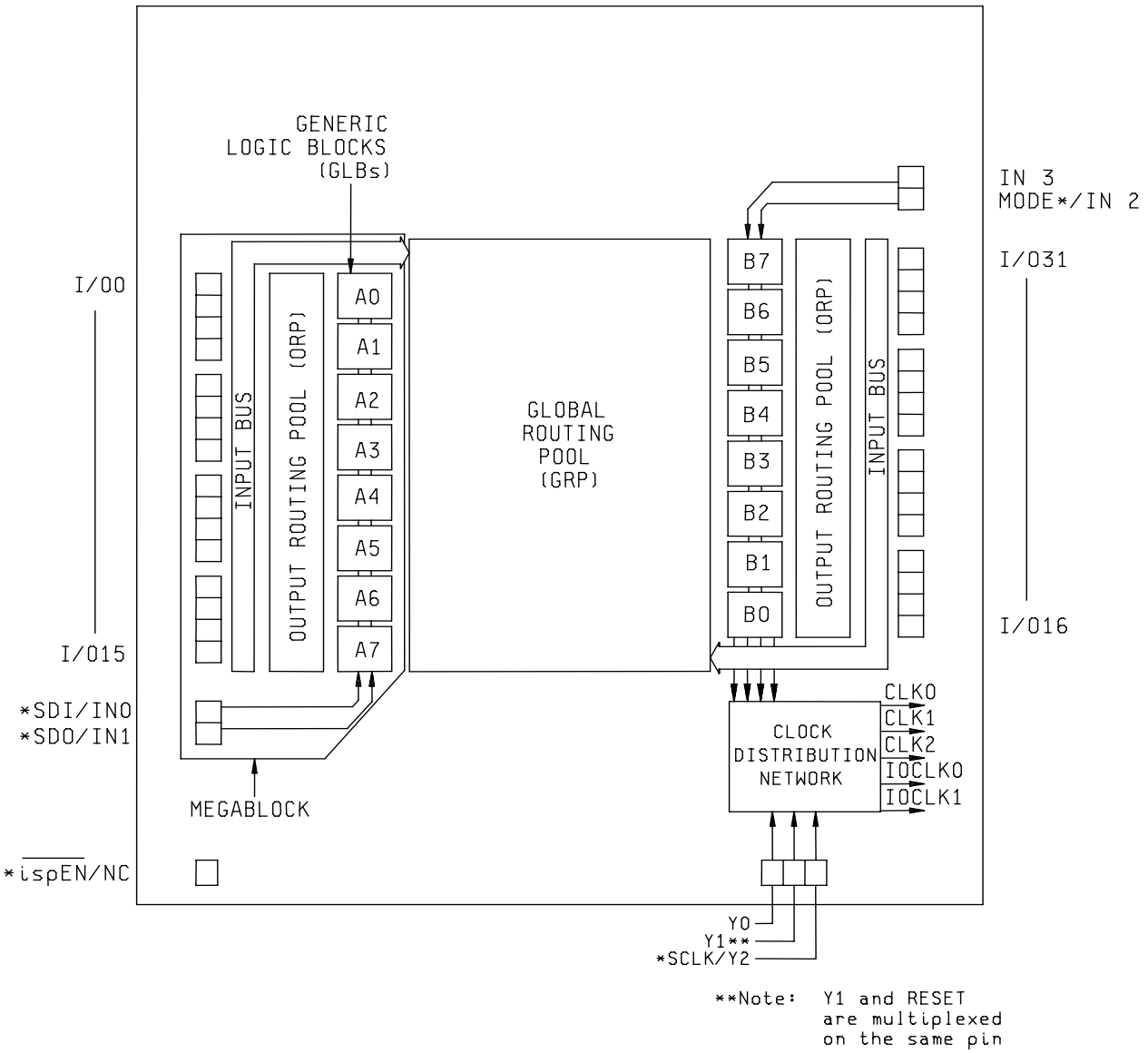
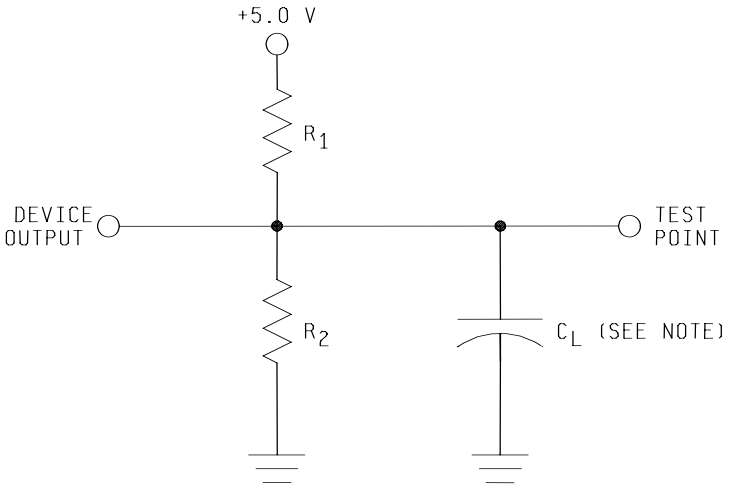


FIGURE 3. Functional block diagram.



Test	R_1	R_2	C_L
t_{PZH}	∞	390Ω	35pF
t_{PZL}	470Ω	390Ω	35pF
t_{PHZ} (at V_{OH} - 0.5 V)	∞	390Ω	5pF
t_{PLZ} (at V_{OL} + 0.5 V)	470Ω	390Ω	5pF
All others	470Ω	390Ω	35pF

Note: C_L includes test fixture and probe capacitance.

FIGURE 4. Switching times test circuit and waveforms.

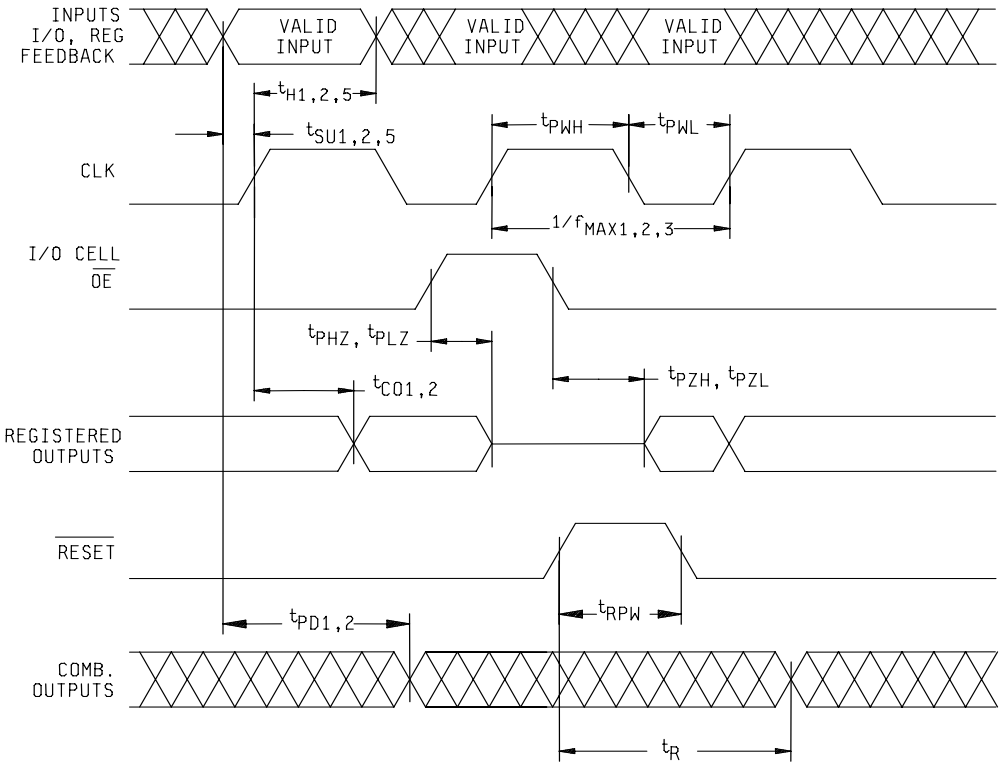


FIGURE 4. Switching times test circuit and waveforms - continued.

3.11 Processing of EEPLDs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Conditions of the supplied devices. Devices will be supplied in cleared state per truth table on figure 2. No provision will be made for supplying written devices.

3.11.2 Writing of EEPLDs. When specified, devices shall be written in accordance with the procedures and characteristics specified in 4.6.

3.11.3 Clearing of EEPLDs. When specified, devices shall be cleared in accordance with the procedures and characteristics specified in 4.7.

3.11.4 Verification of state of EEPLDs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but will guarantee the number of program/erase endurance cycles listed in section 1.3 herein. The vendor's procedure shall be under document control and shall be made available upon request.

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability process. This test shall be done initially and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but will guarantee the number of years listed in section 1.3 herein. The vendors procedure shall be under document control and shall be made available upon request. Data retention capability shall be guaranteed over the full military temperature range.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

(2) Devices shall be burned-in containing a pattern that assures all inputs and I/O's are dynamically switched. This pattern must have all cells programmed in a high or low state (not neutralized).

(3) The burn-in pattern shall be read before and after burn-in. Devices having any logic array bits not in the proper state shall constitute a device failure and shall be added as failures for PDA calculation.

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

d. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7, 8A and 8B shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN}, $C_{I/O}$, and C_Y measurements) shall be measured only for initial qualification and after any process or design changes which may affect input, I/O, or clock capacitance. Capacitance shall be measured between the designated terminal and GND per table I. Sample size is 5 devices with no failures, and all input, I/O, and clock terminals tested.

f. I_{OS} measurements in subgroup 1 may be measured only for the initial test and after process or design changes which may affect I_{OS}. Sample size is 15 devices with no failures, and all I/O terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. All devices shall be programmed with a pattern that assures all inputs and I/O's are dynamically switched.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroups 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 7).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{IL}	±100% of specified limit in table I.
I_{IH}	±100% of specified limit in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroup 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

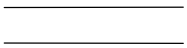
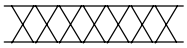
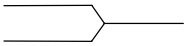
6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the device are specified from the device point of view. Thus, the data propagation delay is shown as a maximum since the device never changes states later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Additional operating data.

6.6.1 In-system programming voltage/timing characteristics. The in-system programming voltage/timing characteristics are as specified in table III and figure 5.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. In-system programming voltage/timing characteristics.

Parameter	Symbol	Conditions $0°C \le T_A \le +70°C$ unless otherwise specified	Device type	Limits		Units
				Min	Max	
Programming voltage	V_{CCP}		All	4.75	5.25	V
Programming supply current	I_{CCP}		All		100	mA
High level input voltage	V_{IHP}	isp $\overline{EN}$ = V_{IHL}	All	2.0	V_{CCP}	V
Low level input voltage	V_{ILP}		All	0	0.8	V
Input current	I_{IP}		All		200	µA
High level output voltage	V_{OHP}		All	2.4	V_{CCP}	V
Low level output voltage	V_{OLP}	I_{OH} = -3.2 mA	All	0	0.5	V
Input rise and fall times	t_r, t_f	I_{OL} = 5.0 mA	All		0.1	µs
isp $\overline{EN}$ to output three-state	t_{en}	See figure 5	All		10	µs
isp $\overline{EN}$ to output active	t_{dis}		All		10	µs
Setup time	t_{su}		All	0.1		µs
Clock to output delay	t_{co}		All	0.1		µs
Hold time	t_h		All	0.1		µs
Clock pulse width, high or low	t_{clkh}, t_{clkl}		All	0.5		µs
Verify pulse width	t_{pwv}		All	20		µs
Programming pulse width	t_{pwp}		All	40	100	ms
Bulk erase pulse width	t_{bew}		All	200		ms
Reset time from valid V_{CCP}	t_{rst}		All	45		µs

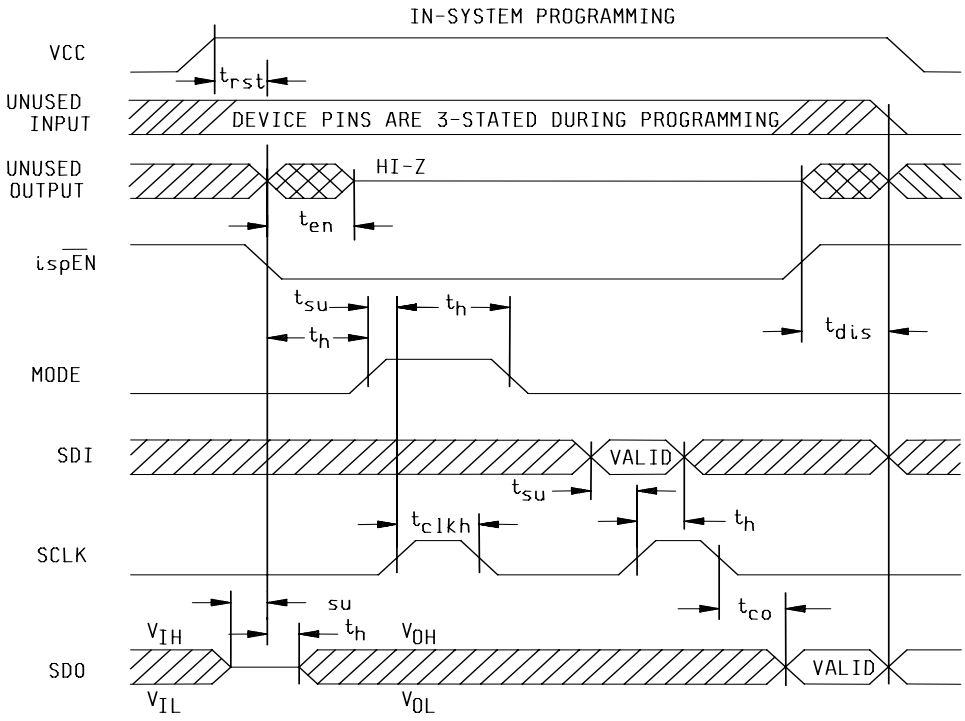


FIGURE 5. In-system programming waveforms.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-07-09

Approved sources of supply for SMD 5962-94762 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9476201MXC	66675	ispLSI1016-60LH/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
66675	Lattice Semiconductor Corporation 5555 NE. Moore Court Hillsboro, OR 97124-6421

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.