Ultralow Power, 2-Channel, Capacitance Converter for Proximity Sensing

FEATURES

- Ultra-low power
  - 2.7 V to 3.6 V, 100 µA
- Response time: 10 ms
- Adaptive environmental compensation
- 2 independent capacitance input channels
  - Sensor capacitance (C_{SENS}) 0 pF up to 13 pF
  - Sensitivity to 1 fF
- EMC tested
- 2 modes of operation
  - Standalone with fixed settings
  - Interfaced to a microcontroller for user-defined settings
- 2 proximity detection output flags
- 2-wire serial interface (I^2C compatible)
- Operating temperature
  - −40°C to +85°C
- 10-lead MSOP package

APPLICATIONS

- Proximity sensing
- Contactless switching
- Position detection
- Level detection

GENERAL DESCRIPTION

The AD7150 delivers a complete signal processing solution for capacitive proximity sensors, featuring an ultra-low power converter with fast response time. The AD7151 is a single-channel, lower power alternative to the AD7150.

The AD7150 uses Analog Devices, Inc., capacitance-to-digital converter (CDC) technology, which combines features important for interfacing to real sensors, such as high input sensitivity and high tolerance of both input parasitic ground capacitance and leakage current.

The integrated adaptive threshold algorithm compensates for any variations in the sensor capacitance due to environmental factors like humidity and temperature or due to changes in the dielectric material over time.

By default, the AD7150 operates in standalone mode using the fixed power-up settings and indicates detection on two digital outputs. Alternatively, the AD7150 can be interfaced to a microcontroller via the serial interface, the internal registers can be programmed with user-defined settings, and the data and status can be read from the part.

The AD7150 operates with a 2.7 V to 3.6 V power supply. It is specified over the temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

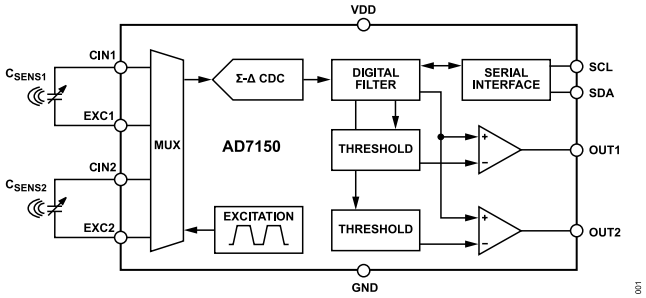

Figure 1.

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REVISION HISTORY

7/2026—Rev. A to Rev. B

Changed Master to Controller and Slave to Target (Throughout) ... 1
Changes to Table 11 ... 19
Changes to Table 13 ... 20
Changes to Address Pointer 0x13, 0x14, 0x15, 0x16 32 Bits, Read-Only, 0xXXXX Section ... 21

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SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V; GND = 0 V; –40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
CAPACITIVE INPUT					
Conversion Input Range CIN to EXC[2]	3.2	4		pF	4 pF input range
	1.6	2		pF	2 pF input range
	0.8	1		pF	1 pF input range
	0.4	0.5		pF	0.5 pF input range
Resolution[3]		2.0		fF	4 pF input range
		1.6		fF	2 pF input range
		1.4		fF	1 pF input range
		1.0		fF	0.5 pF input range
Allowed Capacitance CIN to GND[3]			100	pF	
Allowed Resistance CIN to GND[3]	10			MΩ	
Allowed Serial Resistance[3]			125	kΩ	
Gain Error	−20		+20	%	
Gain Deviation over Temperature[3]		0.5		%	
Gain Matching Between Ranges[3]	−2		+2	%	
Offset Error[3]		50		fF	CIN and EXC pins disconnected
Offset Deviation over Temperature[3]		5		fF	CIN and EXC pins disconnected
Integral Nonlinearity (INL)[3]		0.1		%	
Channel-to-Channel Isolation[3]		60		dB	
Power Supply Rejection[3]		4		fF/V	
CAPDAC[2]					
Full Range	10	12.5		pF	
Resolution (LSB)[3]		200		fF	
Differential Nonlinearity (DNL)[3]			0.25	LSB	
AutoDAC Increment/Decrement[3]	25		75	% of C_{IN} Range	
EXCITATION					
Voltage		±V_{DD}/2		V	
Frequency	30.9	32	32.8	kHz	
Allowed Capacitance EXC to GND[3]			300	pF	
Allowed Resistance EXC to GND[3]	1			MΩ	
LOGIC OUTPUTS (OUT1, OUT2)					
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = −4 mA
Output High Voltage (V_{OH})	V_{DD} – 0.6			V	I_{SOURCE} = 4 mA
SERIAL INTERFACE INPUTS (SCL, SDA)					
Input High Voltage (V_{IH})	1.5			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Leakage Current		±0.1	±5	µA	
Input Pin Capacitance		6		pF	
OPEN-DRAIN OUTPUT (SDA)					
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = −6.0 mA
Output High Leakage Current (I_{OH})		0.1	5	µA	V_{OUT} = V_{DD}
POWER SUPPLY MONITOR					
V_{DD} Threshold Voltage		2.45	2.65	V	
POWER REQUIREMENTS					
V_{DD}-to-GND Voltage	2.7		3.6	V	V_{DD} = 3.3 V, nominal
I_{DD} Current[4]		100	120	µA	
I_{DD} Current Power-Down Mode[4]		1	5	µA	Temperature ≤ 25°C

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SPECIFICATIONS

Table 1. (Continued)

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
		3	10	µA	Temperature = 85°C

1 Capacitance units: one picofarad (1 pF) = 1 × 10^{-12} farad (F); one femtofarad (1 fF) = 10^{-15} farad (F).

2 The CAPDAC can be used to shift (offset) the input range. The total capacitance of the sensor can therefore be up to the sum of the CAPDAC value and the conversion input range. With the autoCAPDAC feature, the CAPDAC is adjusted automatically when the CDC input value is lower than 25% or higher than 75% of the CDC nominal input range.

3 Specification is not production tested but is supported by characterization data at initial product release.

4 Digital inputs equal to V_{DD} or GND.

TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V; GND = 0 V; Input Logic 0 = 0 V; Input Logic 1 = V_{DD}; –40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CONVERTER					
Conversion Time			10	ms	Both channels, 5 ms per channel.
Wake-Up Time from Power-Down Mode[1, 2]		0.15		ms	
Power-Up Time[1, 3]		2		ms	
Reset Time[1, 4]		2		ms	
SERIAL INTERFACE[5, 6]					See Figure 2.
SCL Frequency	0		400	kHz	
SCL High Pulse Width, t_{HIGH}	0.6			µs	
SCL Low Pulse Width, t_{LOW}	1.3			µs	
SCL, SDA Rise Time, t_R			0.3	µs	
SCL, SDA Fall Time, t_F			0.3	µs	
Hold Time (Start Condition), $t_{HD;STA}$	0.6			µs	After this period, the first clock is generated.
Setup Time (Start Condition), $t_{SU;STA}$	0.6			µs	Relevant for repeated start condition.
Data Setup Time, $t_{SU;DAT}$	0.1			µs	
Setup Time (Stop Condition), $t_{SU;STO}$	0.6			µs	
Data Hold Time (Controller), $t_{HD;DAT}$	10			ns	
Bus-Free Time (Between Stop and Start Condition), t_{BUF}	1.3			µs	

1 Specification is not production tested but is supported by characterization data at initial product release.

2 Wake-up time is the maximum delay between the last SCL edge writing the configuration register and the start of conversion.

3 Power-up time is the maximum delay between the V_{DD} crossing the minimum level (2.7 V) and either the start of conversion or when ready to receive a serial interface command.

4 Reset time is the maximum delay between the last SCL edge writing the reset command and either the start of conversion or when ready to receive a serial interface command.

5 Sample tested during initial release to ensure compliance.

6 All input signals are specified with input rise/fall times = 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Output load = 10 pF.

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SPECIFICATIONS

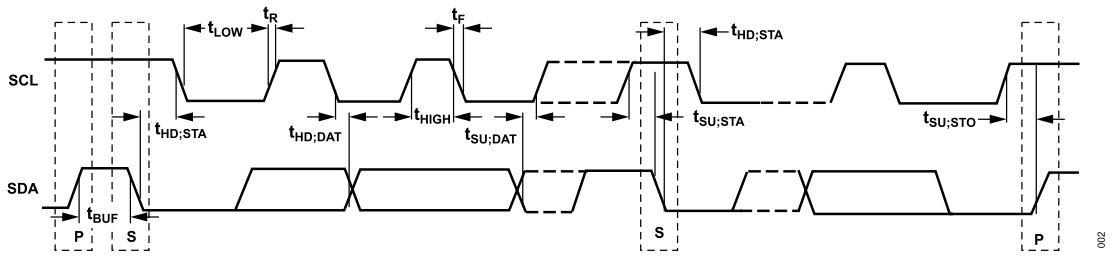

Figure 2. Serial Interface Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Positive Supply Voltage V_{DD} to GND	−0.3 V to +3.9 V
Voltage on Any Input or Output to GND	–0.3 V to V_{DD} + 0.3 V
ESD Rating HBM (ESD Association Human Body Model, S5.1)	4 kV
ESD Rating FICDM (Field-Inducted Charged Device Model)	1 kV
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature	150°C
MSOP Package	
θ_{JA}, Thermal Impedance-to-Air	206°C/W
θ_{JC}, Thermal Impedance-to-Case	44°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

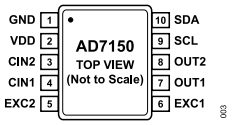

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Pin.
2	VDD	Power Supply Voltage. This pin should be decoupled to GND using a low impedance capacitor, for example, 0.1 µF X7R multilayer ceramic.
3	CIN2	CDC Capacitive Input Channel 2. The measured capacitance (sensor) is connected between the EXC2 pin and the CIN2 pin. If not used, this pin can be left open circuit or connected to GND.
4	CIN1	CDC Capacitive Input Channel 1. The measured capacitance (sensor) is connected between the EXC1 pin and the CIN1 pin. If not used, this pin can be left open circuit or connected to GND.
5	EXC2	CDC Excitation Output Channel 2. The measured capacitance is connected between the EXC2 pin and the CIN2 pin. If not used, this pin should be left as an open circuit.
6	EXC1	CDC Excitation Output Channel 1. The measured capacitance is connected between the EXC1 pin and the CIN1 pin. If not used, this pin should be left as an open circuit.
7	OUT1	Logic Output Channel 1. A high level on this output indicates proximity detected on CIN1.
8	OUT2	Logic Output Channel 2. A high level on this output indicates proximity detected on CIN2.
9	SCL	Serial Interface Clock Input. Connects to the controller clock line. Requires a pull-up resistor if not provided elsewhere in the system.
10	SDA	Serial Interface Bidirectional Data. Connects to the controller data line. Requires a pull-up resistor if not provided elsewhere in the system.

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TYPICAL PERFORMANCE CHARACTERISTICS

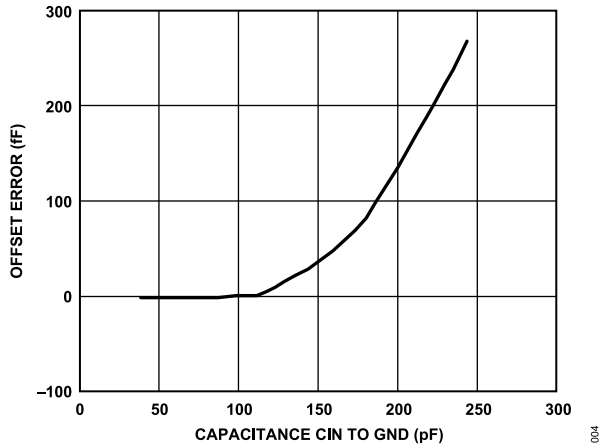

Figure 4. Capacitance Input Offset Error vs. Capacitance CIN to GND, V_{DD} = 3.3 V, EXC Pin Open Circuit

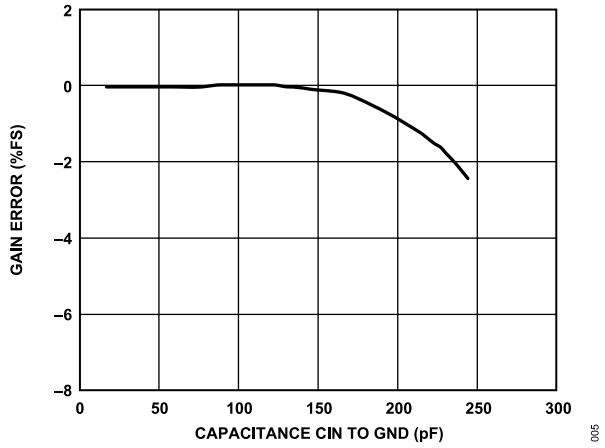

Figure 5. Capacitance Input Gain Error vs. Capacitance CIN to GND, V_{DD} = 3.3 V, CIN to EXC = 2 pF

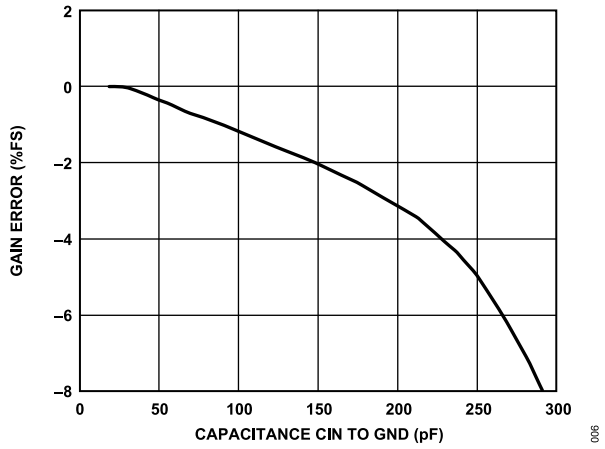

Figure 6. Capacitance Input Gain Error vs. Capacitance CIN to GND, V_{DD} = 3.3 V, CIN to EXC = 10 pF

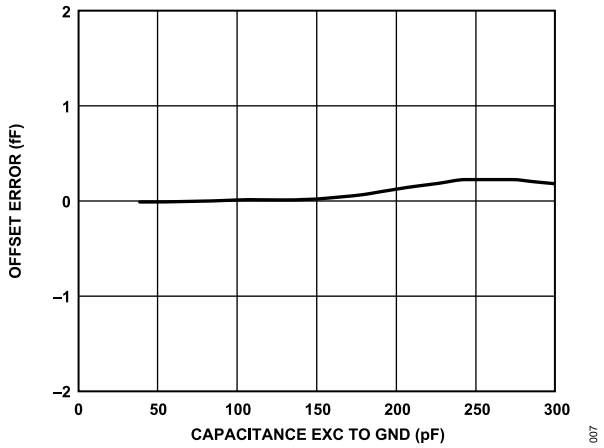

Figure 7. Capacitance Input Offset Error vs. Capacitance EXC to GND, V_{DD} = 3.3 V, CIN Pin Open Circuit

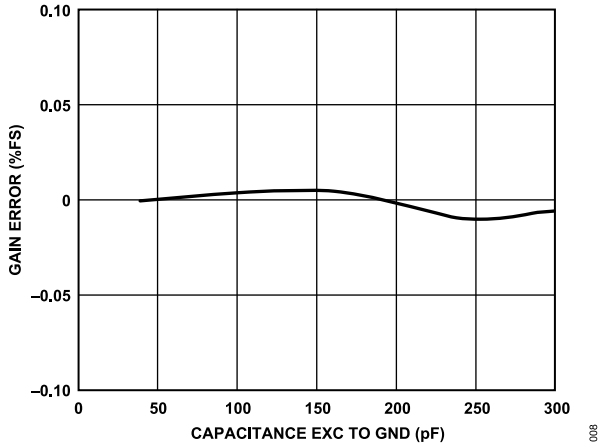

Figure 8. Capacitance Input Gain Error vs. Capacitance EXC to GND, V_{DD} = 3.3 V, CIN to EXC = 2 pF

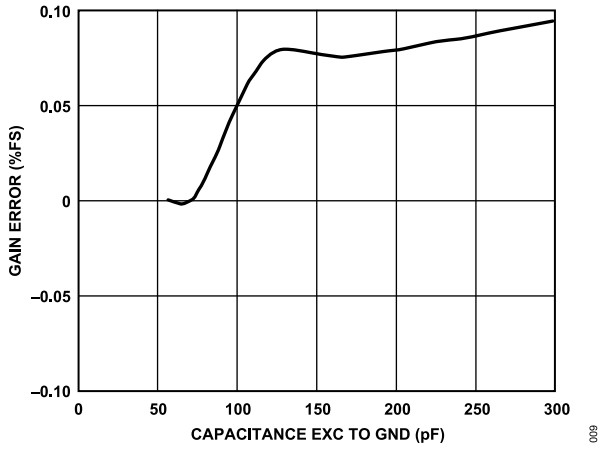

Figure 9. Capacitance Input Gain Error vs. Capacitance EXC to GND, V_{DD} = 3.3 V, CIN to EXC = 10 pF

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TYPICAL PERFORMANCE CHARACTERISTICS

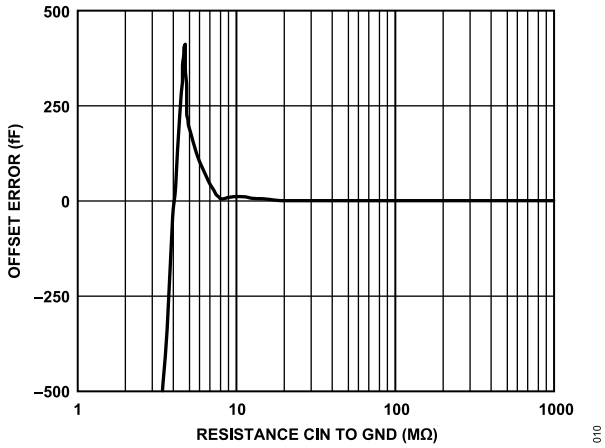

Figure 10. Capacitance Input Offset Error vs. Resistance CIN to GND, V_{DD} = 3.3 V, EXC Pin Open Circuit

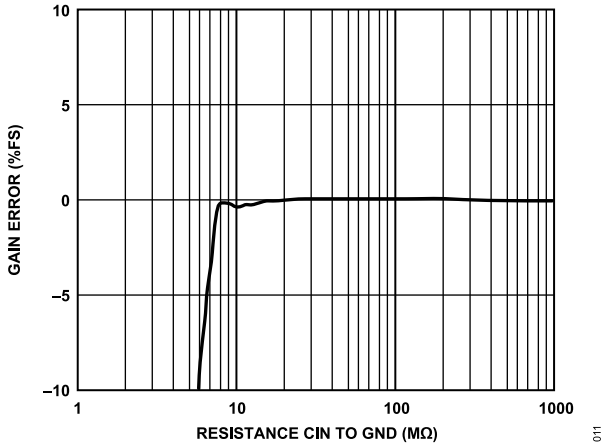

Figure 11. Capacitance Input Gain Error vs. Resistance CIN to GND, V_{DD} = 3.3 V, CIN to EXC = 2 pF

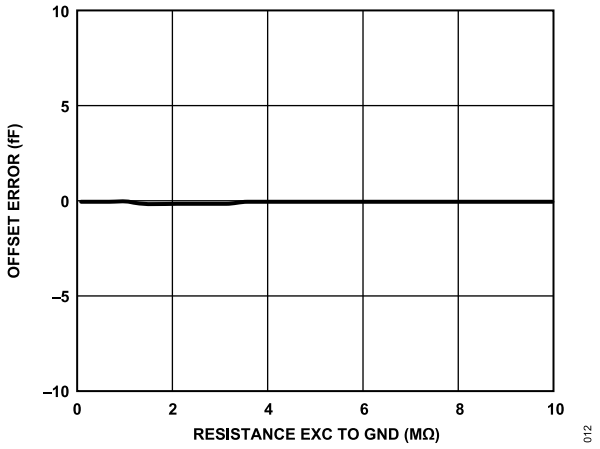

Figure 12. Capacitance Input Offset Error vs. Resistance EXC to GND, V_{DD} = 3.3 V, CIN Pin Open Circuit

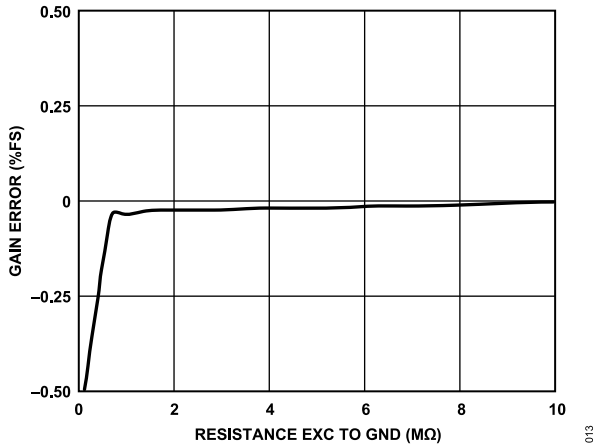

Figure 13. Capacitance Input Gain Error vs. Resistance EXC to GND, V_{DD} = 3.3 V, CIN to EXC = 2 pF

Figure 14. Capacitance Input Gain Error vs. Serial Resistance, V_{DD} = 3.3 V, CIN to EXC = 2 pF

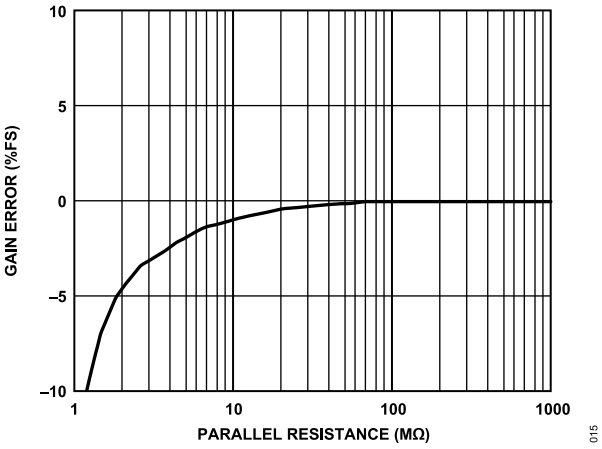

Figure 15. Capacitance Input Gain Error vs. Parallel Resistance, V_{DD} = 3.3 V, CIN to EXC = 2 pF

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TYPICAL PERFORMANCE CHARACTERISTICS

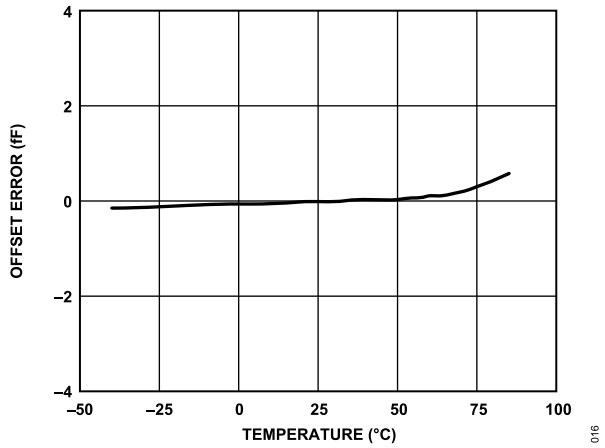

Figure 16. Capacitance Input Offset Error vs. Temperature, V_{DD} = 3.3 V, CIN and EXC Pins Open Circuit

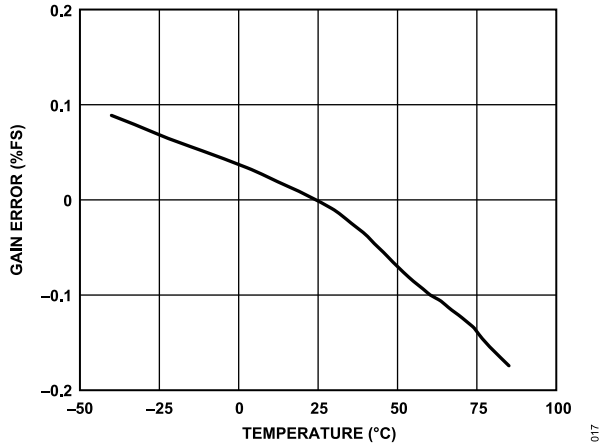

Figure 17. Capacitance Input Gain Error vs. Temperature, V_{DD} = 3.3 V, CIN to EXC = 2 pF

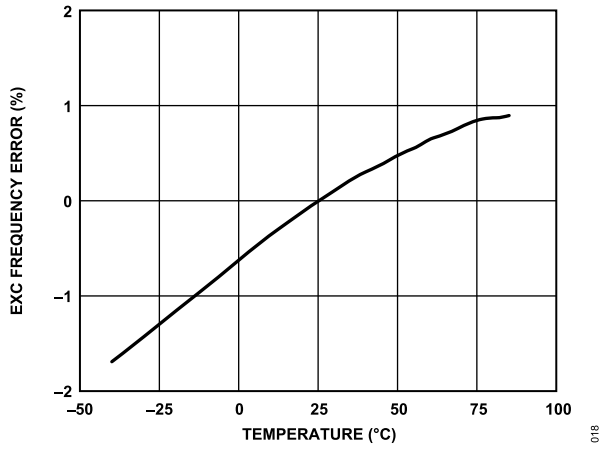

Figure 18. EXC Frequency Error vs. Temperature, V_{DD} = 3.3 V

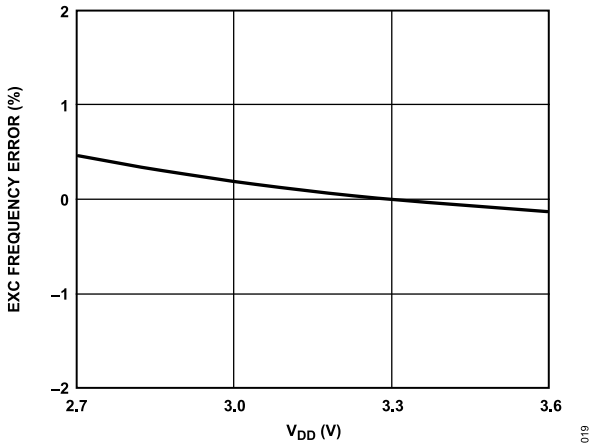

Figure 19. EXC Frequency Error vs. V_{DD}

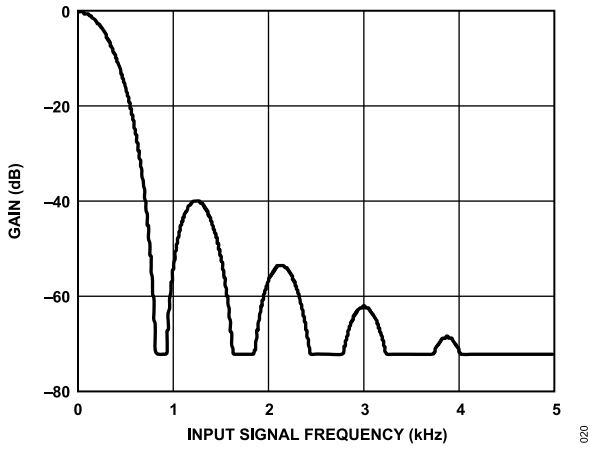

Figure 20. Capacitance Channel Frequency Response

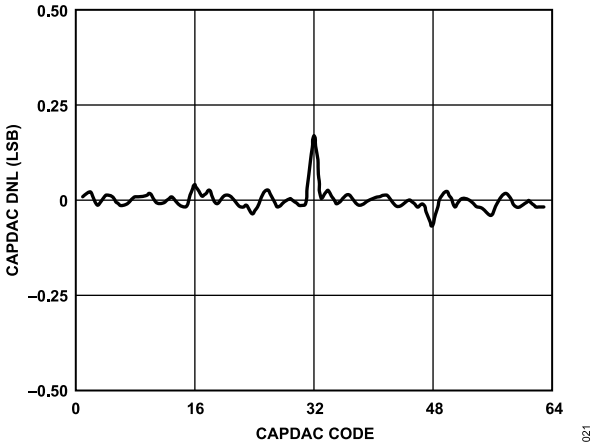

Figure 21. CAPDAC Differential Nonlinearity (DNL), V_{DD} = 3.3 V

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ARCHITECTURE AND MAIN FEATURES

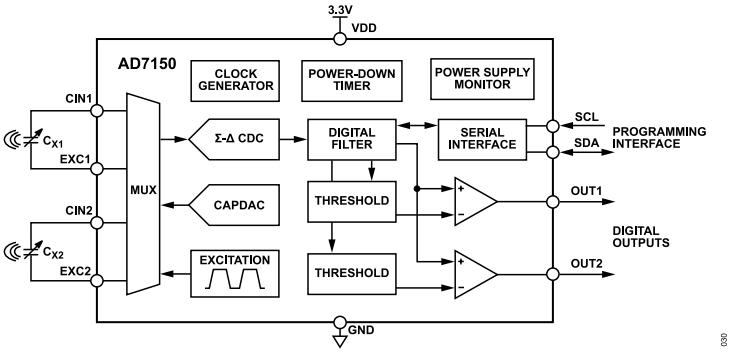

Figure 22. AD7150 Block Diagram

The AD7150 core is a high performance capacitance-to-digital converter (CDC) that allows the part to be interfaced directly to a capacitive sensor.

The comparators compare the CDC result with thresholds, either fixed or dynamically adjusted by the on-chip adaptive threshold algorithm engine. Thus, the outputs indicate a defined change in the input sensor capacitance.

The AD7150 also integrates an excitation source and CAPDAC for the capacitive inputs, an input multiplexer, a complete clock generator, a power-down timer, a power supply monitor, control logic, and an I^{2}C®-compatible serial interface for configuring the part and accessing the internal CDC data and status, if required in the system (see Figure 22).

CAPACITANCE-TO-DIGITAL CONVERTER

Figure 23 shows the CDC simplified functional diagram. The converter consists of a second-order sigma delta (Σ-Δ), charge balancing modulator and a third-order digital filter. The measured capacitance C_X is connected between an excitation source and the Σ-Δ modulator input. The excitation signal is applied on the C_X during the conversion, and the modulator continuously samples the charge going through the C_X. The digital filter processes the modulator output, which is a stream of 0s and 1s containing the information in 0 and 1 density. The data is processed by the adaptive threshold engine and output comparators; the data can be also read through the serial interface.

The AD7150 is designed for floating capacitive sensors. Therefore, both C_X plates have to be isolated from ground or any other fixed potential node in the system.

The AD7150 features slew rate limiting on the excitation voltage output, which decreases the energy of higher harmonics on the excitation signal and dramatically improves the system electromagnetic compatibility (EMC).

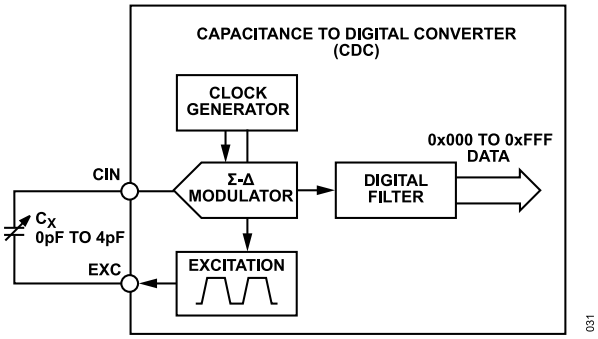

Figure 23. CDC Simplified Block Diagram

CAPDAC

The AD7150 CDC core maximum full-scale input range is 4 pF. However, the part can accept a higher capacitance on the input, and the offset (nonchanging component) capacitance of up to 10 pF can be balanced by a programmable on-chip CAPDAC.

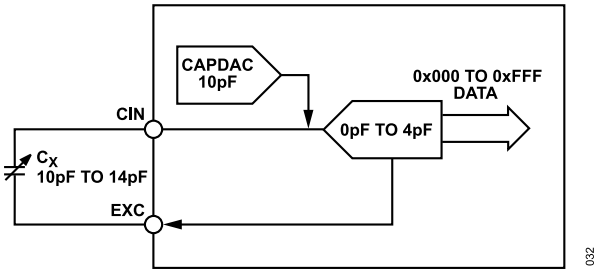

Figure 24. Using CAPDAC

The CAPDAC can be understood as a negative capacitance connected internally to the CIN pin. The CAPDAC has a 6-bit resolution and a monotonic transfer function. Figure 24 shows how to use the CAPDAC to shift the CDC 4 pF input range to measure capacitance between 10 pF and 14 pF.

COMPARATOR AND THRESHOLD MODES

The AD7150 comparators and their thresholds can be programmed to operate in several different modes. In an adaptive mode, the threshold is dynamically adjusted and the comparator output indicates fast changes and ignores slow changes in the input (sensor)

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capacitance. Alternatively, the threshold can be programmed as a constant (fixed) value, and the output then indicates any change in the input capacitance that crosses the defined fixed threshold.

The AD7150 logic output (active high) indicates either a positive or a negative change in the input capacitance, in both adaptive and fixed threshold modes (see Figure 25 and Figure 26).

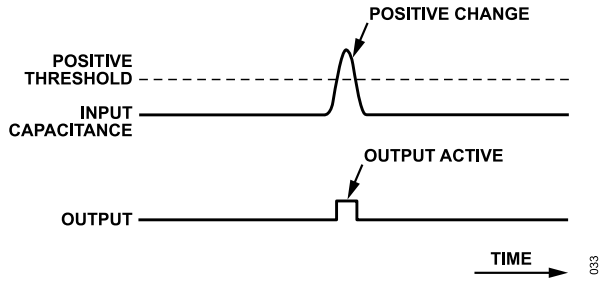

Figure 25. Positive Threshold Mode Indicates Positive Change in Input Capacitance

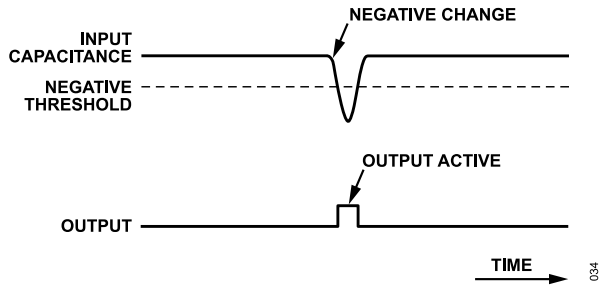

Figure 26. Negative Threshold Mode Indicates Negative Change in Input Capacitance

Additionally, for the adaptive mode only, the comparators can work as window comparators, indicating input either inside or outside a selected sensitivity band (see Figure 27 and Figure 28).

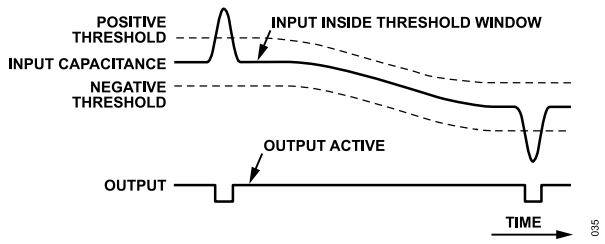

Figure 27. In-Window (Adaptive) Threshold Mode

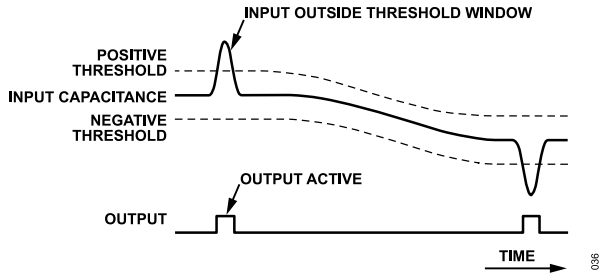

Figure 28. Out-Window (Adaptive) Threshold Mode

ADAPTIVE THRESHOLD

In an adaptive mode, the thresholds are dynamically adjusted, ensuring indication of fast changes (for example, an object moving close to a capacitive proximity sensor) and eliminating slow changes in the input (sensor) capacitance, usually caused by environment changes such as humidity or temperature or changes in the sensor dielectric material over time (see Figure 29).

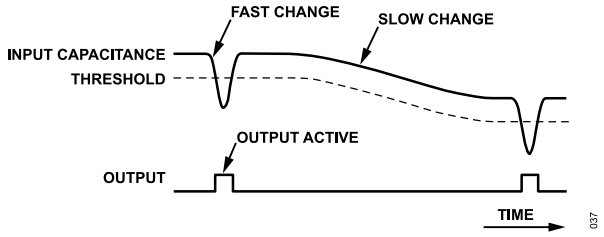

Figure 29. Adaptive Threshold Indicates Fast Changes and Eliminates Slow Changes in Input Capacitance

DATA AVERAGE

The adaptive threshold algorithm is based on an average calculated from previous CDC output data. The response of the average to an input capacitance step change (more exactly, response to the change in the CDC output data) is an exponential settling curve, which can be characterized by the following equation:

$$Average(N) = Average(0) + Change(1 - e^{N/TimeConst}) \quad (1)$$

where:

Average(*N*) is the value of average N complete CDC conversion cycles after a step change on the input.

Average(0) is the value before the step change.

TimeConst can be selected in the range between 2 and 65,536, in steps of power of 2, by programming the ThrSettling bits in the setup registers.

See Figure 30 and the Register Descriptions section.

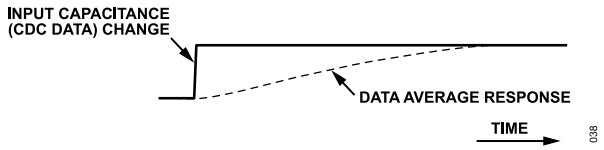

Figure 30. Data Average Response to Data Step Change

SENSITIVITY

In adaptive threshold mode, the output comparator threshold is set as a defined distance (sensitivity) above the data average, below the data average, or both, depending on the selected threshold mode of operation (see Figure 31). The sensitivity value is programmable in the range 0 to 255 LSBs of the 12-bit CDC converter (see the Register Descriptions section).

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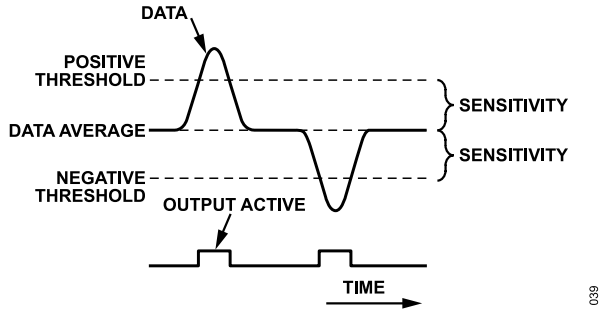

Figure 31. Threshold Sensitivity

HYSTERESIS

In adaptive threshold mode, the comparator features hysteresis. The hysteresis is fixed to one-fourth of the threshold sensitivity and can be programmed on or off. The comparator does not have hysteresis in the fixed threshold mode.

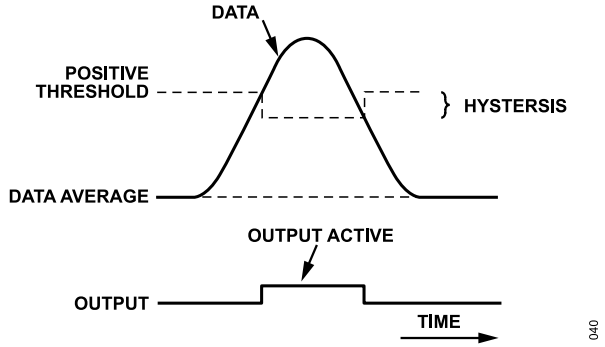

Figure 32. Threshold Hysteresis

TIMEOUT

In the case of a large, long change in the capacitive input, when the data average adapting to a new condition may take too long, a timeout can be set.

The timeout becomes active (counting) when the CDC data goes outside the band of data average ± sensitivity. When the timeout elapses (a defined number of CDC conversions is counted), the data average (and thus the thresholds), is forced to follow the new CDC data value immediately (see Figure 33).

The timeout can be set independently for approaching (for change in data toward the threshold) and for receding (for change in data away from the threshold). See Figure 34, Figure 35, and the Register Descriptions section.

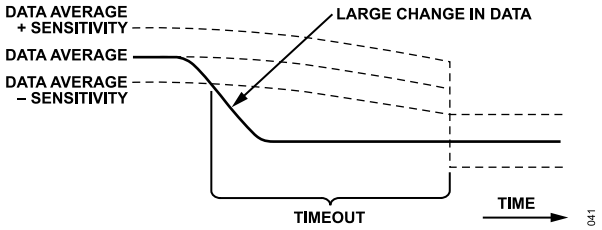

Figure 33. Threshold Timeout After a Large Change in CDC Data

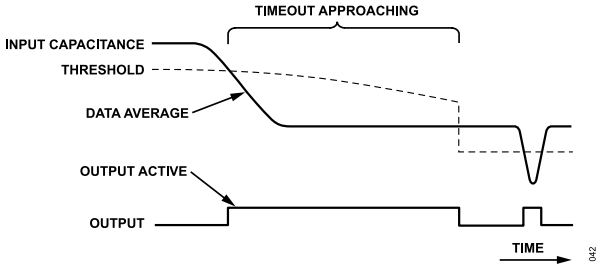

Figure 34. Approaching Timeout in Negative Threshold Mode Shortens False Output Trigger

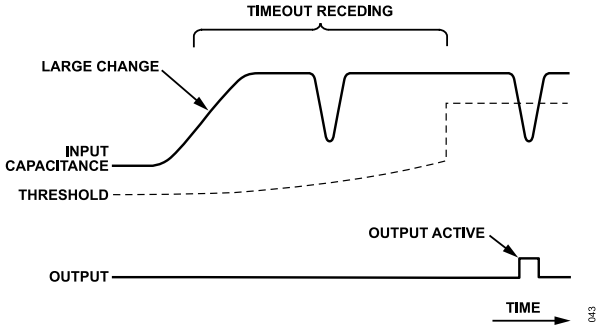

Figure 35. Positive Timeout in Negative Threshold Mode Shortens Period of Missing Output Trigger

AUTOCAPDAC ADJUSTMENT

In adaptive threshold mode, the part can dynamically adjust the CAPDAC to keep the CDC in an optimal operating capacitive range. When the AutoDAC function is enabled, the CAPDAC value is automatically incremented when the data average exceeds three-fourths of the CDC full range, and the CAPDAC value is decremented when the data average goes below one-fourth of the CDC full range. The AutoDAC increment or decrement step depends on the selected CDC capacitive input range. See the Setup Registers section.

POWER-DOWN TIMER

In power sensitive applications, the AD7150 can be set to automatically enter power-down mode after a programmed period of time in which the outputs have not been activated. The AD7150 can be then returned to a normal operational mode either via the serial interface or by the power supply off/on sequence.

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POWER SUPPLY MONITOR

When the AD7150 V_{DD} power supply voltage drops below a defined level needed for correct CDC operation, the on-chip power supply monitor stops the adaptive threshold logic and holds it in reset. After the V_{DD} reaches the required level, the threshold logic is released, and the data average is reset to the value of the first conversion finished at the correct power supply voltage.

This feature prevents the adaptive threshold from being set incorrectly after a very slow rise of the V_{DD} voltage or from being corrupted by accidental drops in the V_{DD} voltage.

The other AD7150 functions continue working below the power supply monitor threshold, down to approximately 1.0 V to 1.8 V, the exact level depending on the manufacturing process variation. In the region of the low V_{DD} voltage, the part is still accessible via the serial interface and continues conversion. However, the conversion results may be incorrect and, therefore, the data should not be considered valid if the part operates below the power supply monitor threshold.

The status of the power supply monitor can be determined by reading the PwrDown bit in the AD7150 status register.

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REGISTER DESCRIPTIONS

Table 5. Register Summary

Register	Pointer (Dec)	Pointer (Hex)	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				Default Value							
Status	0	0x00	R	PwrDown	$\overline{\text{DacStep2}}$	OUT2	$\overline{\text{DacStep1}}$	OUT1	C1/C2	$\overline{\text{RDY2}}$	$\overline{\text{RDY1}}$
				0	1	0	1	0	0	1	1
Ch1 Data High	1	0x01	R	0x00							
Ch1 Data Low	2	0x02	R	0x00							
Ch2 Data High	3	0x03	R	0x00							
Ch2 Data Low	4	0x04	R	0x00							
Ch1 Average High	5	0x05	R	0x00							
Ch1 Average Low	6	0x06	R	0x00							
Ch2 Average High	7	0x07	R	0x00							
Ch2 Average Low	8	0x08	R	0x00							
Ch1 Sensitivity	9	0x09	R/W	Ch1 Sensitivity (in adaptive threshold mode)/Threshold High Byte (in fixed threshold mode)							
Ch1 Threshold High				0x08							
Ch1 Timeout	10	0x0A	R/W	Ch1 Timeout (in adaptive threshold mode)/Threshold Low Byte (in fixed threshold mode)							
Ch1 Threshold Low				0x86							
Ch1 Setup	11	0x0B	R/W	RngH1	RngL1	–	$\overline{\text{Hyst1}}$	ThrSettling1 (4-bit value)			
				0	0	0	0	0x0B			
Ch2 Sensitivity	12	0x0C	R/W	Ch2 Sensitivity (in adaptive threshold mode)/Threshold High Byte (in fixed threshold mode)							
Ch2 Threshold High				0x08							
Ch2 Timeout	13	0x0D	R/W	Ch2 Timeout (in adaptive threshold mode)/Threshold Low Byte (in fixed threshold mode)							
Ch2 Threshold Low				0x86							
Ch2 Setup	14	0x0E	R/W	RngH2	RngL2	–	$\overline{\text{Hyst2}}$	ThrSettling2 (4-bit value)			
				0	0	0	0	0x0B			
Configuration	15	0x0F	R/W	ThrFixed	ThrMD1	ThrMD0	EnCh1	EnCh2	MD2	MD1	MD0
				0	0	0	1	1	0	0	1
Power-Down Timer	16	0x10	R/W	–	–	Power-Down Timeout (6-bit value)					
				0	0	0x00					
Ch1 CAPDAC	17	0x11	R/W	DacEn1	DacAuto1	DacValue1 (6-bit value)					
				1	1	0x00					
Ch2 CAPDAC	18	0x12	R/W	DacEn2	DacAuto2	DacValue2 (6-bit value)					
				1	1	0x00					
Serial Number 3	19	0x13	R	Serial Number – Byte 3 (MSB)							
Serial Number 2	20	0x14	R	Serial Number – Byte 2							
Serial Number 1	21	0x15	R	Serial Number – Byte 1							
Serial Number 0	22	0x16	R	Serial Number – Byte 0 (LSB)							
Chip ID	23	0x17	R	Chip Identification Code							

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REGISTER DESCRIPTIONS

STATUS REGISTER

Address Pointer 0x00
8 Bits, Read-Only, Default Value 0x53 Before Conversion, 0x54 After Conversion

The status register indicates the status of the part. The register can be read via the 2-wire serial interface to query the status of the outputs, check the CDC finished conversion, and check whether the CAPDAC has been changed by the autoCAPDAC function.

Table 6. Status Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	PwrDown	$\overline{\text{DacStep2}}$	OUT2	$\overline{\text{DacStep1}}$	OUT1	C1/C2	$\overline{\text{RDY2}}$	$\overline{\text{RDY1}}$
Default	0	1	0	1	0	0	1	1

Table 7. Status Register Bit Descriptions

Bit	Mnemonic	Description
7	PwrDown	PwrDown = 1 indicates that the part is in a power-down mode or that the part V_{DD} is below the power supply monitor threshold voltage.
6	$\overline{\text{DacStep2}}$	$\overline{\text{DacStep2}}$ = 0 indicates that the Ch2 CAPDAC value was changed after the last CDC conversion as part of the AutoDac function. The bit value is updated after each finished CDC conversion on this channel.
5	OUT2	OUT2 = 1 indicates that the Ch2 data (CIN2 capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion on this channel.
4	$\overline{\text{DacStep1}}$	$\overline{\text{DacStep1}}$ = 0 indicates that the Ch1 CAPDAC value was changed during the last conversion as part of the AutoDac function. The bit value is updated after each finished CDC conversion on this channel.
3	OUT1	OUT1 = 1 indicates that the Ch1 data (CIN1 capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion on this channel.
2	C1/C2	The C1/C2 = 0 indicates that the last finished CDC conversion was on Channel 1.The C1/C2 = 1 indicates that the last finished CDC conversion was on Channel 2.
1	$\overline{\text{RDY2}}$	$\overline{\text{RDY2}}$ = 0 indicates a finished CDC conversion on Ch2. The bit is reset back to 1 when the Ch2 data register is read via the serial interface or after the part reset or power-up.
0	$\overline{\text{RDY1}}$	$\overline{\text{RDY1}}$ = 0 indicates a finished CDC conversion on Ch1. The bit is reset back to 1 when the Ch1 data register is read via serial interface or after the part reset or power-up.

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REGISTER DESCRIPTIONS

DATA REGISTERS

Ch1 Address Pointer 0x01, 0x02
Ch2 Address Pointer 0x03,0x04
16 Bits, Read-Only, Default Value 0x0000

Data from the last complete capacitance-to-digital conversion reflects the capacitance on the input. Only the 12 MSBs (most significant bits) of the data registers are used for the CDC result. The 4 LSBs (least significant bits) are always 0, as shown in Figure 36.

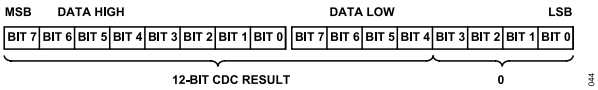

Figure 36. CDC Data Register

The nominal AD7150 CDC transfer function (an ideal transfer function excluding offset and/or gain error) maps the input capacitance between zero scale and full scale to output data codes between 0x3000 and 0xCFF0 only (see Table 8).

Table 8. AD7150 Capacitance-to-Data Mapping

Data	Input Capacitance
0x0000	Not valid, underrange
0x3000	Zero-scale (0 pF)
0x8000	Mid-scale (+1 pF)
0xCFF0	Full-scale (+2 pF)
0xFFF0	Not valid, overrange

The input capacitance can be calculated from the output data using the following equation:

$$C(\text{pF}) = \frac{Data - 12288}{40944} \times Input_Range \quad (2)$$

where *Input_Range* = 4 pF, 2 pF, 1 pF, or 0.5 pF.

The following is the same equation written with hexadecimal numbers:

$$C(\text{pF}) = \frac{Data - 0x3000}{0x9FF0} \times Input_Range \quad (3)$$

A data register is updated after a finished conversion on the capacitive channel, with one exception: when the serial interface read operation from the data register is in progress, the data register is not updated and the new capacitance conversion result is lost.

The stop condition on the serial interface is considered to be the end of the read operation. Therefore, to prevent incorrect data reading through the serial interface, the two bytes of a data register should be read sequentially using the register address pointer auto-increment feature of the serial interface.

AVERAGE REGISTERS

Ch1 Address Pointer 0x05, 0x06
Ch2 Address Pointer 0x07,0x08
16 Bits, Read-Only, Default Value 0x0000

These registers show the average calculated from the previous CDC data. The 12-bit CDC result corresponds to the 12 MSBs of the average register.

The settling time of the average can be set by programming the ThrSettling bits in the setup registers. The average register is overwritten directly with the CDC output data, that is, the history is forgotten if the timeout is enabled and elapses.

FIXED THRESHOLD REGISTERS

Ch1 Address Pointer 0x09, 0x0A
Ch2 Address Pointer 0x0C,0x0D
16 Bits, Read/Write, Factory Preset 0x0886

A constant threshold for the output comparator in the fixed threshold mode can be set using these registers. The 12-bit CDC result corresponds to the 12 MSBs of the threshold register. The fixed threshold registers share the address pointer and location on-chip with the sensitivity and timeout registers. The fixed threshold registers are not accessible in the adaptive threshold mode.

SENSITIVITY REGISTERS

Ch1 Address Pointer 0x09
Ch2 Address Pointer 0x0C
8 Bits, Read/Write, Factory Preset 0x08

Sensitivity registers set the distance of the positive threshold above the data average, and the distance of the negative threshold below the data average, in the adaptive threshold mode.

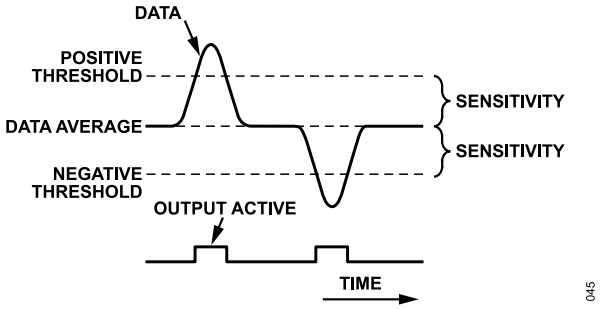

Figure 37. Threshold Sensitivity

The sensitivity is an 8-bit value and is mapped to the lower eight bits of the 12-bit CDC data, that is, it corresponds to the 16-bit data register as shown in Figure 38.

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REGISTER DESCRIPTIONS

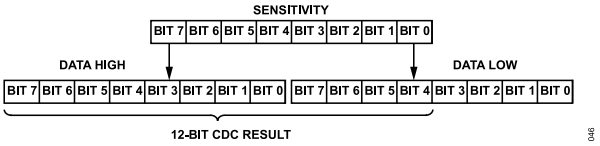

Figure 38. Relation Between Sensitivity Register and CDC Data Register

TIMEOUT REGISTERS

Ch1 Address Pointer 0x0A
Ch2 Address Pointer 0x0D
8 Bits, Read/Write, Factory Preset 0x86

Table 9. Timeout Register Bit Map

Bit	Bits [7:4]	Bits [3:0]
Mnemonic	TimeOutApr	TimeOutRec
Default	0x08	0x06

These registers set timeouts for the adaptive threshold mode.

The approaching timeout starts when the CDC data crosses the data average ± sensitivity band toward the threshold, according to the selected positive, negative, or window threshold mode. The approaching timeout elapses after the number of conversion cycles equals $2^{TimeOutApr}$, where TimeOutApr is the value of the four most significant bits of the timeout register.

The receding timeout starts when the CDC data crosses the data average ± sensitivity band away from the threshold, according to the selected positive or negative threshold mode. The receding timeout is not used in the window threshold mode. The receding timeout elapses after the number of conversion cycles equals $2^{TimeOutRec}$, where TimeOutRec is the value of the four least significant bits of the timeout register.

When either the approaching or receding timeout elapses (that is, after the defined number of CDC conversions is counted), the data average (and thus the thresholds) is forced to follow the new CDC data value immediately.

When the timeout register equals 0, timeouts are disabled.

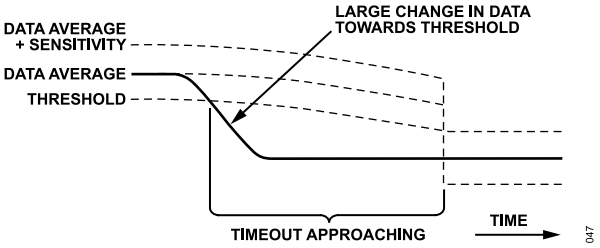

Figure 39. Threshold Timeout Approaching After a Large Change in CDC Data Toward Threshold

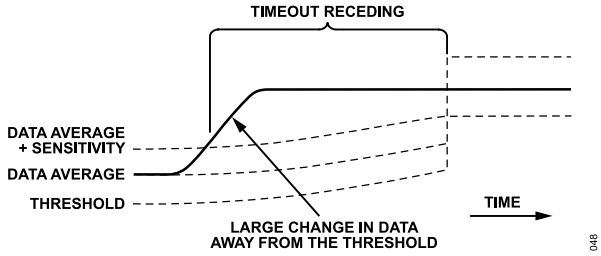

Figure 40. Threshold Timeout Receding After a Large Change in CDC Data Away from Threshold

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REGISTER DESCRIPTIONS

SETUP REGISTERS

Ch1 Address Pointer 0x0B
Ch2 Address Pointer 0x0E
8 Bits, Read/Write, Factory Preset 0x0B

Table 10. Setup Registers Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	RngH	RngL	–	$\overline{\text{Hyst}}$	ThrSettling (4-Bit Value)			
Default	0	0	0	0	0x0B			

Table 11. Setup Registers Bit Descriptions

Bit	Mnemonic	Description
[7:6]	RngH RngL	Range bits set the CDC input range and determine the step for the AutoDAC function. RngH, RngL, Capacitive Input Range (pF), AutoDAC Step (CAPDAC LSB) 0, 0, 2, 4 0, 1, 0.5, 1 1, 0, 1, 2 1, 1, 4, 8
5	–	This bit should be 0 for the specified operation.
4	$\overline{\text{Hyst}}$	$\overline{\text{Hyst}}$ = 1 disables hysteresis in adaptive threshold mode. This bit has no effect in fixed threshold mode; hysteresis is always disabled in the fixed threshold mode.
[3:0]	ThrSettling	Determines the settling time constant of the data average and thus the settling time of the adaptive thresholds.The response of the average to an input capacitance step change (that is, response to the change in the CDC output data) is an exponential settling curve characterized by the following equation: $Average(N) = Average(0) + Change(1 - e^{N/TimeConst})$ where: *Average(N)* is the value of average N complete CDC conversion cycles after a step change on the input. *Average(0)* is the value before the step change. *TimeConst* can be selected in the range between 2 and 65,536 conversion cycle multiples, in steps of power of 2, by programming the ThrSettling bits. $TimeConst = 2^{(ThrSettling + 1)}$ See Figure 41.

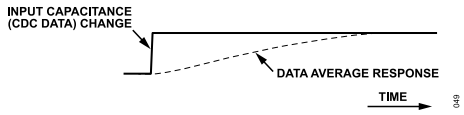

Figure 41. Data Average Response to Data Step Change

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REGISTER DESCRIPTIONS

CONFIGURATION REGISTER

Address Pointer 0x0F
8 Bits, Read/Write, Factory Preset 0x19

Table 12. Configuration Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	ThrFixed	ThrMD1	ThrMD0	EnCh1	EnCh2	MD2	MD1	MD0
Default	0	0	0	1	1	0	0	1

Table 13. Configuration Register Bit Descriptions

Bit	Mnemonic	Description
7	ThrFixed	ThrFixed = 1 sets the fixed threshold mode. The outputs reflect comparison of data and a fixed (constant) value of the threshold registers. ThrFixed = 0 sets the adaptive threshold mode. The outputs reflect comparison of data to the adaptive thresholds. The adaptive threshold is set dynamically, based on the history of the previous data.
[6:5]	ThrMD1 ThrMD0	These bits set the output comparators mode.

ThrMD1	ThrMD0	Threshold Mode	Output Active When: Adaptive Threshold Mode	Output Active When: Fixed Threshold Mode
0	0	Negative	data < average – sensitivity	Data < Threshold
0	1	Positive	data > average + sensitivity	Data > Threshold
1	0	In-Window	data > average – sensitivity AND data < average + sensitivity	–
1	1	Out-Window	data < average – sensitivity OR data > average + sensitivity	–

Bit	Mnemonic	Description
4	EnCh1	Enables conversion on Channel 1.
3	EnCh2	Enables conversion on Channel 2.
[2:0]	MD2 MD1 MD0	Converter mode of operation setup.

MD2	MD1	MD0	Mode	Description
0	0	0	Idle	Part is fully powered up but performing no conversion.
0	0	1	Continuous Conversion	Part is repeatedly performing conversions on the enabled channel(s). If two channels are enabled, the part is sequentially switching between them.
0	1	0	Single Conversion	Part performs a single conversion on the enabled channel. If two channels are enabled, the part performs two conversions, one on each channel. After finishing the conversion(s), the part goes to the idle mode.
0	1	1	Power-Down	Powers down the on-chip circuits, except the digital interface.
1	X	X	Reserved	Do not use these modes.

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REGISTER DESCRIPTIONS

POWER-DOWN TIMER REGISTER

Address Pointer 0x10
8 Bits, Read/Write, Factory Preset 0x00

Table 14. Power-Down Timer Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	Power-Down Timeout (6-Bit Value)					
Default	0	0	0x00					

Table 15. Power-Down Timer Register Bit Descriptions

Bit	Mnemonic	Description
[7:6]	–	These bits must be 0 for proper operation.
[5:0]	Power-Down Timeout	Defines period duration of the power-down timeout. If the output comparator outputs have not been activated during the programmed period, the part enters power-down mode automatically. The part can be then returned to a normal operational mode either via the serial interface or by the power supply off/on sequence. The period is programmable in steps of four hours. For example, setting the value to 0x06 sets the duration to 24 hours. The maximum value of 0x3F corresponds to approximately 10.5 days. The value of 0x00 disables the power-down timeout, and the part does not enter power-down mode automatically.

CAPDAC REGISTERS

Ch1 Address Pointer 0x11
Ch2 Address Pointer 0x12
8 Bits, Read/Write, Factory Preset 0x00

Table 16. CAPDAC Registers Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DacEn	DacAuto	DacValue (6-Bit Value)					
Default	1	1	0x00					

Table 17. CAPDAC Registers Bit Descriptions

Bit	Mnemonic	Description
7	DacEn	DacEn = 1 enables capacitive DAC.
6	DacAuto	DacAuto = 1 enables the AutoDAC function in the adaptive threshold mode. When the AutoDAC function is enabled, the part dynamically adjusts the CAPDAC to keep the CDC in an optimal operating capacitive range. The CAPDAC value is automatically incremented when the data average exceeds ¾ of the CDC full range, and the CAPDAC value is decremented when the data average goes below ¼ of the CDC full range. The AutoDAC increment or decrement step depends on the selected CDC capacitive input range. Bit has no effect in fixed threshold mode; the AutoDAC function is always disabled in the fixed threshold mode.
[5:0]	DacValue	CAPDAC value, Code 0x00 ≈ 0 pF, Code 0x3F ≈ CAPDAC full range.

SERIAL NUMBER REGISTER

Address Pointer 0x13, 0x14, 0x15, 0x16
32 Bits, Read-Only, 0xXXXX

This register contains a 32-bit serial number code used in factory manufacturing and test processes. The value is not guaranteed to be unique.

CHIP ID REGISTER

Address Pointer 0x17
8 Bits, Read-Only, 0xXX

This register holds the chip identification code, used in factory manufacturing and testing.

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SERIAL INTERFACE

The AD7150 supports an I^{2}C-compatible, 2-wire serial interface. The two wires on the serial bus (interface) are called SCL (clock) and SDA (data). These two wires carry all addressing, control, and data information one bit at a time over the bus to all connected peripheral devices. The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the data transfer. The devices on the bus are classified as either controller or target devices. A device that initiates a data transfer message is called a controller, while a device that responds to this message is called a target.

To control the AD7150 device on the bus, the following protocol must be followed. First, the controller initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that the start byte follows. This 8-bit start byte is made up of a 7-bit address plus an R/W bit indicator.

All peripherals connected to the bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The bits arrive MSB first. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. An exception to this is the general call address, which is described in the General Call section. In the idle condition, the device monitors the SDA and SCL lines waiting for the start condition and the correct address byte.

The R/W bit determines the direction of the data transfer. A Logic 0 LSB in the start byte means that the controller writes information to the addressed peripheral. In this case, the AD7150 becomes a target receiver. A Logic 1 LSB in the start byte means that the controller reads information from the addressed peripheral. In this case, the AD7150 becomes a target transmitter. In all instances, the AD7150 acts as a standard target device on the serial bus.

The start byte address for the AD7150 is 0x90 for a write and 0x91 for a read.

READ OPERATION

When a read is selected in the start byte, the register that is currently addressed by the address pointer is transmitted to the SDA line by the AD7150. This is then clocked out by the controller device, and the AD7150 awaits an acknowledge from the controller.

If an acknowledge is received from the controller, the address auto-incrementer automatically increments the address pointer register and outputs the next addressed register content to the SDA line for transmission to the controller. If no acknowledge is received, the AD7150 returns to the idle state and the address pointer is not incremented. The address pointers' auto-incrementer allows block data to be written to or read from the starting address and subsequent incremental addresses.

In continuous conversion mode, the address pointers' auto-incrementer should be used for reading a conversion result. This means that the two data bytes should be read using one multibyte read transaction rather than two separate single byte transactions. The single byte data read transaction may result in the data bytes from two different results being mixed. The same applies for four data bytes if both capacitive channels are enabled.

The user can also access any unique register (address) on a one-to-one basis without having to update all the registers. The address pointer register contents cannot be read.

If an incorrect address pointer location is accessed or if the user allows the auto-incrementer to exceed the required register address, the following applies:

- In read mode, the AD7150 continues to output various internal register contents until the controller device issues a no acknowledge, start, or stop condition. The address pointers' auto-incrementer contents are reset to point to the status register at the 0x00 address when a stop condition is received at the end of a read operation. This allows the status register to be read (polled) continually without having to constantly write to the address pointer.
- In write mode, the data for the invalid address is not loaded into the AD7150 registers, but an acknowledge is issued by the AD7150.

WRITE OPERATION

When a write is selected, the byte following the start byte is always the register address pointer (subaddress) byte, which points to one of the internal registers on the AD7150. The address pointer byte is automatically loaded into the address pointer register and acknowledged by the AD7150. After the address pointer byte acknowledge, a stop condition, a repeated start condition, or another data byte can follow from the controller. A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If a stop condition is encountered by the AD7150, it returns to its idle condition and the address pointer is reset to 0x00.

If a data byte is transmitted after the register address pointer byte, the AD7150 loads this byte into the register that is currently addressed by the address pointer register and sends an acknowledge, and the address pointer auto-incrementer automatically increments the address pointer register to the next internal register address. Thus, subsequent transmitted data bytes are loaded into sequentially incremented addresses.

If a repeated start condition is encountered after the address pointer byte, all peripherals connected to the bus respond exactly as outlined previously for a start condition; that is, a repeated start condition is treated the same as a start condition. When a controller device issues a stop condition, it relinquishes control of the bus, allowing another controller device to take control of the bus. Therefore, a controller wanting to retain control of the bus issues successive start conditions known as repeated start conditions.

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SERIAL INTERFACE

AD7150 RESET

To reset the AD7150 without having to reset the entire serial bus, an explicit reset command is provided. This uses a particular address pointer word as a command word to reset the part and upload all default settings. The AD7150 does not respond to the serial bus commands (do not acknowledge) during the default values upload for approximately 2 ms.

The reset command address word is 0xBF.

GENERAL CALL

When a controller issues a target address consisting of seven 0s with the eighth bit (R/W bit) set to 0, this is known as the general call address. The general call address is for addressing every device connected to the serial bus. The AD7150 acknowledges this address and reads in the following data byte.

If the second byte is 0x06, the AD7150 is reset, completely uploading all default values. The AD7150 does not respond to the serial bus commands (do not acknowledge) during the default values upload for approximately 2 ms.

The AD7150 does not acknowledge any other general call commands.

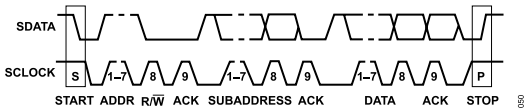

Figure 42. Bus Data Transfer

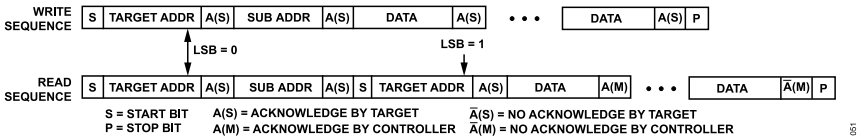

Figure 43. Write and Read Sequences

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HARDWARE DESIGN CONSIDERATIONS

OVERVIEW

The AD7150 is an interface to capacitive sensors.

On the input side, the sensor (C_X) can be connected directly between the AD7150 EXC and CIN pins. The way it is connected and the electrical parameters of the sensor connection, such as parasitic resistance or capacitance, can affect the system performance. Therefore, any circuit with additional components in the capacitive front end, such as overvoltage protection, has to be carefully designed considering the AD7150 specified limits and information provided in this section.

On the output side, the AD7150 can work as a standalone device, using the power-up default register settings and flagging the result on digital outputs. Alternatively, the AD7150 can be interfaced to a microcontroller via the 2-wire serial interface, offering flexibility by overwriting the AD7150 register values from the host with a user-specific setup.

PARASITIC CAPACITANCE TO GROUND

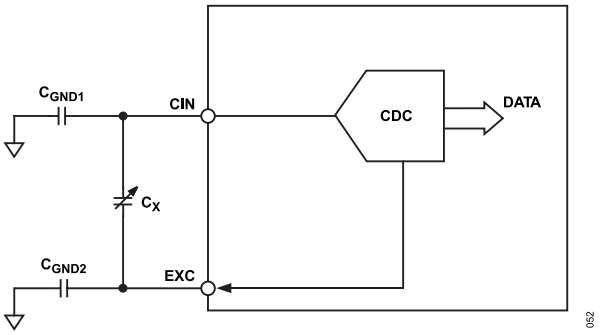

Figure 44. Parasitic Capacitance to Ground

The CDC architecture used in the AD7150 measures the capacitance, C_X, connected between the EXC pin and the CIN pin. In theory, any capacitance C_{GND} to ground should not affect the CDC result (see Figure 44).

The practical implementation of the circuitry in the chip implies certain limits, and the result is gradually affected by capacitance to ground (see Table 1 for information about the allowed capacitance to GND for CIN and information about excitation).

See Figure 4 to Figure 9.

PARASITIC RESISTANCE TO GROUND

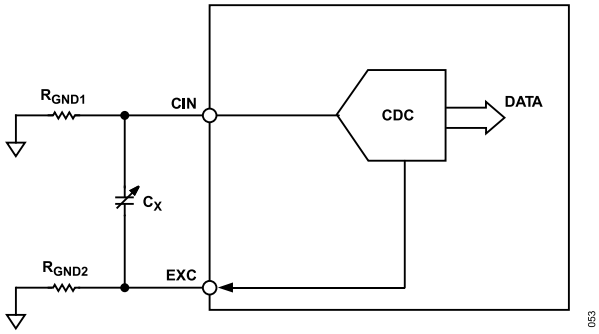

Figure 45. Parasitic Resistance to Ground

The AD7150 CDC result is affected by a leakage current from C_X to ground; therefore, C_X should be isolated from the ground. The equivalent resistance between C_X and ground should be maximized (see Figure 45).

See Figure 10 to Figure 13.

PARASITIC PARALLEL RESISTANCE

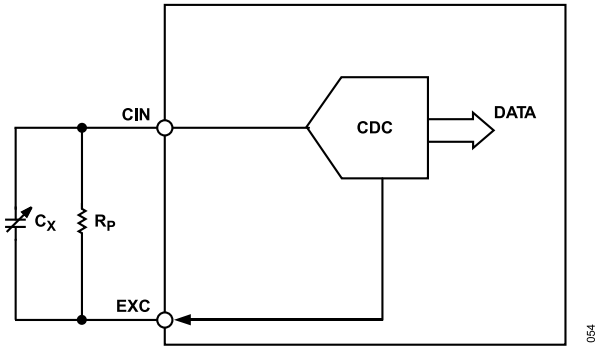

Figure 46. Parasitic Parallel Resistance

The AD7150 CDC measures the charge transfer between the EXC and CIN pins. Any resistance connected in parallel to the measured capacitance C_X (see Figure 46), such as the parasitic resistance of the sensor, also transfers charge. Therefore, the parallel resistor is seen as an additional capacitance in the output data. The equivalent parallel capacitance (or error caused by the parallel resistance) can be approximately calculated as

$$C_P = \frac{1}{R_P \times f_{EXC} \times 4} \quad (4)$$

where R_P is the parallel resistance and f_{EXC} is the excitation frequency.

See Figure 15.

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HARDWARE DESIGN CONSIDERATIONS

PARASITIC SERIAL RESISTANCE

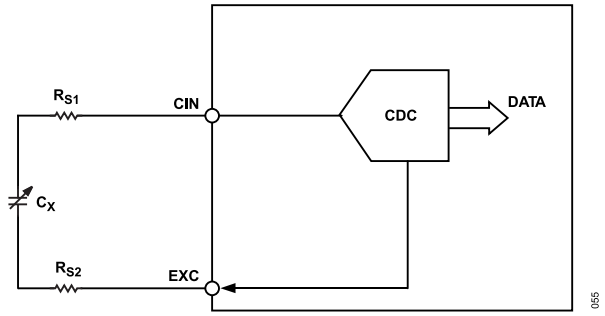

Figure 47. Parasitic Serial Resistance

The AD7150 CDC result is affected by a resistance in series with the measured capacitance. The total serial resistance (R_{S1} + R_{S2} in Figure 47) should be on the order of hundreds of Ω.

See Figure 14.

INPUT OVERVOLTAGE PROTECTION

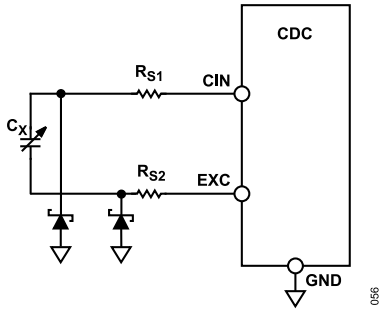

Figure 48. AD7150 CIN Overvoltage Protection

The AD7150 capacitive input has an internal ESD protection. However, some applications may require an additional overvoltage protection, depending on the application-specific requirements. Any additional circuit in the capacitive front end must be carefully designed, especially with respect to the limits recommended for maximum capacitance to ground, maximum serial resistance, maximum leakage, and so on.

INPUT EMC PROTECTION

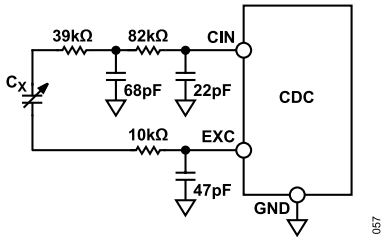

Figure 49. AD7150 CIN EMC Protection

Some applications may require an additional input filter for improving electromagnetic compatibility (EMC). Any input filter must be carefully designed, considering the balance between the system capacitance performance and system electromagnetic immunity.

Figure 49 shows one of the possible input circuit configurations significantly improving the system immunity against high frequency noise and slightly affecting the AD7150 performance in terms of additional gain and offset error.

POWER SUPPLY DECOUPLING AND FILTERING

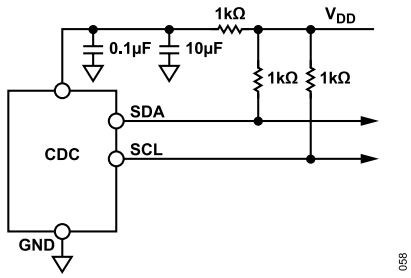

Figure 50. AD7150 V_{DD} Decoupling and Filtering

The AD7150 has good dc and low frequency power supply rejection but may be sensitive to higher frequency ripple and noise, specifically around the excitation frequency and its harmonics. Figure 50 shows a possible circuit configuration for improving the system immunity against ripple and noise coupled to the AD7150 via the power supply.

If the serial interface is connected to the other circuits in the system, it is better to connect the pull-up resistors on the other side of the V_{DD} filter than to connect to the AD7150. If the AD7150 is used in standalone mode and the serial interface is not used, it is better to connect the pull-up resistors directly to the AD7150 V_{DD}.

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HARDWARE DESIGN CONSIDERATIONS

APPLICATION EXAMPLES

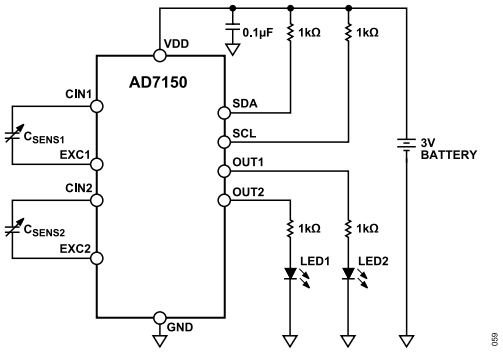

Figure 51. AD7150 Standalone Operation Application Diagram

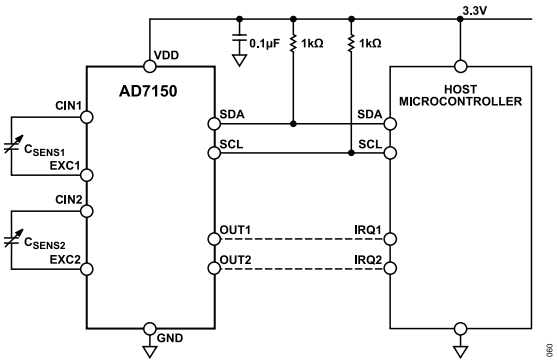

Figure 52. AD7150 Interfaced to a Host Microcontroller

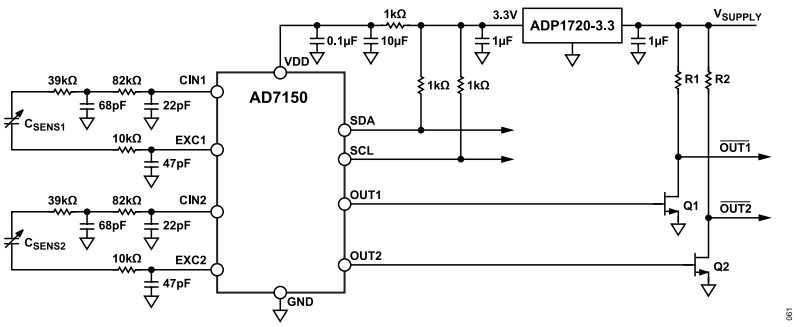

Figure 53. AD7150 Standalone Operation with EMC Protection

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OUTLINE DIMENSIONS

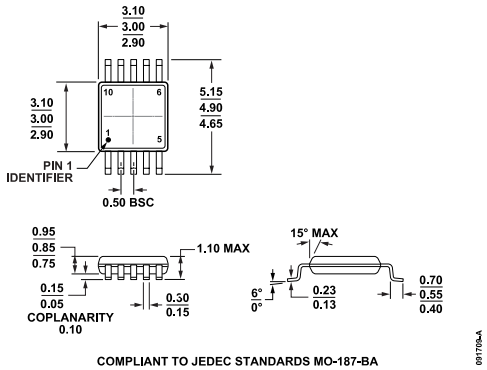

Figure 54. 10-Lead Mini Small Outline Package [MSOP] (RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
AD7150BRMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C4Z
AD7150BRMZ-REEL	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C4Z

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-AD7150EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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