

MOSFET – Power, Dual N- & P-Channel, SO8

100 V, 83 mΩ, 4.5 A,
-100 V, 131 mΩ, -3.6 A

NTMC083NP10M5L

Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- The Part is Not ESD Protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- Motor Drive, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise specified)

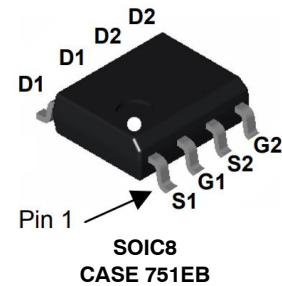
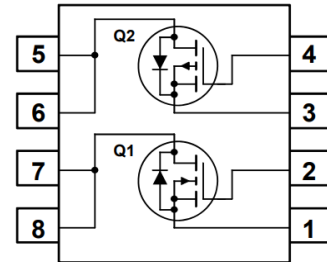
Parameter			Symbol	Q1	Q2	Unit
Drain-to-Source Breakdown Voltage			$V_{(BR)DSS}$	100	-100	V
Gate-to-Source Voltage			V_{GS}	± 20	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	4.1	-3.3	A
		$T_C = 100\text{ }^{\circ}\text{C}$		2.5	-2	
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	3.1	3.1	W
		$T_C = 100\text{ }^{\circ}\text{C}$		1.2	1.2	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	2.9	-2.4	A
		$T_A = 100\text{ }^{\circ}\text{C}$		1.8	-1.4	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	1.6	1.6	W
		$T_A = 100\text{ }^{\circ}\text{C}$		0.6	0.6	
Pulsed Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$		I_{DM}	20	20	A
Operating Junction and Storage Temperature Range			T_J , T_{stg}	-55 to +150		$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	3	3	A
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 6\text{ A}$, 8.2 A , $L = 1\text{ mH}$)			E_{AS}	18	34	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T_L	260	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

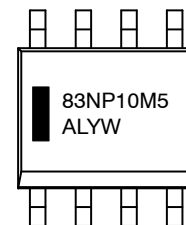
1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	83 mΩ @ 10 V	4.5 A
-100 V	131 mΩ @ 10 V	-3.6 A

Dual-Channel MOSFET



MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Junction-to-Case-Steady State (Note 3)	40	40	°C/W
$R_{\theta JA}$	Junction-to-Ambient-Steady State (Note 3)	78	78	

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS (Q1, N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		60		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 28\text{ }\mu\text{A}$	1.0	1.9	3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = 22\text{ }\mu\text{A}$, ref to 25°C		8.2		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$		59.4	83	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 1.2\text{ A}$		96.3	118	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 4\text{ A}$		7.1		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		1.21		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		222		pF
Output Capacitance	C_{OSS}			55.4		
Reverse Transfer Capacitance	C_{RSS}			2.6		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 50\text{ V}, I_D = 1.5\text{ A}$		3		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.6		
Gate-to-Source Charge	Q_{GS}			0.9		
Gate-to-Drain Charge	Q_{GD}			1		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 50\text{ V}, I_D = 1.5\text{ A}$		5		

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 1.5\text{ A}, R_G = 6\text{ }\Omega$		8.4		ns
Rise Time	t_r			8		
Turn-Off Delay Time	$t_{d(OFF)}$			8.9		
Fall Time	t_f			6.2		
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 50\text{ V}, I_D = 1.5\text{ A}, R_G = 6\text{ }\Omega$		5.7		ns
Rise Time	t_r			2		
Turn-Off Delay Time	$t_{d(OFF)}$			11.2		
Fall Time	t_f			4.6		

OFF CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 1.5\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 125^\circ\text{C}$		1.3		

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ELECTRICAL CHARACTERISTICS (Q1, N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$, $I_S = 0.8\text{ A}$		19		ns
Charge Time	t_a			13		
Discharge Time	t_b			6		
Reverse Recovery Charge	Q_{RR}			11		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (Q2, P-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		54		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -28\text{ }\mu\text{A}$	-2.0	-3.0	-4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = -28\text{ }\mu\text{A}$, ref to 25°C		6.61		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -1.5\text{ A}$		109	131	$\text{m}\Omega$
		$V_{GS} = -6\text{ V}$, $I_D = -1\text{ A}$		141	198	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}$, $I_D = -7\text{ A}$		7.9		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		3.36		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$, $V_{DS} = -50\text{ V}$		525		pF
Output Capacitance	C_{OSS}			88		
Reverse Transfer Capacitance	C_{RSS}			4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}$, $V_{DS} = -50\text{ V}$, $I_D = -1.5\text{ A}$		8.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.8		
Gate-to-Source Charge	Q_{GS}			2.7		
Gate-to-Drain Charge	Q_{GD}			1.3		
Total Gate Charge	$Q_{G(TOT)}$			5.2		
		$V_{GS} = 6\text{ V}$, $V_{DD} = 50\text{ V}$, $I_D = -1.5\text{ A}$		5.2		

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}$, $V_{DS} = -50\text{ V}$, $I_D = -1.5\text{ A}$, $R_G = 6\text{ }\Omega$		10.1		ns
Rise Time	t_r			2.7		
Turn-Off Delay Time	$t_{d(OFF)}$			15.9		
Fall Time	t_f			6.8		
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -6\text{ V}$, $V_{DS} = -50\text{ V}$, $I_D = -41.5\text{ A}$, $R_G = 6\text{ }\Omega$		13.3		ns
Rise Time	t_r			5.7		
Turn-Off Delay Time	$t_{d(OFF)}$			12.5		
Fall Time	t_f			7		

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ELECTRICAL CHARACTERISTICS (Q2, P-CHANNEL) ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}$, $I_S = -1.5\text{ A}$	$T_J = 25\text{ }^{\circ}\text{C}$		-0.8	-1.2	V
Forward Diode Voltage			$T_J = 125\text{ }^{\circ}\text{C}$		-0.7		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$, $I_S = -0.8\text{ A}$			31		ns
Charge Time	t_a				23		
Discharge Time	t_b				8		
Reverse Recovery Charge	Q_{RR}				42		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Device Marking	Package	Shipping (Qty / Packing) [†]
NTMC083NP10M5L	83NP10M5	SO8 (Pb-Free/Halogen Free)	2500 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

TYPICAL CHARACTERISTICS – N-CANNEL

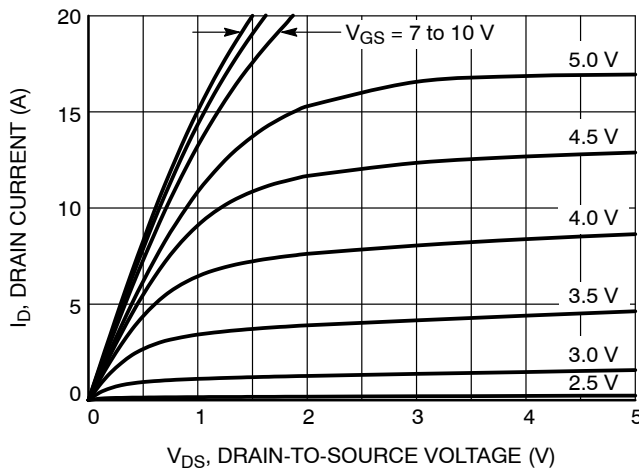


Figure 1. On-Region Characteristics

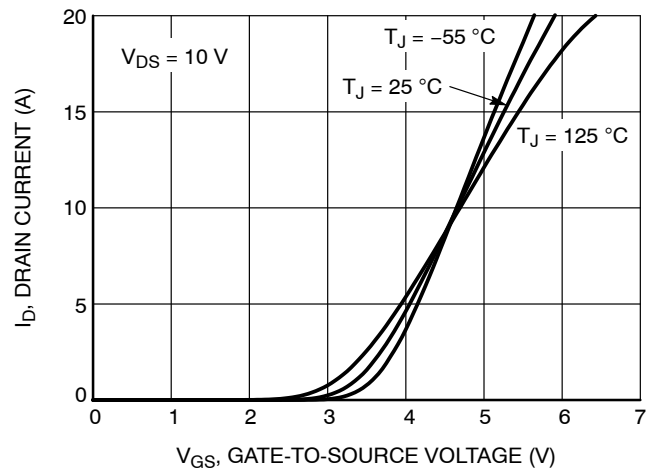


Figure 2. Transfer Characteristics

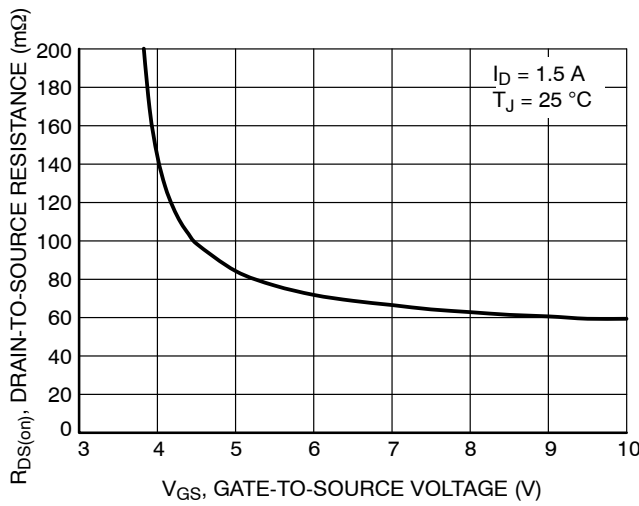


Figure 3. On-Resistance vs. Gate-to-Source Voltage

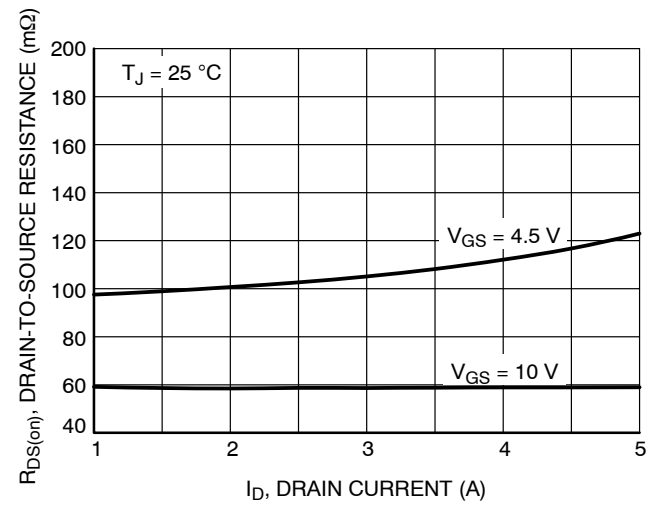


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

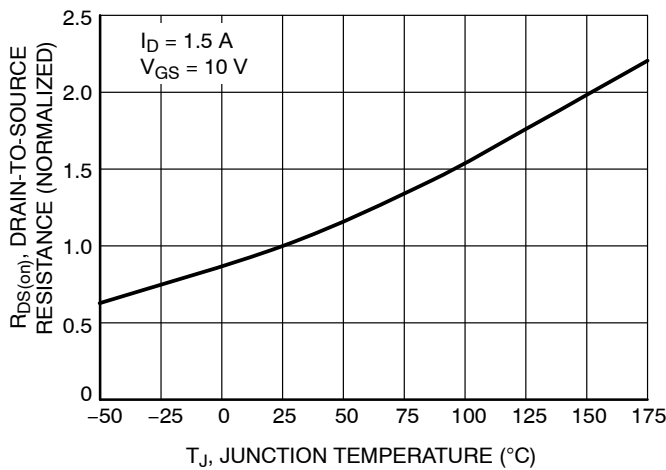


Figure 5. On-Resistance Variation with Temperature

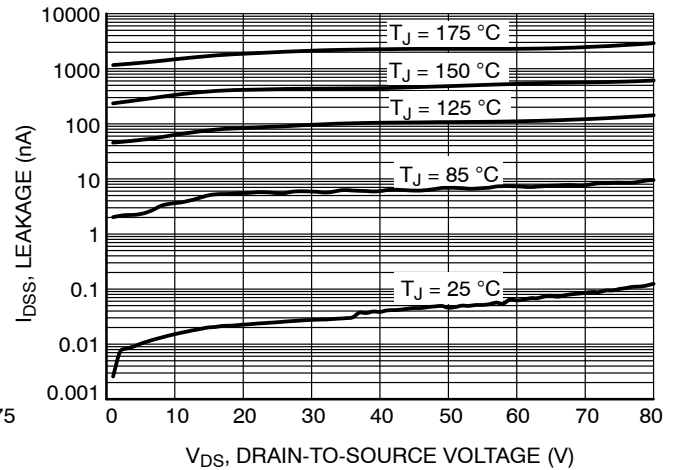


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – N-CANNEL

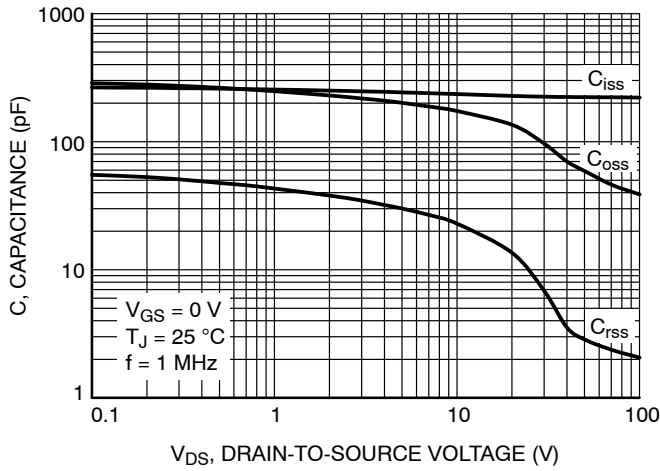


Figure 7. Capacitance Variation

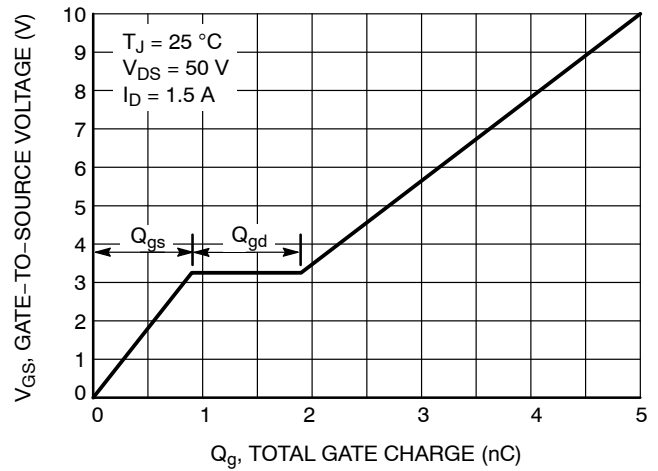


Figure 8. Gate-to-Source vs. Total Charge

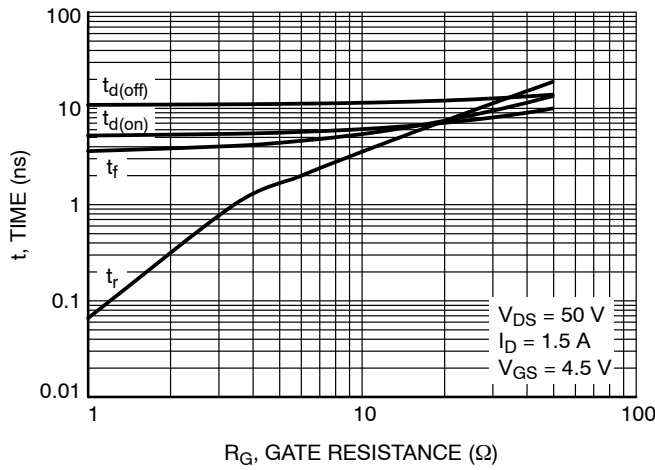


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

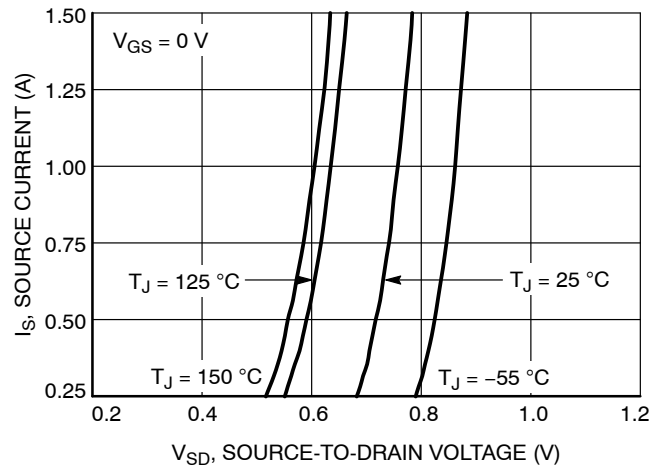


Figure 10. Diode Forward Voltage vs. Current

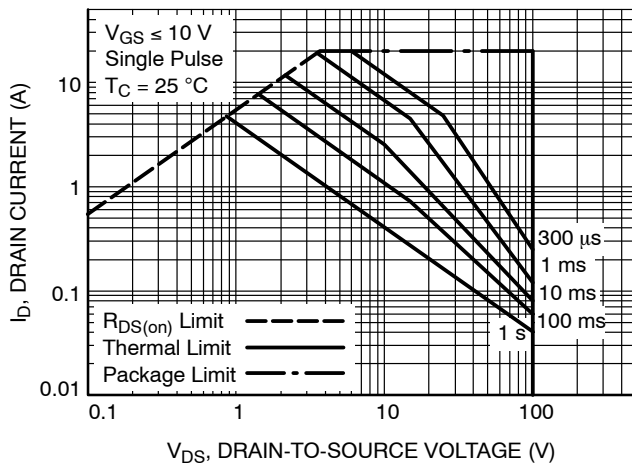


Figure 11. Maximum Rated Forward Biased Safe Operating Area

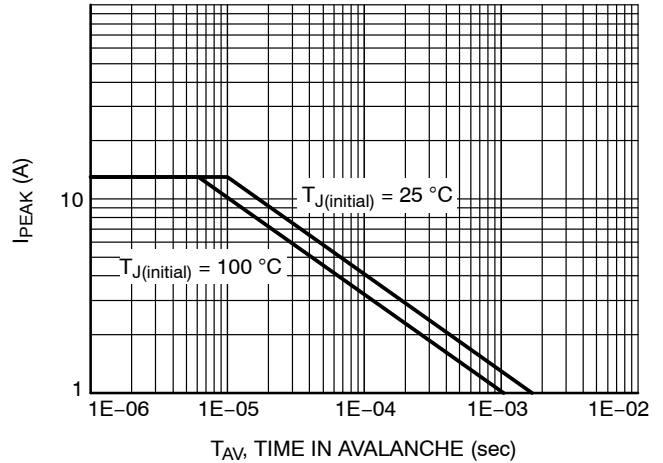


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS – N-CHANNEL

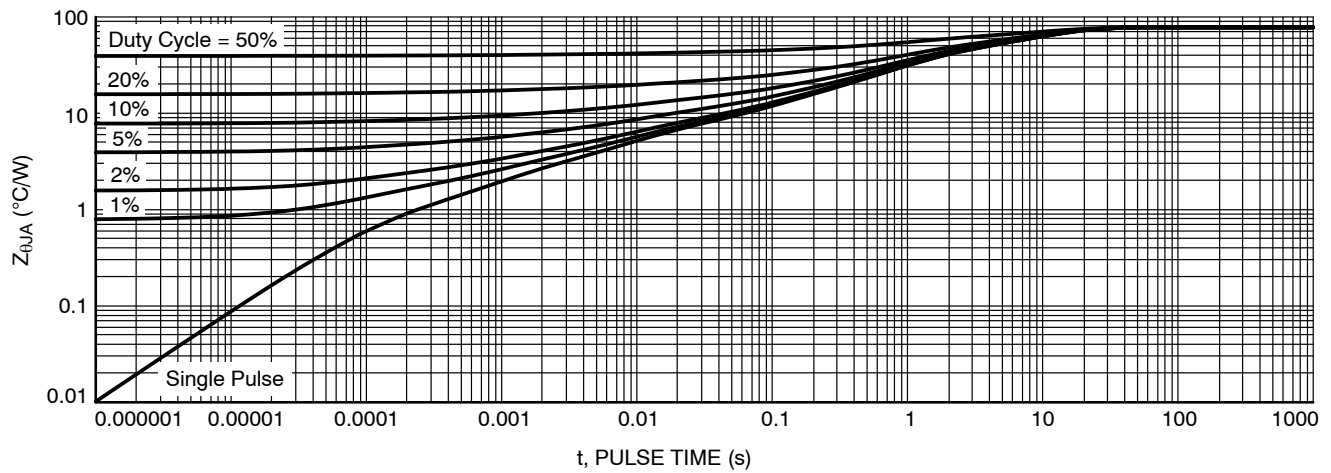


Figure 13. Thermal Response

TYPICAL CHARACTERISTICS – P-CHANNEL

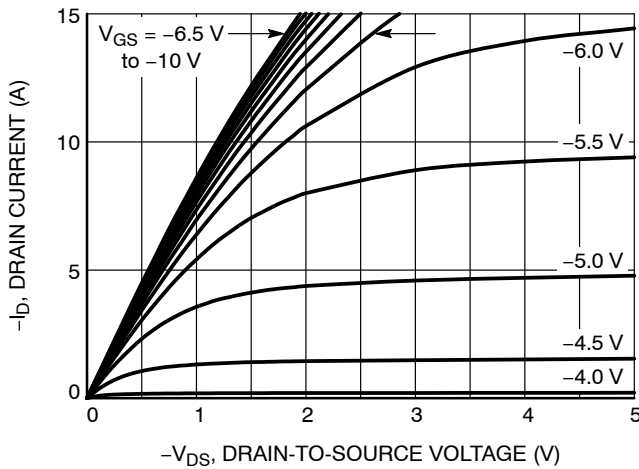


Figure 14. On-Region Characteristics

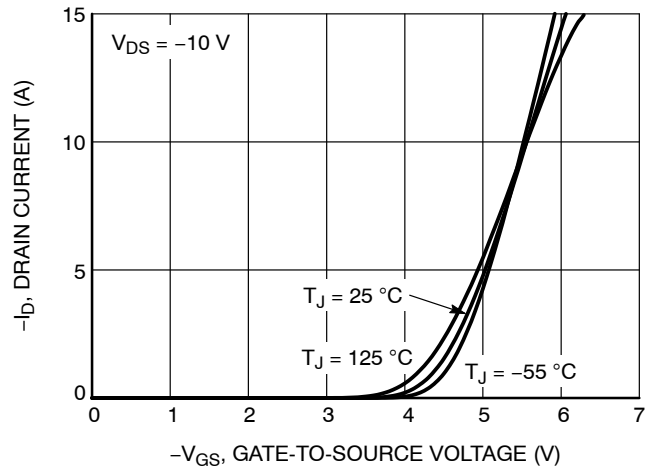


Figure 15. Transfer Characteristics

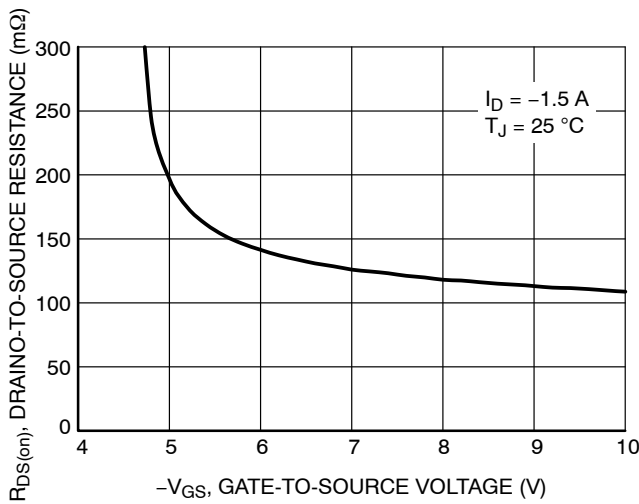


Figure 16. On-Resistance vs. Gate-to-Source Voltage

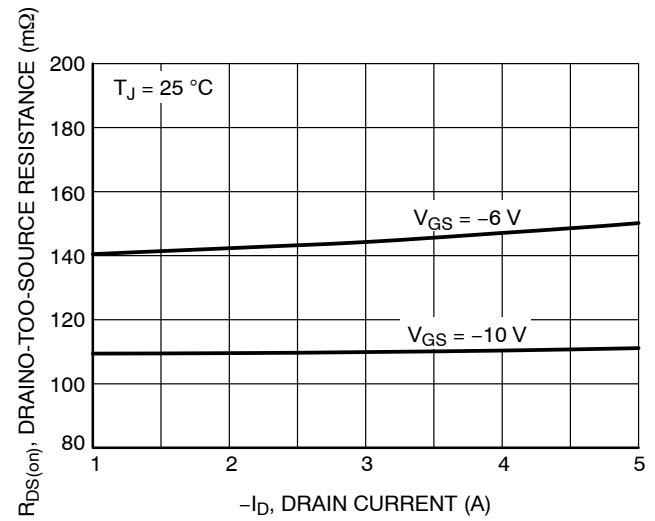


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

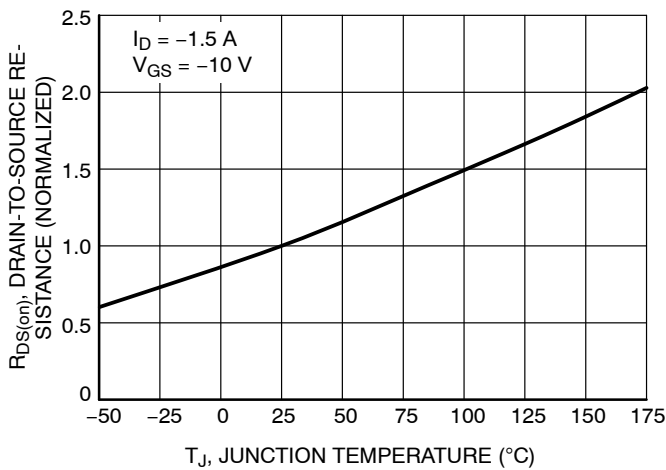


Figure 18. On-Resistance Variation with Temperature

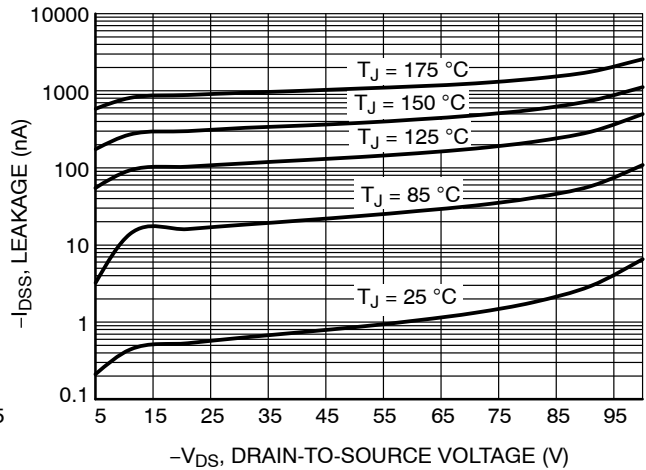


Figure 19. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – P-CHANNEL

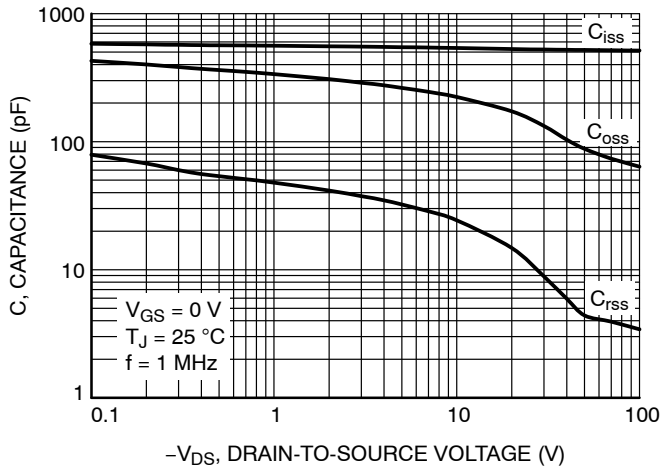


Figure 20. Capacitance Variation

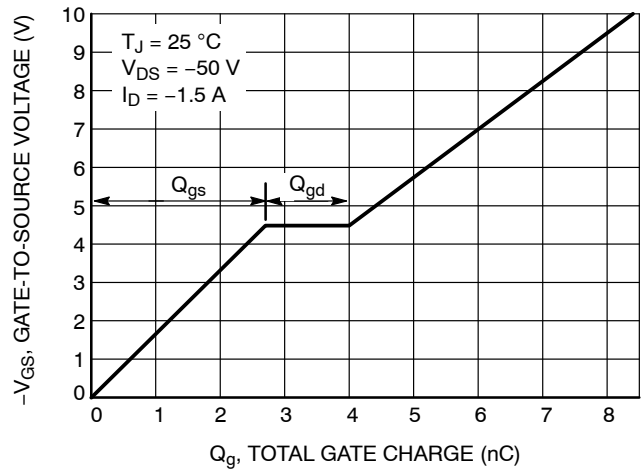


Figure 21. Gate-to-Source vs. Total Charge

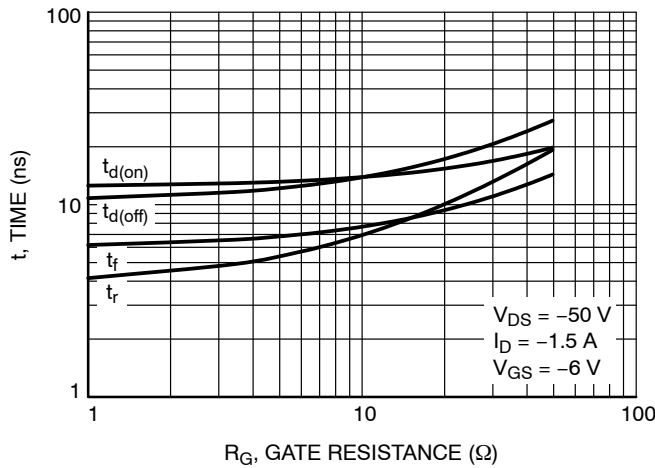


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

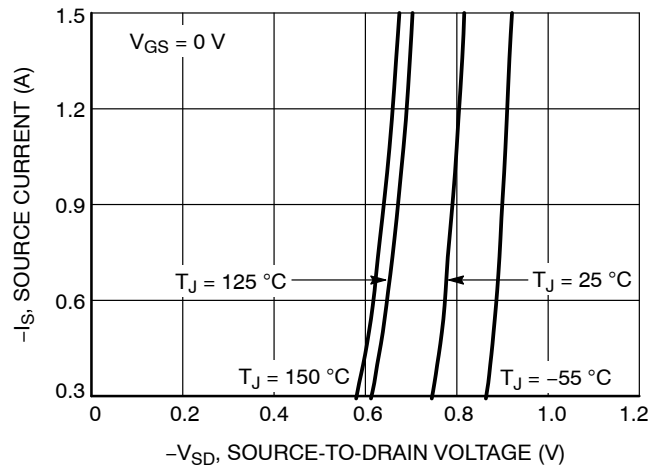


Figure 23. Diode Forward Voltage vs. Current

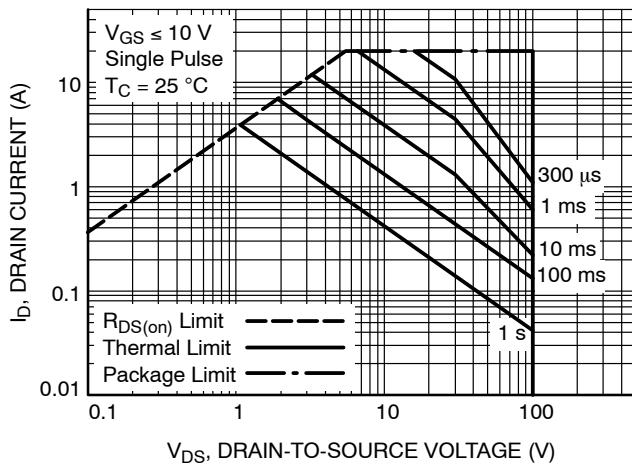


Figure 24. Maximum Rated Forward Biased Safe Operating Area

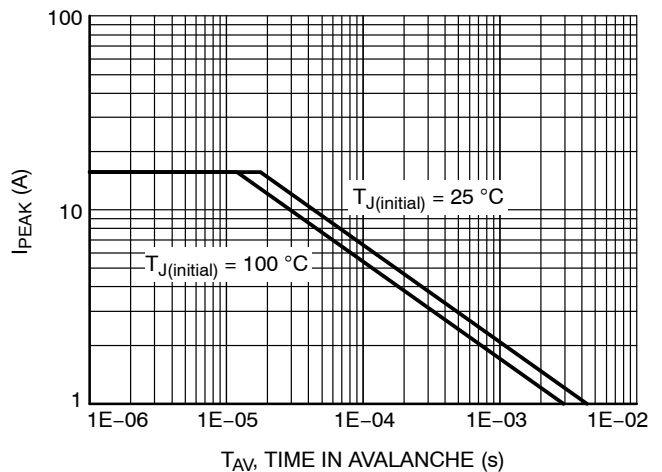


Figure 25. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS – P-CHANNEL

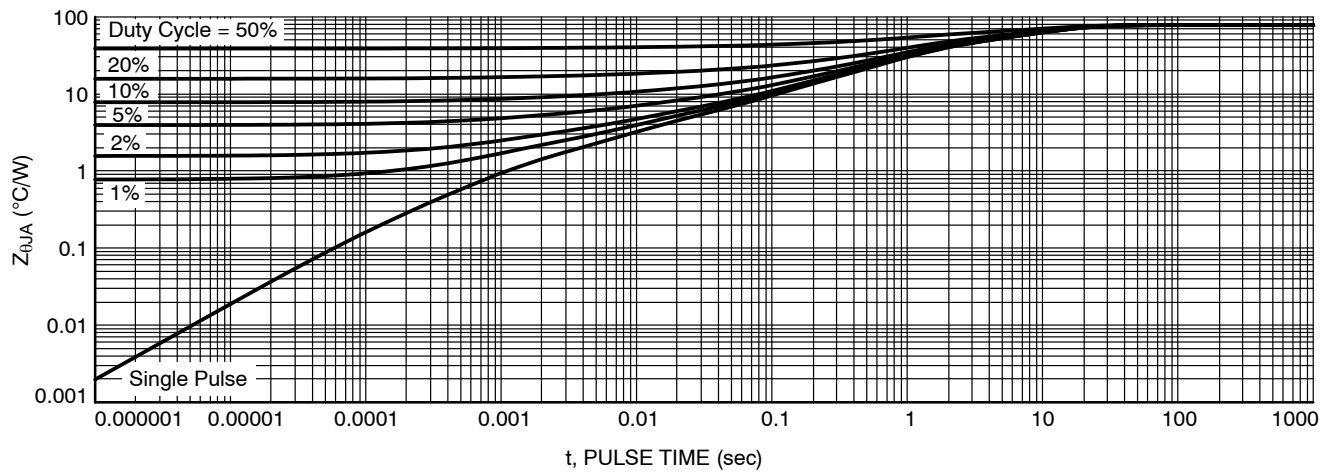


Figure 26. Thermal Response

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REVISION HISTORY

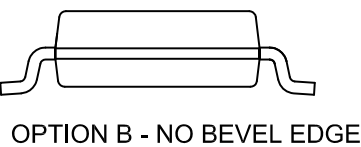
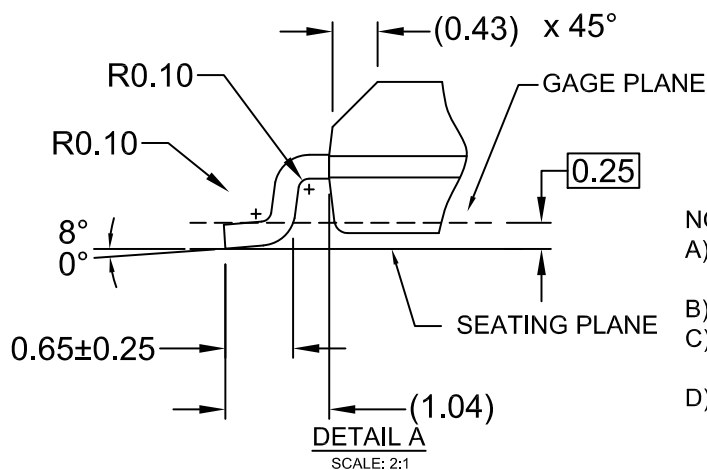
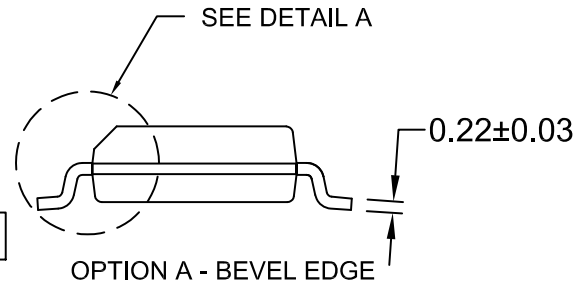
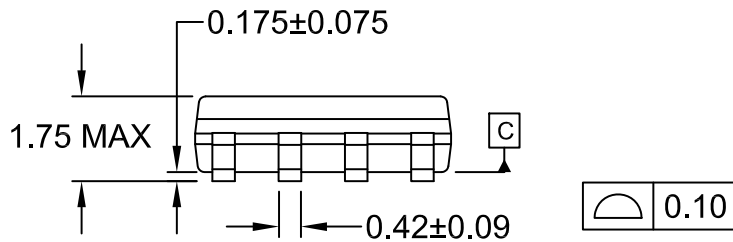
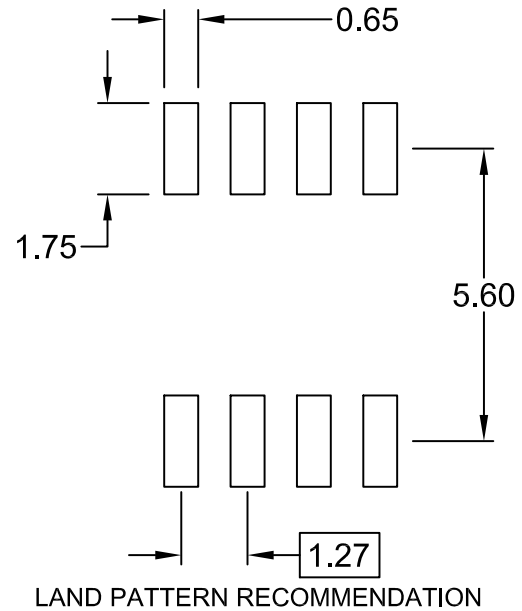
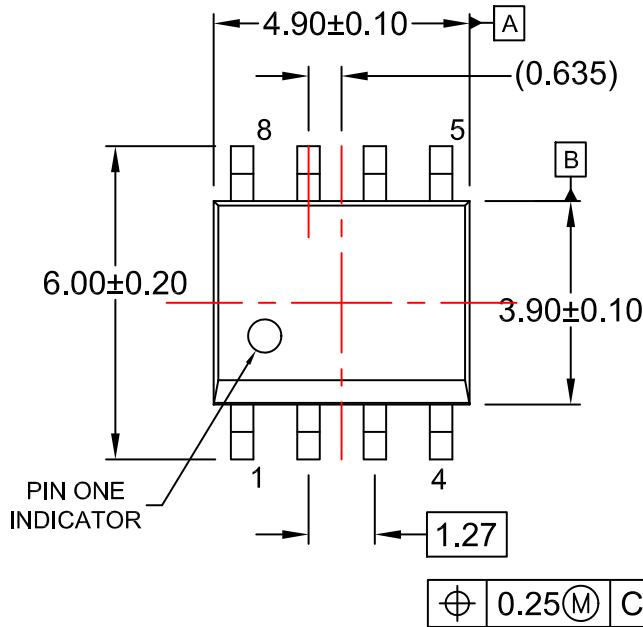
Revision	Description of Changes	Date
2	Revision to Update V_{GS} from 110 V to -10 V + Rebrand to onsemi format	4/14/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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