REVISIONS				
LTR	DESCRIPTION		DATE (YR-MO-DA)	APPROVED
A	Boilerplate update and part of five year review. tcr		06-12-14	Raymond Monnin

REV																		
SHEET																		
REV	A	A	A	A														
SHEET	15	16	17	18														

REV STATUS			REV		A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS			SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Gary L. Gross	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING	CHECKED BY Ray Monnin	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, MEMORY, DIGITAL, CMOS 256K X 8-BIT UVEPROM, MONOLITHIC SILICON
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	DRAWING APPROVAL DATE 92-06-11	

	REVISION LEVEL A	SIZE A	CAGE CODE **67268**	**5962-90912**
AMSC N/A		SHEET 1 OF 18		

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5962-E078-07

1. SCOPE

1.1 <u>Scope</u>. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 <u>PIN</u>. The PIN is as shown in the following example:

```
   5962        -      90912         01          M            X            X
    |                   |            |           |            |            |
Federal             RHA          Device      Device        Case         Lead
stock class      designator       type        class       outline      finish
designator       (see 1.2.1)   (see 1.2.2)    designator  (see 1.2.4)  (see 1.2.5)
    _____/              (see 1.2.3)
                   V
            Drawing number
```
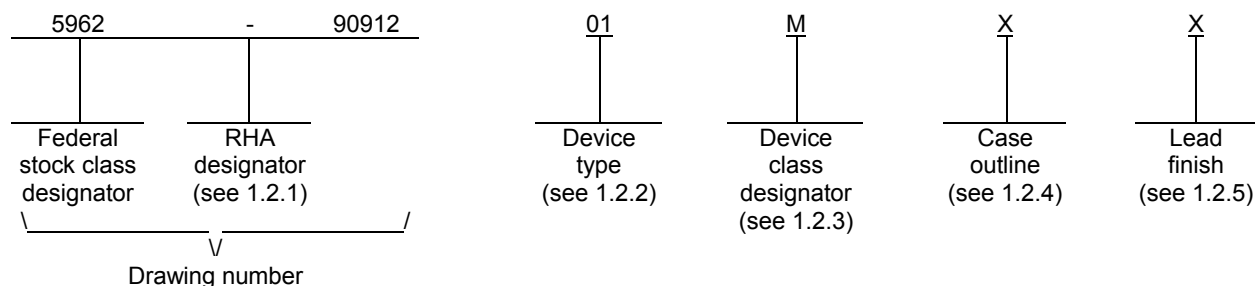
1.2.1 <u>RHA designator</u>. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	27C020	(256K X 8) UVEPROM	250 ns
02	27C020	(256K X 8) UVEPROM	200 ns
03	27C020	(256K X 8) UVEPROM	150 ns

1.2.3 <u>Device class designator</u>. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style 1/
X	GDIP1-T32 or CDIP2-T32	32	Dual-in-line package
Y	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Lid shall be transparent to permit ultraviolet light erasure.

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1.3 <u>Absolute maximum ratings</u>. <u>2</u>/

Storage temperature range .... -65°C to +150°C
Input or output voltage range with respect to ground .... -0.6 V dc to V_{CC} +0.5 V dc
Voltage on A9 with respect to ground .... -0.6 V dc to +13.0 V dc
V_{PP} supply voltage range with respect to ground during programming .... -0.6 V dc to +13.5 V dc
V_{CC} supply voltage range with respect to ground .... -0.6 V dc to +7.0 V dc
Maximum power dissipation P_D .... 330 mW
Lead temperature (soldering, 10 sec.) .... +300°C
Thermal resistance, junction-to-case (Θ_{JC}):
    Case X and Y .... See MIL-STD-1835
Junction temperature (T_J) .... +150°C <u>3</u>/
Endurance .... 50 cycles/byte, minimum
Data retention .... 10 years, minimum

1.4 <u>Recommended operating conditions</u>.

Case operating temperature range (T_C) .... -55°C to +125°C
Supply voltage range (V_{CC}) .... 4.5 V dc to 5.5 V dc

2. APPLICABLE DOCUMENTS

   2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

   DEPARTMENT OF DEFENSE SPECIFICATION

      MIL-PRF-38535   - Integrated Circuits, Manufacturing, General Specification for.

   DEPARTMENT OF DEFENSE STANDARDS

      MIL-STD-883   -   Test Method Standard Microcircuits.
      MIL-STD-1835   -   Interface Standard Electronic Component Case Outlines.

   DEPARTMENT OF DEFENSE HANDBOOKS

      MIL-HDBK-103 -   List of Standard Microcircuit Drawings.
      MIL-HDBK-780 -   Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

   2.2 <u>Non-Government publications</u>. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

   AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

      ASTM Standard F1192-00   -   Standard Guide for the Measurement of Single Event Phenomena (SEP) induced by
                                     Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

<u>2</u>/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the
    maximum levels may degrade performance and affect reliability.

<u>3</u>/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in
    accordance with method 5004 of MIL-STD-883.

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ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78   -   IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item   drawing shall be as specified on figure 2 herein. When required in screening (see 4.2 herein) or qualification conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Processing EPROMS. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.5.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.5.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

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3.5.3 <u>Erasure of EPROMS</u>. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5 herein.

3.5.4 <u>Verification of erasure or programmed EPROMS</u>. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.6.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 <u>Notification of change for device class M</u>. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 <u>Verification and review for device class M</u>. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 <u>Microcircuit group assignment for device class M</u>. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.12 <u>Endurance</u>. A reprogrammability test shall be completed as part of the vendors reliability monitors, this reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. This test shall consist of 20 program/erase cycles on 25 devices with the following conditions:

(1) All devices selected for testing shall be programmed per 3.2.3.2 herein (see 4.6).

(2) Verify pattern (see 3.5.4).

(3) Erase (see 4.5).

(4) Verify pattern erasure (see 3.5.4).

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TABLE I. <u>Electrical performance characteristics</u>.

Test	Symbol	Conditions -55°C ≤ T_A ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input load current	I_{LI}	V_{IN} = 0 V to 5.5 V	1,2,3	All	-1	+1	µA
Output leakage current	I_{LO}	V_{OUT} = 0 V to 5.5 V	1,2,3	All	-10	+10	µA
V_{PP} load current read	I_{PP1}	V_{PP} = 5.5 V, $\overline{CE}$ = $\overline{OE}$ = V_{IL}	1,2,3	All		100	µA
V_{CC} active current	I_{CC1}	$\overline{CE}$ = V_{IL} I_{OUT} = 0 mA V_{CC} = V_{PP} = 5.5 V f = 1/t_{AVQV}	1,2,3	All		60	mA
V_{CC} standby current (TTL)	I_{CC2}	$\overline{CE}$ = V_{IH} V_{CC} = 5.5 V	1,2,3	All		1	mA
V_{CC} super standby current (CMOS)	I_{CC3}	$\overline{CE}$ = V_{CC} + 0.3 V V_{CC} = 5.5 V	1,2,3	All		100	µA
Input low voltage	V_{IL}		1,2,3	All	-0.1 <u>1/</u>	0.8	V
Input high voltage	V_{IH}		1,2,3	All	2.0	V_{CC} +0.5 V <u>1/</u>	V
Output low voltage	V_{OL}	I_{OL} = 2.1 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All		0.45	V
Output high voltage	V_{OH}	I_{OH} = -400 µA, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	All	2.4		V

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - continued.

Test	Symbol	Conditions -55°C ≤ T_A ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input capacitance 1/ 2/	C_{IN}	T_A = +25°C, f = 1 MHz V_{IN} = 0 V, see 4.4.1e	4	All		12	pF
Output capacitance 1/ 2/	C_{OUT}	T_A = +25°C, f = 1 MHz, V_{OUT} = 0 V, see 4.4.1e	4	All		15	pF
Functional tests		See 4.4.1c	7, 8A, 8B	All			
Address to output delay	t_{AVQV}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} See figures 3 and 4 as applicable	9, 10, 11	01 02 03		250 200 150	ns
$\overline{CE}$ to output delay 3/	t_{ELQV}	$\overline{OE}$ = V_{IL} See figures 3 and 4 as applicable	9, 10, 11	01 02 03		250 200 150	ns
$\overline{OE}$ to output delay 3/	t_{OLQV}	$\overline{CE}$ = V_{IL} See figures 3 and 4 as applicable	9, 10, 11	01 02 03		100 75 65	ns
$\overline{CE}$ or $\overline{OE}$ high to output float 4/	t_{EHQZ} t_{OHQZ}	$\overline{CE}$ or $\overline{OE}$ = V_{IL} See figures 3 and 4 as applicable	9, 10, 11	01 02 03		60 60 50	ns
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first 4/	t_{AXQX}	See figures 3 and 4	9, 10, 11	All	0		ns

1/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

2/ All pins not being tested shall be grounded.

3/ Input rise and fall times ≤ 20 ns for all device types.

4/ May not be tested, but shall be guaranteed to the limits specified in table I.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line No.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, method 5005, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ 8/
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ 8/
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9,10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta
    values shall be computed with reference to the previous interim electrical parameters
    (lines 1 and 3).
7/ See 4.4.1d.
8/ The device manufacturer may at this option, either complete subgroup 1 electrical parameter
    measurements, including delta measurements, within 96 hours after burn-in completion (removal
    of bias); or may complete subgroup 1 electrical measurements without delta measurements within
    24 hours after burn-in completion (removal of bias).

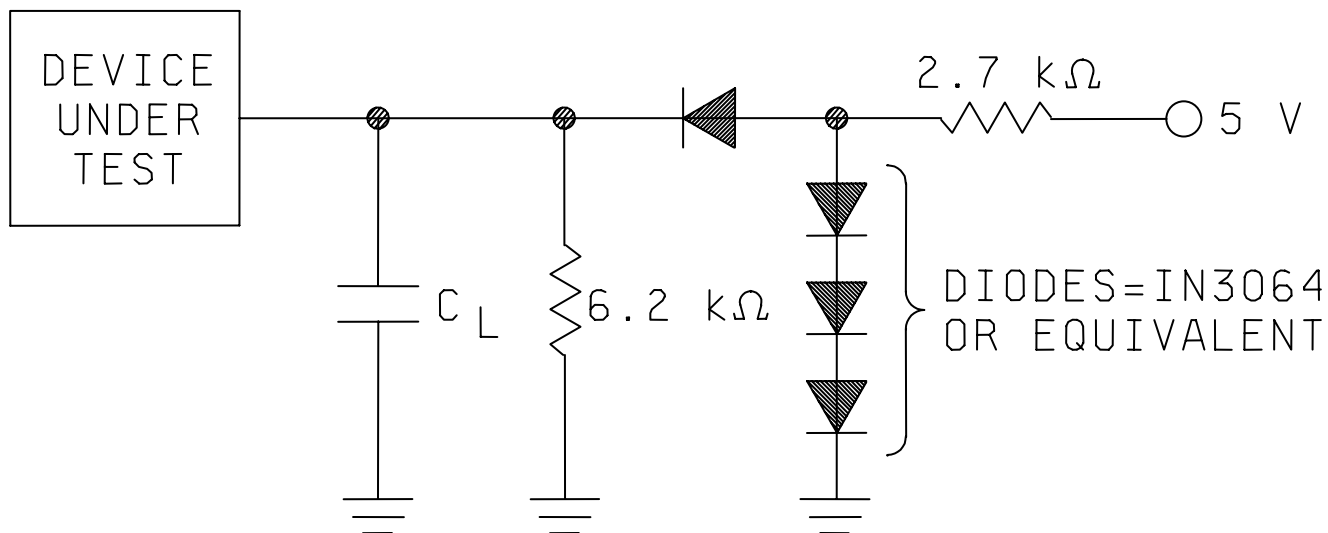| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE **A**		5962-90912
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TABLE IIB. <u>Delta limits at +25°C.</u>

Test 1/	Device types
	All
I_{CC3} standby	±10% of specified value in table I
I_{LI}	±10% of specified value in table I
I_{OZ}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after
   the required burn-in and life tests to determine the delta.

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Device types	All
Case outlines	X and Y
Terminal number	Terminal symbol
1	V_{PP}
2	A_{16}
3	A_{15}
4	A_{12}
5	A_7
6	A_6
7	A_5
8	A_4
9	A_3
10	A_2
11	A_1
12	A_0
13	I/O
14	I/O
15	I/O
16	GND
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	$\overline{CE}$ (E)
23	A_{10}
24	$\overline{OE}$ (G)
25	A_{11}
26	A_9
27	A_8
28	A_{13}
29	A_{14}
30	A_{17}
31	$\overline{PGM}$ (P)
32	V_{CC}

FIGURE 1. Terminal connections.

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Mode		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
								Pins
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Standby (TTL)		V_{IH}	X	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm$ 0.3 V	X	X	X	X	X	Hi-Z
Output disable		V_{IL}	V_{IH}	X	X	X	X	Hi-Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto select (Notes 1, 3, 4)	Manufacturer code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	
	Device	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	

NOTES:
1. V_H = HIGH voltage +12.0 $\pm$0.5 V
2. X = Either V_{IH} or V_{IL}
3. A_1 - A_8 = A_{10} - A_{17} = V_{IL}
4. V_{PP} (see 4.6)

FIGURE 2. Truth table.

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DEVICE
UNDER
TEST

2.7 kΩ

5 V

C$_L$

6.2 kΩ

DIODES=IN3064
OR EQUIVALENT

C_L = 100 pF including jig capacitance

FIGURE 3. Switching time test circuit (or equivalent).

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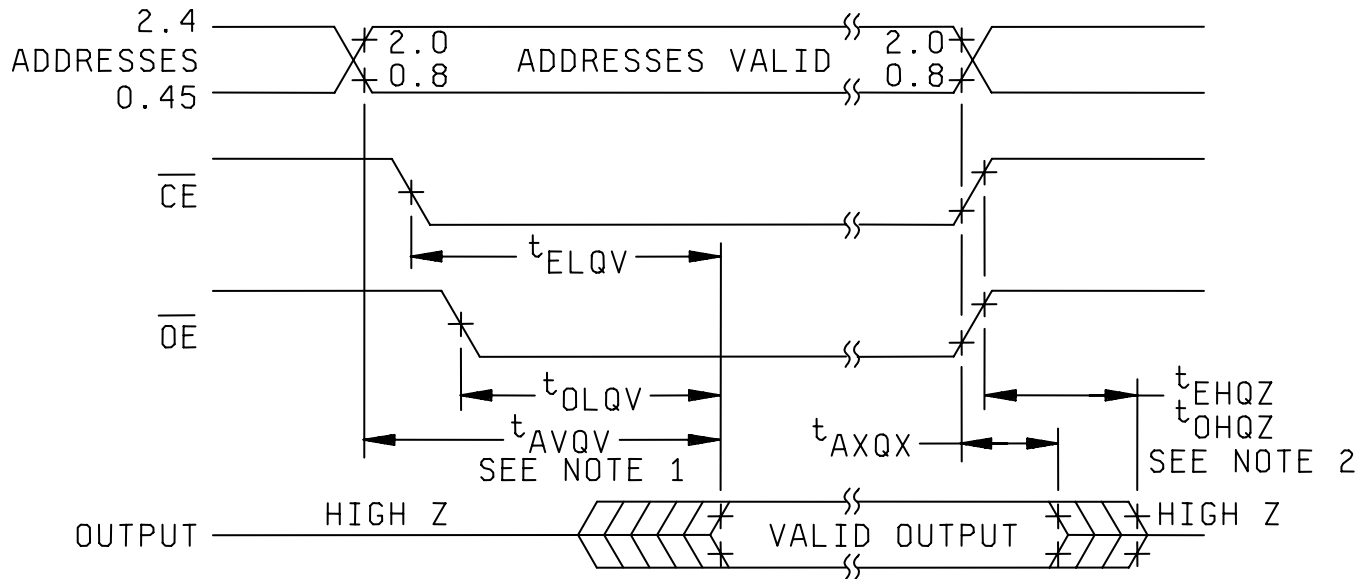
NOTES:

1. $\overline{OE}$ may be delayed up to t_{AVQV} - t_{OLQV} after the falling edge of $\overline{CE}$ without impact on t_{AVQV}.

2. t_{EHQZ} or t_{OHQZ} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 4. Read cycle waveforms.

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4. VERIFICATION

4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 <u>Additional criteria for device class M</u>.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.6 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in.

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

  (1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

<u>Method A</u>. (Steps 1 through 4 may be performed at wafer level.)

  (1) Program at +25°C with a greater than 95 percent pattern (example, diagonal "1's") (see 3.5.2 and 3.5.3).

  (2) Unbiased bake for 24 hours at +175°C.

  (3) Test at T_C = +25°C (minimum) (see 3.5.3), including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

  (4) Erase.

  (5) Program at +25°C with a checkerboard pattern (see 3.5.2 and 3.5.3)

  (6) Test at T_C = +25°C (minimum), including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

  (7) Burn-in (see 4.2.1c).

  (8) Test at T_C = +25°C (see 3.5.3), including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

  (9) Test at T_C = +125°C (minimum), including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

  (10) Test at T_C = -55°C, including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

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(11) Erase (see 3.5.1). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100-percent seal tested in accordance with method 5004 of MIL-STD-883.

(12) Verify erasure at +25°C (see 3.5.3).

4.2.2 <u>Additional criteria for device classes Q and V</u>.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 <u>Group A inspection</u>.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups B, C, and D testing).

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4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply to group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 <u>Additional criteria for device class M</u>.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883. After the completion of all testing, the devices shall be erased and verified prior to delivery.

4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified.

4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 <u>Erasing procedures</u>. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (one week at 12000 µW/cm^2). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.6 <u>Programming procedures</u>. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 <u>Delta measurements for device classes Q, and V</u>. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and herein:

C_{IN} and C_{OUT} .... Input and bidirectional output, terminal-to-GND capacitance.
GND .... Ground zero voltage potential.
I_{CC} .... Supply current.
I_{LI} .... Input load current.
T_C .... Case temperature.
T_A .... Ambient temperature.
V_{CC} .... Positive supply voltage.
O/V .... Latch-up over-voltage
O/I .... Latch-up over-current

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:

```
                              t   X   X   X   X
Signal name from which interval is defined _____|   |   |   |
Transition direction for first signal      _____|   |   |
Signal name to which interval is defined    _____|   |
Transition direction for second signal       _____|
```

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a. Signal definitions:
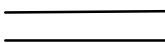
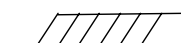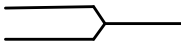   A = Address
   D = Data in
   O = Data out
   W = Write enable
   E = Chip enable

b. Transition definitions:

   H = Transition to high
   L = Transition to low
   V = Transition to valid
   X = Transition to invalid or don't care
   Z = Transition to off (high impedance)

   6.5.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

   6.5.3 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

   6.6 Sources of supply.

   6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

   6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-12-14

Approved sources of supply for SMD 5962-90912 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9091201MXA	0C7V7	AT27C020-250DM/883
5962-9091201MXA	3/	Am27C020-250/BXA
5962-9091201MYA	0C7V7	AT27C020-250LM/883
5962-9091201MYA	3/	Am27C020-250/BUA
5962-9091202MXA	0C7V7	AT27C020-200DM/883
5962-9091202MXA	3/	Am27C020-200/BXA
5962-9091202MYA	0C7V7	AT27C020-200LM/883
5962-9091202MYA	3/	Am27C020-200/BUA
5962-9091203MXA	0C7V7	AT27C020-150DM/883
5962-9091203MXA	3/	Am27C020-150/BXA
5962-9091203MYA	0C7V7	AT27C020-150LM/883
5962-9091203MYA	3/	Am27C020-150/BUA

1/ The lead finish shown for each PIN representing a hermetic package
     is the most readily available from the manufacturer listed for that part.
     If the desired lead finish is not listed contact the vendor to determine
     its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to
     this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE
     number

     0C7V7

Vendor name
and address

QP Semiconductor
2945 Oakmead Village Ct.
Santa Clara, CA 95051-0812

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.