

N-Channel 100-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
100	0.025 at $V_{GS} = 10$ V	40
	0.028 at $V_{GS} = 4.5$ V	38

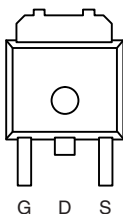
FEATURES

- TrenchFET® Power MOSFET
- 175 °C Maximum Junction Temperature
- 100 % R_g Tested



Available
RoHS*
COMPLIANT

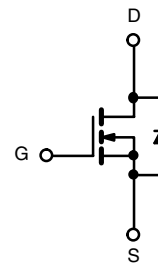
TO-252



Top View

Drain Connected to Tab

Ordering Information: SUD40N10-25
SUD40N10-25-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C) ^b	I_D	40	A
	I_D	23	
Pulsed Drain Current	I_{DM}	70	
Continuous Source Current (Diode Conduction)	I_S	40	
Avalanche Current	I_{AS}	40	mJ
Single Pulse Avalanche Energy (Duty Cycle ≤ 1 %)	E_{AS}	80	
Maximum Power Dissipation	P_D	136 ^b	W
	P_D	3 ^a	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^a	R_{thJA}	15	18	°C/W
	R_{thJA}	40	50	
Junction-to-Case	R_{thJC}	0.85	1.1	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See SOA curve for voltage derating.

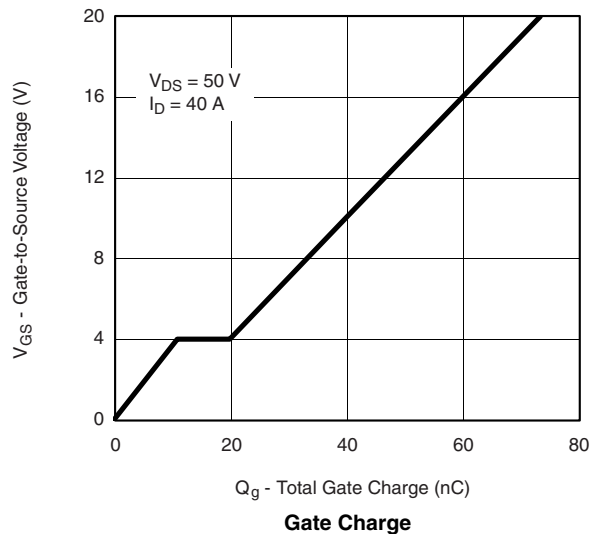
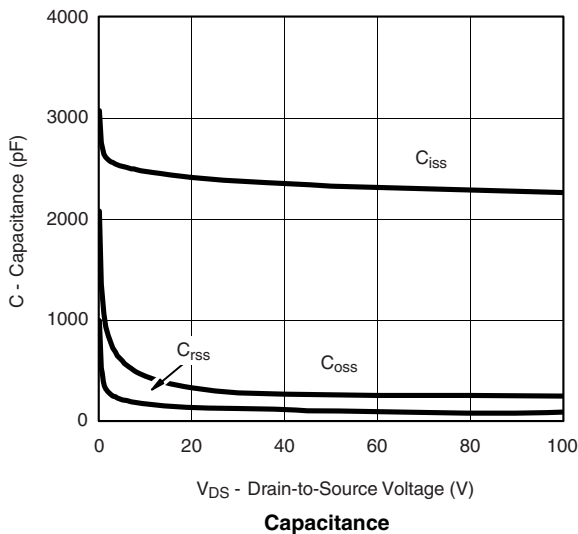
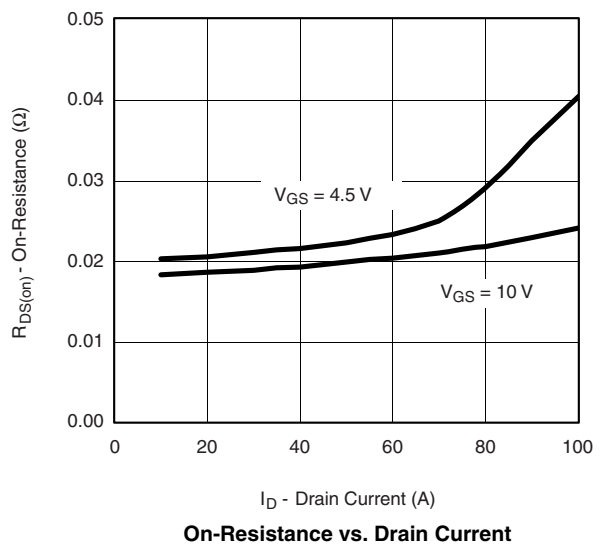
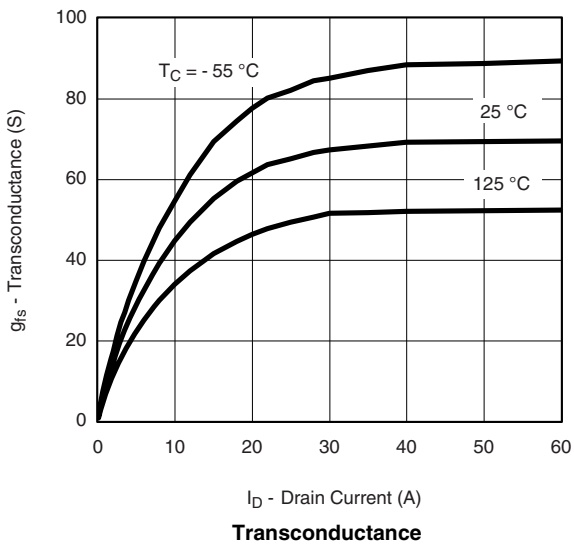
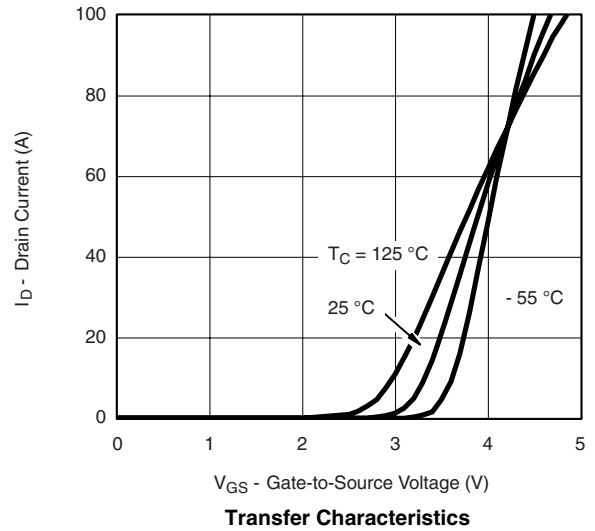
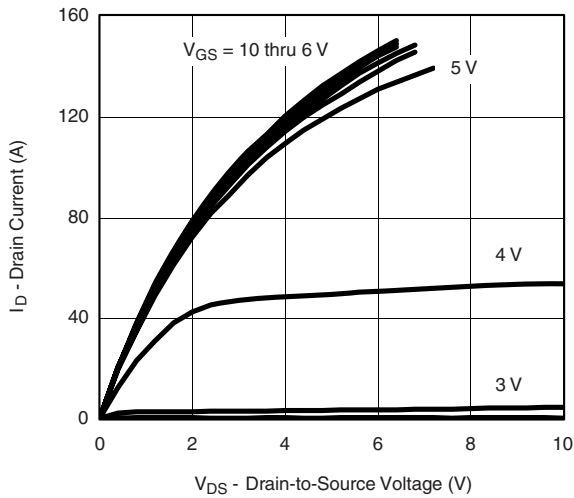
* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.0		3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$			50	
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 175\text{ }^{\circ}\text{C}$			250	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}$, $V_{GS} = 10\text{ V}$	70			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$		0.02	0.025	Ω
		$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$			0.05	
		$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$, $T_J = 175\text{ }^{\circ}\text{C}$			0.063	
		$V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$		0.022	0.028	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 40\text{ A}$		70		S
Dynamic ^a						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $F = 1\text{ MHz}$		2400		pF
Output Capacitance	C_{oss}			290		
Reverse Transfer Capacitance	C_{rss}			120		
Total Gate Charge ^c	Q_g	$V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$		40	60	nC
Gate-Source Charge ^c	Q_{gs}			11		
Gate-Drain Charge ^c	Q_{gd}			9		
Gate Resistance	R_g		1		3.5	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}$, $R_L = 1.25\text{ }\Omega$ $I_D \cong 40\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 2.5\text{ }\Omega$		8	13	ns
Rise Time ^c	t_r			40	60	
Turn-Off Delay Time ^c	$t_{d(off)}$			15	25	
Fall Time ^c	t_f			80	120	
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^{\circ}\text{C}$						
Pulsed Current	I_{SM}				70	A
Diode Forward Voltage ^b	V_{SD}	$I_F = 40\text{ A}$, $V_{GS} = 0\text{ V}$		1.0	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 40\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$		75	120	ns

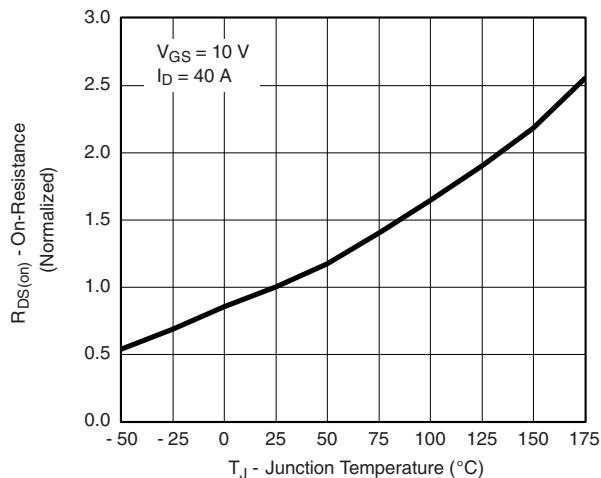
Notes:

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
c. Independent of operating temperature.

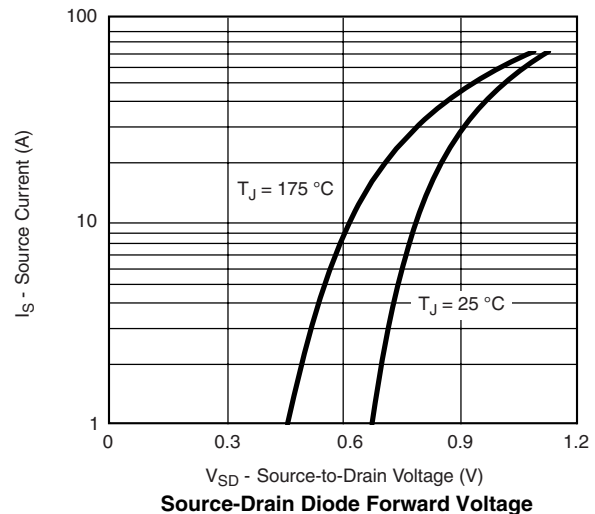
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


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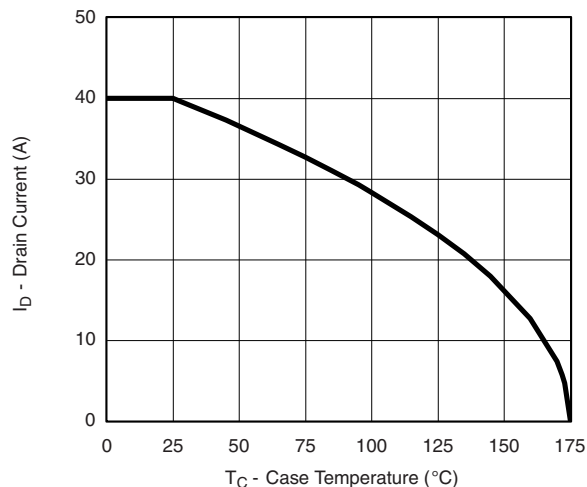


On-Resistance vs. Junction Temperature

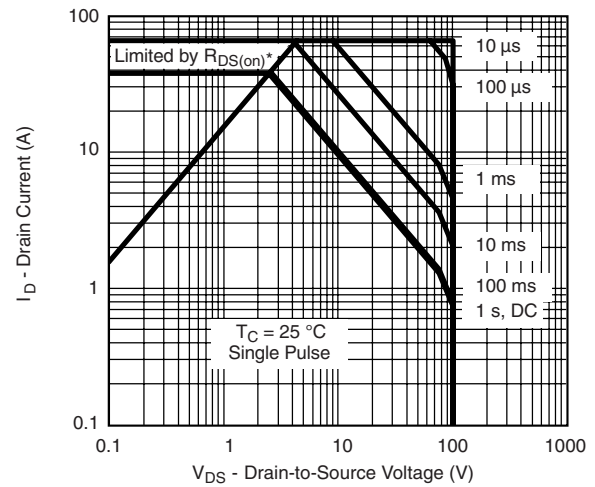


Source-Drain Diode Forward Voltage

THERMAL RATINGS

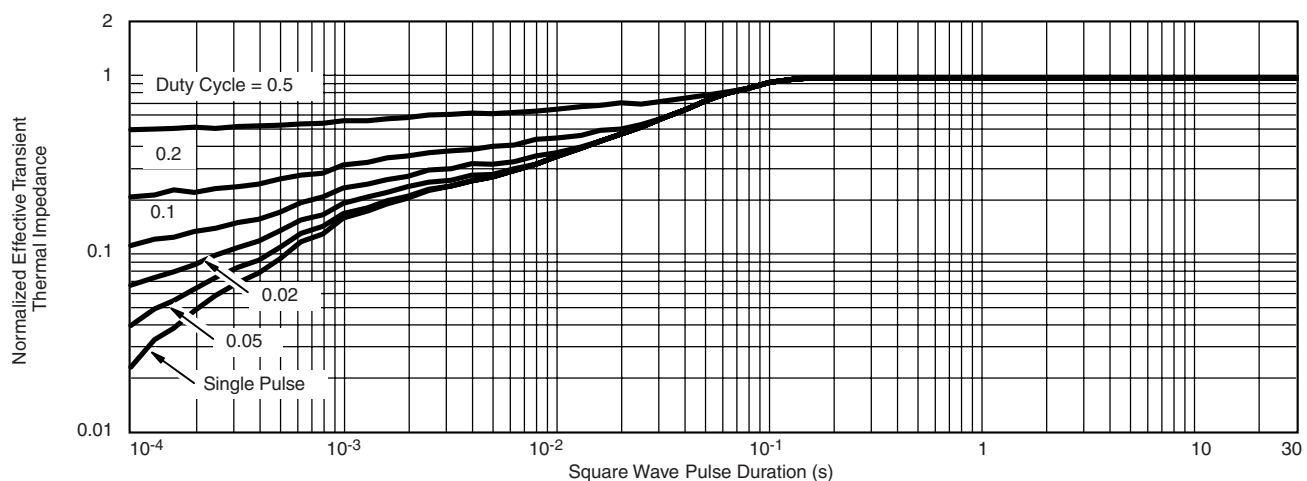


Maximum Avalanche Drain Current vs. Case Temperature



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71140>.

TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



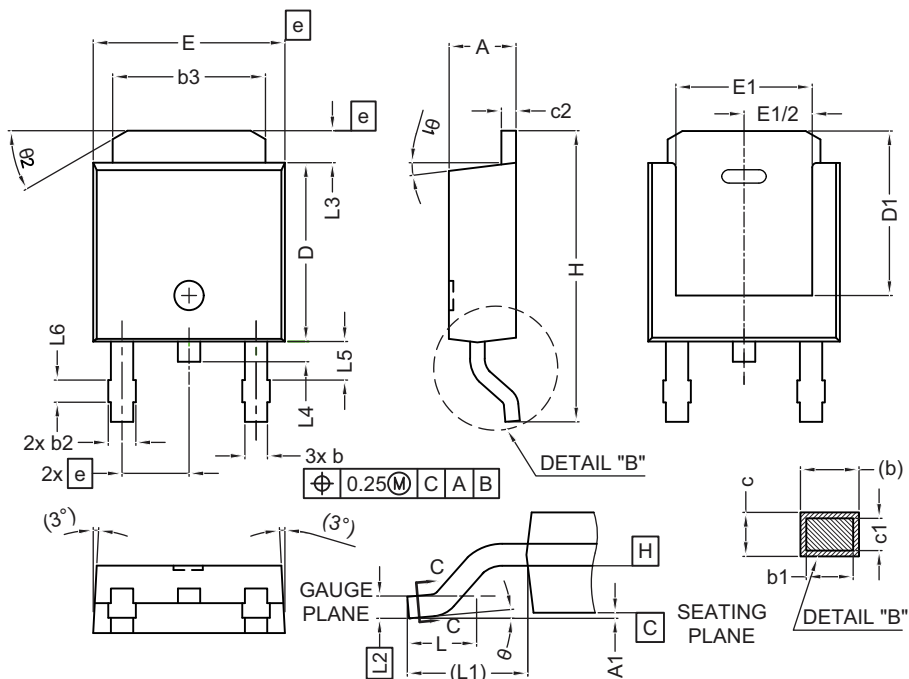
MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
theta	0°	10°
theta1	0°	15°
theta2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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