ASSP

EPCglobal Class1 Generation2 Compliant

FRAM Embedded UHF Band RFID LSI

MB97R8120/8130

■ 1. OVERVIEW

This document provides LSI specifications for the passive RFID Tag LSI "MB97R8120/30" (USER bank 8kBytes) based on "EPCglobal Class 1 Generation 2 Ver.1.2.0".

In this specification, the term “interrogator” used in EPCglobal standard is described as R/W (reader/writer). The term “Tag” is used as is.

■ 1.1 FEATURES

• Compliant with EPCglobal Class 1 Generation 2 (C1G2)
  －Carrier frequency: 860 to 960 MHz
  －Data rate
  R/W → Tag: 26.7 kbps to 128 kbps (assuming equiprobable data)
  Tag → R/W: 40 kbps to 640 kbps
• Serial Interface (SPI):MB97R8130
  －Slave mode operation : USER memory area can be read/written through SPI.
  －Arbitration feature between RF and SPI access controlled by SPIREQ and SPIACK.
• FRAM: Non-volatile memory with High speed read and write
  －USER bank size: 61,440 bits
  －EPC length: up to 480bits
  －BlockPermalock: 8 Areas of USER bank to be write-protected in units of 512 words (=8,192bits).
  －Read/Write Endurance: 10^{13} times
  －Memory data retention: 10 years (+85 ^{o}C)

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■ 1.2 BLOCK DIAGRAM

■ 1.2.1 MB97R8120 Block Diagram

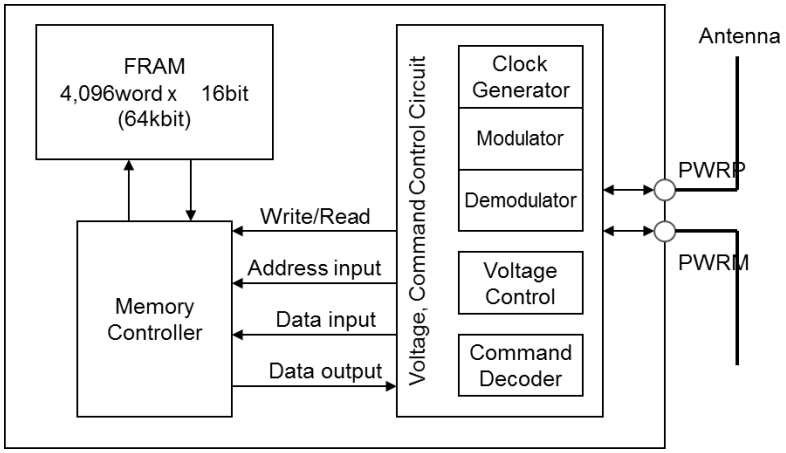


Figure 1.2.1 - BLOCK DIAGRAM(MB97R8120)

■ 1.2.2 MB97R8130 Block Diagram

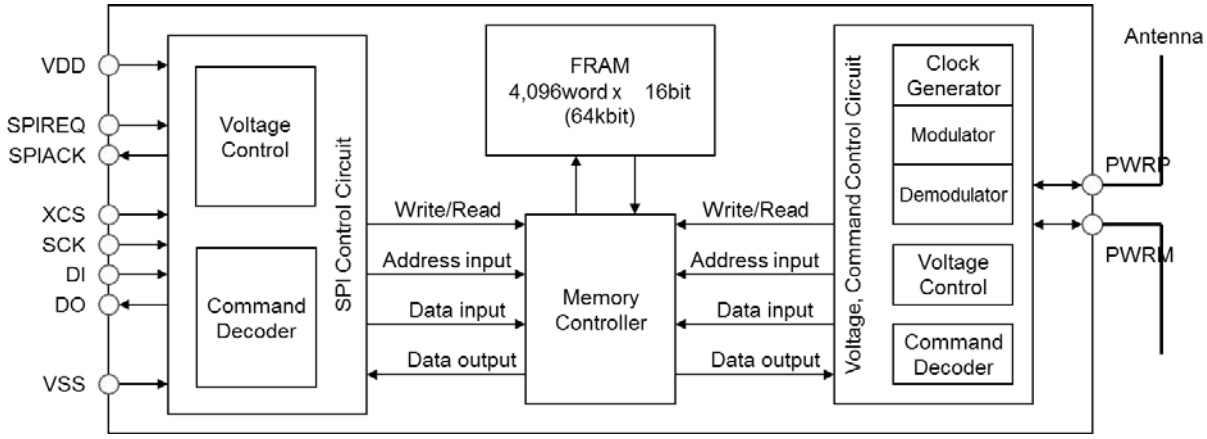


Figure 1.2.2 - BLOCK DIAGRAM(MB97R8130)

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■ 1.3 PAD CONFIGURATION

■ 1.3.1 MB97R8120 Pad Configuration

Figure.1.3.1 shows the pad layout of MB97R8120, and Table 1.3.1 shows the pad information.

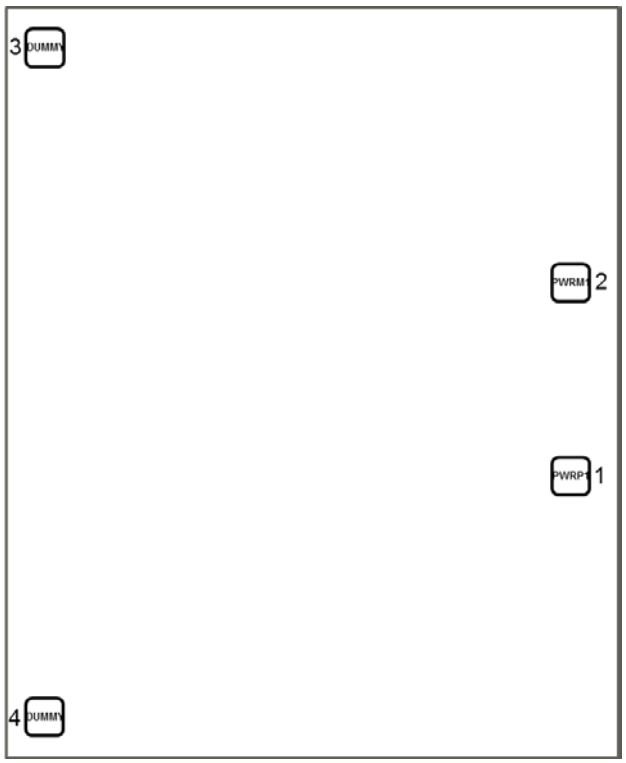


Figure 1.3.1 MB97R8120 Pad Layout

Table 1.3.1 MB97R8120 Pad Information

No.	Pad	Function
1	PWRP	Antenna pad for RF communication
2	PWRM	Antenna pad for RF communication
3	Dummy	*
4	Dummy	*

*. Dummy pads (No.3, 4) shall be electrically isolated from antenna pads (No.1,2) when they are connected to the antenna pattern on a tag/or an inlay. Because the dummy pad is used as power input for probing test stage, it may cause something harm for RF communication if they are connected with antenna.

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■ 1.3.2 MB97R8130 Pin Configuration

MB97R8130 is assembled into TSSOP16 package. Figure 1.3.2 shows the pin layout of the package, and Table 1.3.2 shows the pin information.

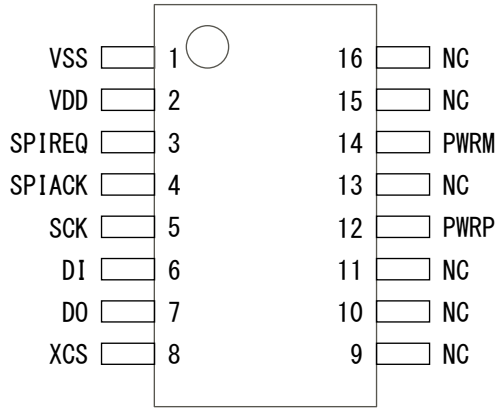


Figure 1.3.2 Pin location of MB97R8130 TSSOP16 Package

Table 1.3.2 Pin information of MB97R8130 TSSOP16 package

No.	Pin	In/Out	Function
1	VSS	VSS	Ground
2	VDD	In(Power)	Voltage apply for SPI communication
3	SPIREQ	In	SPI Slave Request input
4	SPIACK	Out	Response to SPI Slave request (SPI status output)
5	SCK	In	SPI Clock
6	DI	In	SPI Data Input
7	DO	Out	SPI Data Output
8	XCS	In	SPI Chip Select
9	NC	−	Open
10	NC	−	Open
11	NC	−	Open
12	PWRP	In/Out	Antenna pad for RF communication
13	NC	−	Open
14	PWRM	In/Out	Antenna pad for RF communication
15	NC	−	Open
16	NC	−	Open

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■ 2 RF INTERFACE

RF signal interface is compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0.

■ 2.1 Modulation type, communications timing

Compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0

■ 2.2 Inventory, Tag selection

Compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0

■ 2.3 Tag state-transition

Compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0

■ 2.4 RF communication Error code

This LSI replies error code if it encounters an error when executing a handle-based command under Open state or Secured state. Error code is shown in Table 2.4, which is compliant with EPCglobal Class 1 Generation 2 Ver.1.2.0 (AnnexI).

Table 2.4 Error code

Error code	Error code name	Error description
00h	Other errors	Other errors not covered by the following errors
03h	Memory overrun	The specified memory location does not exist.
04h	Memory locked	The specified memory location is locked or permalocked
0Bh	Insufficient power	Insufficient power to perform the operation

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■ 3 SPI INTERFACE (MB97R8130 only)

■ 3.1 Overview

This LSI has SPI (Serial Peripheral Interface) interface that enables to operate as SPI slave device. In SPI mode, the memory data can be accessed through the SPI interface (External power is required for the operation).

■ 3.2 SPI Mode

This LSI supports SPI mode 0 (CPOL=0, CPHA=0).

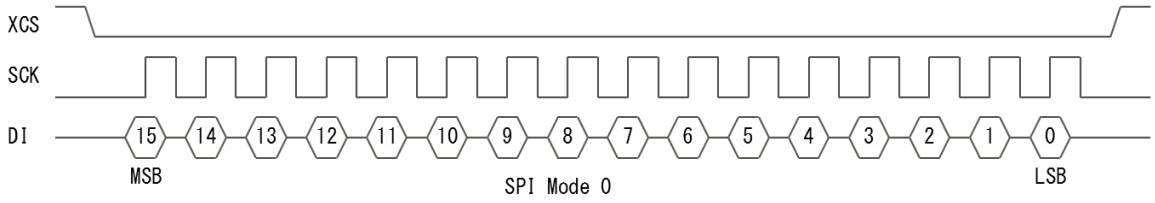


Figure 3.2 – SPI mode

■ 3.3 SPI Interface

■ 3.3.1 Connection to SPI Interface

This LSI can work as a slave mode of SPI. It can be connected to the microcontroller equipped with SPI port as shown in the Figure 3.3.1.

In order to start SPI slave communication, SPI controller shall set SPIREQ to “H” level to request the communication. After SPIACK outputs “H” level, XCS shall be set to “L” level. And then SPI slave communication will be enabled. SPI controller shall stay SPIREQ “H” level, and can continue to execute commands without any interruption from RF interface during when SPIACK is “H” level. Any command from RF interface is invalid during SPI slave operation. When SPIACK is “L” level, SPI slave communication cannot be enabled.

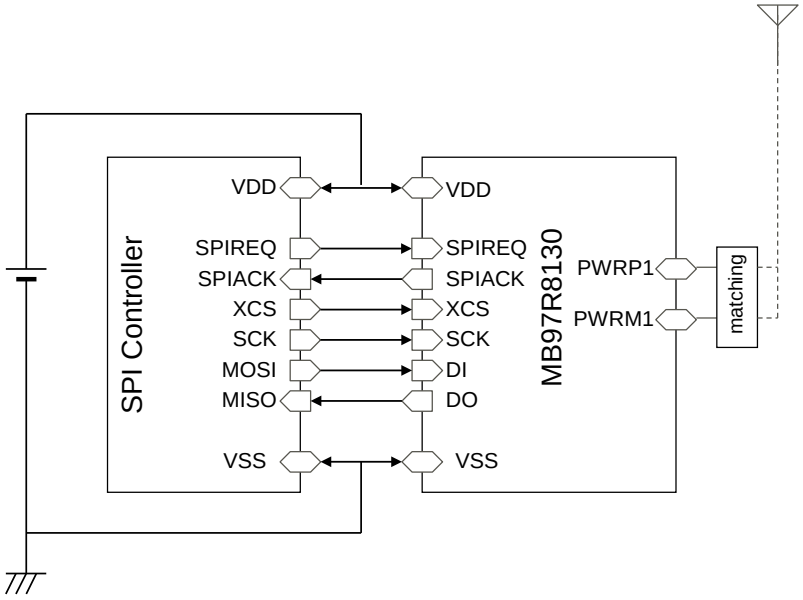


Figure 3.3.1 – SPI Slave interface connection

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■ 3.3.2 Power down mode

This LSI implements Power down mode if SPIREQ is switched to “L” level, which enables to reduce current consumption of the battery connected between VDD-VSS. (refer to 7.4.1) When the voltage is applied on VDD, and SPIREQ=”L” level without RF carrier, the output of both SPIACK and DO becomes undefined, it is recommended for controller to deactivate the signal to SPIACK and DO. All the control pin (including XCS) excepting VDD must be “L” level in power down mode.

■ 3.3.3 Usage

Please refer to Chapter 5.2 and 5.3.regarding the usage of SPI slave interface.

■ 3.4 Power sequence and Arbitration

■ 3.4.1 Arbitration between RF and SPI slave communication

The arbitration feature manages memory access from either RF interface or SPI interface in order to avoid any interruption to each other. SPIREQ and SPIACK manages to switch communication from RF interface to SPI interface by activating VDD, and vice versa.
In order to start SPI slave communication, the master device connected to this LSI shall set SPIREQ to “H” level to request communication. Upon the request, this LSI sets SPIACK to “H” level after completing active communication from RF interface. Then XCS shall be set to “L” level, and SPI slave communication will be ready.
The example of arbitration sequence between RF and SPI slave communication is shown in Figure 3.4.1.
As described, when SPIACK is “L” level, any command input from SPI slave interface is prohibited even if XCS is in “L” level. When SPIACK is “H” level, any command from RF interface is invalid and SPI slave communication will be continued. In this case, SPIREQ shall be set to “L” after completing active communication from SPI interface in order to switch to RF communication.

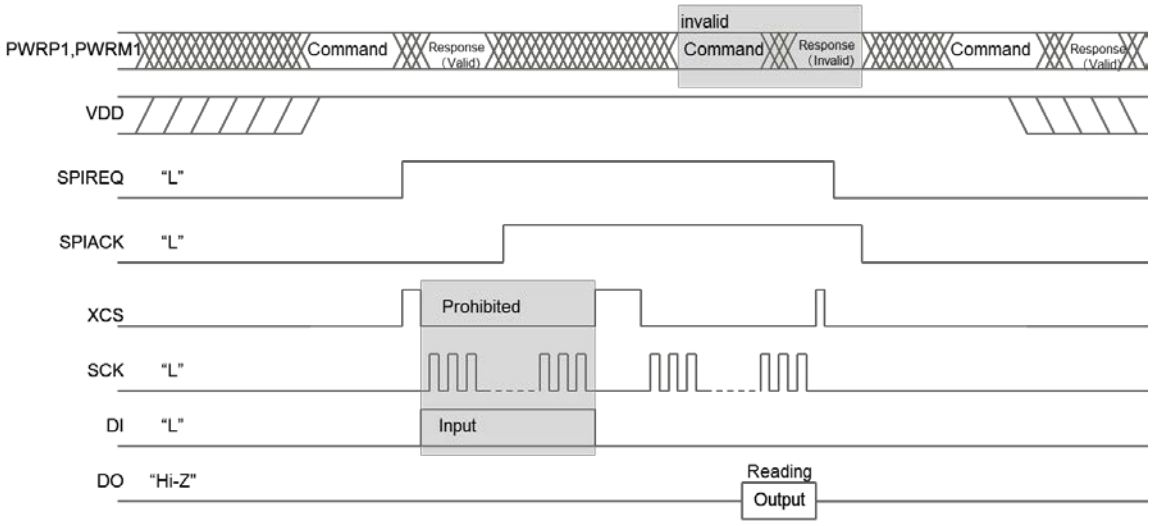


Figure 3.4.1 —The arbitration sequence between RF communication and SPI slave communication

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■ 4 MEMORY

■ 4.1 Memory address

■ 4.1.1 Address description

The memory address is allocated in the units of 16bits (=1word). The logical address in each memory bank is described as WordAdr in this document. WordPtr is the address specified by RF command access, which is described in EBV(Extensible bit vectors) format conforming to EPCglobal Class 1 Generation 2 standard (AnnexA). EBV format is shown in Talbe4.1.1. The address description in this document is shown in Table4.1.2. And the practical examples of the comparison between WordPtr and WordAdr are shown in Table4.1.3.

Table 4.1.1 EBV format (Excerpt from EPCglobal standard)

	0	0	0000000				
	1	0	0000001				
$2^7 - 1$	127	0	1111111				
2^7	128	1	0000001	0	0000000		
$2^{14} - 1$	16383	1	1111111	0	1111111		
2^{14}	16384	1	0000001	1	0000000	0	0000000

Table 4.1.2 Address description in this document

Address range	WordAdr[13:0] *1	WordPtr[7:0] or WordPtr[15:8] (RF access)	Comparison between WordPtr and WordAdr
0000h to 007Fh	0000h to 007Fh	00h to 7Fh	WordPtr={0, WordAdr[6:0]} *2
0080h to 0EFFh	0080h to 0EFFh	8100h to 9D7Fh	WordPtr={1,WordAdr[13:7], 0,WordAdr[6:0]} *2

*1. The address specified by SPI slave access is 2bits of MemBank and 14bits of WordAdr (16bits total).
*2. Underlined 0,1 is defined by EBV format.

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Table 4.1.3 Comparison between WordPtr and WordAdr

WordAdr = 0000h

WordAdr[13:0]			13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000h			0	0	0	0	0	0	0	0	0	0	0	0	0	0

WordPtr[7:0]									7	6	5	4	3	2	1	0
00h									0	0	0	0	0	0	0	0

SPI Slave address[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000h	MemBank		0	0	0	0	0	0	0	0	0	0	0	0	0	0

WordAdr = 007Fh

WordAdr[13:0]			13	12	11	10	9	8	7	6	5	4	3	2	1	0
007Fh			0	0	0	0	0	0	0	1	1	1	1	1	1	1

WordPtr[7:0]									7	6	5	4	3	2	1	0
7Fh									0	1	1	1	1	1	1	1

SPI Slave address[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000h	MemBank		0	0	0	0	0	0	0	1	1	1	1	1	1	1

WordAdr = 0080h

WordAdr[13:0]			13	12	11	10	9	8	7	6	5	4	3	2	1	0
0080h			0	0	0	0	0	0	1	0	0	0	0	0	0	0

WordPtr[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8100h	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

SPI Slave address[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0080h	MemBank		0	0	0	0	0	0	1	0	0	0	0	0	0	0

WordAdr = 0EFFh

WordAdr[13:0]			13	12	11	10	9	8	7	6	5	4	3	2	1	0
0EFFh			0	0	1	1	1	0	1	1	1	1	1	1	1	1

WordPtr[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
9D7Fh	1	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1

SPI Slave address[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0EFFh	MemBank		0	0	1	1	1	0	1	1	1	1	1	1	1	1

* The data stored in bit15, bit7 of WordPtr is defined by EBV format.

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■ 4.2 Memory Map

■ 4.2.1 Memory bank

The Non-volatile memory (FRAM) of this LSI is divided into the following four banks.

Table 4.2.1 Memory map

Bank		Address		Command Accessibility							
MemBank [1:0]	Definition	WordAdr[13:0]	WordPtr[15:8] WordPtr[7:0]	RF						SPI Slave	
				Read	Write	BlockWrite	BlockErase	BlockPermalock	Select	SpiRead	SpiWrite
11	USER	0000h to 0EFFh	00h to 9D7Fh	✓	✓	✓	✓	✓	✓	✓	✓
10	TID	0000h to 000Ch	00h to 0Ch	✓	—	—	—	—	✓	✓	—
01	EPC	0000h to 001Fh	00h to 1Fh	✓	✓	✓	✓	—	✓	✓	—
00	RESERVED	0000h to 003Fh	00h to 3Fh	✓	✓	—	—	—	—	—	—

USER, TID, EPC, and RESERVED memory banks contain the data in the format defined by EPCglobal C1G2 specification (Chapter 6.3.2.1). In each memory bank, the WordAdr and the WordPtr start from zero (00h).

■ 4.2.2 TID bank

The memory map of TID bank is shown in Table 4.2.2. TID bank can only be read, and the setting values cannot be changed. For details, please refer to EPCglobal Class 1 Generation 2 standard.

Table 4.2.2 TID bank memory map

		MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB	
WordAdr	WordPtr																	Setting Value
00h	00h	Allocation Class								Designer								E281h
01h	01h	Designer				Product ID								Version				0081h
02h	02h	XTID header																3C00h
03h	03h	Serial Number																*unique*
04h	04h	Serial Number																*unique*
05h	05h	Serial Number																*unique*
06h	06h	optional command support																1DDEh
07h	07h	BlockErase parameter																0002h
08h	08h	BlockErase parameter																0310h
09h	09h	BlockWrite parameter																0002h
0Ah	0Ah	BlockWrite parameter																0310h
0Bh	0Bh	Permalock Block size																0200h
0Ch	0Ch	User memory size																0F00h

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■ 4.2.3 EPC bank

The memory map of EPC bank is shown in Table 4.2.3.

Table 4.2.3 EPC bank memory map

		MSB															LSB	
WordAdr	WordPtr	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default Value
00h	00h	Stored CRC																
01h	01h	Stored PC																3400h
02h	02h	EPC data																0000h
03h	03h	EPC data(Serial Number *)																*unique*
04h	04h	EPC data(Serial Number *)																*unique*
05h	05h	EPC data(Serial Number *)																*unique*
06h	06h	EPC data																0000h
07h	07h	EPC data																0000h
08h	08h	EPC data																0000h
09h	09h	EPC data																0000h
0Ah	0Ah	EPC data																0000h
0Bh	0Bh	EPC data																0000h
0Ch	0Ch	EPC data																0000h
0Dh	0Dh	EPC data																0000h
0Eh	0Eh	EPC data																0000h
0Fh	0Fh	EPC data																0000h
10h	10h	EPC data																0000h
・・・	・・・	EPC data																0000h
1Fh	1Fh	EPC data																0000h

*. As default value, the same serial number is stored in WordAdr=03h to 05h of EPC bank as the number stored in WordAdr=03h to 05h of TID bank.

The length of EPC is specified by EPC length field of Stored PC. The length is preprogrammed to 6 (words) as default value, which indicates 6words of EPC (WordAdr 02h to 07h). It is possible to expand the length up to 30words (WordAdr 02h to 1Fh) by programming the data of EPC length field
This LSI does not support XPC_W1 and XPC_W2. Stored CRC is not preprogrammed, because it is reflected after the response to ACK command.

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■ 4.2.4 USER bank

The memory map of USER is divided into 8 Area groups as shown in Table 4.2.4.1.

Table 4.2.4.1 USER bank memory map

		MSB															LSB	
WordAdr	WordPtr	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default Value
000h to 1FFh	00h to 837Fh	User data (Area0)																0000h
200h to 3FFh	8400h to 877Fh	User data (Area1)																0000h
400h to 5FFh	8800h to 8B7Fh	User data (Area2)																0000h
600h to 7FFh	8C00h to 8F7Fh	User data (Area3)																0000h
800h to 9FFh	9000h to 937Fh	User data (Area4)																0000h
A00h to BFFh	9400h to 977Fh	User data (Area5)																0000h
C00h to DFFh	9800h to 9B7Fh	User data (Area6)																0000h
E00h to EFFh	9C00h to 9D7Fh	User data (Area7)																0000h

Each area can be protected by Area Password (refer to Chapter6.2). And the same area is allocated for PermalockBlock (refer to Chapter5.1.3).
Regarding the memory access from RF communication (BlockWrite, BlockErase, and Read command), when the address reaches to WordPtr=8F7Fh (WordAdr=7FFh) among the range specified by WordCount, the address to be followed will be WordPtr=9000h (WordAdr=800h). In the same case from SPI slave communication (SpiWrite, SpiRead command), the address counter rollovers from WordAdr=7FFh to 000h.

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■ 4.2.5 RESERVED bank

RESERVED bank is used for Password data management.
32bits Password can be set by 2steps of 16bits writing, 1st for [31:16] and 2nd for [15:0] by Req_RN and Write command as a set of sequence respectively without any other command between the steps.

Table 4.2.5 RESERVED bank memory map

		MSB															LSB	
WordAdr	WordPtr	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default Value
00h	00h	Kill password [31:16]																0000h
01h	01h	Kill password [15:0]																0000h
02h	02h	Access password [31:16]																0000h
03h	03h	Access password [15:0]																0000h
04h	04h	Reserved																0000h
・・・	・・・																	0000h
1Fh	1Fh	Reserved																0000h
20h	20h	Area password（Setting) (Area0) [31:16]																0000h
21h	21h	Area password（Setting) (Area0) [15:0]																0000h
22h	22h	Area password（Setting) (Area1) [31:16]																0000h
23h	23h	Area password（Setting) (Area1) [15:0]																0000h
24h	24h	Area password（Setting) (Area2) [31:16]																0000h
25h	25h	Area password（Setting) (Area2) [15:0]																0000h
26h	26h	Area password（Setting) (Area3) [31:16]																0000h
27h	27h	Area password（Setting) (Area3) [15:0]																0000h
28h	28h	Area password（Setting) (Area4) [31:16]																0000h
29h	29h	Area password（Setting) (Area4) [15:0]																0000h
2Ah	2Ah	Area password（Setting) (Area5) [31:16]																0000h
2Bh	2Bh	Area password（Setting) (Area5) [15:0]																0000h
2Ch	2Ch	Area password（Setting) (Area6) [31:16]																0000h
2Dh	2Dh	Area password（Setting) (Area6) [15:0]																0000h
2Eh	2Eh	Area password（Setting) (Area7) [31:16]																0000h
2Fh	2Fh	Area password（Setting) (Area7) [15:0]																0000h
30h	30h	Area password（Authentication） (Area0) [31:16]																0000h
31h	31h	Area password（Authentication） (Area0) [15:0]																0000h
32h	32h	Area password（Authentication） (Area1) [31:16]																0000h
33h	33h	Area password（Authentication） (Area1) [15:0]																0000h
34h	34h	Area password（Authentication） (Area2) [31:16]																0000h
35h	35h	Area password（Authentication） (Area2) [15:0]																0000h
36h	36h	Area password（Authentication） (Area3) [31:16]																0000h
37h	37h	Area password（Authentication） (Area3) [15:0]																0000h
38h	38h	Area password（Authentication） (Area4) [31:16]																0000h
39h	39h	Area password（Authentication） (Area4) [15:0]																0000h
3Ah	3Ah	Area password（Authentication） (Area5) [31:16]																0000h
3Bh	3Bh	Area password（Authentication） (Area5) [15:0]																0000h
3Ch	3Ch	Area password（Authentication） (Area6) [31:16]																0000h
3Dh	3Dh	Area password（Authentication） (Area6) [15:0]																0000h
3Eh	3Eh	Area password（Authentication） (Area7) [31:16]																0000h
3Fh	3Fh	Area password（Authentication） (Area7) [15:0]																0000h

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■ 5 COMMAND(Tag operation)

■ 5.1 RF communication command

All mandatory commands and optional commands specified in EPCglobal C1G2 Ver.1.2.0. (Chapter 6.3.2.11) are supported as described in Table 5.1.
However, Parts of the specification of BlockWrite, BlockErase, BlockPermalock command (Optional command), and Read command (Mandatory command) are different from EPC C1G2 standard as described in Chapter 5.1.1, 5.1.2, 5.1.3, and 5.1.4.

Table 5.1 – RF mode command

Type	Command name	Command code
Mandatory	QueryRep	00
	ACK	01
	Query	1000
	QueryAdjust	1001
	Select	1010
	NAK	1100 0000
	Req_RN	1100 0001
	Read	1100 0010
	Write	1100 0011
	Kill	1100 0100
	Lock	1100 0101
Optional	Access	1100 0110
	BlockWrite	1100 0111
	BlockErase	1100 1000
	BlockPermalock	1100 1001

※Differences from EPCglobal C1G2 Ver. 1.2.0
(1) Stored CRC-16
If Stored PC and/or EPC data stored in EPC bank are renewed, StoredCRC-16 will not be updated when the power is turned on, but it is updated on the response to ACK command without truncation.
(2)UMI
UMI is fixed to “1” on this LSI. According to EPCglobal C1G2 Ver. 1.2.0, UMI stored in bit[10] of StoredPC in EPC bank shall be calculated by OR of bit[12:8] of WordAdr=00h in USER bank.
(3)Response to Read command when the WordCount is specified to 00h
According to EPCglobal C1G2 Ver. 1.2.0, the tag shall reply the whole data from the specified WordPtr to the last address of the bank, when the WordCount is specified to 00h.
USER bank of this LSI consists of 8 areas and can be protected by Area Password. Therefore, if parts of the data to be read is protected by Area Password, any data cannot be read and error code “04h” (indicating Memory locked) will be replied.
(4)Area Password
Area Password for data protection is stored in WordPtr=20h to 3Fh (WordAdr=20h to 3Fh) of RESERVED bank. As described in Chapter 6, Write command is used for Area Password setting and authentication when the command accesses to the specific address.

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■ 5.1.1 BlockWrite (Optional command)

BlockWrite command format is shown in Table5.1.1. Part of the function are different from what is specified in EPCglobal C1G2 Ver.1.2.0 as following.

・MemBank specifies only EPC and USER bank. If BlockWrite command is executed on RESERVED and TID bank, error code “03h” (indicating Memory overrun) is replied. In this case, the data will not be written into the specified address.

・WordCount specifies the number of words to be written. If 00h is specified, the command will be ignored. When the specified address is located in EPC bank or some address located in WordPtr=00h to 8F7Fh (WordAdr=000h to 7FFh) of USER bank, WordCount shall be 16(10h) or less. If it is 17(11h) or more, error code “03h” (indicating Memory overrun) will be replied. When the specified address is located in WordPtr=9000h to 9D7Fh (WordAdr=800h to EFFh), WordCount shall be specified up to 255(FFh). In this case, the data up to 16words is to be written into the specified address after CRC verification, but the data over 16words is to be written continuously without CRC verification. Therefore if the communication is terminated without any response because of low power detection, some data may have been written before the termination. When the specified address is all or partially locked by the BlockPermalock command or protected by Area Password, any data will not be written and error code “04h” (indicating Memory locked) is replied.

Table 5.1.1 － BlockWrite command

	Command	MemBank	WordPtr	WordCount	Data	RN	CRC
Number of bits	8	2	EBV	8	WordCount *16	16	16
Description	1100 0111	01:EPC 11:USER	Starting Address Pointer	Number of words to write	Data to be written	handle	CRC-16

When the address reaches WordPtr=8F7Fh (WordAdr=7FFh) among the range specified by WordCount, the address to be followed will be WordPtr=9000h (WordAdr=800h).

* In SPI slave communication, the address counter rollovers from WordAdr=7FFh to 000h.

■ 5.1.2 BlockErase (Optional command)

BlockErase command format is shown in Table5.1.2. Parts of the function are different from what is specified in EPCglobal C1G2 Ver.1.2.0 as described as follows.

・MemBank specifies only EPC and USER bank. If BlockErase command is executed on RESERVED and TID bank, error code “03h” (indicating Memory overrun) is replied. In this case, the data will not be erased.

・WordCount specifies the number of data to be erased. If 00h is specified, the command will be ignored. 01h to 10h shall be specified. When the specified address is all or partially locked by the BlockPermalock command or protected by Area Password, any data will not be erased and error code “04h” (indicating Memory locked) is replied.

Table 5.1.2 - BlockErase Command

	Command	MemBank	WordPtr	WordCount	RN	CRC
Number of bits	8	2	EBV	8	16	16
Decription	1100 1000	01:EPC 11:USER	Starting Address Pointer	Number of words to erase	handle	CRC-16

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■ 5.1.3 BlockPermalock (Optional command)

The unit of Block to be locked is defined as 512 words for this LSI. The BlockPermalock command can be executed to the 8 blocks of USER bank which is 7 areas of 8k bits and 1 area of 4k bits.

■ 5.1.3.1 BlockPermalock （Setting）

The format of the BlockPermalock command for Permalock setting is shown in Table 5.1.3.1. The Read/Lock value is set to “1”, and the specified bock will be locked permanently. Lock data field is described in Chapter 5.1.3.3.

Table 5.1.3.1 – BlockPermalock command (Permalock)

	Command	RFU	Read /Lock	Mem Bank	BlockPtr	Block Range	LockData	RN	CRC
Number of bits	8	8	1	2	8	8	16	16	16
Description	1100 1001	0000 0000	1:Perma Lock	11:USER	0000 0000	0000 0001	0:Retain current permalock setting 1:Assert permalock	handle	CRC -16

There is a limitation as follows. If any other value is set, error code “03h” (indicating Memory overrun) will be replied and permalock operation is terminated.

- MemBank: Only executed for USER bank.
- BlockPtr: Only 00h is supported.
- BlockRange: Only 01h is supported.

■ 5.1.3.2 BlockPermalock （Read）

The format of the BlockPermalock command for reading permalock status is shown in Table 5.1.3.2.1. The Read/Lock value is set to “0”, and the permalock status of 8blocks of UER bank can be read. The response is shown in Table 5.1.3.2.2.

Table 5.1.3.2.1 – BlockPermalock command (Read)

	Command	RFU	Read /Lock	MemBank	BlockPtr	Block Range	RN	CRC
Number of bits	8	8	1	2	8	8	16	16
Description	1100 1001	0000 0000	0:Read	11:USER	0000 0000	0000 0001	handle	CRC-16

Table 5.1.3.2.2 – Response to BlockPermalock command (Read)

	Header	LockData	RN	CRC
Number of bits	1	16	16	16
Description	0	Permalock bits	handle	CRC-16

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There is a limitation as follows. If any other value is set, error code “03h” (indicating Memory overrun) will be replied and reading operation is terminated.

- MemBank: Only executed for USER bank.
- BlockPtr: Only 00h is supported.
- BlockRange: Only 01h is supported.

■ 5.1.3.3 BlockPermalock and Permalocked Block

16bits of Lock data and corresponded block is shown in Table 5.1.3.3.

Table 5.1.3.3 – BlockPermalock data

Bit	Area	WordAdr	WordPtr
15	0	000h to 1FFh	00h to 837Fh
14	1	200h to 3FFh	8400h to 877Fh
13	2	400h to 5FFh	8800h to 8B7Fh
12	3	600h to 7FFh	8C00h to 8F7Fh
11	4	800h to 9FFh	9000h to 937Fh
10	5	A00h to BFFh	9400h to 977Fh
9	6	C00h to DFFh	9800h to 9B7Fh
8	7	E00h to EFFh	9C00h to 9D7Fh
7	—	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

When Lock data is set by BlockPermalock command (refer to Chapter 5.1.3.1), Bit[7:0] shall be set to “0” because of no target block.

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■ 5.1.4 Read (Mandatory)

The command format is shown in Table 5.1.4.1

Table 5.1.4.1– Read command

	Command	MemBank	WordPtr	WordCount	RN	CRC
Number of bits	8	2	EBV	8	16	16
Description	1100 0010	00:RESERVED 01:EPC 10:TID 11:USER	Starting Address Pointer	Number of Words to read	handle	CRC-16

When the address reaches WordPtr=8F7Fh (WordAdr=7FFh) among the range specified by WordCount, the address to be followed will be WordPtr=9000h (WordAdr=800h).
* In SPI slave communication, the address counter rollovers from WordAdr=7FFh to 000h.

When WordCount is set to “00h”, the response will be as shown in Table 5.1.4.2.

Table 5.1.4.2– Response to Read command with WordCount “00h”

MemBank	Area Password	Response
11:USER	Zero Password (All Area)	The data from the specified WordPtr (Table 5.1.4.1) to 9D7Fh (WordAdr=EFFh) are replied as normal response.
	Non zero Password (Some Area)	No data is read. Error code “04h” (indicating Memory locked) is replied. (refer to Chapter 2.4)
10:TID	—	The data from the specified WordPtr (Table 5.1.4.1) to 0Fh are replied as normal response.
01:EPC	—	The data from the specified WordPtr (Table 5.1.4.1) to the WordPtr corresponding to the length of EPC are replied as normal response.
00:RESERVED	—	The data from the specified WordPtr (Table 5.1.4.1) to 3Fh are replied as normal response.

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■ 5.1.5 Lock (Mandatory)

The command format is shown in Table 5.1.5. When the Access Password(WordAdr=02h to 03h (WordPtr=02h to 03h)) is locked by setting Payload bit [17,16] and [7,6], Area Passwords(WordAdr=20h to 3Fh (WordPtr=20h to 3Fh)) are also locked automatically.
Regardless whether the password is locked or not, Area Password authentication can be executed by Write command. The detail of the command is specified in EPCglobal C1G2 Ver.1.2.0 (Chapter 6.3.2.11.3.5).

Table 5.1.5– Lock command

	Command	Payload	RN	CRC
Number of bits	8	20	16	16
Description	1100 0101	Mask and Action Fields	handle	CRC-16

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■ 5.2 SPI slave communication command (MB97R8130 only)

This LSI will support 3 types of operate-code for SPI slave interface. The operate-code is 8bits code described in Table 5.2. If other codes are used, the command is ignored. If XCS is raised during the input sequence of operate-code, the command cannot be executed.

Table 5.2 - Operate-code for SPI slave interface

Code name	Function	Operate-code
SpiRead	Read data in units of 16bits from USER memory area.	0000 0011
SpiWrite	Write data in units of 16bits into USER memory area.	0000 0010
SpiRDSR	Read 16bits of Error information register(SPI slave)	0000 0101

■ 5.2.1 SpiRead

SpiRead command is to read memory data in units of 16bits (1word). The address shall be specified as 2bits of MemBank followed by 14bits of WordAdr (Total 16bits). The command sequence is described in Figure 5.2.1. Through DI pin, the following data shall be input synchronously to the rising edge of SCK after XCS is fallen.
SpiRead operate code (8bit:03h)
MemBank (2bit)
WordAdr (14bit)
USER bank, TID bank and EPC bank are readable banks. The upper 2 bit of WordAdr shall be fixed to “00”.
In response to the command input, the reading data will be output from DO synchronously to the falling edge of SCK. During the period of output from DO, any input from DI will be ignored. SpiRead command will be terminated when XCS is raised, and the output from DO will be “Hi-Z”.
The command keeps on reading with automatically incremented address by continuous 16cycles of clock to SCK before XCS rising. If WordAdr is specified as 000h to 7FFh of USER bank and the incremented address reaches to WordAdr=7FFh, the address will roll over to WordAdr=000h and read operation is continued. If WordAdr is specified as 800h to EFFh of USER bank and the incremented address reaches to WordAdr=EFFh, the address will not roll over to WordAdr=000h nor WordAdr=800h. In this case, the DO output will be “0”.
When Membank is specified as TID bank or EPC bank, the address will be automatically incremented up to the most significant WordAdr described in Chaper 4.2, and the address will not roll over after that. In this case, the DO output will be “0” until when XCS is raised.

In the following cases, the memory data will not be read out and DO output will be “0”.
1) LSI is in Killed state
2) The specified address is protected by Password
3) MemBank is specified with RESERVED bank

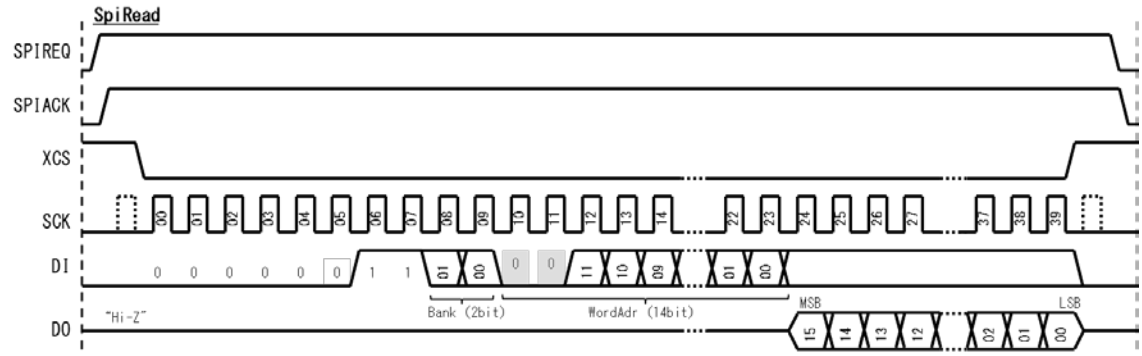


Figure 5.2.1 – SpiRead command sequence

When Access Password is set, the data cannot be read and the output will be “0”. Therefore Access Password shall be cleared before SPI slave communication. If the specified area includes the WordAdr protected by Area Password, only unprotected address will be read and “0” will be output instead from protected address.

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■ 5.2.2 SpiWrite

SpiWrite command is to write data into memory in units of 16 bits (1 word). The address shall be specified as 2bits of MemBank followed by 14bits WordAdr (Total 16bits). The command sequence is described in Figure 5.2.2. Through DI pin, the following data shall be input synchronously to the rising edge of SCK after XCS is fallen.

SpiWrite operate-code (8bit:02h)
MemBank (2bit)
WordAdr (14bit)
Written data (N*16bit)

USER bank is writable bank, and the other banks are not writable. The upper 2 bit of WordAdr shall be fixed to "00".

The command keeps on writing with automatically incremented address by continuous 16 cycles of clock to SCK and 16bits of writing data together before XCS rising. If XCS is raised on the timing before completing 16cycles of clock, the writing data will not be written into memory. If WordAdr is specified as 000h to 7FFh of USER bank and the incremented address reaches to WordAdr=7FFh, the address will roll over to WordAdr=000h and write operation is continued. If WordAdr is specified as 800h to EFFh of USER bank and the incremented address reaches to WordAdr=EFFh, the address will not roll over to WordAdr=000h nor WordAdr=800h. In this case, writing operation completes at WordAdr =EFFh.

In the following cases, the writing data cannot be written, and error information will be stored into SPI error information. (refer to Chapter 5.3.1 for detail).

1) LSI is in Killed state
2) The specified address is protected by Password
3) The specified MemBank is not USER bank
4) WordAdr is over EFFh
5) The specified address is in the locked area

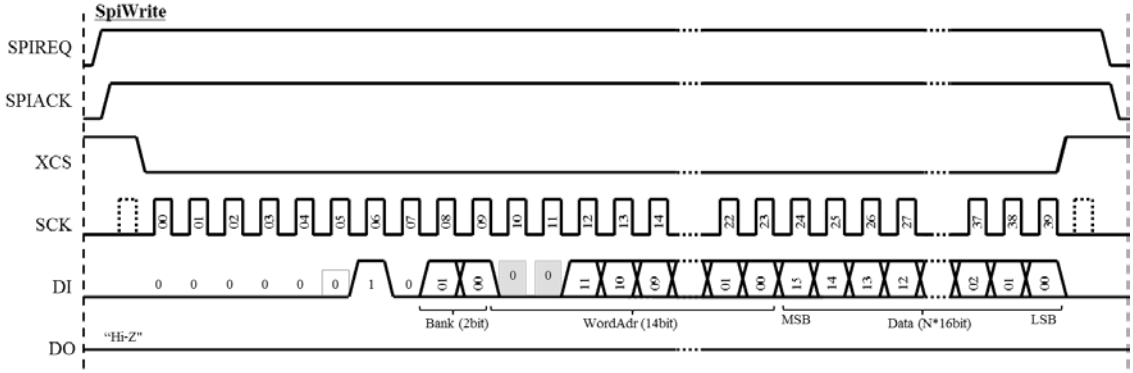


Figure 5.2.2 – SpiWrite command sequence

When Access Password is set, the data cannot be written. Therefore Access Password shall be cleared before SPI slave communication. If the specified area includes the WordAdr protected by Area Password, only unprotected address will be written and nothing will happen on protected address. If the specified area includes the WordAdr locked by Lock command or BlockPermalock command, only writable address will be written and nothing will happen on locked address for writing.

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■ 5.2.3 SpiRDSR

The SpiRDSR command is to read 16 bits of error information on SPI slave communication (refer to Chapter 5.3.1). The command sequence is described in Figure 5.2.3.

Through DI pin, the following data shall be input synchronously to the rising edge of SCK after XCS is fallen.

SpiRDSR operate-code (8bit:05h)

In response to the command input, the 16 bits of error information will be output from DO synchronously to the falling edge of SCK. And SpiRDSR command will be completed when XCS is raised. If XCS is raised before the command completes 16 cycles of clock to SCK, the command will be terminated and the output from DO will be “Hi-Z”. During the period of output from DO, any input from DI will be ignored. If XCS keeps “L” level after the command complete reading, the output from DO will be “L” level.

The error information will be cleared after SpiRDSR command is completed.

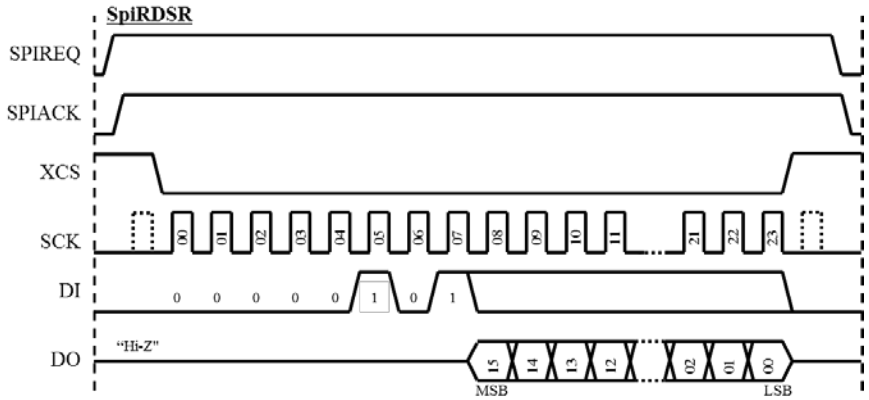


Figure 5.2.3 – SpiRDSR command sequence

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■ 5.3 Error handling to SPI slave communication

On SPI slave communication, an error occurs under the following condition. If an error occurs in SPIRead command operation, the output from DO will be “0” and error information will be stored in error information register.

・Specified memory are is locked.

・Killed status

The data stored in error information register can be read by SpiRDSR command.

■ 5.3.1 Error information register (SPI slave communication)

Error information during SPI slave communication will be stored in the error information as shown in Table 5.3.1. These information can be read by SpiRDSR command.

The information will be cleared after the following operation.

・SpiRDSR command execution

・Power is off

Writing operation to error information register is ignored.

Table 5.3.1 Error information register format

Bit	Description
15	0 (Fixed)
14	0 (Fixed)
13	0 (Fixed)
12	0 (Fixed)
11	0 (Fixed)
10	0 (Fixed)
9	0 (Fixed)
8	0 (Fixed)
7	0 (Fixed)
6	0 (Fixed)
5	0 (Fixed)
4	0 (Fixed)
3	0 (Fixed)
2	0 (Fixed)
1	0: Normal 1: Specified address partly locked
0	0: Normal 1: Killed Status

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■ 6 DATA PROTECTION

■ 6.1 LOCK Command, BlockPermalock Command, and Data protection area

This chapter describes the access control (hereinafter referred to as “Data protection”) for writing and reading memory. LOCK command can protect data in units of Bank except RESERVED Bank. And Kill Password and Access Password stored in RESERVED bank is protected. Area Password (refer to Chapter 6.2) stored in WordPtr=20h to 2Fh (WordAdr=20h to 2Fh) of RESERVED bank are also protected by the same payload [7:6] of Lock command as Access Password protection.

Table 6.1.1 Memory bank and Lock/BlockPermalock

MemBank	LOCK	WordPtr		BlockPermalock	Remarks
00:RESERVED	payload[9:8]	00h to 01h		−	Kill Password
	payload[7:6]	02h to 03h		−	Access Password
		20h to 2Fh		−	Area Password
01:EPC	payload[5:4]	all		−	
10:TID	payload[3:2]	all		−	
11:USER	payload[1:0]	000h to 1FFh		Mask[15]	Area0
		200h to 3FFh		Mask[14]	Area1
		400h to 5FFh		Mask[13]	Area2
		600h to 7FFh		Mask[12]	Area3
		800h to 9FFh		Mask[11]	Area4
		A00h to BFFh		Mask[10]	Area5
		C00h to DFFh		Mask[9]	Area6
		E00h to EFFh		Mask[8]	Area7

Please refer to EPCglobal C1G2 Ver.1.2.0 6.3.2.11.3.9) for the behavior to the combination of Lock command and BlockPermalock command.

■ 6.2 Data Protection for USER bank

USER bank is divided into 8 areas and each area can be access-controlled by Password Authentication.

■ 6.2.1 Area Password setting

Area Password can be set to the WordPtr=20h to 2Fh (WordAdr=20h to 2Fh) of RESERVED bank (refer to Table 4.2.5) by Write command as described in Table 6.2.1. This command is executed only in Secured state.

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Table 6.2.1 Write command (Area Password setting)

	Command	MemBank	WordPtr	Data	RN	CRC
Number of bits	8	2	EBV	16	16	16
Description	1100 0011	00:RESERVED	Starting Address Pointer (20h-2Fh)	RN16 ⊻ Password to be set	handle	CRC-16

■ 6.2.2 Area Password Authentication

Area Password authentication can be set to the WordPtr=30h to 3Fh (WordAdr=30h to 3Fh) of RESERVED bank (refer to Table 4.2.5) by Write command as described in Table 6.2.2. 16bits of Password data will be sent twice for authentication as well as Access command. This command is executed only in Secured state.

Table 6.2.2 Write command (Area Password authentication)

	Command	MemBank	WordPtr	Data	RN	CRC
Number of bits	8	2	EBV	16	16	16
Description	1100 0011	00:RESERVED	Starting Address Pointer (30h-3Fh)	RN16 ⊻ (1/2 Password)	handle	CRC-16

When the authentication is failed, LSI will not reply, which is the same as failure case in the authentication of Access command. When the authentication is succeeded, the state of LSI will be transferred into AreaSecured state, and the area becomes be readable and writeable.
If the Password is set to 0, the state returns to Secured state regardless whether it was AreaSecured state or not. Because the authentication shall be applied to area by area, it is necessary to execute additional Area Password Authentication to the target area under Secured state.

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■ 7 ELECTRICAL CHARACTERISTICS

■ 7.1 Absolute Maximum Rating

Table 7.1 - Absolute Maximum Rating

Parameter	Symbol	Value			Unit	Conditions/Remarks
		MIN	TYP	MAX		
Maximum input voltage	Vmax	—	—	4.0	V	PWRP1-PWRM1,PWRP3-PWRM3
Power supply voltage	VDD	-0.5	—	+4.0	V	
Input voltage	VIN	-0.5	—	VDD+0.5	V	
Output voltage	VOUT	-0.5	—	VDD+0.5	V	
ESD voltage immunity	VESD	-	—	±1200	V	Human Body Model
Storage temperature	Tstg	-40	—	+85	℃	

■ 7.2 Recommended Operation Conditions

Table 7.2 - Recommended Operation Conditions

Parameter	Symbol	Value			Unit	Conditions/Remarks
		MIN	TYP	MAX		
Operating ambient temperature	Ta	-40	—	+85	℃	
Retention guaranteed temperature	Trtn1	-40	—	+85	℃	Retention guaranteed period: 10years
RF communication						
Antenna input frequency	Fclk	860	—	960	MHz	
Receiving modulation depth	(A-B)/A	80	90	100	%	
Receiving bit rate	F_fwd	26.7	—	128	kbps	PIE code: mark rate =1/2
Receiving waveform rise time	Tr	1	—	500	µs	
Receiving waveform settling time	Ts	—	—	1500	µs	
Receiving waveform fall time	Tf	1	—	500	µs	
SPI slave communication						
Power supply voltage	VDD	1.8	—	3.6	V	

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■ 7.3 RF Communication Characteristics

Table 7.3.1 － RF Communication Characteristics (MB97R8120: Bare die)

Parameter	Symbol	Value			Unit	Conditions/Remarks	
		MIN	TYP	MAX			
Minimum operating power when reading	PR_MIN	－	－12	－	dBm	920MHz	Measured with bare die Tari=25us,RTcal=2.5Tari,TRcal=3.0RTcal, DR=8,FM0,BLF=43kbps, DSB-ASK, Modulation depth=90% memory access length≦6Word (※1)
		－	－12	－	dBm	866MHz	
Minimum operating power when writing	PW_MIN	－	－12	－	dBm	920MHz	
		－	－12	－	dBm	866MHz	
Maximum operating power	PMAX		+20		dBm		
Equivalent input capacitance (PWRP1-PWRM1)	CP	－	0.8	－	pF	920MHz	Input power= -12dBm, parallel model
		－	0.8	－	pF	866MHz	Input power= -12dBm, parallel model
Equivalent input resistance (PWRP1-PWRM1)	RP	－	4.1	－	KΩ	920MHz	Input power= -12dBm, parallel model
		－	4.9	－	KΩ	866MHz	Input power= -12dBm, parallel model
Returning bit rate	F_rtrn	40	－	640	kbps		

Table 7.3.2 － RF Communication Characteristics (MB97R8130: TSSOP16 package)

Parameter	Symbol	Value			Unit	Conditions/Remarks	
		MIN	TYP	MAX			
Minimum operating power when reading	PR_MIN	－	－8.8	－	dBm	920MHz	Measured with TSSOP16 package Tari=25us,RTcal=2.5Tari,TRcal=3.0RTcal, DR=8,FM0,BLF=43kbps, DSB-ASK, Modulation depth=90% memory access length≦6Word (※1)
		－	－6.5	－	dBm	866MHz	
Minimum operating power when writing	PW_MIN	－	－8.8	－	dBm	920MHz	
		－	－6.5	－	dBm	866MHz	
Maximum operating power	PMAX		+20		dBm		
Equivalent input capacitance （PWRP1-PWRM1)	CP	－	1.1	－	pF	920MHz	Input power= -8.8dBm, parallel model
		－	1.2	－	pF	866MHz	Input power= -6.5dBm, parallel model
Equivalent input resistance (PWRP1-PWRM1)	RP	－	2.1	－	KΩ	920MHz	Input power= -8.8dBm, parallel model
		－	1.1	－	KΩ	866MHz	Input power= -6.5dBm, parallel model
Returning bit rate	F_rtrn	40	－	640	kbps		

※1 These characteristics are the values for the standalone LSI, and do not specify the values when the LSI is connected to other devices.

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■ 7.4 SPI Slave Communication (MB97R8130)

■ 7.4.1 DC Characteristics

Table 7.4.1 - DC Characteristics

Parameter		Symbol	Value			Unit	Conditions
			MIN	TYP	MAX		
Input leakage current		ILI	—	—	±5	μA	VIN = VDD (SPIREQ pin)
			—	—	±1	μA	VIN = 0V (SPIREQ pin) VIN = 0V to VDD (the other pins※1)
Output leakage current		ILO	—	—	±1	μA	VOUT = 0V to VDD, when output is "Hi-Z" (output pin ※2)
Power supply	ICC	ICC	—	70	200	μA	SCK = 2MHz, Vdd=3.0V
	IPD1	IPD1	—	1	10	μA	SPIREQ ＝ 0V or open No RF reception
	ISB	ISB	—	20	40	μA	SPIREQ ＝ VDD XCS=VDD
"H" level Input voltage		VIH	VDDx0.7	—	VDD+0.3	V	※3
"L" level Input voltage		VIL	−0.3	—	VDDx0.3	V	※3
"H" level Output voltage		VOH	VDD-0.5	—	VDD	V	IOH＝−2mA ※2
"L" level Output voltage		VOL	0	—	0.4	V	IOL＝ 2mA ※2
SPI pin pull-down resistance		RIN	0.8	1	1.2	MΩ	VIN = VDD SPIREQ Pin

※1：XCS、SCK、DI Pin ※2：DO、SPIACK Pin ※3：SPIREQ、XCS、SCK、DI Pin

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■ 7.4.2 AC Characteristics

Table 7.4.2 – AC Characteristics

Parameter	Symbol	Value			Unit	Pin
		MIN	TYP	MAX		
SCK clock frequency	f_{CK}	—	—	2	MHz	SCK
Clock high time	t_{CH}	200	—	—	ns	SCK
Clock low time	t_{CL}	200	—	—	ns	SCK
Chip select set time	t_{CSU}	60	—	—	ns	XCS,SCK
Chip select hold time	t_{CSH}	20	—	—	ns	XCS,SCK
Output enable time	t_{ODLZ}	20			ns	DO,SCK
Output disable time	t_{ODz}	—	—	60	ns	DO,SCK
Output data valid time	t_{ODV}	—	—	80	ns	DO,XCS
Output hold time	t_{OH}	0	—	—	ns	DO,SCK
Deselect time	t_D	280	—	—	ns	XCS
Data rise time	t_R	—	—	5	ns	DI,XCS,SPIREQ
Data fall time	t_F	—	—	5	ns	DI,XCS,SPIREQ
Data set up time	t_{DIS}	20	—	—	ns	DI,SCK
Data hold time	T_{DIH}	20	—	—	ns	DI,SCK

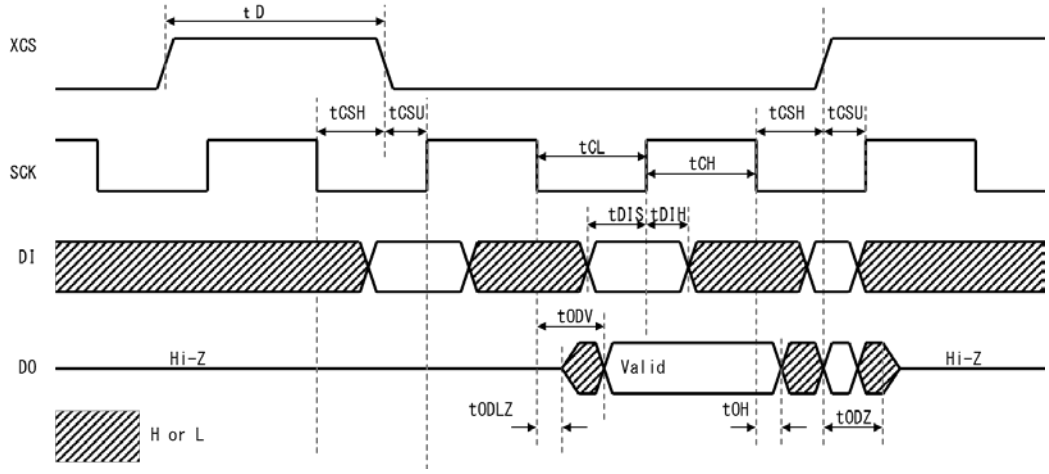


Figure 7.4.2 – SPI slave timing

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■ 7.4.3 Power Sequence for SPI Slave Communication Mode.

The power sequence in SPI slave communication mode is shown in Figure 7.4.3.1 (with VDD off control), and Figure 7.4.3.2 (without VDD off control).

Power-up sequence of SPI slave communication;

Before starting communication, VDD shall be set to “H” level and SPIREQ shall be set to “H” level in a row. Then SPIACK outputs “H” level in the time of tOAV from the rising edge of SPIREQ. In parallel, XCS shall be set to “H” level within the time of tCUS from the rising edge of SPIREQ. SPI slave communication can start when XCS is set to “L” level in the time of tPU from the rising edge of SPIACK.

Power-down sequence of SPI slave communication;

After taking the period of tPD from the rising edge of XCS, SPIREQ shall be set to “L” level. Then SPIACK outputs “L” level in the time of tOHA from the falling edge of SPIREQ. In parallel, XCS shall be set to “L” level within the time of tCHS from the falling edge of SPIREQ. When VDD will be turned off, VDD shall be set to “L” level in more than the time of tPH from the falling edge of SPIACK.

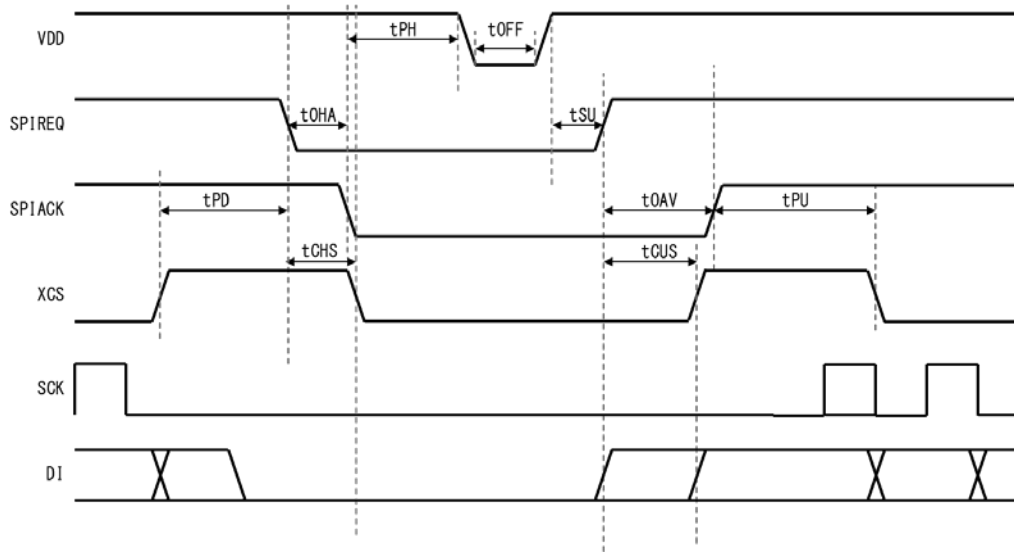


Figure 7.4.3.1 Power sequence (with VDD off control)

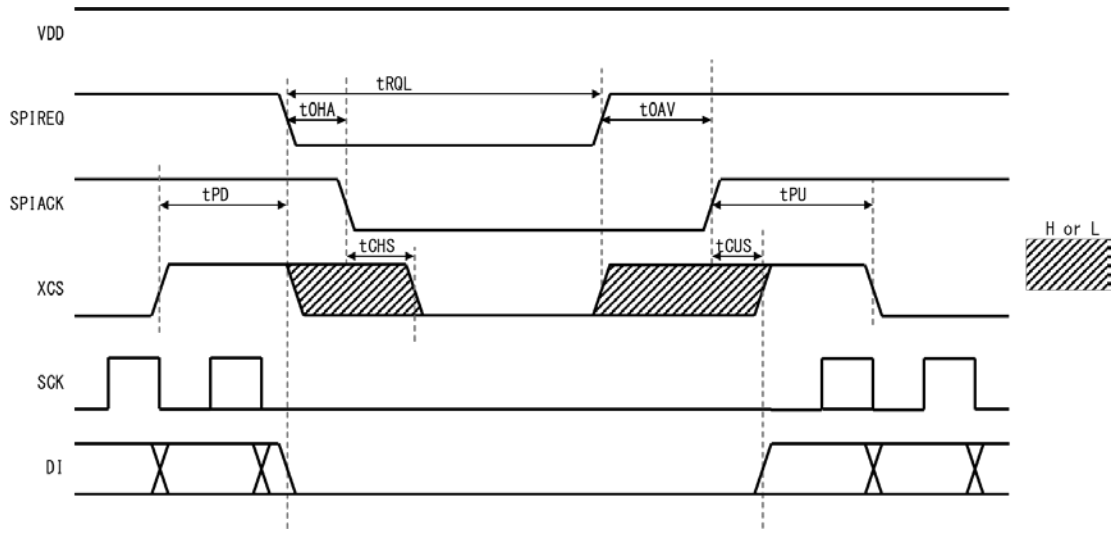


Figure 7.4.3.2 Power sequence (without VDD off control)

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Table 7.4.3 Timing specifications during SPI slave communication

Parameter	Symbol	Value			Unit
		MIN	TYP	MAX	
SPIREQ rising start time	tSU	500	—	—	µs
SPIREQ low time	tRQL	1000	—	—	µs
Power hold time	tPH	0	—	—	µs
XCS level hold time at power ON	tPU	10	—	—	µs
XCS level hold time at power OFF	tPD	1	—	—	µs
Power off time	tOFF	1000	—	—	µs
Output SPIACK definite time	tOAV	1	—	20000	µs
Output SPIACK hold time	tOHA	5	—	10000	ns
XCS setup time(start)	tCUS	—	—	1	µs
XCS hold time(start)	tCHS	0	—	—	µs

If the device does not operate within the specified conditions of cycle or power on/off sequence, memory data cannot be guaranteed.

■ 8 REFLOW CONDITION AND FLOOR LIFE(MB97R8130)

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

■ 9 ORDERING INFORMATION

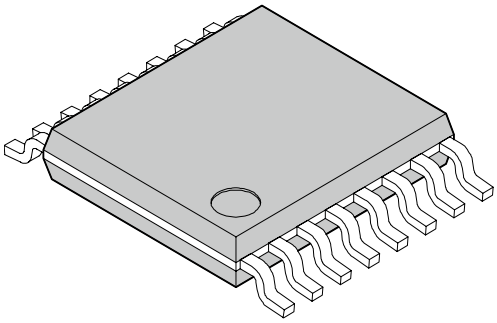
Part Number	Interface	Die / Package	Shipping form	Minimum Shipping Quantity
MB97R8120-DIAB15	RF	Die 150±22.54µm thick	Sawn wafer with Frame Ring	-*
MB97R8130PFT-G-JNE1	RF+SPI	16-pin plastic TSSOP (FPT-16P-M08)	Tube	-*
MB97R8130PFT-G-JNEFE1			Embossed carrier tape (EF Type)	1500
MB97R8130PFT-G-JNERE1			Embossed carrier tape (ER Type)	1500

*. Please contact our sales office about minimum shipping quantity.

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■ 10 PACKAGE INFORMATION(MB97R8130)

16-pin plastic TSSOP

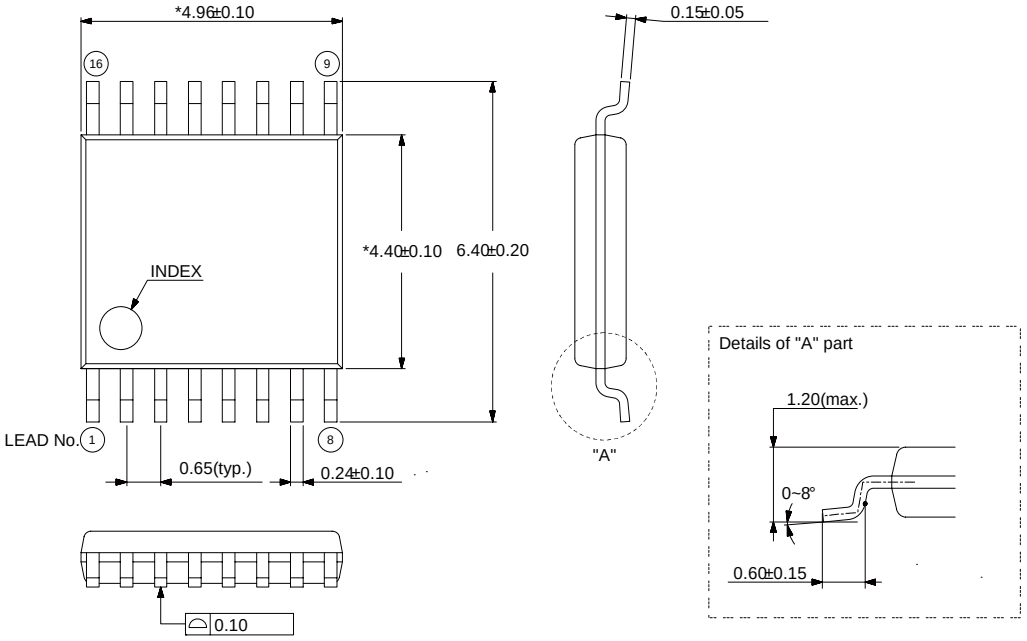


MB97R8130 / FPT-16P-M08

Lead pitch	0.65 mm
Package width · package length	4.40 mm · 4.96 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.20 mm Max

16-pin plastic TSSOP
(FPT-16P-M08)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm .

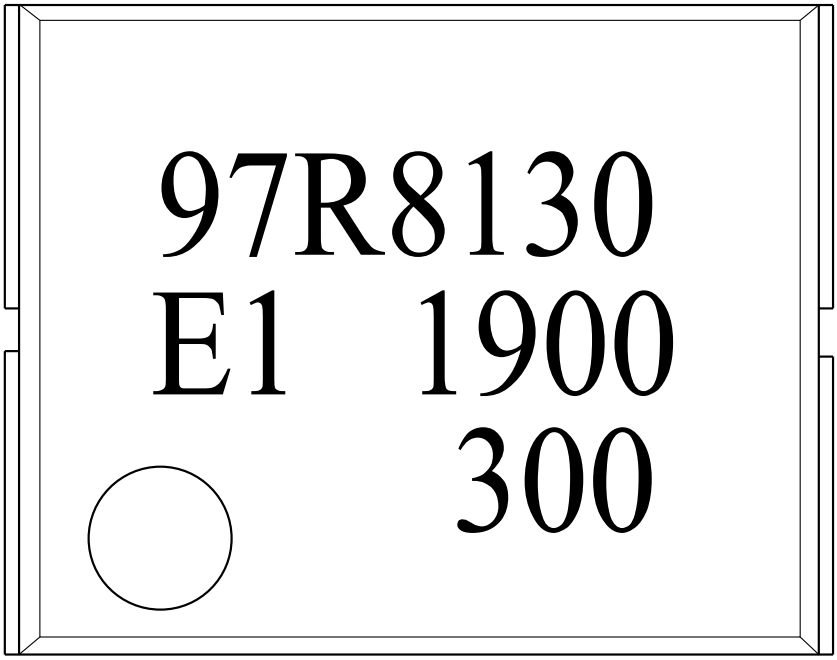
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■ 11 MARKING(MB97R8130)

[MB97R8130PFT-G-JNE1]

[MB97R8130PFT-G-JNEFE1]

[MB97R8130PFT-G-JNERE1]



[FPT-16P-M08]

97R8130: Product Name

E1: Lead-free

1900: Year and Week code

300: Reference number

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■ 12 PACKING INFORMATION (MB97R8130)

■ 12.1 Tube

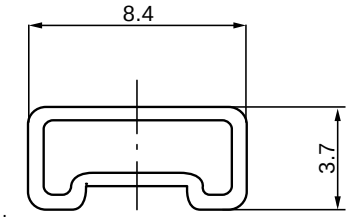
1 Maximum quantity

Maximum quantity		
ICs pcs/tube(520mm)	ICs pcs/inner box	ICs pcs/outer box
90	7,200 (80 tubes/inner box)	28,800 (4 inner boxes/outer box)

2 IC orientation



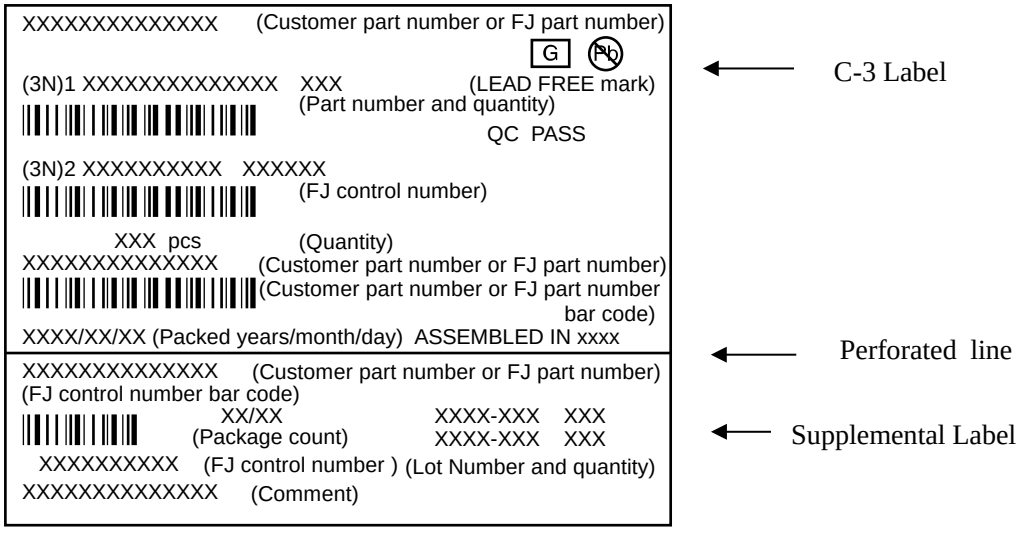
3 Tube dimension



No heat resistance.
Package should not be baked by using tube.

4 Product label indicators

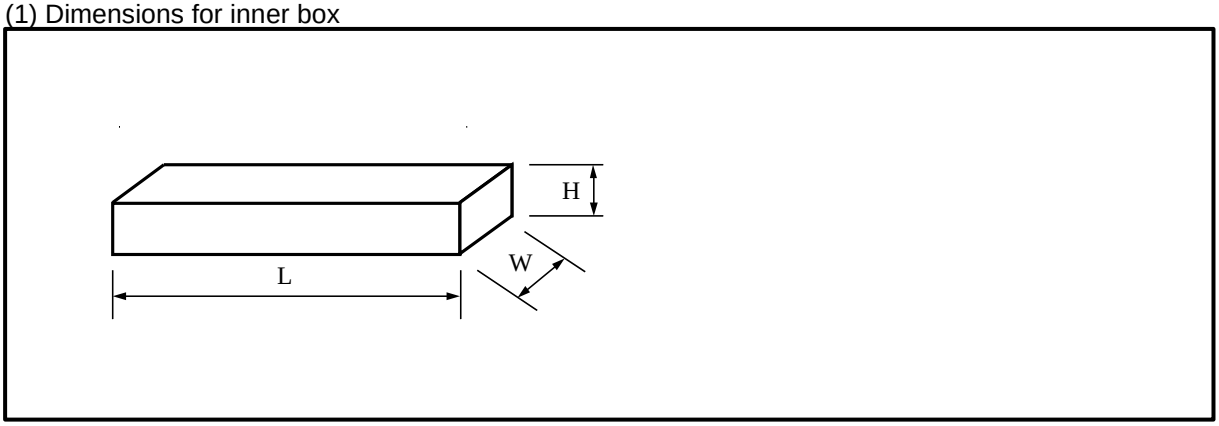
Label I: Label on Inner box/Moisture Barrier Bag
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



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5 Dimensions for Containers

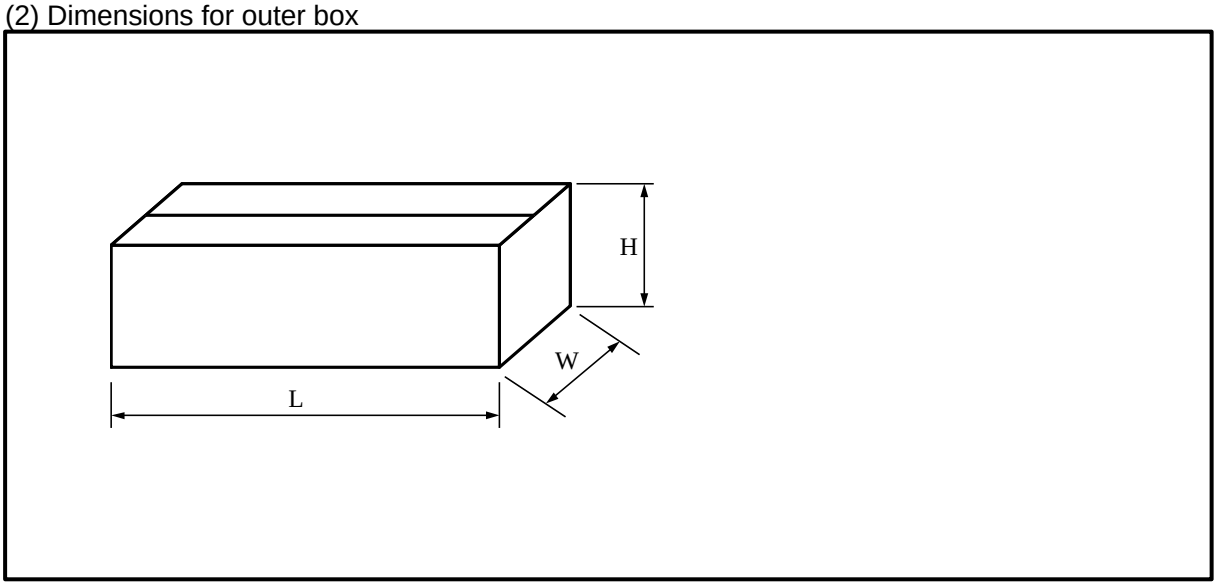
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
549	277	180

(Dimensions in mm)

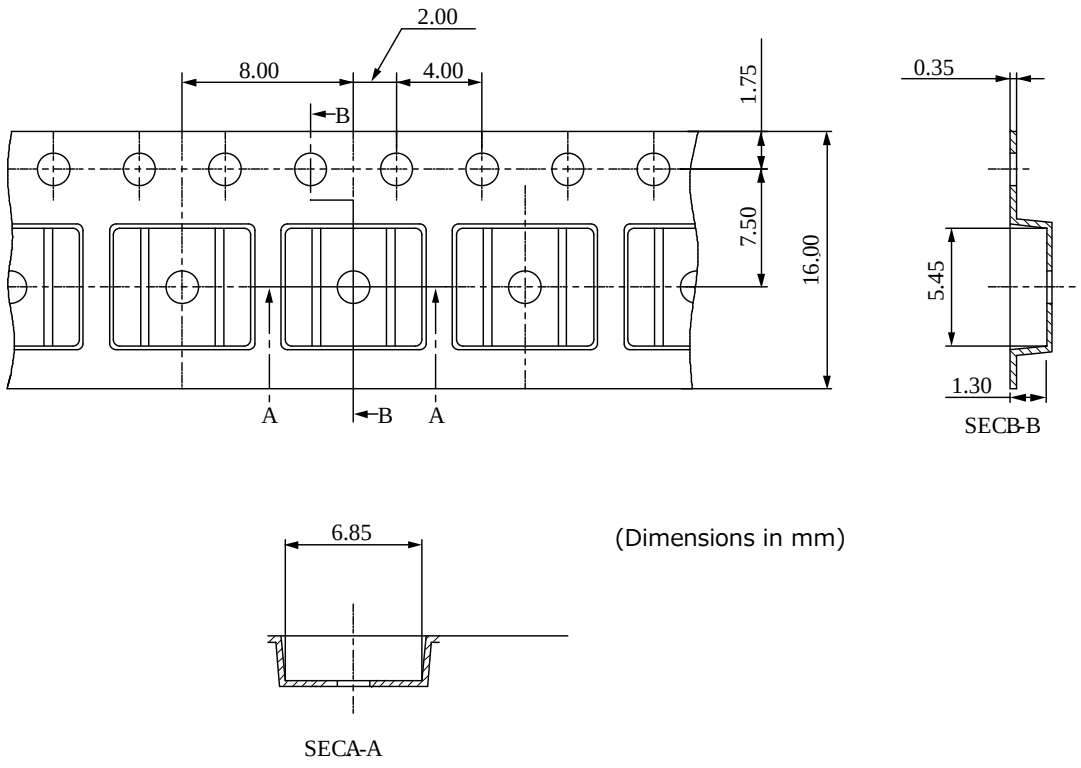
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■ 12.2 Emboss Tape(Φ330mm Reel)

1 Maximum quantity

Maximum quantity		
ICs pcs/reel(Φ330mm)	ICs pcs/inner box	ICs pcs/outer box
1,500	1,500 (1 bag/inner box)	10,500 (7 inner boxes/outer box)

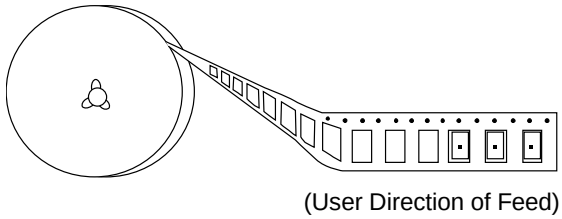
2 Tape dimensions



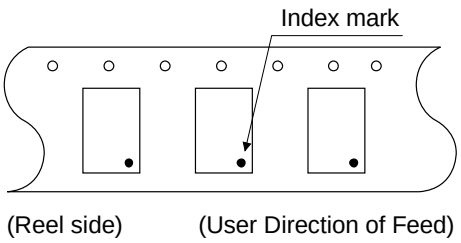
Material : Conductive polystyrene
Heat proof temperature : No heat resistance. Package should not be baked by using tape and/or reel.

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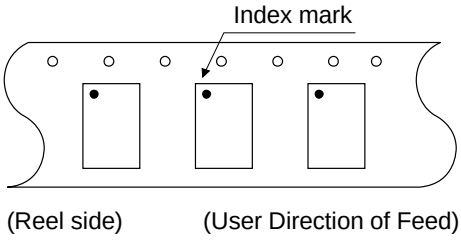
3 IC orientation



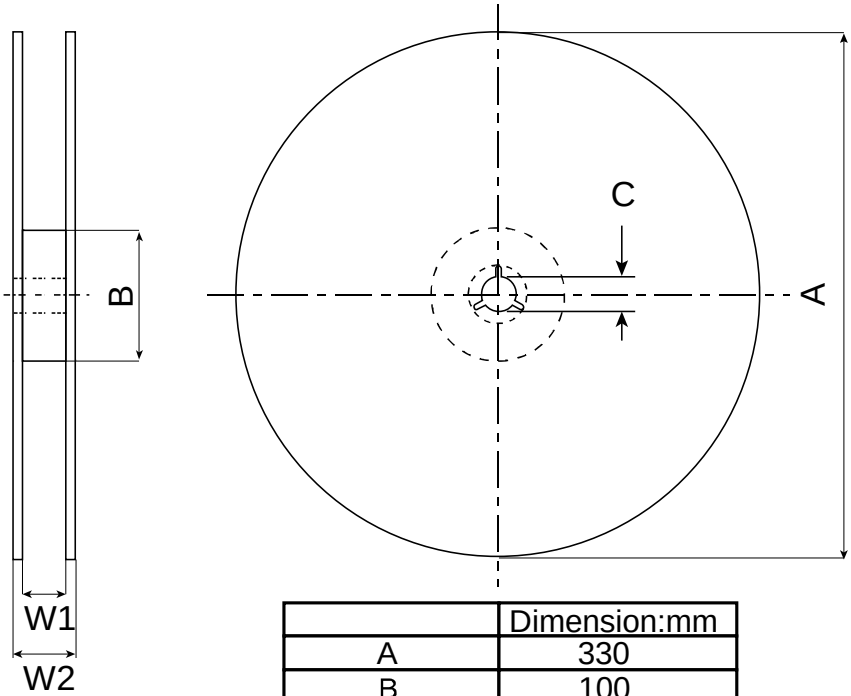
• EF type [MB97R8130PFT-G-JNEFE1]



• ER type [MB97R8130PFT-G-JNERE1]



4 Reel dimensions



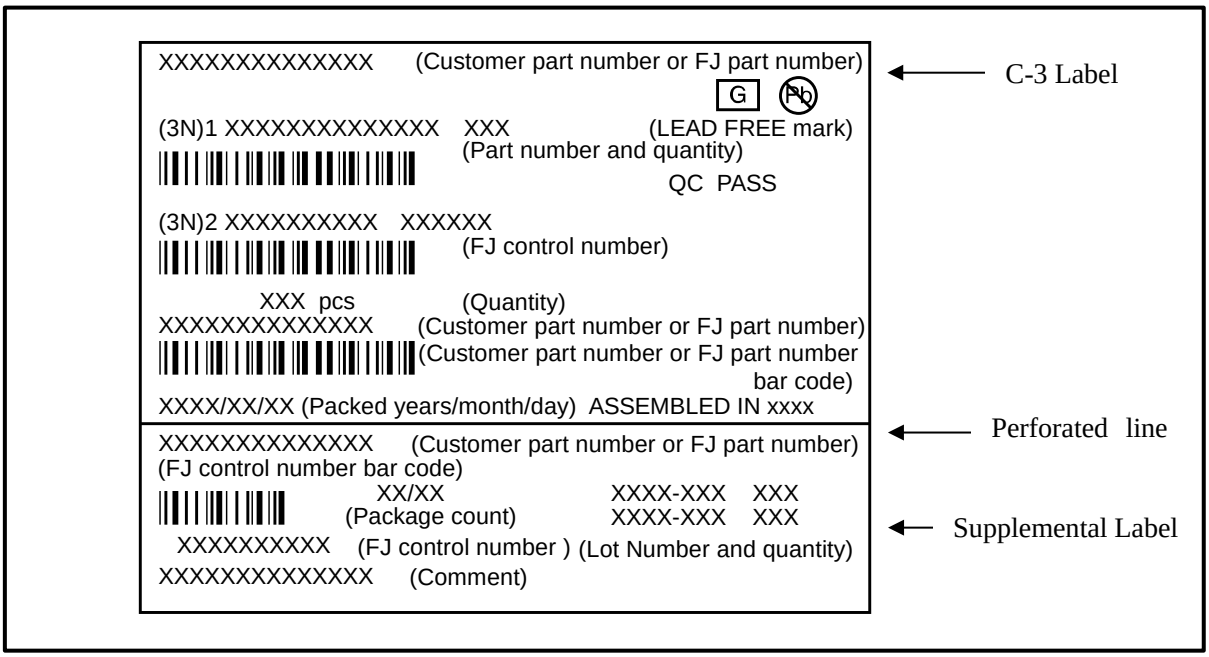
	Dimension:mm
A	330
B	100
C	13
W1	16.4
W2	21.2

No heat resistance. Package should not be baked by using tape and/or reel.

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5 Product label indicators

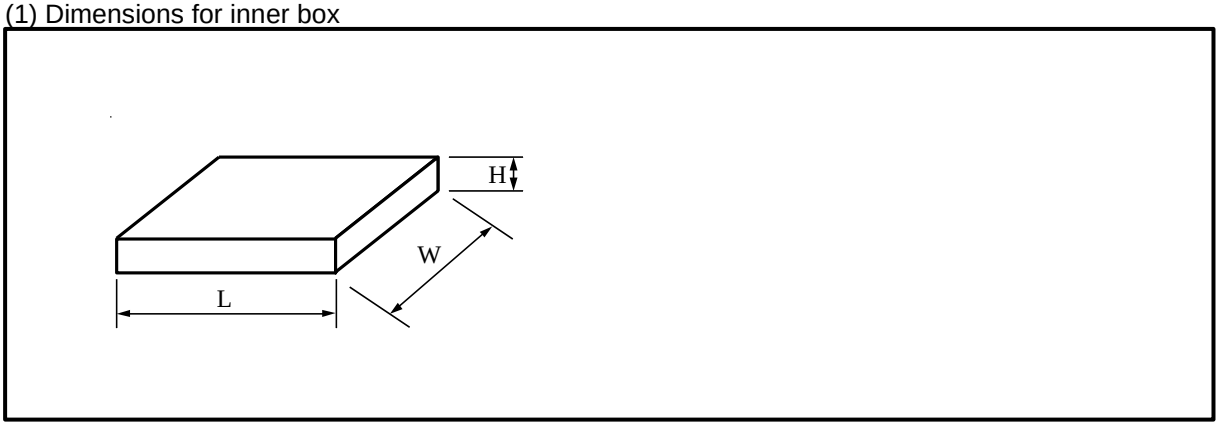
Label I: Label on Inner box/Moisture Barrier Bag
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



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6 Dimensions for containers

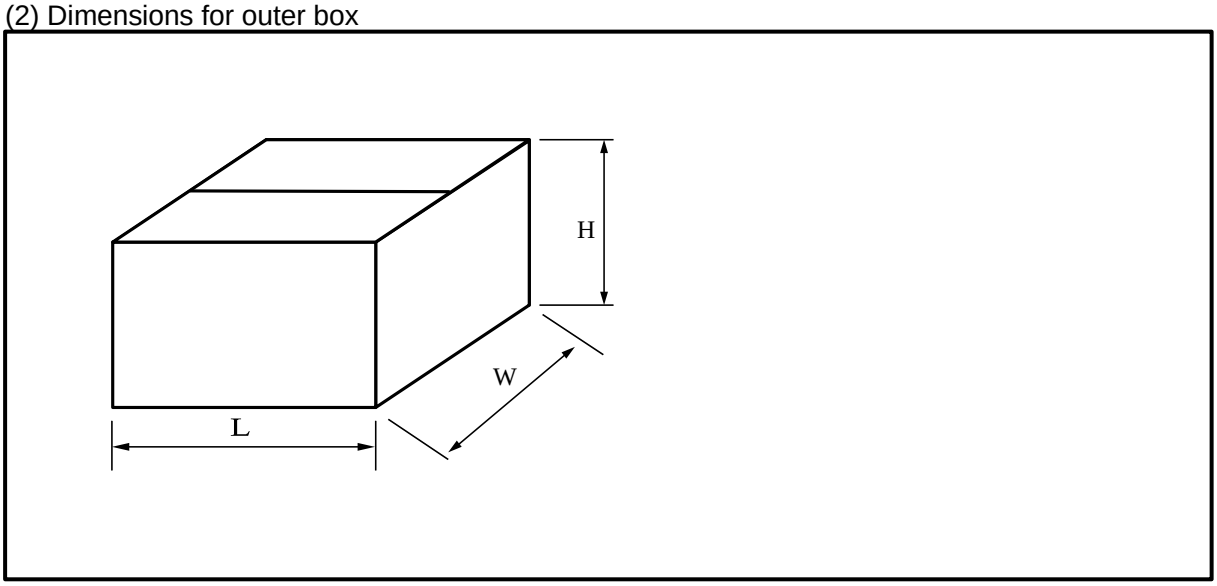
(1) Dimensions for inner box



L	W	H
365	345	40

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
415	400	315

(Dimensions in mm)

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■ 13 OTHERS

■ 13.1 Note items

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■ 14 MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
6	■ 3.3.1 Connection to SPI Interface	Figure 3.3.1 SPI Slave Interface Connection is revised.

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