STEREO DIGITAL AUDIO LIP-SYNC DELAY

FEATURES

- Digital Audio Format: 16-24-bit I^2S
- Single Serial Input Port
- Delay Time: 170 ms/ch at fs = 48 kHz
- Delay Resolution: 256 samples
- Delay Memory Cleared on Power-Up or After Delay Changes
  - Eliminates Erroneous Data From Being Output
- 3.3 V Operation With 5 V Tolerant I/O
- Supports Audio Bit Clock Rates of 32 to 64 fs with fs = 32 kHz–192 kHz
- No External Crystal or Oscillator Required
  - All Internal Clocks Generated From the Audio Clock
- Surface Mount 4mm × 4mm, 16-pin QFN Package

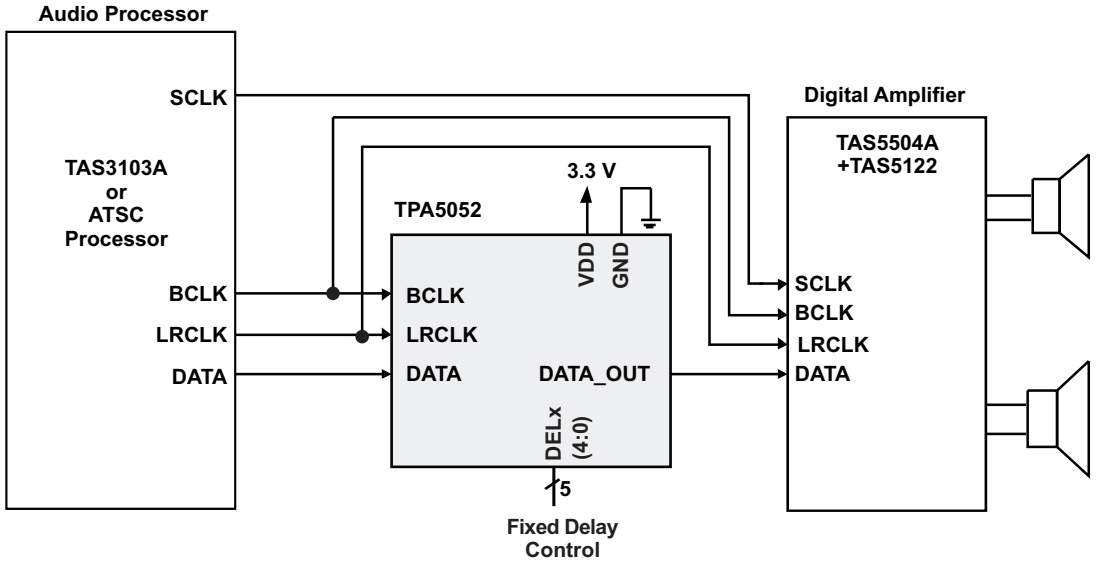
APPLICATIONS

- High Definition TV Lip-Sync Delay
- Flat Panel TV Lip-Sync Delay
- Home Theater Rear-Channel Effects
- Wireless Speaker Front-Channel Synchronization
- Camcorders

DESCRIPTION

The TPA5052 accepts a single serial audio input, buffers the data for a selectable period of time, and outputs the delayed audio data on a single serial output. In systems with complex video processing algorithms, one device allows delay of up to 170 ms/ch (fs = 48 kHz) to synchronize the audio stream to the video stream. If more delay is needed, the devices can be connected in series.

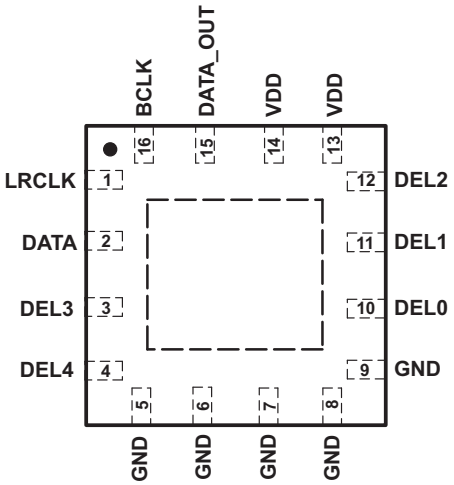
SIMPLIFIED APPLICATION DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTIONS

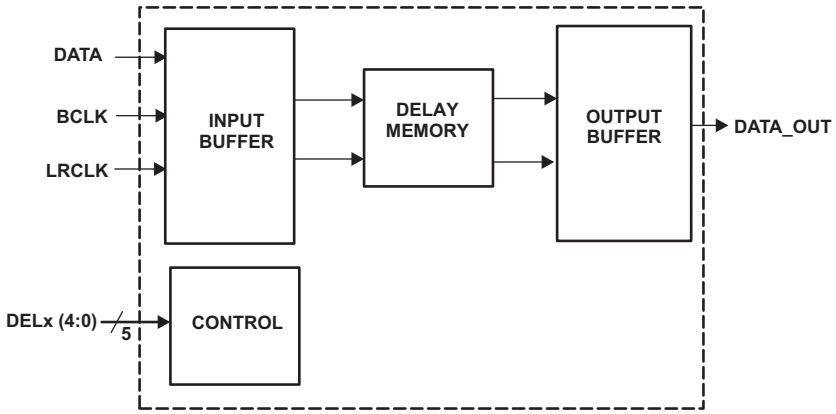
RSA (QFN) PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DEL0	10	I	Delay select pin – LSB. 5V tolerant input.
DEL1	11	I	Delay select pin. 5V tolerant input.
DEL2	12	I	Delay select pin. 5V tolerant input.
DEL3	3	I	Delay select pin. 5V tolerant input.
DEL4	4	I	Delay select pin - MSB. 5V tolerant input.
BCLK	16	I	Audio data bit clock input for serial input. 5V tolerant input.
DATA	2	I	Audio serial data input for serial input. 5V tolerant input.
DATA_OUT	15	O	Delayed audio serial data output.
GND	5–9	P	Ground – All ground terminals must be tied to GND for proper operation
LRCLK	1	I	Left and Right serial audio sampling rate clock (fs). 5V tolerant input.
VDD	13, 14	P	Power supply interface. Both pins must be tied to power supply.
Thermal Pad		-	Connect to ground. Must be soldered down in all applications to properly secure device on the PCB.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) (1)

			VALUE	UNIT
V_{DD}	Supply voltage		–0.3 to 3.6	V
V_I	Input voltage	DATA, LRCLK, BCLK, DEL[4:0]	–0.3 to 5.5	V
	Continuous total power dissipation		See Dissipation Rating Table	
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 125	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS(1)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RSA	2.5 W	25 mW/°C	1.375 W	1 W

(1) This data was taken using 1 oz trace and copper pad that is soldered directly to a JEDEC standard high-k PCB. The thermal pad must be soldered to a thermal land on the printed-circuit board. See TI Technical Briefs SCBA017D and SLUA271 for more information about using the QFN thermal pad.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage	VDD	3	3.6	V
V_{IH}	High-level input voltage	DATA, LRCLK, BCLK, DEL[4:0]	2		V
V_{IL}	Low-level input voltage	DATA, LRCLK, BCLK, DEL[4:0]		0.8	V
T_A	Operating free-air temperature		–40	85	°C

DC CHARACTERISTICS

T_A = 25°C, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 3.3 V, fs = 48 kHz, BCLK = 32 × fs		1.8	3	mA
I_{OH}	High-level output current	DATA_OUT = 2.6 V	5		13	mA
I_{OL}	Low-level output current	DATA_OUT = 0.4 V	5		13	mA
I_{IH}	High-level input current	DATA, LRCLK, BCLK, V_I = 5.5V, VDD = 3V			20	µA
		DEL[4:0], V_I = 3.6V, VDD = 3.6V			5	
I_{IL}	Low-level input current	DATA, LRCLK, BCLK, DEL[4:0], V_I = 0V, VDD = 3.6V			1	µA

Serial Audio Input Ports

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	Frequency, BCLK 32 × fs, 48 × fs, 64 × fs		1.024		12.288	MHz
t_{su1}	Setup time, LRCLK to BCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from BCLK rising edge		10			ns
t_{su2}	Setup time, DATA to BCLK rising edge		10			ns
t_{h2}	Hold time, DATA from BCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	BCLK duty cycle			50%		
	LRCLK duty cycle			50%		
	BCLK rising edges between LRCLK rising edges	LRCLK duty cycle = 50%	32		64	BCLK edges

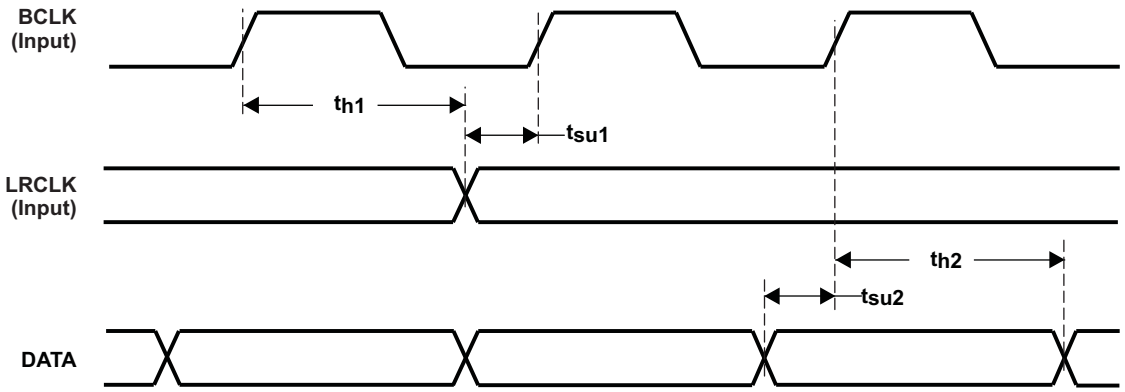


Figure 1. Serial Data Interface Timing

APPLICATION INFORMATION

AUDIO SERIAL INTERFACE

The audio serial interface for the TPA5052 consists of a 3-wire synchronous serial port. It includes LRCLK, BCLK, and DATA. BCLK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the TPA5052 on the rising edge of BCLK. LRCLK is the serial audio left/right word clock. It is used to latch serial data into the internal registers of the serial audio interface. LRCLK is operated at the sampling frequency, fs. BCLK can be operated at 32 to 64 times the sampling frequency for I^{2}S formats. A system clock is not necessary for the operation of the TPA5052.

I^{2}S TIMING

The I^{2}S data format diagram is shown in Figure 2.

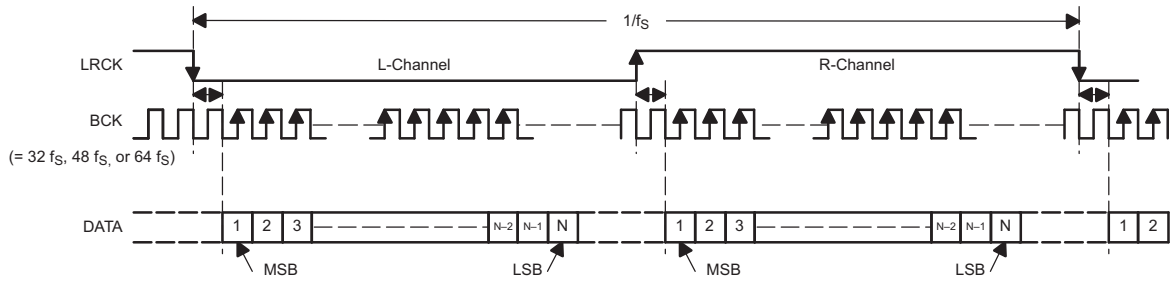


Figure 2. I^{2}S Data Format; L-Channel = LOW, R-Channel = HIGH

GENERAL DELAY OPERATION

The delay of the TPA5052 is set using the 5 delay pins (DEL4, DEL3, DEL2, DEL1, DEL0). The minimum delay is 255 samples, and occurs when all five pins are at logic 0. The maximum delay is 8191 samples, and occurs when all five pins are at logic 1. The delay can be increased by changing the values on each pin from a 0 to a 1. See Table 1. Delay pin DEL4 is the MSB, and DEL0 is the LSB.

The delay is calculated with the following forumula:

Audio Delay (in samples) = 4096 x (DEL4) + 2048 x (DEL3) + 1024 x (DEL2) + 512 x (DEL1) + 256 x (DEL0) + 255

Audio Delay (ms) = Audio Delay (in samples) x (1/fs)

Both channels have the same amount of delay. They cannot be controlled individually.

Table 1. Delay Settings

DEL4	DEL3	DEL2	DEL1	DEL0	Delay in Samples
0	0	0	0	0	255
0	0	0	0	1	511
0	0	0	1	0	767
0	0	0	1	1	1023
↓	↓	↓	↓	↓	↓
1	1	1	1	1	8191

TPA5052 Operation

Only a single decoupling capacitor (0.1 µF–1 µF) is required across VDD and GND. The DELx terminals can be directly connected to VDD or GND. Table 1 describes the delay settings selectable via the DELx terminals. A schematic implementation of the TPA5052 is shown in Figure 3.

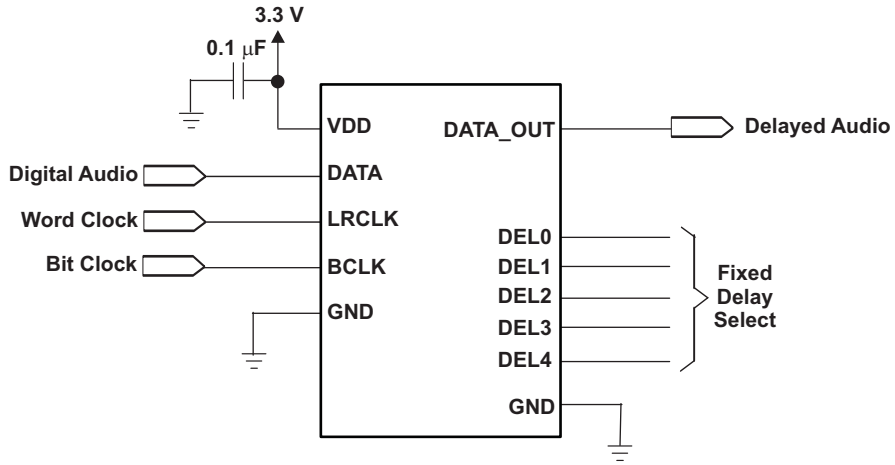


Figure 3. TPA5052 Schematic

COMPLETE UPDATE

To avoid pops and clicks in the audio stream when the delay is changed, the TPA5052 holds each channel in an internal mute mode until all the set number of samples have passed. For example, if the delay is set to 511 samples, the TPA5052 holds each channel in mute until all 511 samples of audio data have passed.

APPLICATION EXAMPLES

Connecting Two Devices in Series to Increase the Delay

It is sometimes desirable to increase the delay time beyond the limit which one device provides. In such cases, the TPA5052 device can be placed in a series to increase the delay. See Figure 4 for an example.

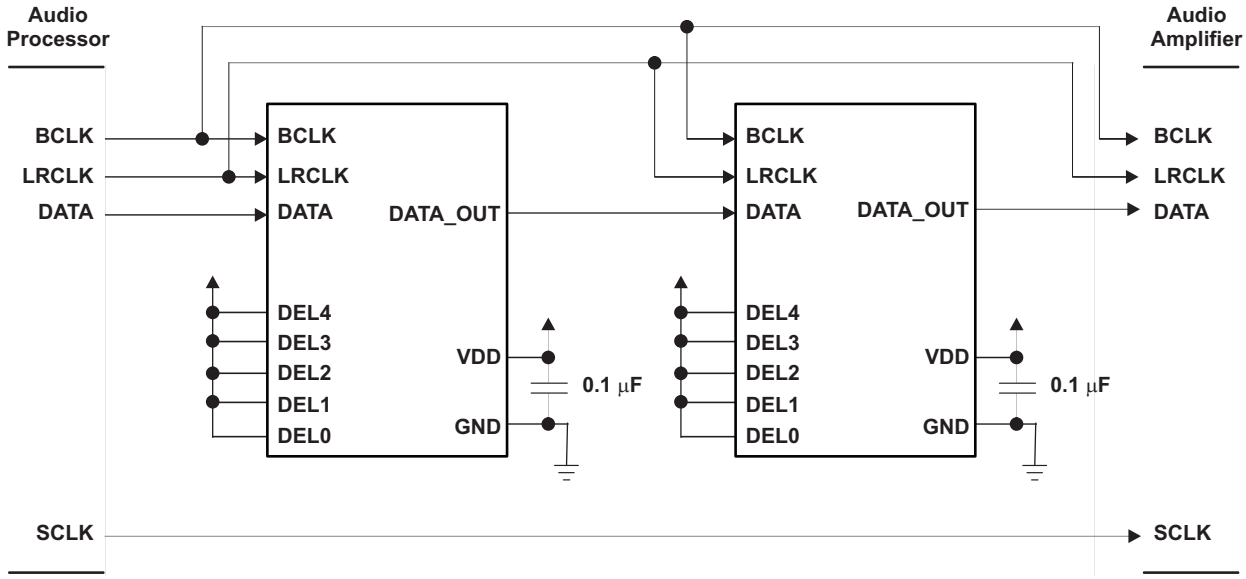


Figure 4. Two Devices in Series

DEVICE CURRENT CONSUMPTION

The TPA5052 draws different amounts of supply current depending upon the conditions under which it is operated. As V_{DD} increases, so too does I_{DD}. Likewise, as V_{DD} decreases, I_{DD} decreases. The same is true of the sampling frequency, fs. An increase in fs causes an increase in I_{DD}. Figure 5 illustrates the relationship between operating condition and typical supply current.

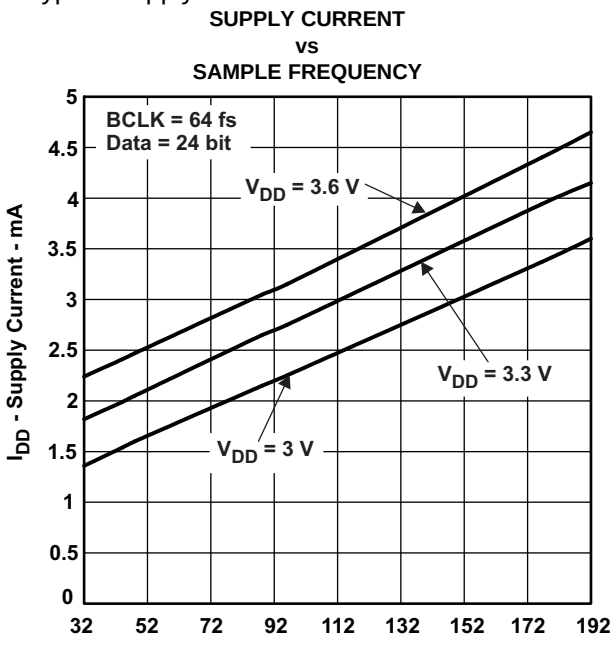


Figure 5. Typical Supply Current

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA5052RSAR	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 5052
TPA5052RSAR.A	Active	Production	QFN (RSA) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 5052
TPA5052RSAT	Active	Production	QFN (RSA) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 5052
TPA5052RSAT.A	Active	Production	QFN (RSA) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 5052

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

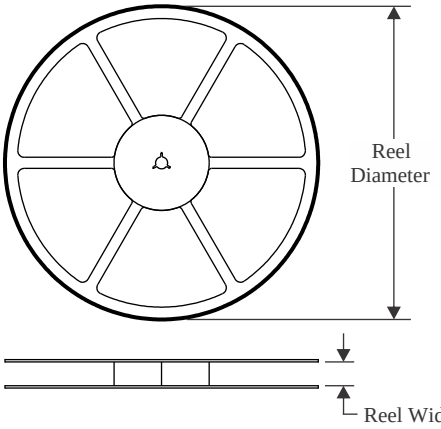
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

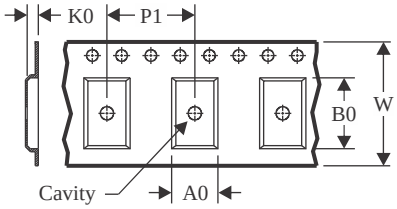
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

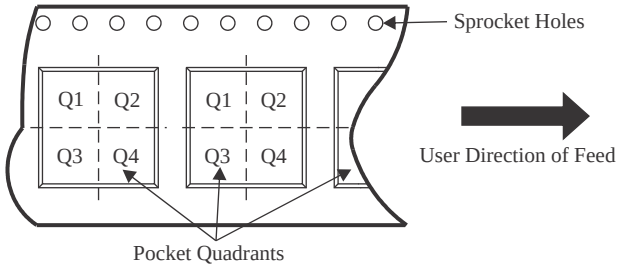


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

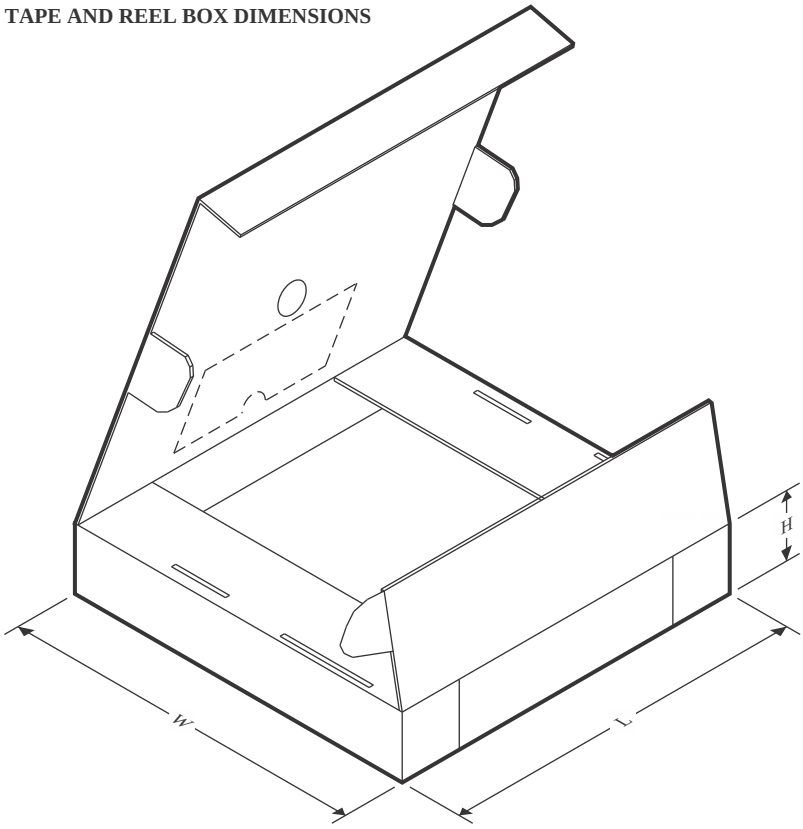
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA5052RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA5052RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA5052RSAR	QFN	RSA	16	3000	356.0	356.0	35.0
TPA5052RSAT	QFN	RSA	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

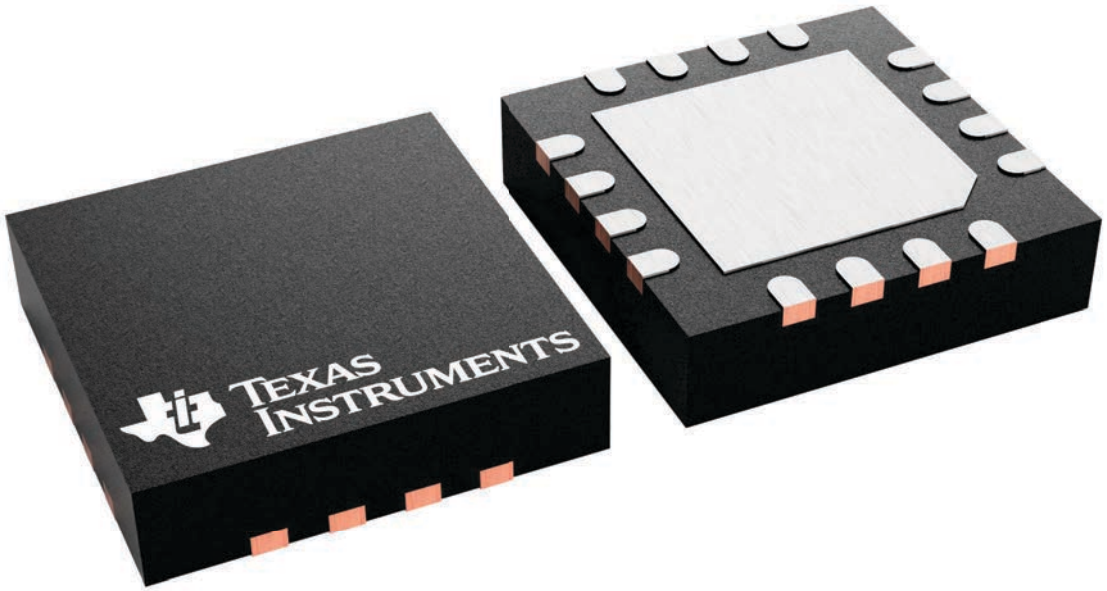
RSA 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

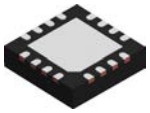
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230969/A

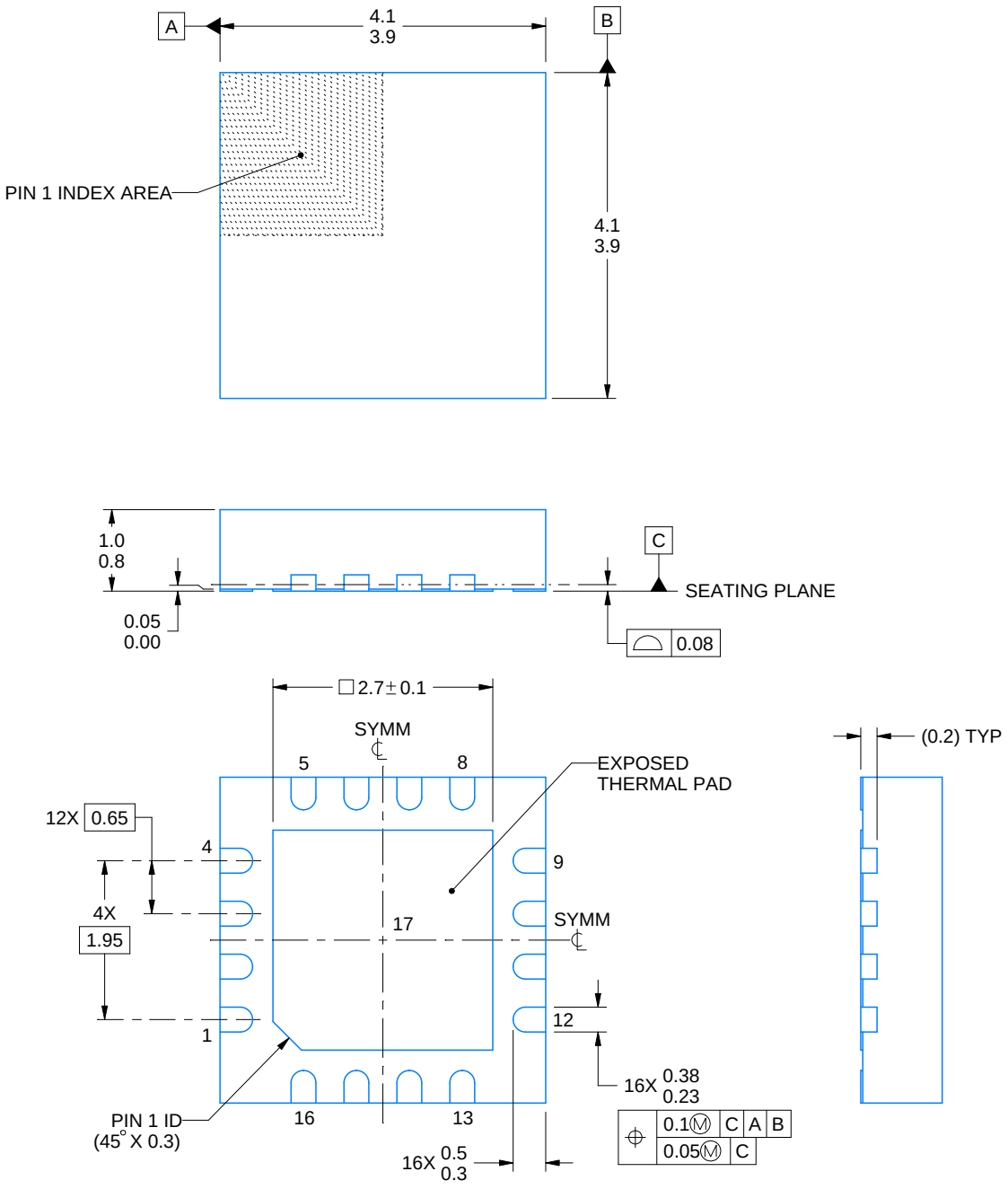
RSA0016B



PACKAGE OUTLINE

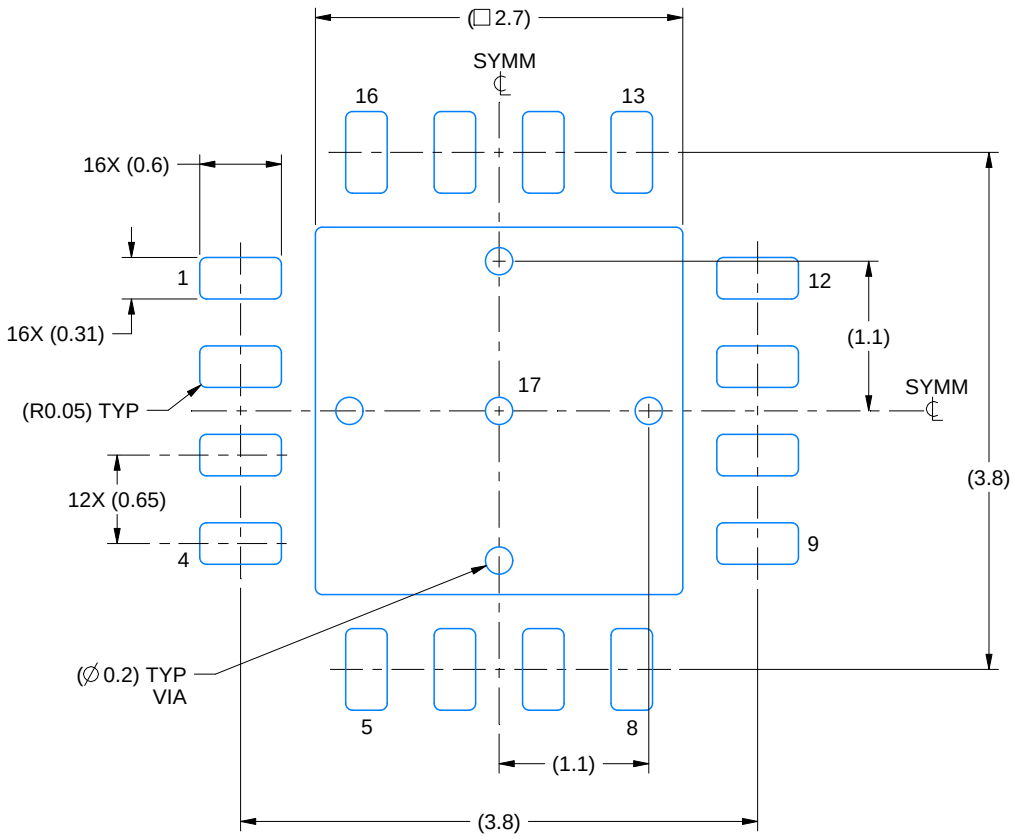
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

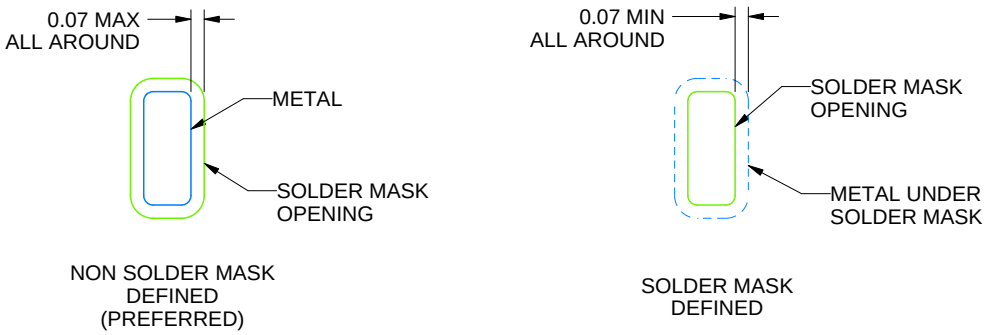


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

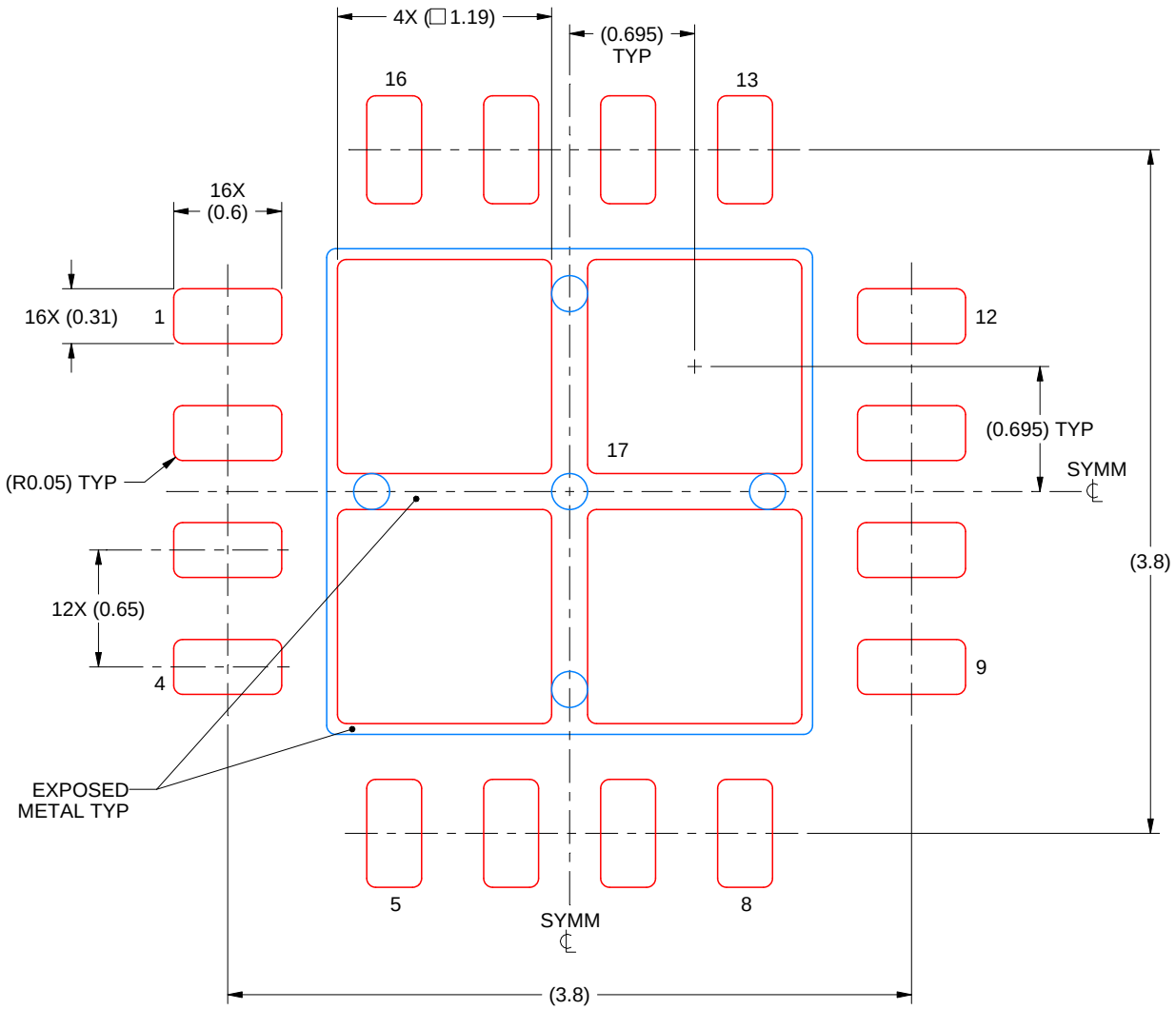
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSA0016B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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