Input Rail-to-Rail Open Drain Output Low Supply Current CMOS Comparators for Automotive

BU7233YF-C

General Description

BU7233YF-C is an input Rail-to-Rail, open drain, dual comparators. It has a wide operating temperature range. It features low operating supply voltage from 1.8 V to 5.5 V, low supply current and extremely low input bias current.

Features

- AEC-Q100 Qualified(Note 1)
- Low Operating Supply Voltage
- Low Supply Current
- Input Rail-to-Rail
- Open Drain Output Type
- Wide Operating Temperature Range
- Low Input Bias Current

(Note 1) Grade 1

Applications

- Voltage Detection Equipment
- Limit Comparator
- Automotive Electronics Equipment

Key Specifications

- Operating Supply Voltage:
  - Single Supply: 1.8 V to 5.5 V
  - Dual Supply: ±0.9 V to ±2.75 V
- Supply Current: 10 uA (Typ)
- Temperature Range: -40 °C to +125 °C
- Input Offset Current: 1 pA (Typ)
- Input Bias Current: 1 pA (Typ)

Special Characteristics

- Input Offset Voltage
  - -40 °C to +125 °C: 15 mV(Max)

Package

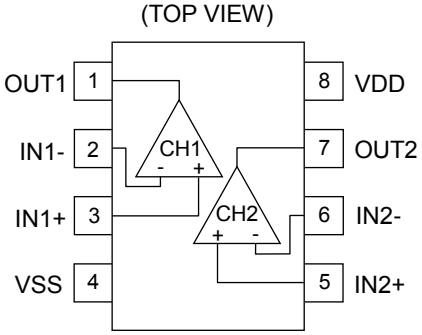
	W(Typ) x D(Typ) x H(Max)
SOP8	5.00mm x 6.20mm x 1.71mm



SOP8

Pin Configuration

(TOP VIEW)



○Product structure：Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

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Pin Description

Pin No.	Pin Name	Function
1	OUT1	Output
2	IN1-	Inverting input
3	IN1+	Non-inverting input
4	VSS	Ground/Negative power supply
5	IN2+	Non-inverting input
6	IN2-	Inverting input
7	OUT2	Output
8	VDD	Positive power supply

Block Diagram

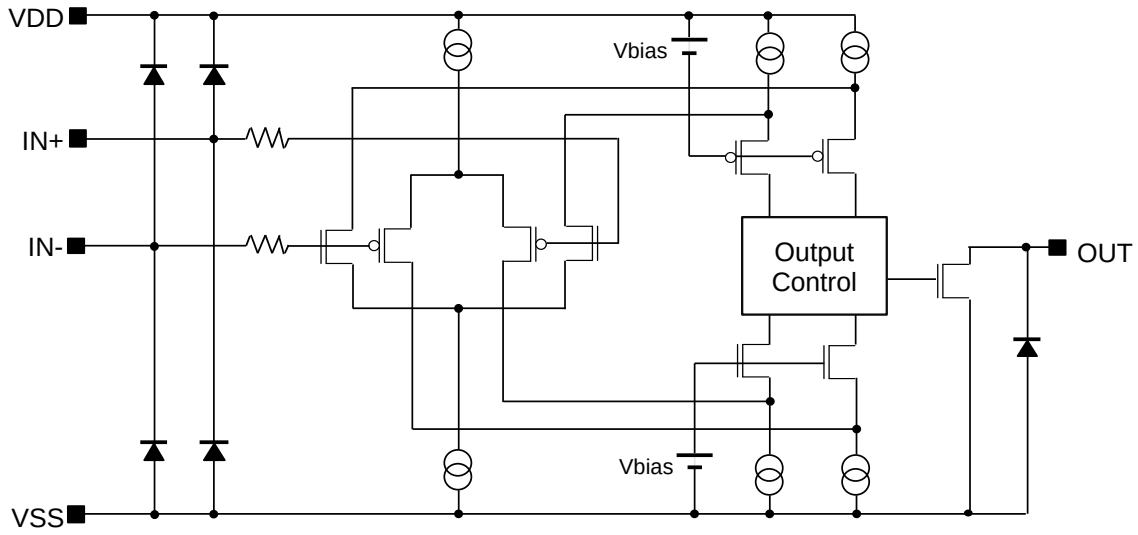


Figure 1.Block Diagram (One channel only)

Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}-V_{SS}	7	V
Power Dissipation	Pd	0.68*(Note 2,3)*	W
Differential Input Voltage*(Note 4)*	V_{ID}	V_{DD} - V_{SS}	V
Input Common-mode Voltage Range	V_{ICM}	(V_{SS}-0.3) to (V_{DD}+0.3)	V
Input Current	I_I	±10	mA
Operating Supply Voltage	V_{opr}	1.8 to 5.5 ±0.9 to ±2.75	V
Operating Temperature	T_{opr}	-40 to +125	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_{jmax}	150	°C

(Note 2) To use at temperature above Ta=25 °C reduce 5.5 mW/°C.
(Note 3) Mounted on an FR4 glass epoxy PCB 70 mm×70 mm×1.6 mm (Copper foil area less than 3 %).
(Note 4) The differential input voltage is the voltage difference between inverting input and non-inverting input. The input pin voltage is set to more than VSS.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

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Electrical Characteristics (Unless otherwise specified V_{DD}=3 V, V_{SS}=0 V, Ta=25 °C)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage *(Note 5,6)*	V_{IO}	25 °C	-	1	14	mV	-
		Full Range	-	-	15		
Input Offset Current *(Note 5)*	I_{IO}	25 °C	-	1	-	pA	-
Input Bias Current *(Note 5,6)*	I_B	25 °C	-	1	300	pA	-
		Full Range	-	-	6000		
Supply Current *(Note 6)*	I_{DD}	25 °C	-	10	25	µA	R_L=∞ All Comparators
		Full Range	-	-	50		
Maximum Output Voltage(High) *(Note 6)*	V_{OH}	25 °C	V_{DD}-0.05	-	-	V	R_L=10 kΩ, V_{RL}=3 V
		Full Range	V_{DD}-0.1	-	-		
Maximum Output Voltage(Low) *(Note 6)*	V_{OL}	25 °C	-	-	V_{SS}+0.05	V	R_L=10 kΩ
		Full Range	-	-	V_{SS}+0.1		
Large Signal Voltage Gain *(Note 8)*	A_V	25 °C	-	100	-	dB	R_L=10 kΩ
Input Common-mode Voltage Range	V_{ICM}	25 °C	0	-	3	V	-
Common-mode Rejection Ratio	CMRR	25 °C	-	80	-	dB	-
Power Supply Rejection Ratio	PSRR	25 °C	-	80	-	dB	-
Output Sink Current *(Note 6,7)*	I_{SINK}	25 °C	3	7	-	mA	V_{OUT}=V_{SS}+0.4 V
		Full Range	1	-	-		
Output Fall Time	t_F	25 °C	-	20	-	ns	R_L=10 kΩ V_{RL}=3 V C_L=15 pF V_{IN-}=1.5 V 100 mV Overdrive
Propagation Delay Time L to H *(Note 6,8)*	t_{PLH}	25 °C	-	1.8	-	µs	
		Full Range	-	-	5		
Propagation Delay Time H to L *(Note 6)*	t_{PHL}	25 °C	-	0.6	-	µs	
		Full Range	-	-	3		

(Note 5) Absolute value
(Note 6) Full Range: Ta=-40 °C to +125 °C
(Note 7) Consider the power dissipation of the IC under high temperature environment when selecting the output current value.
There may be a case where the output current value is reduced due to the rise in IC temperature caused by the heat generated inside the IC.
(Note 8) Propagation Delay Time L to H and Large Signal Voltage Gain is affected by the pull-up resistance value.

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Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute Maximum Ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Supply Voltage (V_{DD}/V_{SS})
Indicates the maximum voltage that can be applied between the VDD pin and VSS pin without deterioration or destruction of characteristics of internal circuit.

1.2 Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting pins without damaging the IC.

1.3 Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting pins without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.

1.4 Power Dissipation (Pd)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25 °C (normal temperature). As for package product, Pd is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical Characteristics

2.1 Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting pin and inverting pins. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

2.2 Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting pins.

2.3 Input Bias Current (I_B)
Indicates the current that flows into or out of the input pin. It is defined by the average of input bias currents at the non-inverting and inverting pins.

2.4 Supply Current (I_{DD})
Indicates the current that flows within the IC under specified no-load conditions.

2.5 Maximum Output Voltage(High) / Maximum Output Voltage(Low) (V_{OH}/V_{OL})
Indicates the voltage range of the output under specified load condition. It is typically divided into maximum output voltage High and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

2.6 Large Signal Voltage Gain (A_V)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting pin and inverting pin. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage) / (Differential input voltage)

2.7 Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.

2.8 Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of input common-mode voltage)/(Input offset fluctuation)

2.9 Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
PSRR= (Change of power supply voltage)/(Input offset fluctuation)

2.10 Output Sink Current (I_{SINK})
The maximum current that can be output from the IC under specific output conditions. The output sink current indicates the current flowing into the IC.

2.11 Output Fall Time (t_F)
Indicates the time required for an output voltage step to change from 90 % to 10 % of its final value.

2.12 Propagation Delay Time L to H /Propagation Delay Time H to L (t_{PLH} / t_{PHL})
Indicates the time to reach 50 % of the output voltage after the step voltage is applied at the input pin.

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Typical Performance Curves

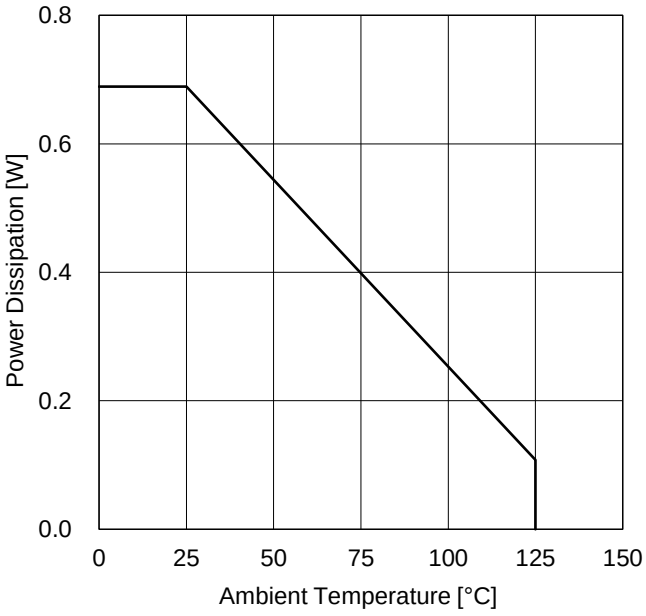


Figure 2. Power Dissipation vs Ambient Temperature (Derating Curve)

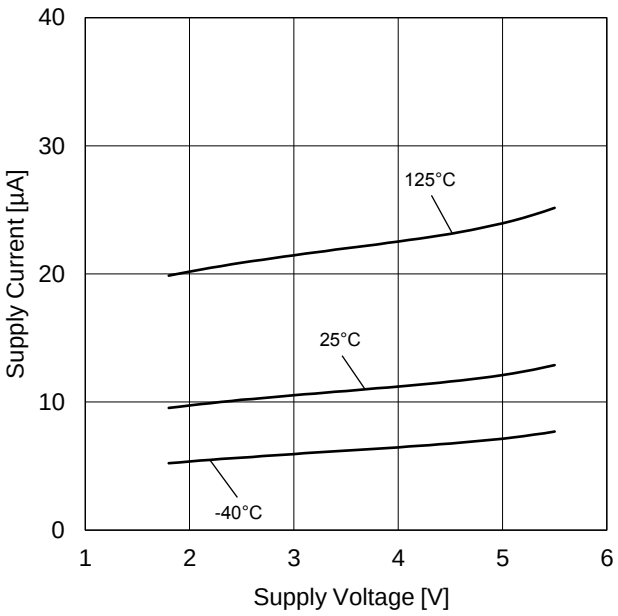


Figure 3. Supply Current vs Supply Voltage

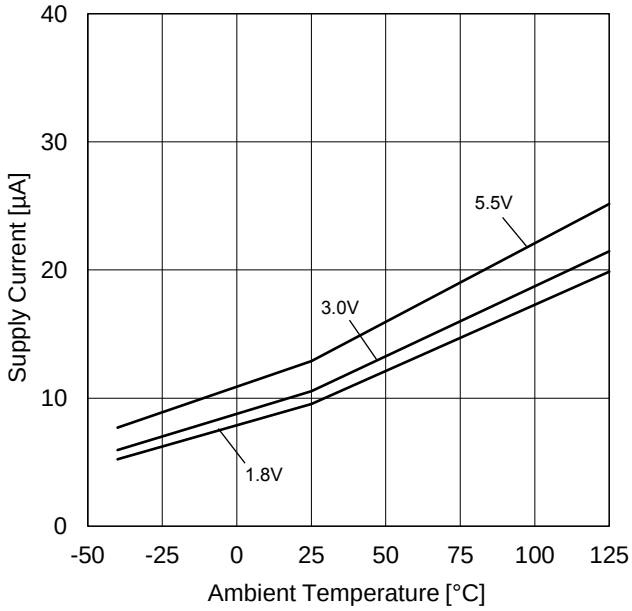


Figure 4. Supply Current vs Ambient Temperature

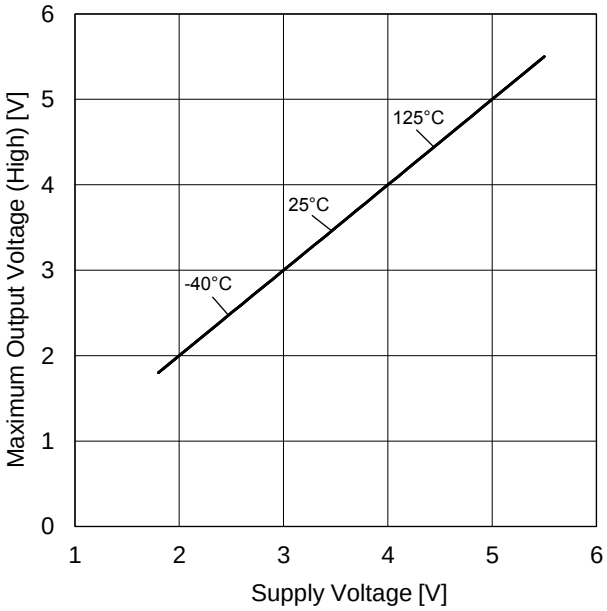


Figure 5. Maximum Output Voltage (High) vs Supply Voltage
(R_L=10 kΩ, V_{RL}=V_{DD})

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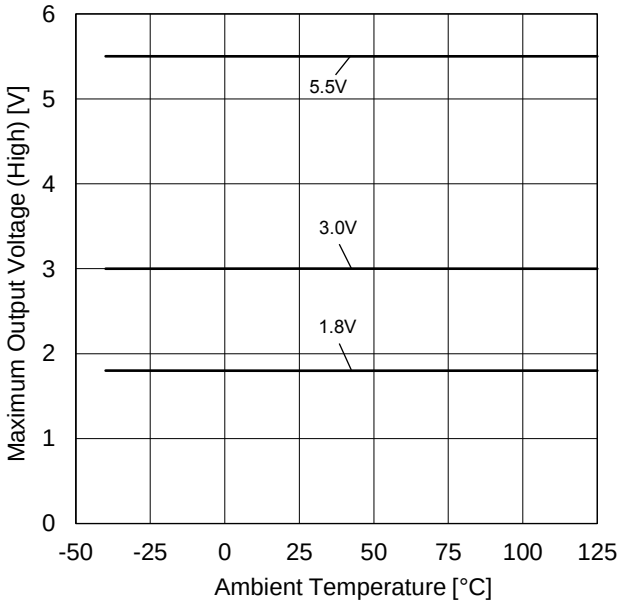


Figure 6. Maximum Output Voltage (High) vs Ambient Temperature
(R_L=10 kΩ, V_{RL}=V_{DD})

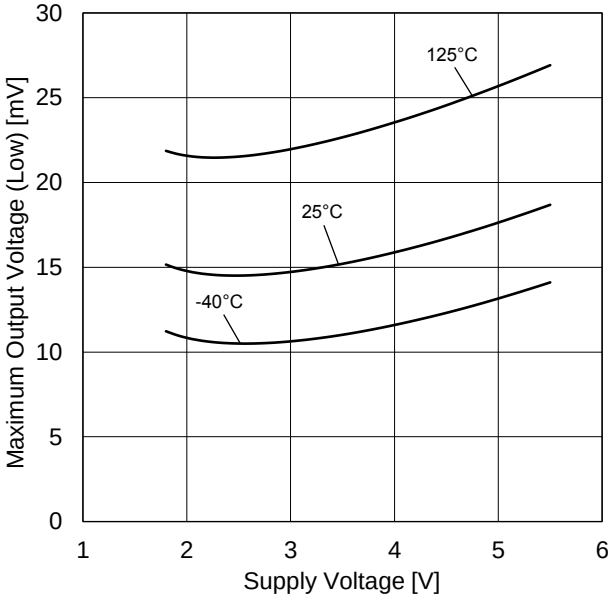


Figure 7. Maximum Output Voltage (Low) vs Supply Voltage
(R_L=10 kΩ, V_{RL}=V_{DD})

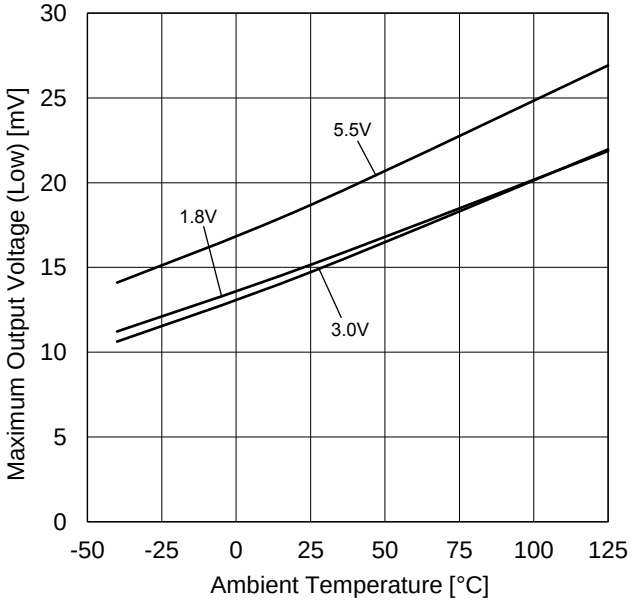


Figure 8. Maximum Output Voltage (Low) vs Ambient Temperature
(R_L=10 kΩ, V_{RL}=V_{DD})

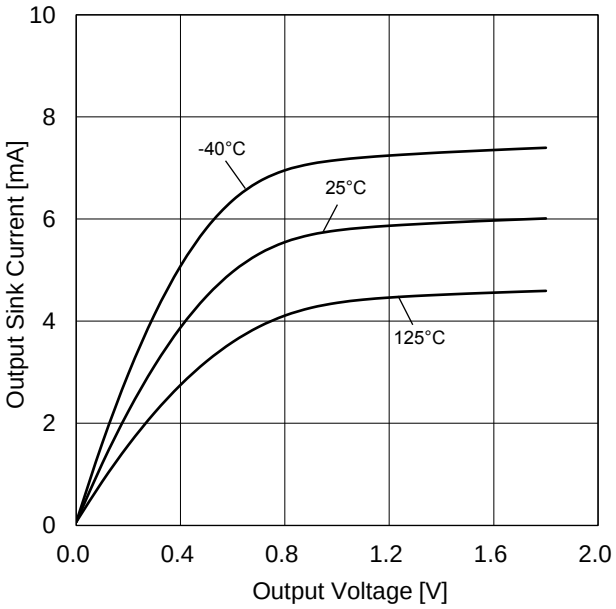


Figure 9. Output Sink Current vs Output Voltage
(V_{DD}=1.8 V)

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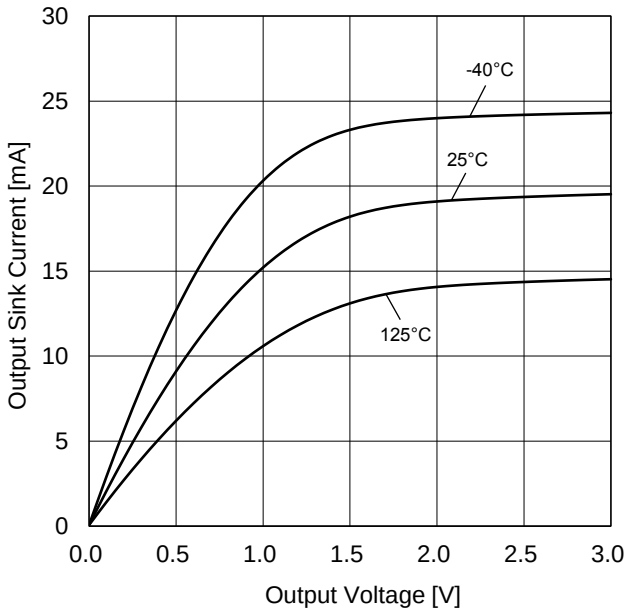


Figure 10. Output Sink Current vs Output Voltage
(V_{DD}=3 V)

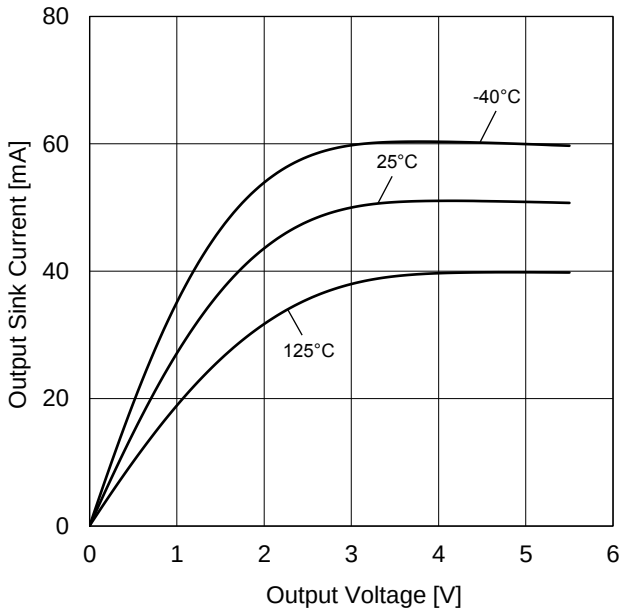


Figure 11. Output Sink Current vs Output Voltage
(V_{DD}=5.5 V)

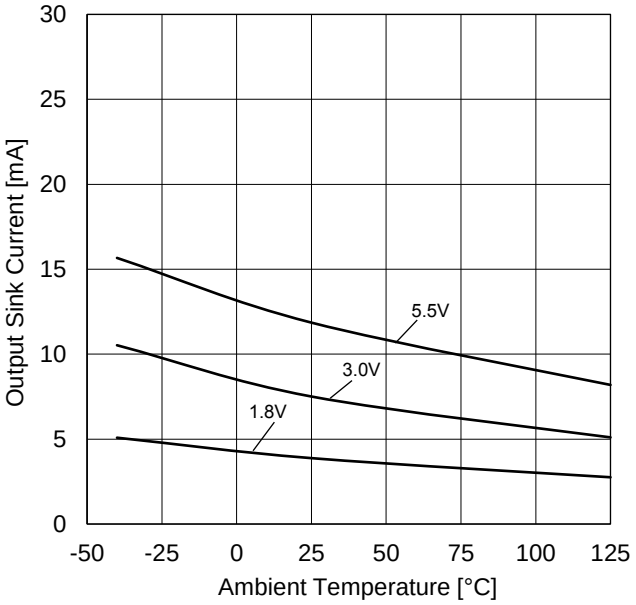


Figure 12. Output Sink Current vs Ambient Temperature
(V_{OUT}=V_{SS}+0.4 V)

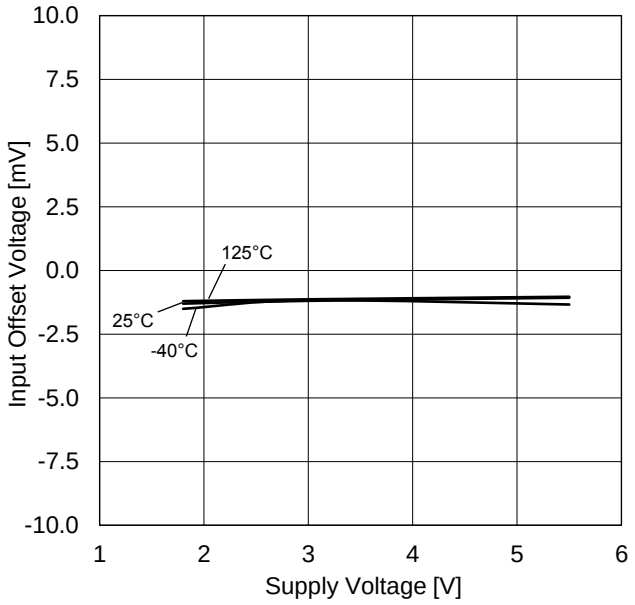


Figure 13. Input Offset Voltage vs Supply Voltage
(V_{ICM}=V_{DD}, E_K=-V_{DD}/2)

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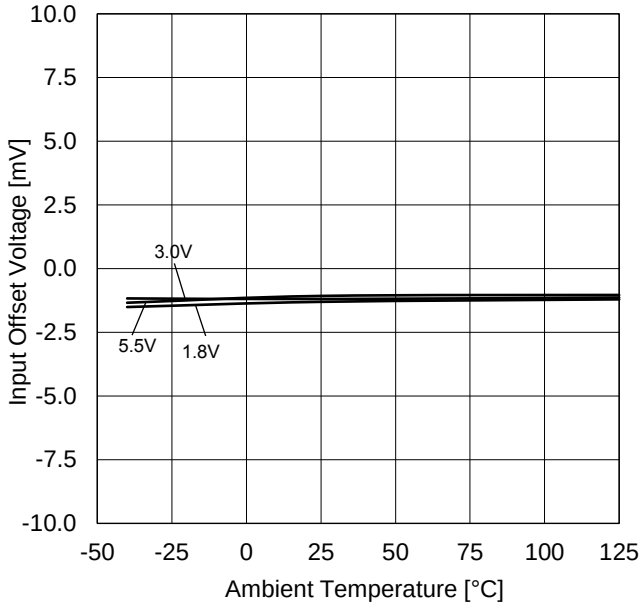


Figure 14.Input Offset Voltage vs Ambient Temperature
(V_{ICM}=V_{DD}, E_K=-V_{DD}/2)

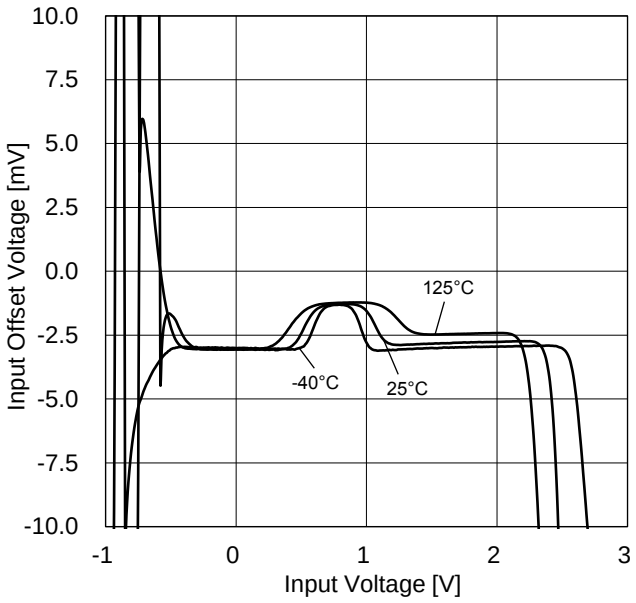


Figure 15. Input Offset Voltage vs Input Voltage
(V_{DD}=1.8 V)

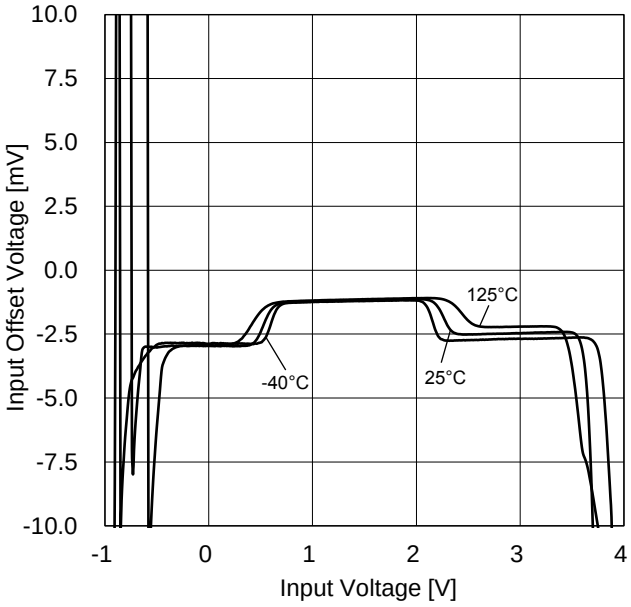


Figure 16. Input Offset Voltage vs Input Voltage
(V_{DD}=3 V)

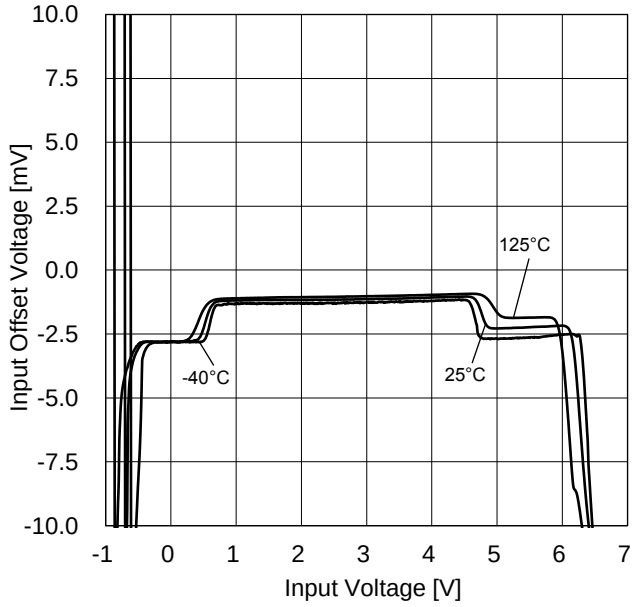


Figure 17. Input Offset Voltage vs Input Voltage
(V_{DD}=5.5 V)

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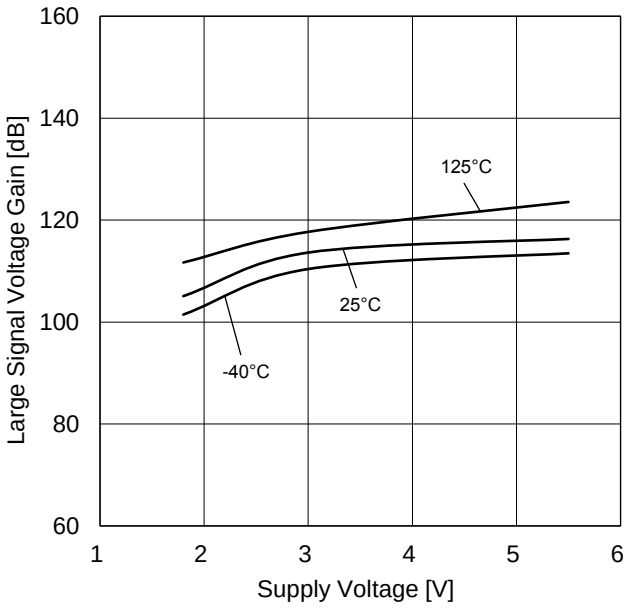


Figure 18. Large Signal Voltage Gain vs Supply Voltage

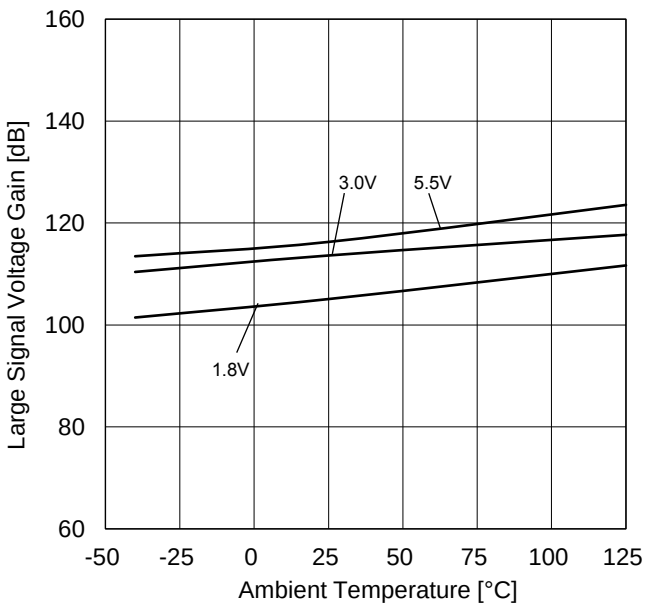


Figure 19. Large Signal Voltage Gain vs Ambient Temperature

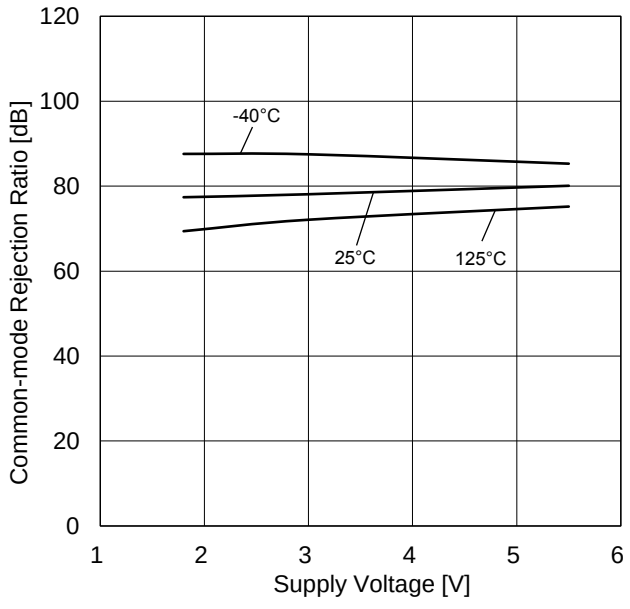


Figure 20. Common-mode Rejection Ratio vs Supply Voltage

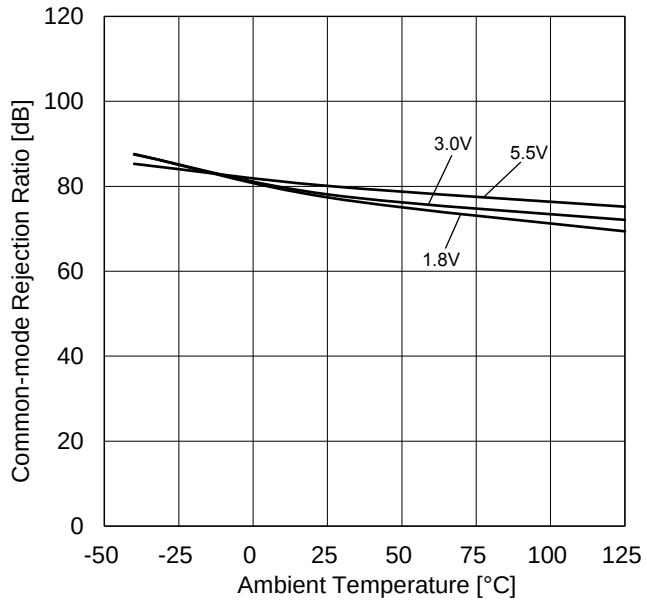


Figure 21. Common-mode Rejection Ratio vs Ambient Temperature

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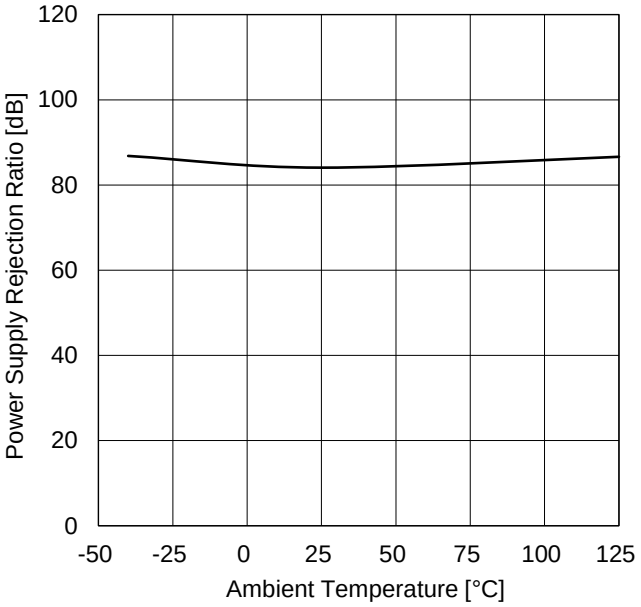


Figure 22. Power Supply Rejection Ratio vs Ambient Temperature

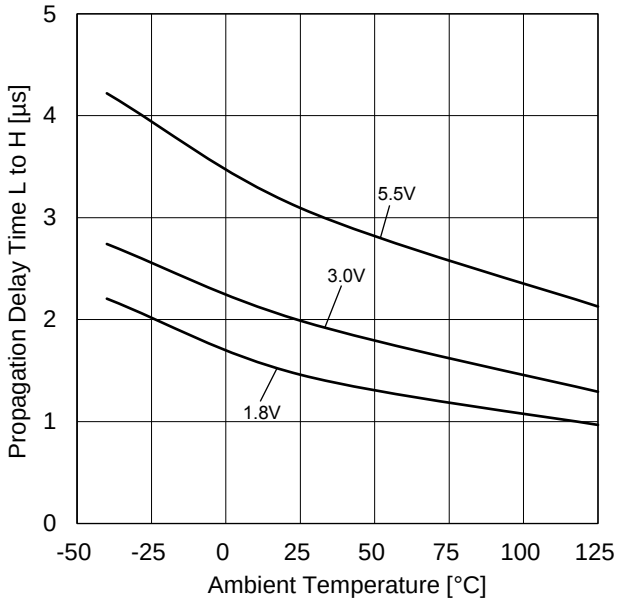


Figure 23. Propagation Delay Time L to H vs Ambient Temperature
(R_L=10 kΩ, V_{RL}=3 V, C_L=15 pF,
V_{IN-}=1.5 V, 100 mV Overdrive)

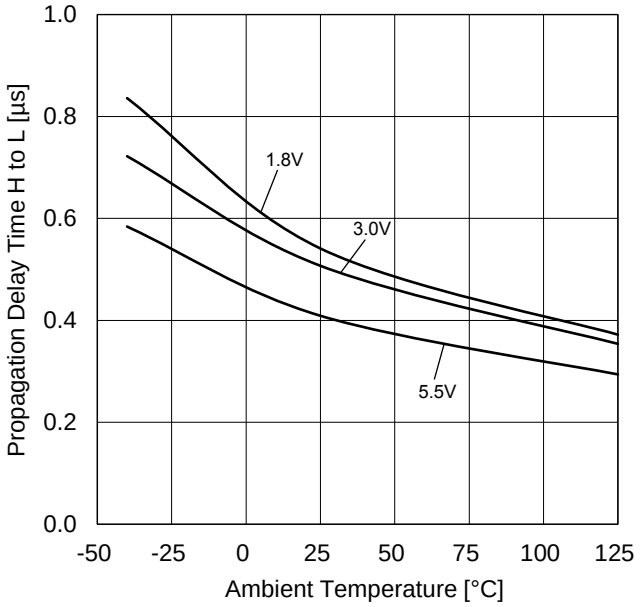


Figure 24.Propagation Delay Time H to L vs Ambient Temperature
(R_L=10 kΩ, V_{RL}=3 V, C_L=15 pF,
V_{IN-}=1.5 V, 100 mV Overdrive)

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Application Information

NULL Method Conditions for Test Circuit 1

V_{DD}, V_{SS}, E_K, V_{ICM}, V_{RL} Unit:V

Parameter	V_F	SW1	SW2	SW3	V_{DD}	V_{SS}	E_K	V_{ICM}	V_{RL}	Calculation
Input Offset Voltage	V_{F1}	ON	ON	ON	3	0	-0.1	0.25	3	1
Large Signal Voltage Gain	V_{F2}	ON	ON	ON	3	0	-0.3	0.25	3	2
	V_{F3}						-2.7			
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	V_{F4}	ON	ON	ON	3	0	-0.1	0.25	3	3
	V_{F5}							3		
Power Supply Rejection Ratio	V_{F6}	ON	ON	ON	1.8	0	-0.1	0	1.8	4
	V_{F7}				5.5				5.5	

- Calculation -

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1 + R_F/R_S} \text{ [V]}$$

2. Large Signal Voltage Gain (A_V)

$$Av = 20\text{Log}\frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F3} - V_{F2}|} \text{ [dB]}$$

3. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20\text{Log}\frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F5} - V_{F4}|} \text{ [dB]}$$

4. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20\text{Log}\frac{\Delta V_{DD} \times (1+ R_F/R_S)}{|V_{F7} - V_{F6}|} \text{ [dB]}$$

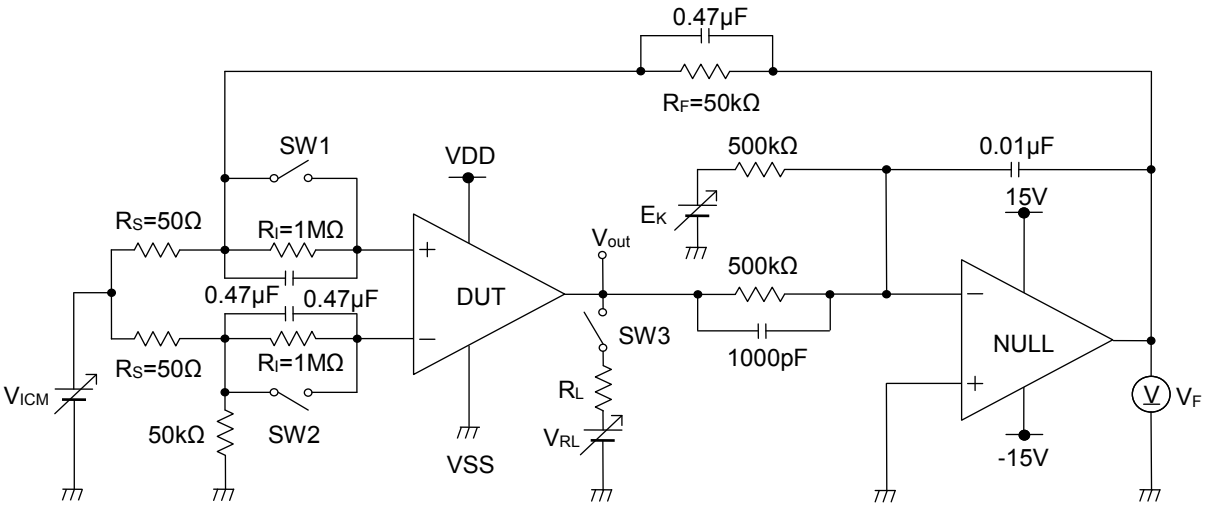


Figure 25. Test Circuit 1 (One channel only)

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Application Information - continued

Switch Conditions for Test Circuit 2

Parameter	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Supply Current	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage (R_L=10 kΩ)	OFF	ON	ON	ON	OFF	OFF	ON	OFF
Output Sink Current	OFF	ON	ON	OFF	OFF	ON	OFF	OFF
Propagation Delay Time	ON	OFF	ON	ON	ON	OFF	OFF	ON

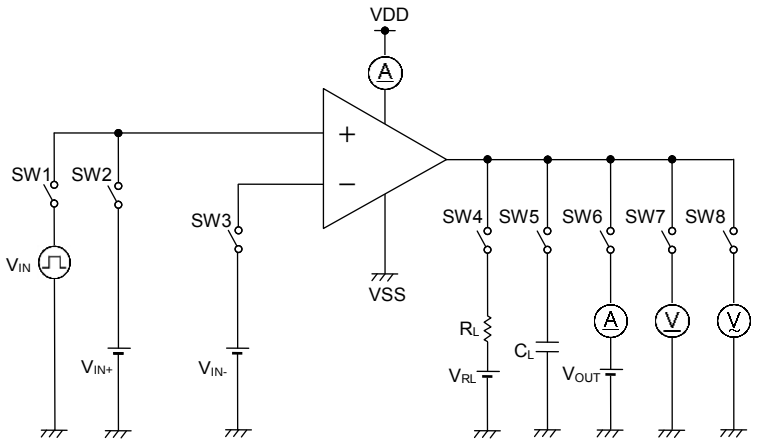


Figure 26. Test Circuit 2 (One channel only)

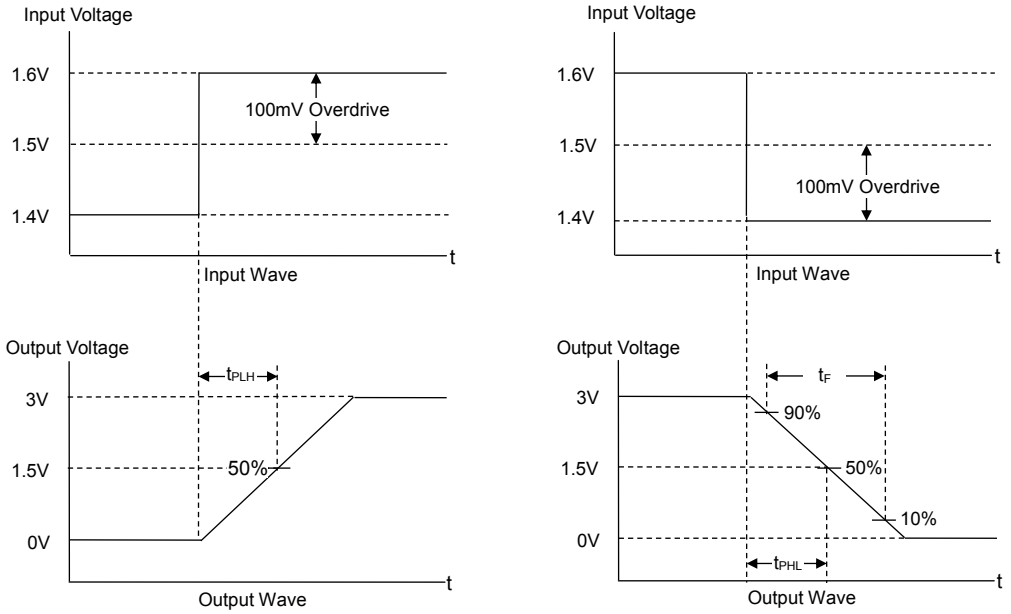


Figure 27. Propagation Delay Time Input and Output Wave

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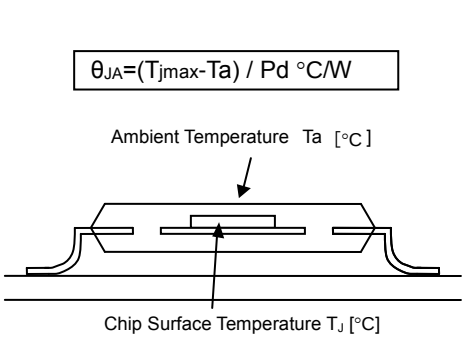
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Power Dissipation

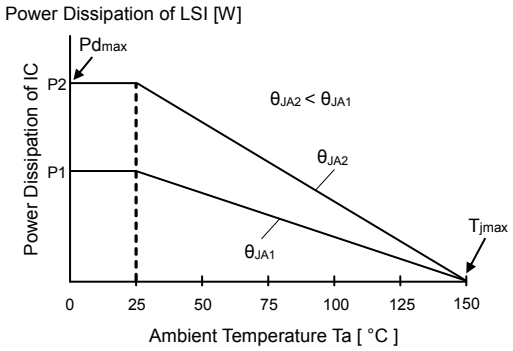
Power dissipation (total loss) indicates the power that the IC can consume at Ta=25 °C (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power. Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol θ_{JA} °C/W, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.
Figure 28(a) shows the model of the thermal resistance of the package. The equation below shows how to compute for the thermal resistance (θ_{JA}), given the ambient temperature (Ta), maximum junction temperature (T_{jmax}), and power dissipation (Pd).

$$\theta_{JA} = (T_{jmax}\text{-}Ta) / Pd \quad °C/W$$

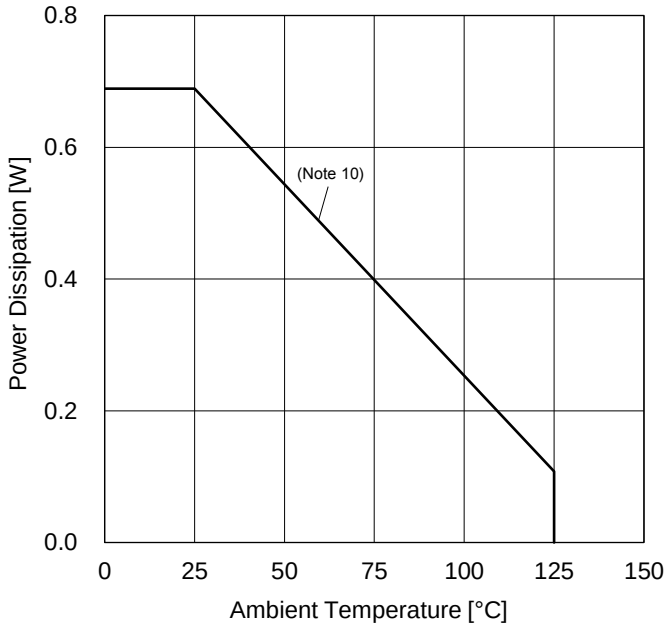
The derating curve in Figure 28(b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance (θ_{JA}), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 28(c) shows the derating curve for BU7233YF-C.



(a) Thermal Resistance



(b) Derating Curve



(c) BU7233YF-C

Figure 28. Thermal Resistance and Derating Curve

(Note 10)	Unit
5.5	mW/°C

When using the unit above Ta =25 °C, subtract the value above per Celsius degree. Power dissipation is the value when FR4 glass epoxy board 70 mm × 70 mm × 1.6 mm (copper foil area less than 3 %) is mounted.

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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_d stated in this specification is when the IC is mounted on a 70 mm x 70 mm x 1.6 mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_d rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. Unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

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Operational Notes – continued

13. Unused Circuits
When there are unused comparators, it is recommended that they are connected as in Figure 29, setting the non-inverting input pin to the VDD, inverting input pin to the VSS.

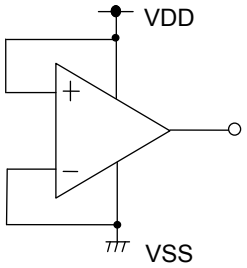


Figure 29. Example of Application Circuit for Unused Comparator

14. Input Voltage
Applying V_{SS}-0.3V to V_{DD}+0.3V to the input pin is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

15. Power Supply(Single/Dual)
The voltage comparator operates when the voltage supplied is between VDD and VSS. Therefore, the single supply voltage comparator can be used as dual supply voltage comparator as well.

16. Output Capacitor
If a large capacitor is connected between the output pin and VSS pin, current from the charged capacitor will flow into the output pin and may destroy the IC when the VDD pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 0.1μF between output pin and VSS pin.

17. Latch up
Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up and protect the IC from abnormaly noise.

18. Open Drain Output
Please connect and use a pull-up resistor to the output since this IC has an open-drain output.

19. Supply Voltage Start-up
When start up the supply voltage that the IC has output the applied VDD pin voltage until voltage reaches around 1V. This function is not depending on input condition. This voltage has a possibility of the malfunction. Please give the special consideration for startup order of supply voltage.

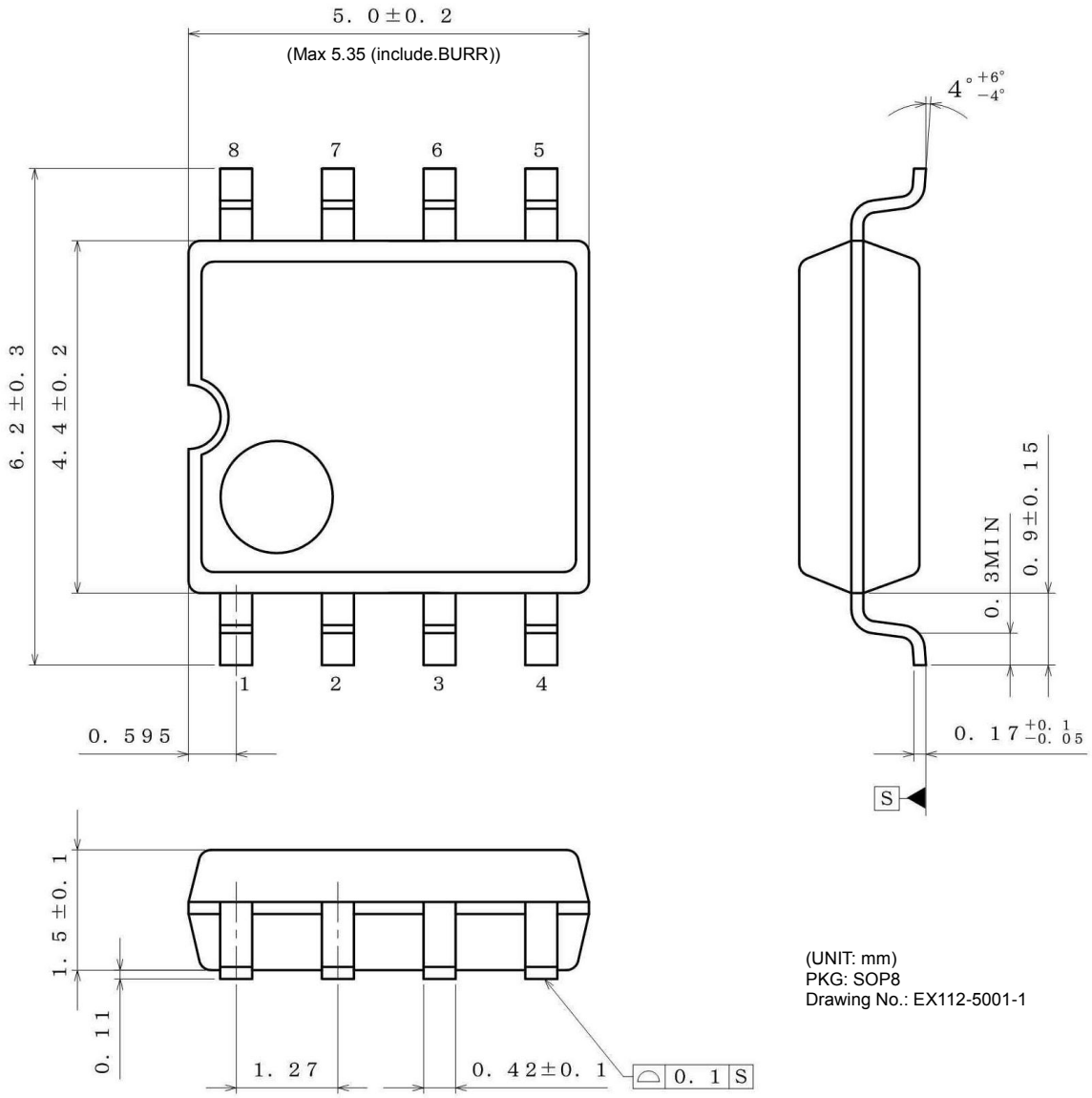
20. Ceramic Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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Physical Dimensions, Tape and Reel Information

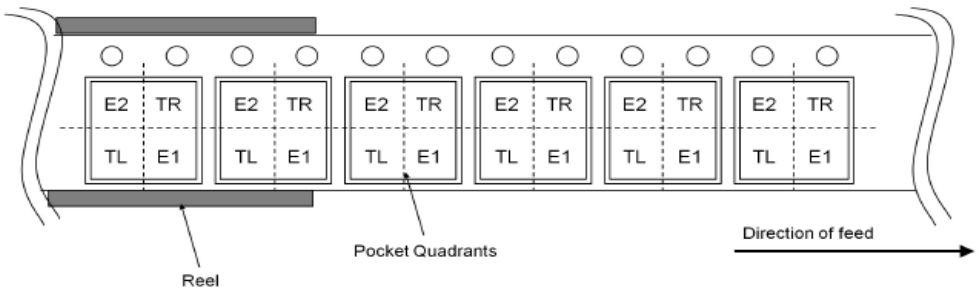
Package Name	SOP8



(UNIT: mm)
PKG: SOP8
Drawing No.: EX112-5001-1

<Tape and Reel information>

Tape	**Embossed carrier tape**
Quantity	**2500pcs**
Direction of feed	**E2** **(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)**



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Ordering Information

B U 7 2 3 3 Y F - C E2

Part Number
BU7233YF

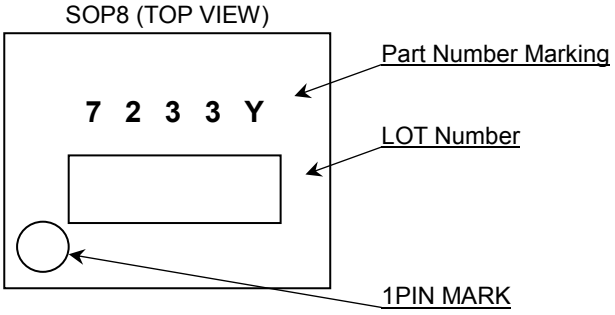
Package
F : SOP8

Product Rank
C: Automotive
Packaging and Forming Specification
E2: Embossed Tape and Reel

Line-up

Topr	Channels	Package		Orderable Part Number
-40°C to +125°C	2ch	SOP8	Reel of 2500	BU7233YF-CE2

Marking Diagram

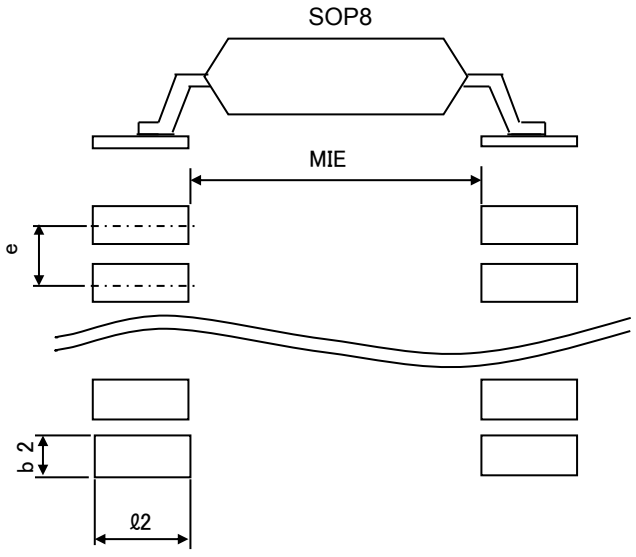


Part Number Marking	Package	Orderable Part Number
7233Y	SOP8	BU7233YF-CE2

Land Pattern Data

All dimensions in mm

Package	Land pitch e	Land space MIE	Land length ≧ℓ2	Land width b2
SOP8	1.27	4.60	1.10	0.76



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Revision History

Date	Revision	Changes
25.Feb.2015	001	New Release
17.Mar.2015	002	The correction of graph data and test circuit
17.Feb.2016	003	Applications : Change, Note : Addition(Note9), Typical Performance Curves : Change(temperature-axis range), Marking Diagrams : Change(table), Application Information : Correction(NULL Method /Switch Conditions)
19.Feb.2018	004	Full swing → Rail-to-Rail Split Supply → Dual Supply Deletion of (Note 5) Update : Physical Dimensions, Tape and Reel Information

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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