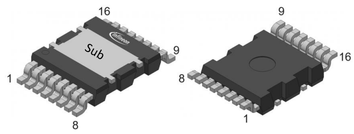
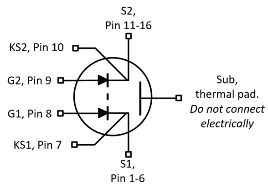
CoolGaN™ BDS 650 V G5

TOLT



CoolGaN™ Bi-directional switch, enhancement-mode

Infineon's CoolGaN™ Bi-Directional Switch (BDS) is an innovative solution in gallium nitride (GaN) transistor technology. The CoolGaN™ BDS 650 V G5 enables efficient voltage blocking in both directions, making it a versatile option for a wide range of applications. The CoolGaN™ BDS monolithically integrates a substrate voltage control circuit, thanks to Infineon's proprietary technology, this reduces design complexity. IGLT65R055B2 is offered in Infineon's TOLT, top-side cooling package specially designed to enable the highest power densities for power-demanding industrial applications.



Features

- 650 V CoolGaN™ technology with 850 V_{SS} surge immunity
- Superior rugged Gate Injection Transistor (GIT) structure
- Dual-gate for independent bi-directional functionality
- Superior performance of $R_{SS(on)}$ over operating frequency
- Reliable Thermal Cycling on-Board (TCoB) performance
- Optimized for soft switching operation
- 2 kV HBM ESD standard

Benefits

- Effective replacement of back-to-back uni-directional products
- Improves system efficiency and power density
- Enables higher switching frequency
- System cost reduction
- Enables new single stage isolated topologies

Potential applications

- Cycloconverter in solar µ-inverter
- Vienna type rectifier in industrial/server SMPS and UPS
- T-type PFC, inverter in motor drives
- HERIC inverter in string solar inverter

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Please note: The substrate thermal pad is for thermal coupling only, it should be electrically isolated from any electrical node in the system via isolation material.

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{SS,cont}$	340	V_{AC}
$R_{SS(on),typ}$	55	mΩ
$Q_{GxSx,diode}$	5.4	nC
$I_{SS,pulse}$	±73	A
Q_{oss} @ 400 V_{SS} (switch)	72	nC

Part number	Package	Marking	Related links
IGLT65R055B2	PG-HDSOP-16	65R055B2	see Appendix A

Table of contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-to-source voltage, continuous	$V_{SS,cont}$	-	-	340	V_{AC}	V_{GS}=0 V
Source-to-source voltage, transient	$V_{SS,trans}$	-650	-	650	V	t_{TRANS}=5 ms; V_{GS}=0 V
Source-to-source voltage, surge	$V_{SS,surge}$	-850	-	850	V	t_{SURGE}=1 µs; V_{GS}=0 V
Source-to-source AC line frequency	f_{SS}	45	-	-	Hz	V_{SS}=305 V_{AC}; ±431 V_{pk}
RMS current, source-to-source	$I_{SS,RMS}$	-21.8	-	21.8	A	T_C=25°C;
		-14		14		T_C=125°C; T_j=$T_{j,max}$
Pulsed current, source-to-source	$I_{SS,pulse}$	-73.6	-	73.6	A	T_j=25°C; I_{GS}=30.0 mA
		-45		45		T_j=125°C; I_{GS}=30.0 mA
Gate current, steady state (single gate)	$I_{G,ss}$	-	-	30.0	mA	T_j=-40°C to T_j=150°C; see Table 8
Gate current, pulsed (single gate) 1)	$I_{G,pulse}$	-	-	3000	mA	T_j=-40°C to T_j=150°C; t_{PULSE}=50 ns, f=100 kHz; see Table 8
Gate source voltage, continuous 1)	V_{GS}	-10	-	-	V	T_j=-40°C to T_j=150°C; see Table 8
Gate source voltage, pulsed 1)	$V_{GxSx,pulse}$	-25	-	-	V	T_j=-40°C to T_j=150°C; t_{PULSE}=50 ns, f=100 kHz; open source
Power dissipation	P_{tot}	-	-	135	W	T_C=25°C
Operating junction temperature	T_j	-40	-	150	°C	T_j=125°C; V_{GySy}=3 V; see Diagram 5, 6
Storage temperature	T_{stg}	-40	-	150	°C	Max shelf life depends on storage conditions
Source-to-source voltage slew-rate	dv/dt	-	-	40	V/ns	-

1) We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for more details.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.92	°C/W	-
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL3

3 Electrical characteristics

at T_j=25°C, unless specified otherwise

Table 4 Gate characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage: switch mode (OFF) to diode mode	$V_{GxSx(th), diode}$	0.8	1.15	1.6	V	I_{SS}=3.0 mA; V_{GySy}=0 V; V_{SS}=10 V; T_j=25°C;
		-	0.95	-		I_{SS}=3.0 mA; V_{GySy}=0 V; V_{SS}=10 V; T_j=125°C; see Table 9
Gate threshold voltage: diode mode to switch mode (ON)	$V_{GxSx(th), switch}$	0.7	1.00	1.5	V	I_{SS}=3.0 mA; I_{GySy}=5 mA; V_{SS}=10 V; T_j=25°C;
		-	0.83	-		I_{SS}=3.0 mA; I_{GySy}=5 mA; V_{SS}=10 V; T_j=125°C; see Table 9
Gate-Source reverse clamping voltage	$V_{GS, clamp}$	-8	-	-	V	$I_{GS,ss}$=-1 mA
Gate charge: diode mode to switch mode (ON)	$Q_{GxSx, switch}$	-	5.4	-	nC	V_{GxSx}=0 to 3 V; I_{GySy}=5 mA; V_{SS}=400 V, I_{SS}=9 A
Gate resistance	$R_{GS,int}$	-	1	-	Ω	LCR impedance measurement; f=f_{res}

Table 5 On-state characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-to-source on-state resistance	$R_{SS(on)}$	-	55	70	mΩ	I_{GS}=30.0 mA; I_{SS}=9 A; T_j=25°C
			103	-		I_{GS}=30.0 mA; I_{SS}=9 A; T_j=150°C

Table 6 Dynamic characteristics - switch mode, see Table 10

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance: switch mode	$C_{iss,switch}$	-	346	-	pF	V_{GS}=0 V; V_{SS}=400 V; f=1 MHz
Output capacitance: switch mode	$C_{oss,switch}$		147			
Reverse Transfer capacitance: switch mode	$C_{rss,switch}$		3			
Effective output capacitance, energy related: switch mode 2)	$C_{o(er),switch}$	-	166	-	pF	V_{GS}=0 V; V_{SS}=400 V
Effective output capacitance, time related: switch mode 3)	$C_{o(tr),switch}$	-	180	-	pF	V_{GS}=0 V; V_{SS}=0 to 400 V; I_{SS}=const
Output charge: switch mode	$Q_{oss,switch}$	-	72	-	nC	V_{GS}=0 V; V_{SS}=400 V

2) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{SS} is rising from 0 to 400 V
3) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{SS} is rising from 0 to 400 V

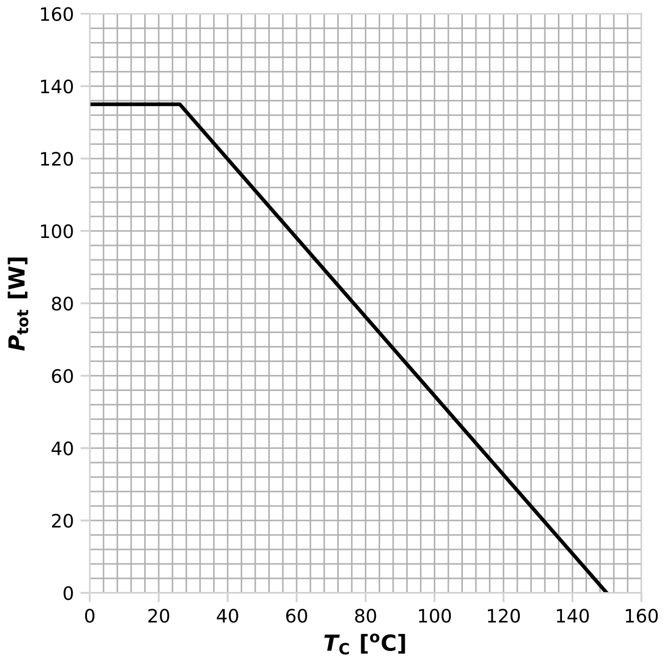
Table 7 Dynamic characteristics - diode mode, see Table 11

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance: diode mode	$C_{iss,diode}$	-	351	-	pF	V_{GxSx}=0 V; V_{GySy}=3 V; V_{SySx}=400 V; f=1 MHz
Output capacitance: diode mode	$C_{oss,diode}$		172			
Reverse Transfer capacitance: diode mode	$C_{rss,diode}$		4			
Effective output capacitance, energy related: diode mode [4]	$C_{o(er),diode}$	-	198	-	pF	V_{GxSx}=0 V; V_{GySy}=3 V; V_{SySx}=400 V
Effective output capacitance, time related: diode mode [5]	$C_{o(tr),diode}$	-	224	-	pF	V_{GxSx}=0 V; V_{GySy}=3 V; V_{SySx}=0 to 400 V; I_{SS}=const
Output charge: diode mode	$Q_{oss,diode}$	-	90	-	nC	V_{GxSx}=0 V; V_{GySy}=3 V; V_{SySx}=400 V

4) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{SS} is rising from 0 to 400 V
5) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{SS} is rising from 0 to 400 V

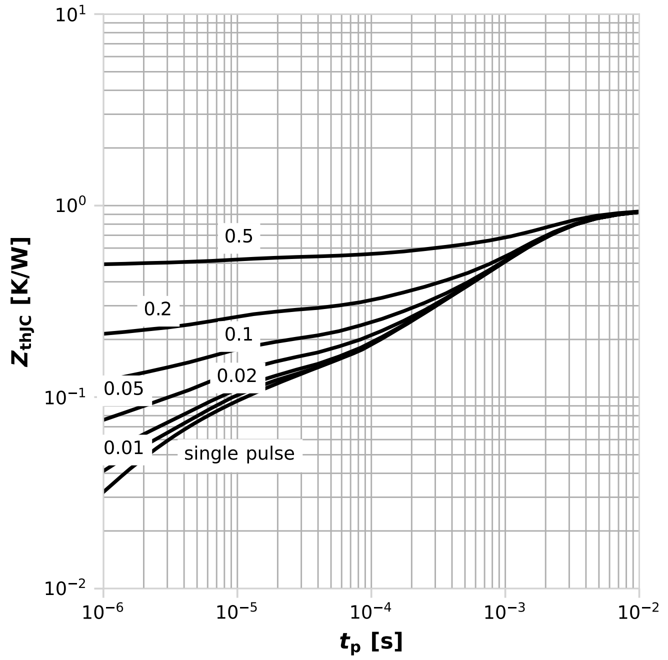
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



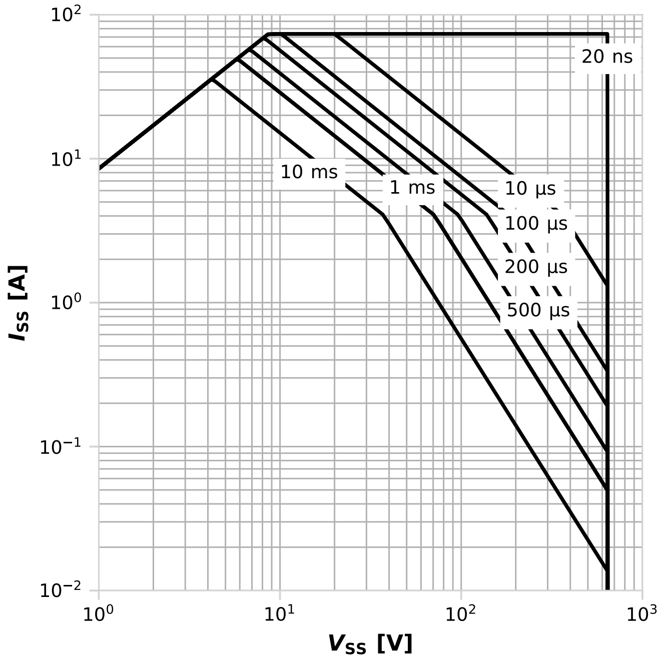
P_{tot}=f(T_C)

Diagram 2: Max. transient thermal impedance



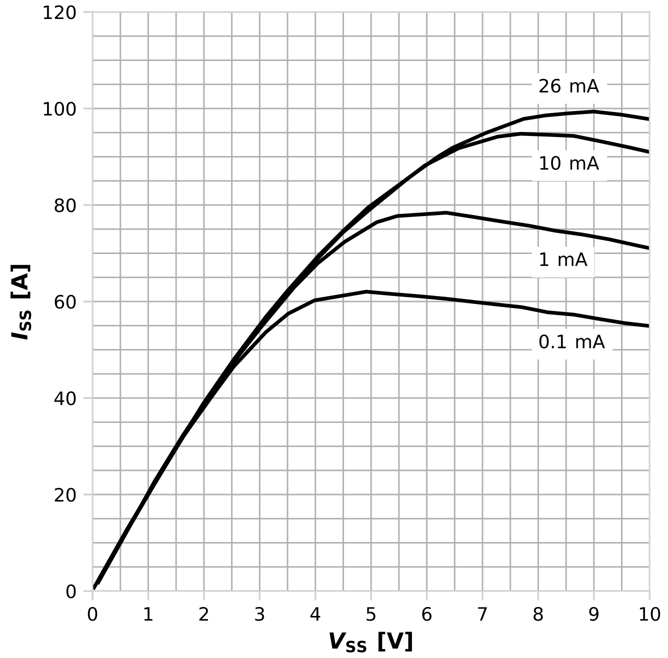
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 3: Safe operating area



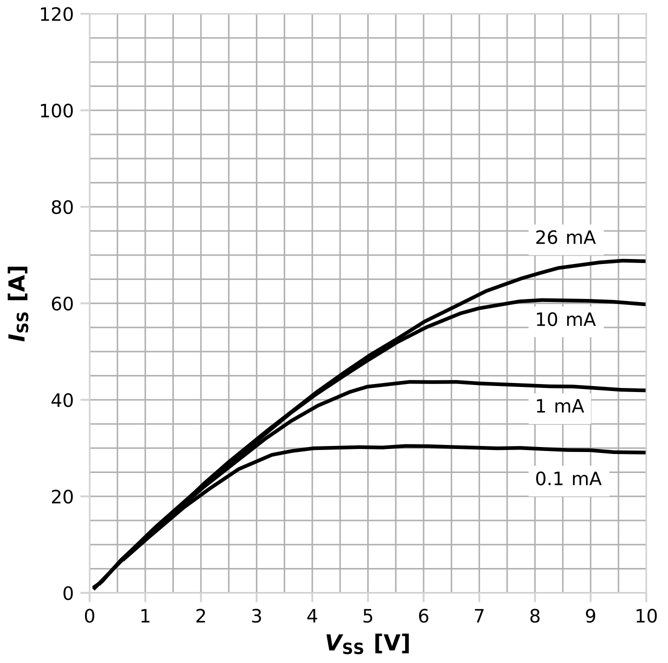
I_{SS}=f(V_{SS}); T_C=25°C; D=0; parameter: t_p

Diagram 4: Typ. output characteristics



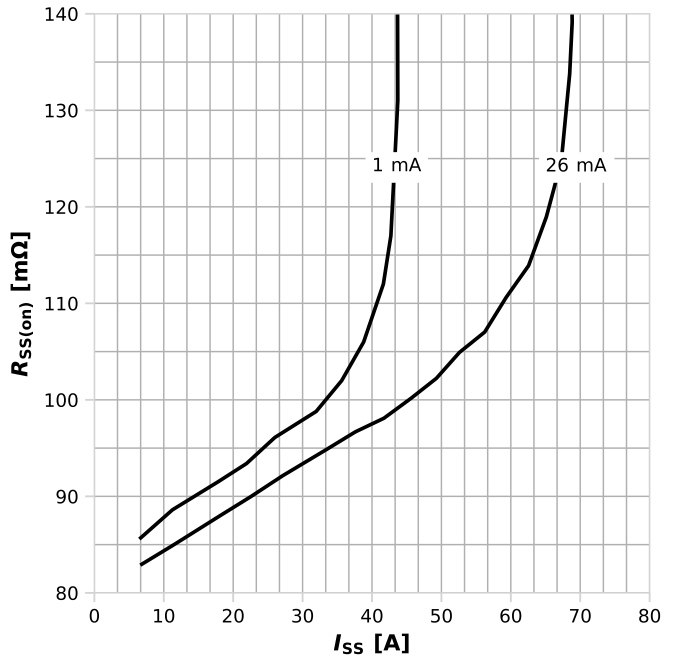
I_{SS}=f(V_{SS}); V_{GySy}=3 V; T_j=25°C; parameter: I_{GxSx}

Diagram 5: Typ. output characteristics



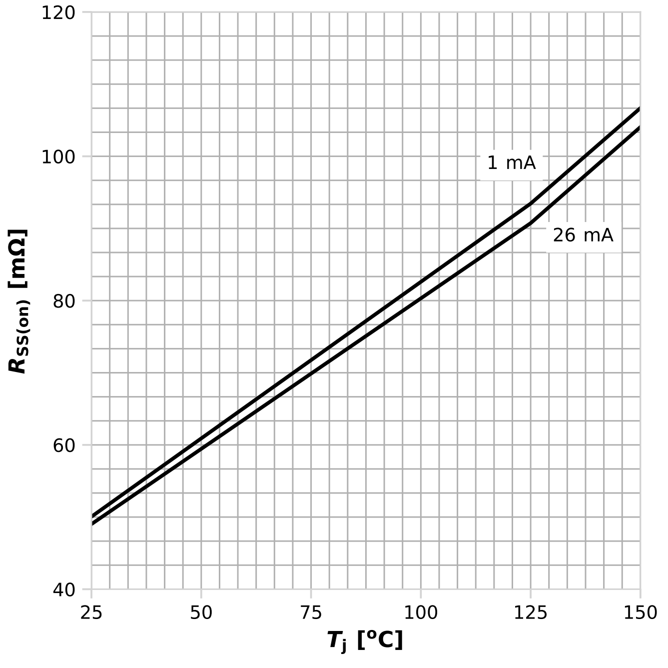
I_{SS}=f(V_{SS}); V_{GySy}=3 V; T_j=125°C; parameter: I_{GxSx}

Diagram 6: Typ. source on-state resistance



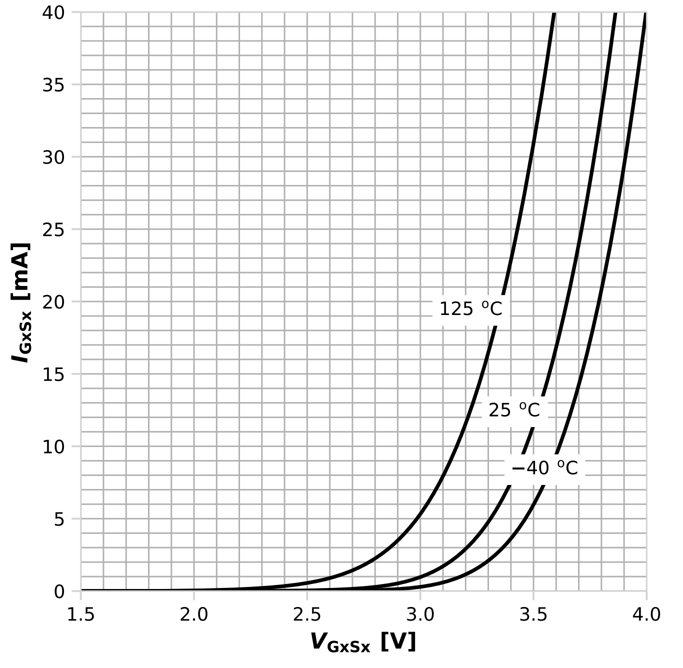
$R_{SS(on)}$=f(I_{SS}); V_{GySy}=3 V; T_j=125°C; parameter: I_{GxSx}

Diagram 7: Typ. source-source on-state resistance



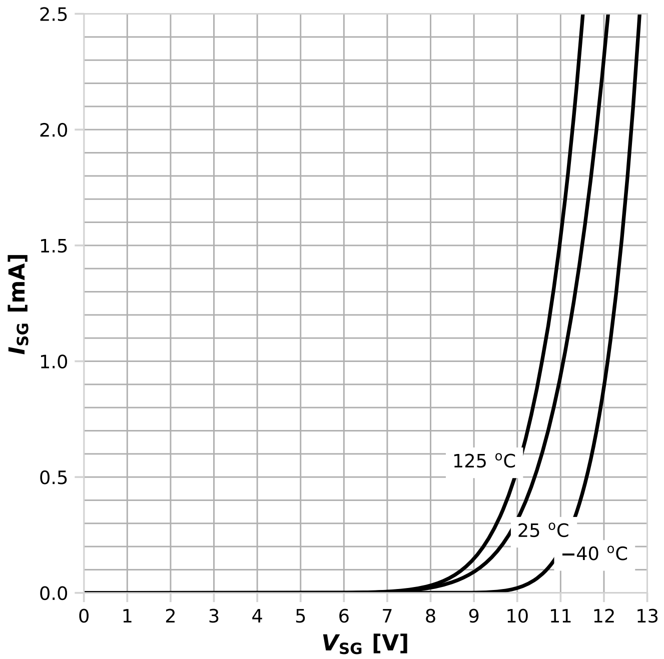
$R_{SS(on)}$=f(T_j); V_{GySy}=3 V; I_{SS}=20 A; parameter: I_{GxSx}

Diagram 8: Typ. gate characteristics forward



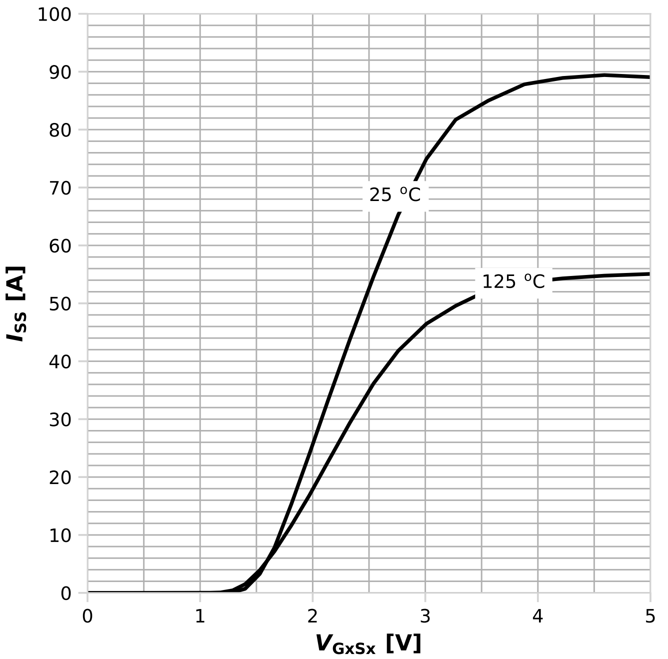
I_{GS}=f(V_{GxSx}); open S_y, G_y; parameter: T_j

Diagram 9: Typ. gate characteristics reverse



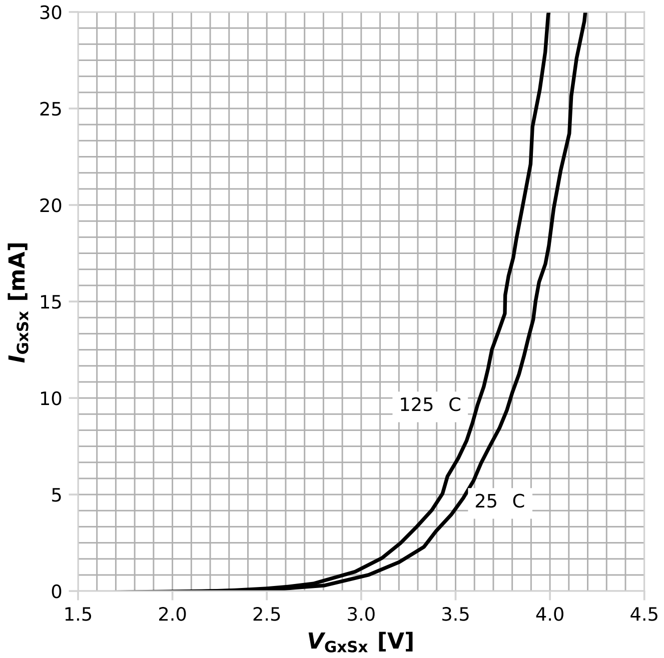
I_{SG}=f(V_{SG}); parameter: T_j

Diagram 10: Typ. transfer characteristics



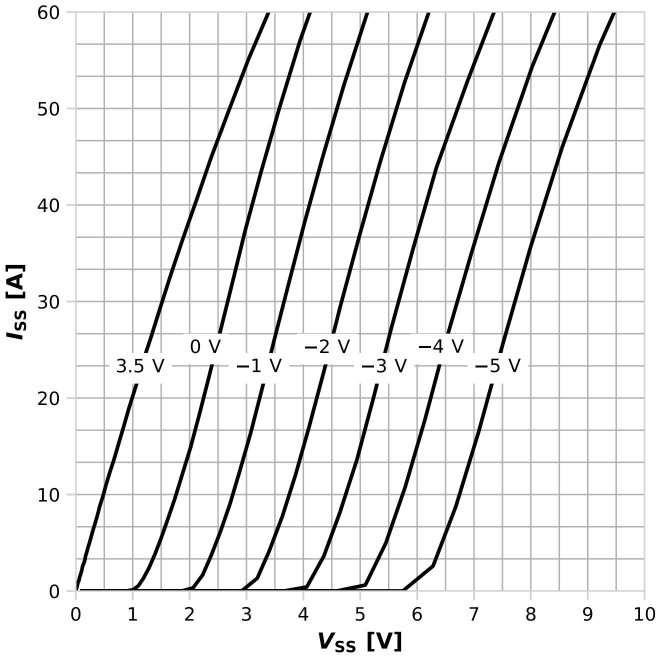
I_{SS}=f(V_{GxSx}); V_{GySy}=3 V; V_{SS}=8 V; parameter: T_j

Diagram 11: Typ. transfer gate current characteristics



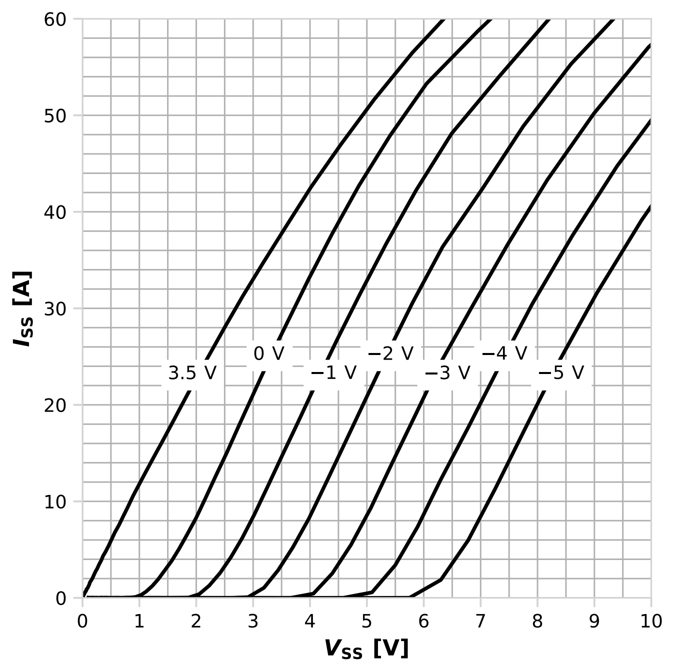
I_{GxSx}=f(V_{GxSx}); V_{GySy}=3 V; V_{SS}=8 V; parameter: T_j

Diagram 12: Typ. channel reverse characteristics



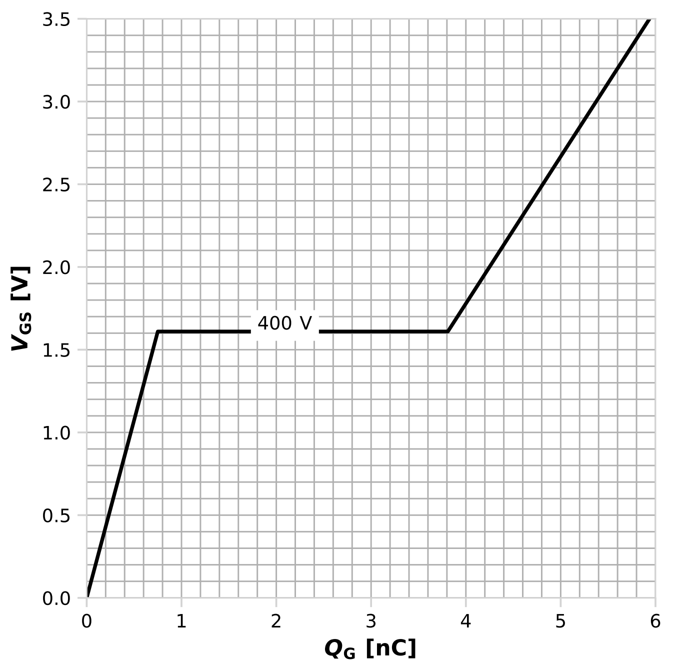
I_{SS}=f(V_{SS}); I_{GySy}=37 mA; T_j=25°C; parameter: V_{GxSx}

Diagram 13: Typ. channel reverse characteristics



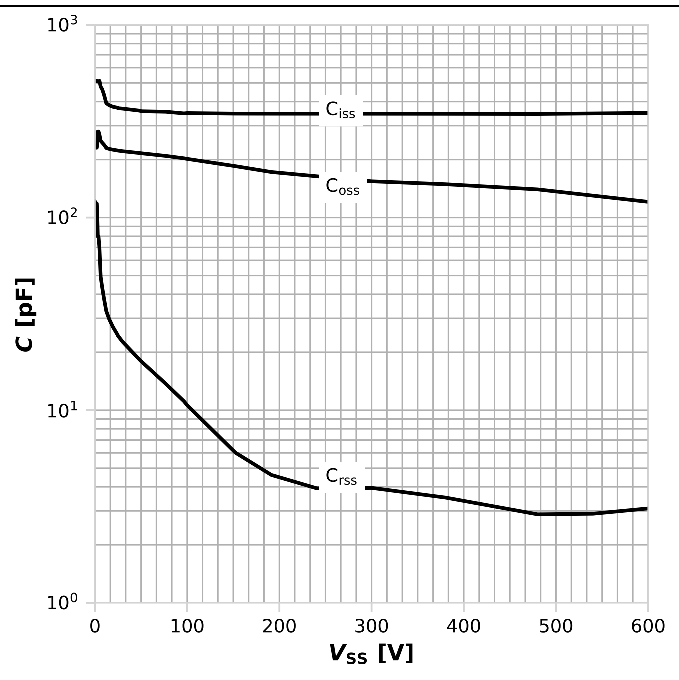
I_{SS}=f(V_{SS}); I_{GySy}=37 mA; T_j=125°C; parameter: V_{GxSx}

Diagram 14 Typ. gate charge



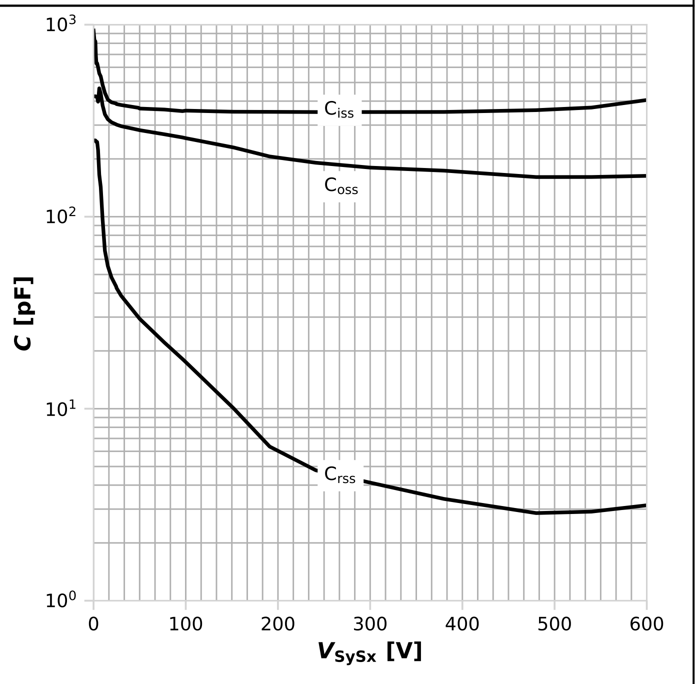
V_{GxSx}=f(Q_G); V_{GySy}=3 V; I_{SS}=9.3 A pulsed; parameter: V_{SS}

Diagram 15: Typ. capacitances in switch mode (OFF-OFF)

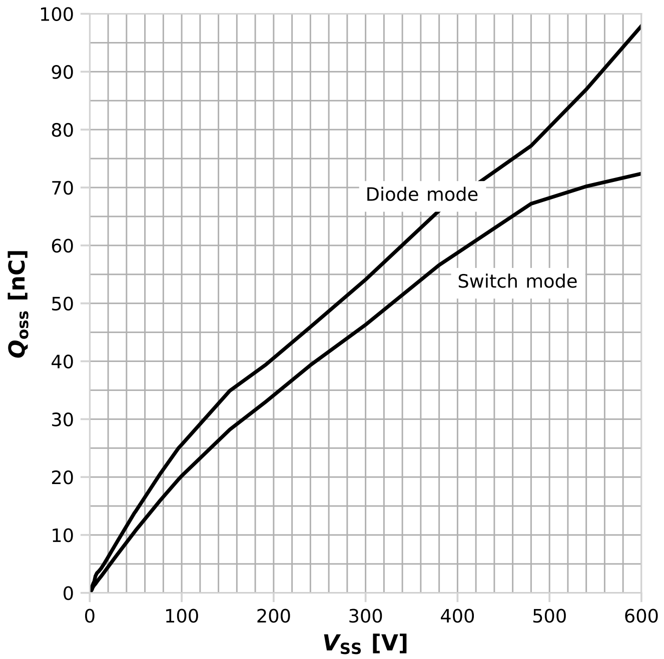
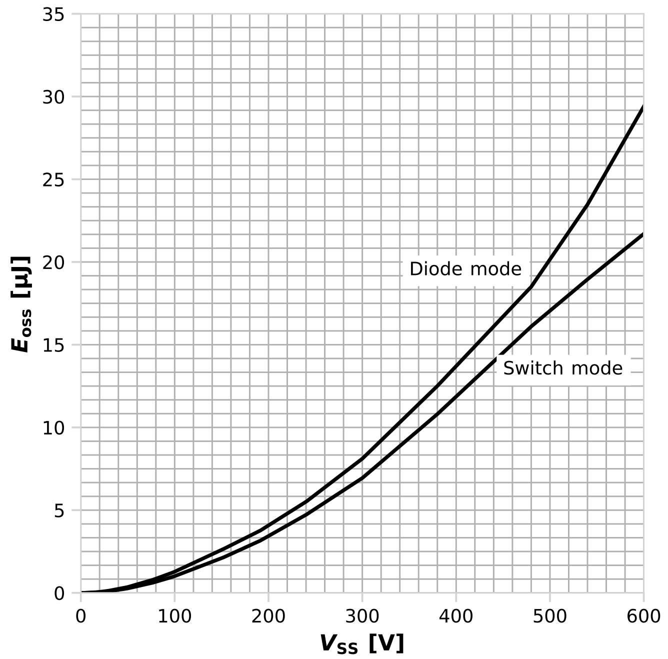


C_{zss}=f(V_{SS}); V_{GS}=0 V

Diagram 16: Typ. capacitances in diode mode (ON-OFF)



C_{zss}=f($V_{Sy\text{-}Sx}$); V_{GySy}=3 V; V_{GxSx}=0 V

Diagram 17: Typ. output charge	Diagram 18: Typ. Coss stored Energy
	
Q_{oss}=f(V_{SS}); parameter: modes	E_{oss}=f(V_{SS}); parameter: modes

5 Test circuits

Table 8 Gate current switching waveform

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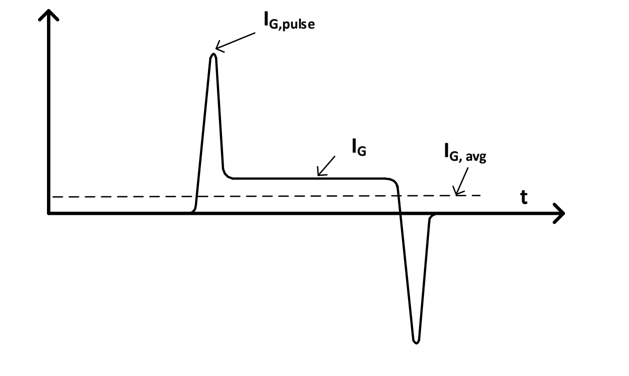
<tr><th>Gate current switching waveform</th></tr>
<tr><td>
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Table 9 Test condition

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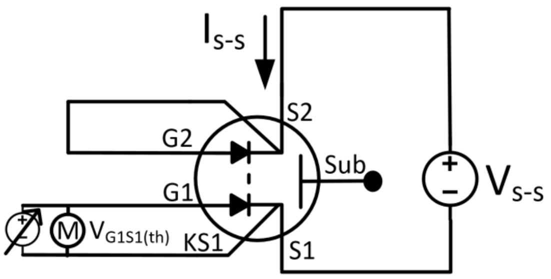
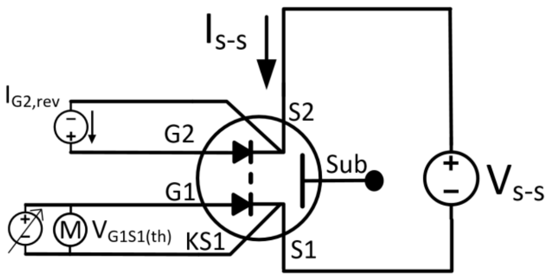
<tr><th>$V_{GXSX(th)}$ test condition (diode mode)</th><th>$V_{GXSX(th)}$ test condition (switch mode)</th></tr>
<tr><td>
</td><td>
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</table>

6 Modes of operation

Table 10 Switch mode

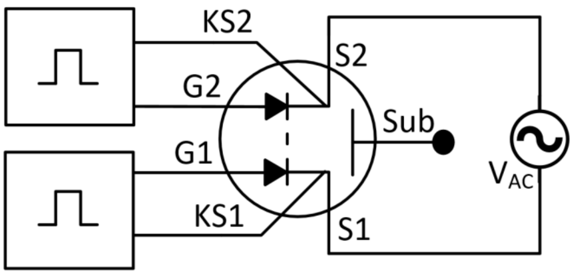
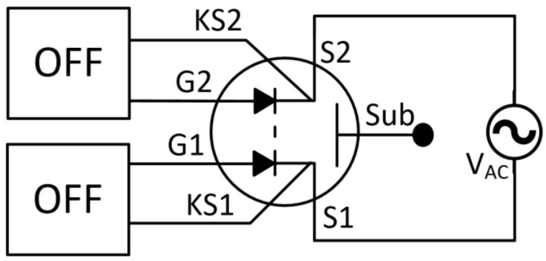
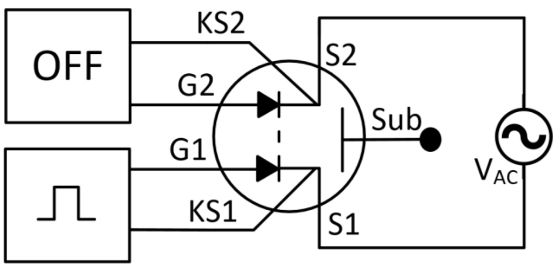
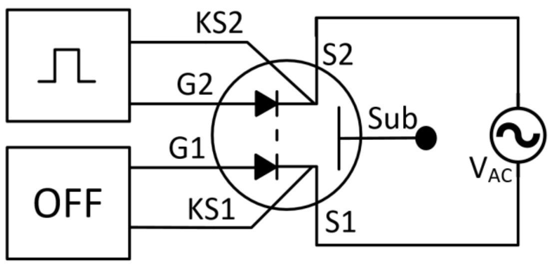
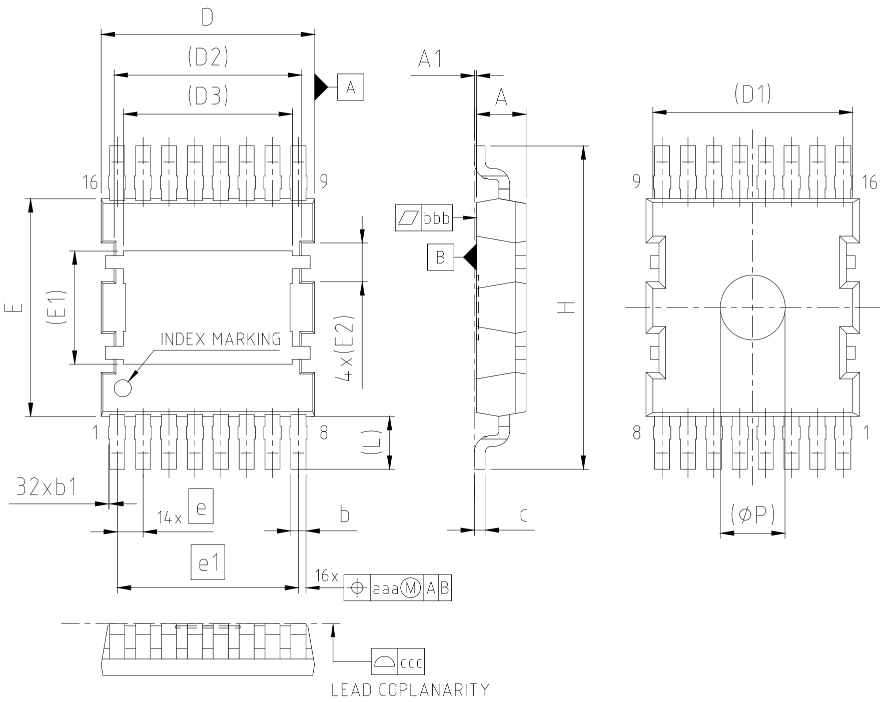
Switch mode (ON-ON)	Switch mode (OFF-OFF)
	

Table 11 Diode mode

Diode mode (OFF-ON)	Diode mode (ON-OFF)
	

7 Package outlines



PACKAGE - GROUP NUMBER:	PG-HDSOP-16-U06				
DIMENSIONS	**MILLIMETERS**		**DIMENSIONS**	**MILLIMETERS**	
	MIN.	MAX.		MIN.	MAX.
A	2.25	2.35	**e**	1.20	
A1	---	0.15	**e1**	8.40	
b	0.60	0.80	**H**	14.80	15.20
b1	---	0.15	**L**	2.45	
c	0.40	0.60	**ØP**	3.00	
D	9.70	10.10	**aaa**	0.25	
D1	9.27		**bbb**	0.02	
D2	8.70		**ccc**	0.10	
D3	7.83				
E	10.00	10.30			
E1	5.26				
E2	1.80				

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-HDSOP-16, dimensions in mm

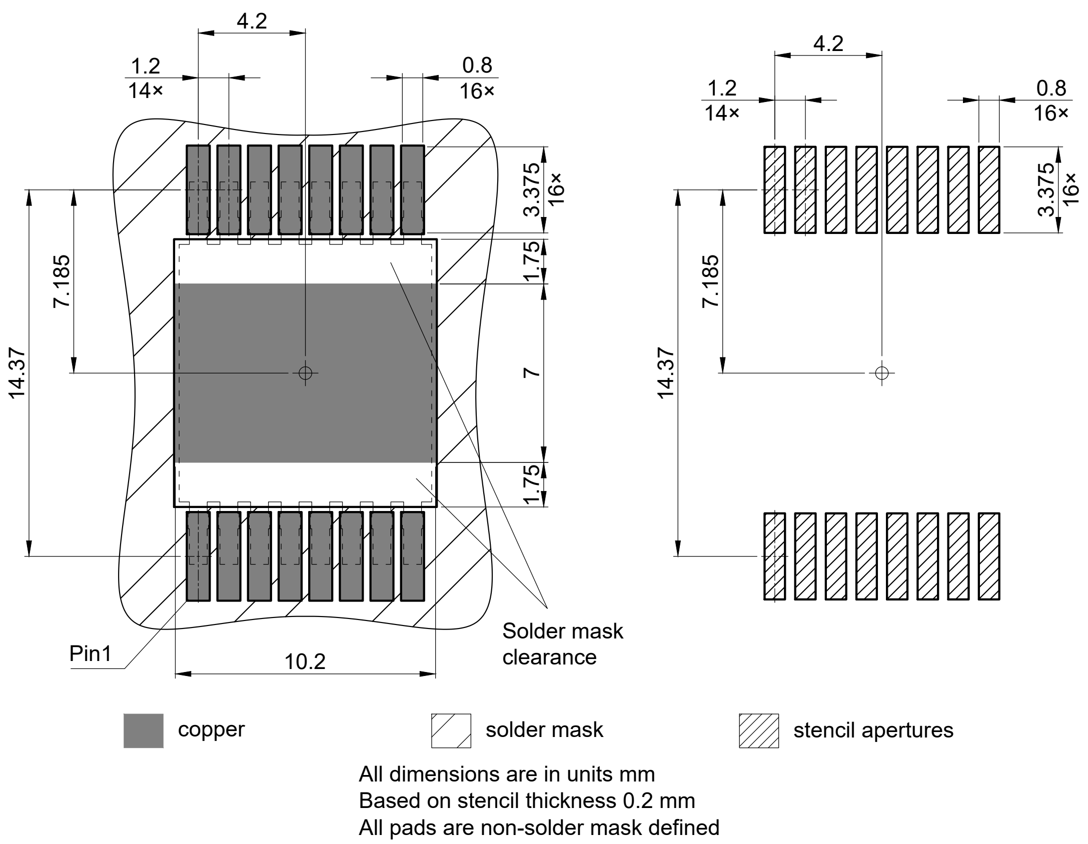


Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm

8 Appendix A

Table 12 Related links

- IFX CoolGaN^{TM} GaN 650 V webpage
- IFX CoolGaN^{TM} GaN 650 V reliability white paper
- IFX CoolGaN^{TM} GaN 650 V gate driver application note
- IFX CoolGaN^{TM} GaN 650 V applications information

Revision history

IGLT65R055B2

Revision 2025-05-09, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-05-09	Final

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