

MOSFET
OptiMOS™ 6 Power-Transistor, 200 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020
- 100% avalanche tested

Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	12.9	mΩ
I_D	87	A
Q_{oss}	116	nC
Q_G	37	nC
Q_{rr} (1000A/μs)	271	nC

Part number	Package	Marking	Related links
IPF129N20NM6	PG-TO263-7	129N20N6	-

D²-PAK 7pin

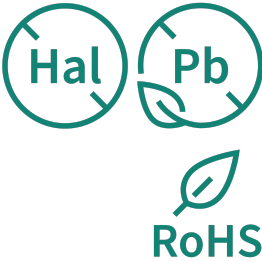
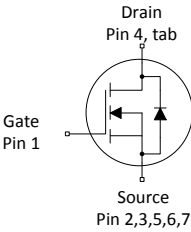
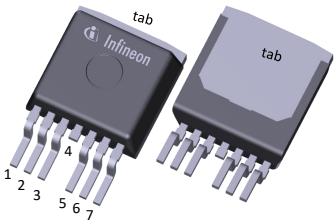




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	87	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
				62		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
				64		$V_{GS}=15\text{ V}$, $T_C=100\text{ °C}$
				11		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	348	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	258	mJ	$I_D=39\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	234	W	$T_C=25\text{ °C}$
				3.8		$T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.32	0.64	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	40		
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}		-	62		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.7	4.5	V	$V_{DS}=V_{GS}$, $I_D=129\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=160\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=160\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	11	12.9	m Ω	$V_{GS}=10\text{ V}$, $I_D=65\text{ A}$
			9.5	12		$V_{GS}=15\text{ V}$, $I_D=65\text{ A}$
Gate resistance	R_G	-	3.8	-	Ω	-
Transconductance ⁶⁾	g_{fs}	18	36	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=65\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2900	3800	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁷⁾	C_{oss}		460	600		
Reverse transfer capacitance ⁷⁾	C_{rss}		19	33		
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=100\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=32.5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		13			
Turn-off delay time	$t_{d(off)}$		20			
Fall time	t_f		7			

⁷⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	20	-	nC	$V_{DD}=100\text{ V}$, $I_D=32.5\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		10.7	-	nC	
Gate to drain charge ⁹⁾	Q_{gd}		7.6	11.4	nC	
Switching charge	Q_{sw}		16.9	-	nC	
Gate charge total ⁹⁾	Q_g		37	56	nC	
Gate plateau voltage	$V_{plateau}$		6.9	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	32	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ⁹⁾	Q_{oss}	-	116	151	nC	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ See "Gate charge waveforms" for parameter definition

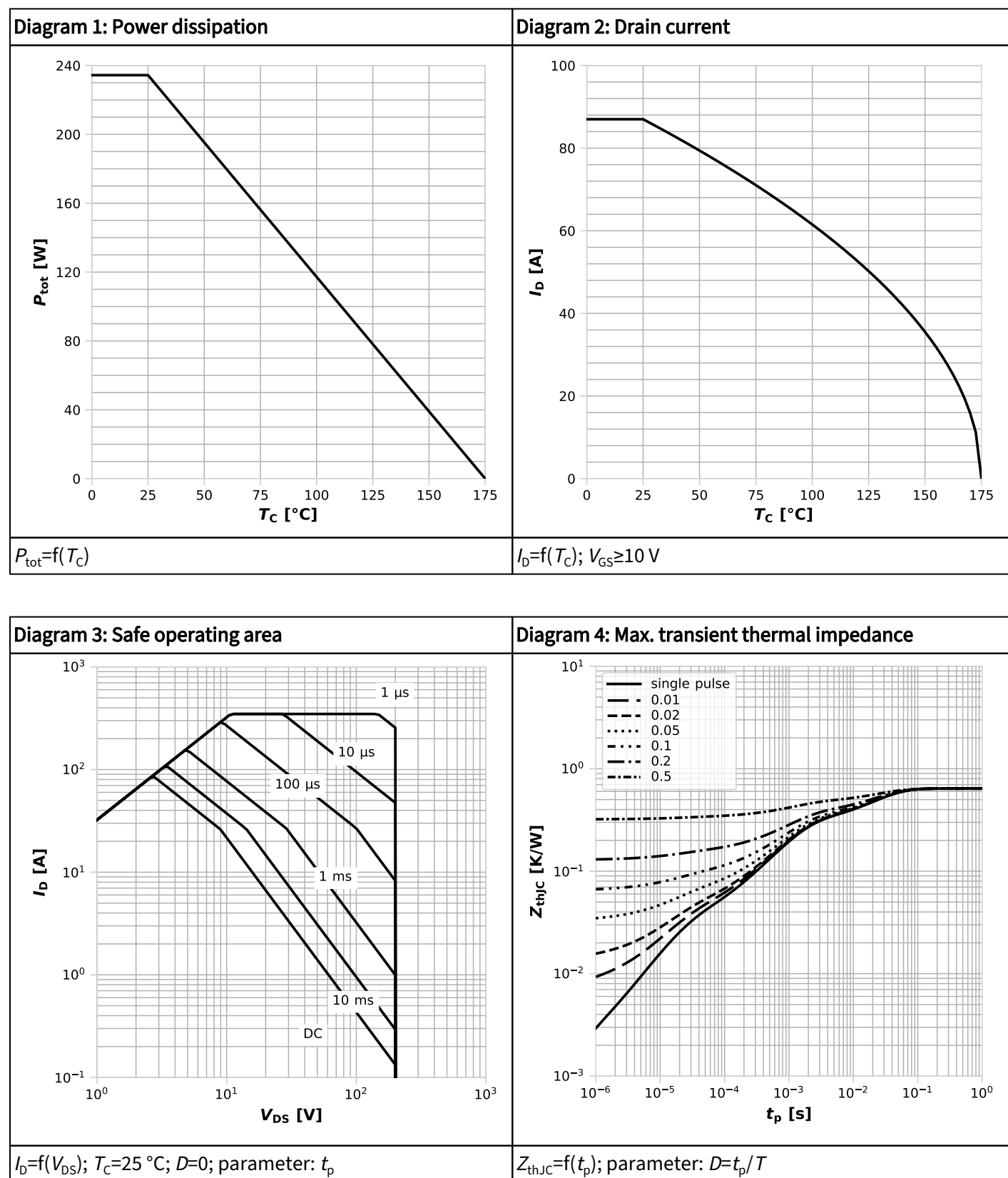
⁹⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	87	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			348		
Diode forward voltage	V_{SD}	-	0.90	1.0	V	$V_{GS}=0\text{ V}$, $I_F=65\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	46	-	ns	$V_R=100\text{ V}$, $I_F=32.5\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		43	86	nC	
Reverse recovery time	t_{rr}	-	39	-	ns	$V_R=100\text{ V}$, $I_F=32.5\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁰⁾	Q_{rr}		271	542	nC	

¹⁰⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams



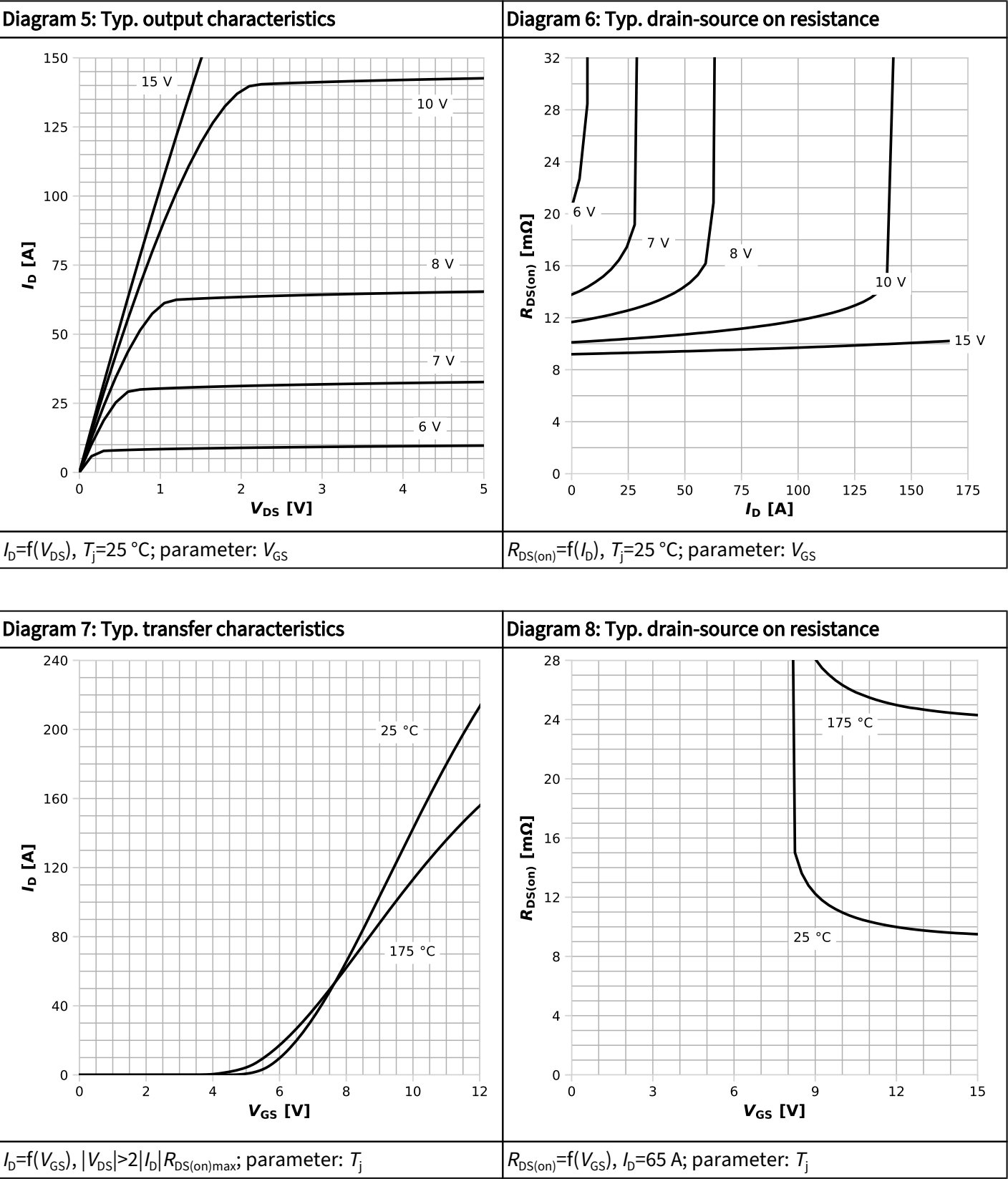
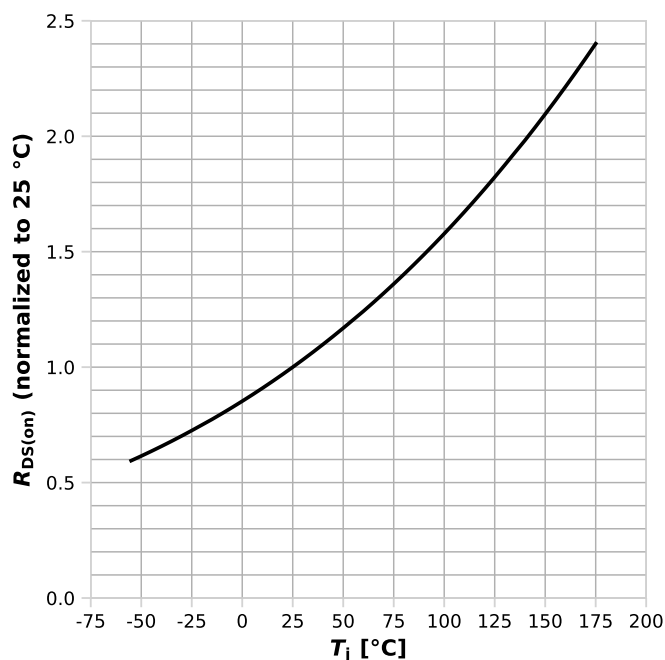
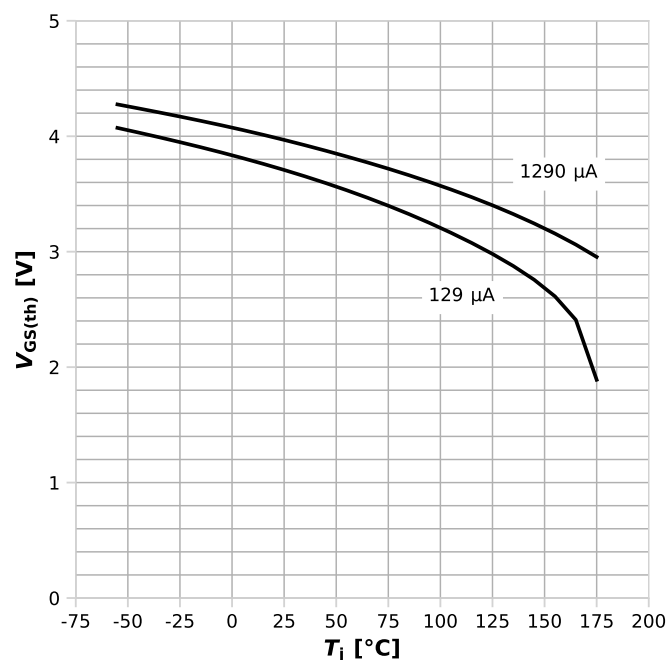


Diagram 9: Normalized drain-source on resistance



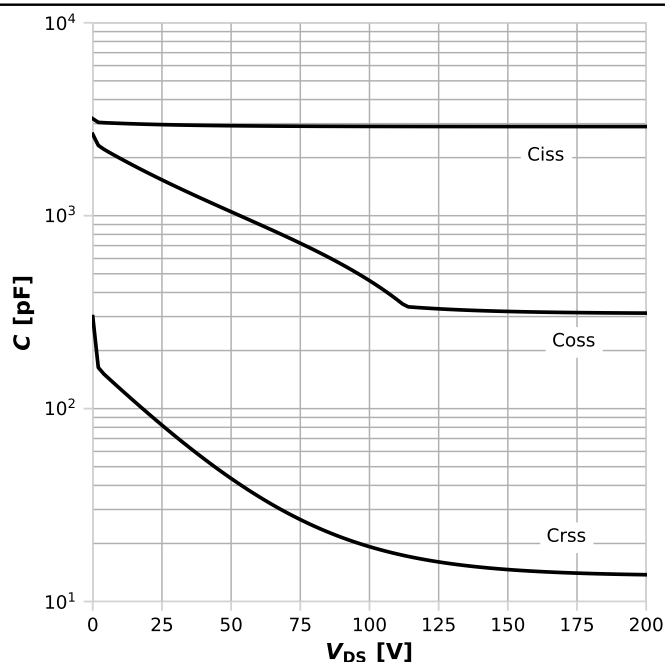
$$R_{DS(on)} = f(T_j), I_D = 65 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



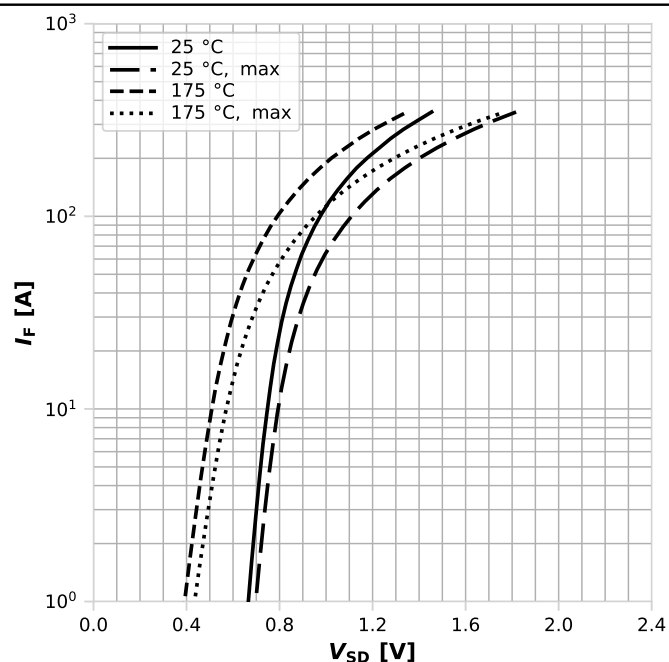
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances

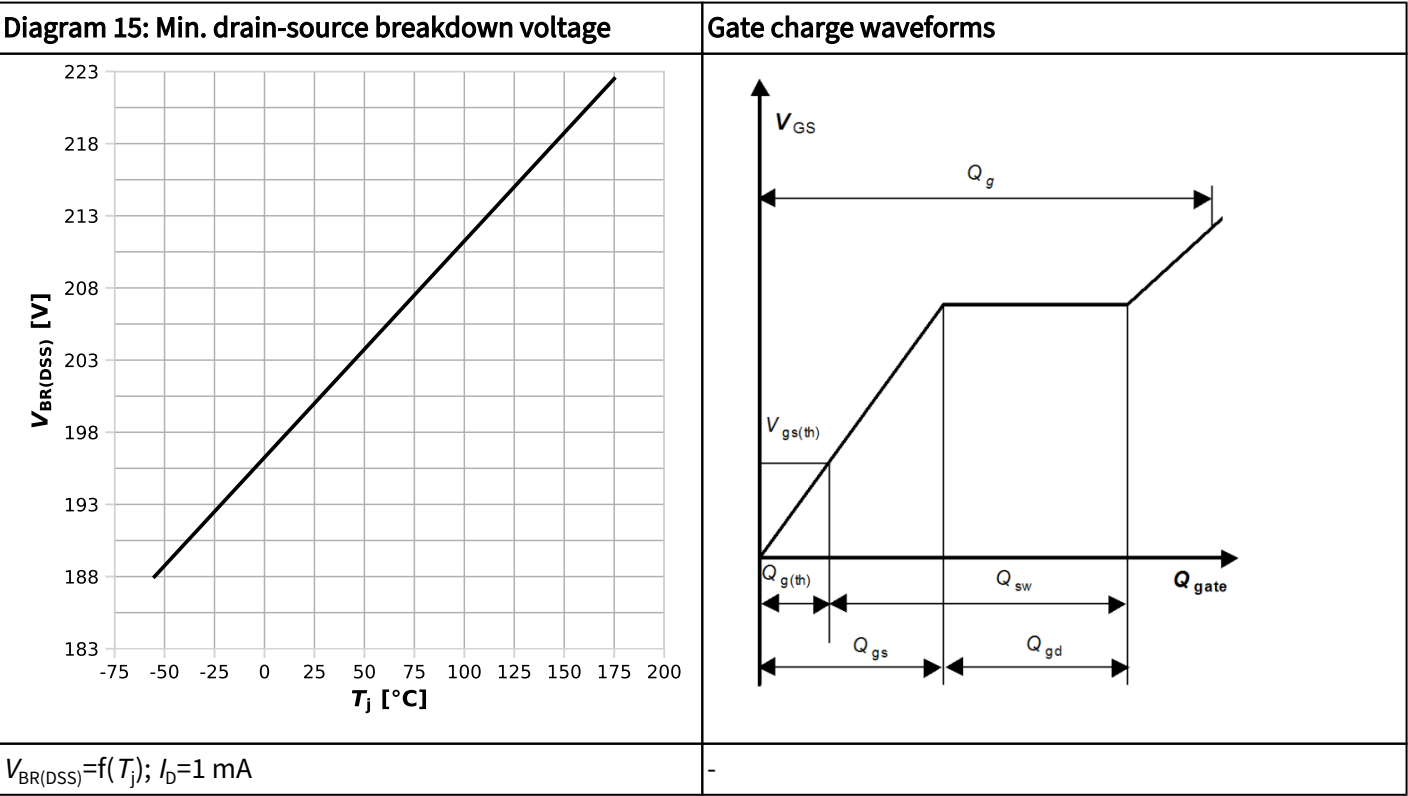
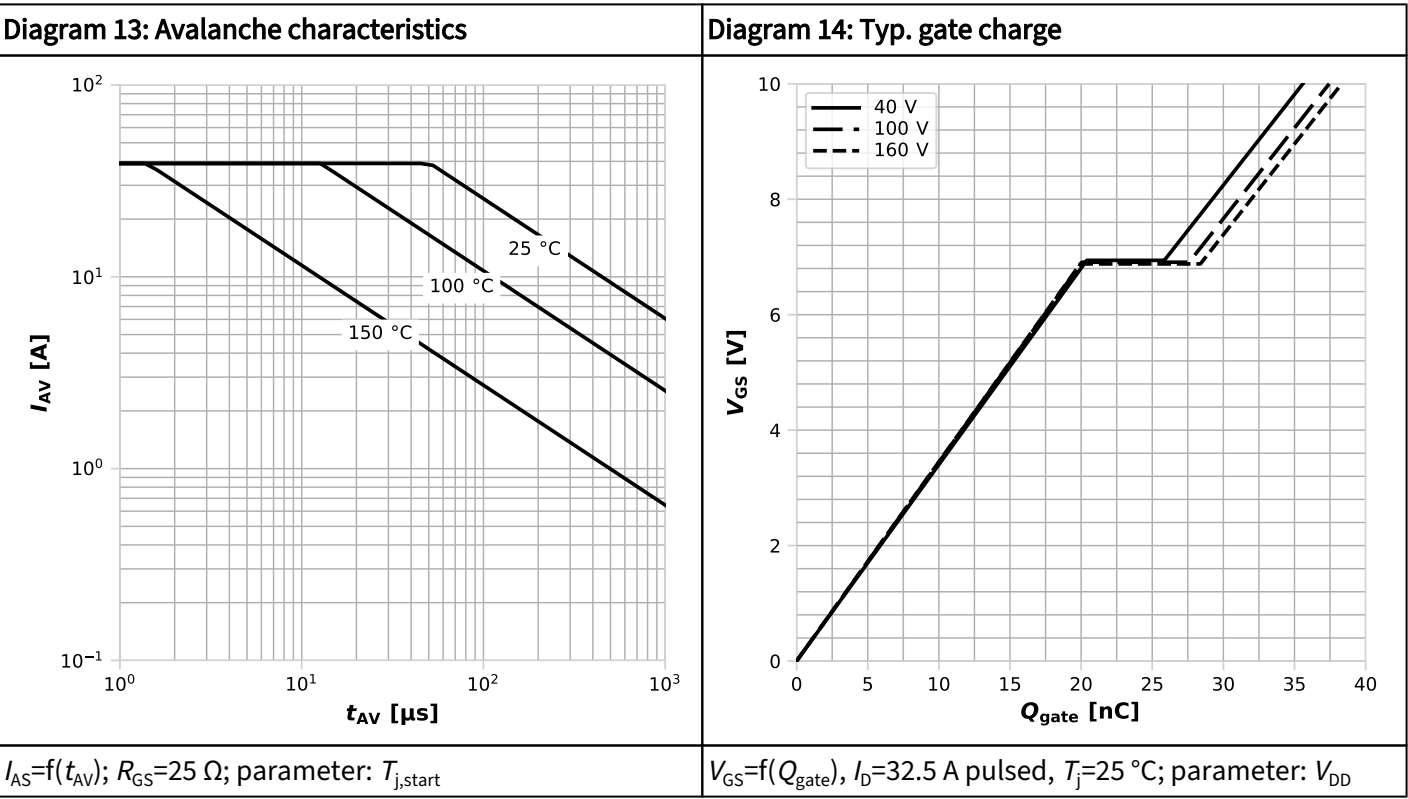


$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



$$I_F = f(V_{SD}); \text{ parameter: } T_j$$



5 Package outlines

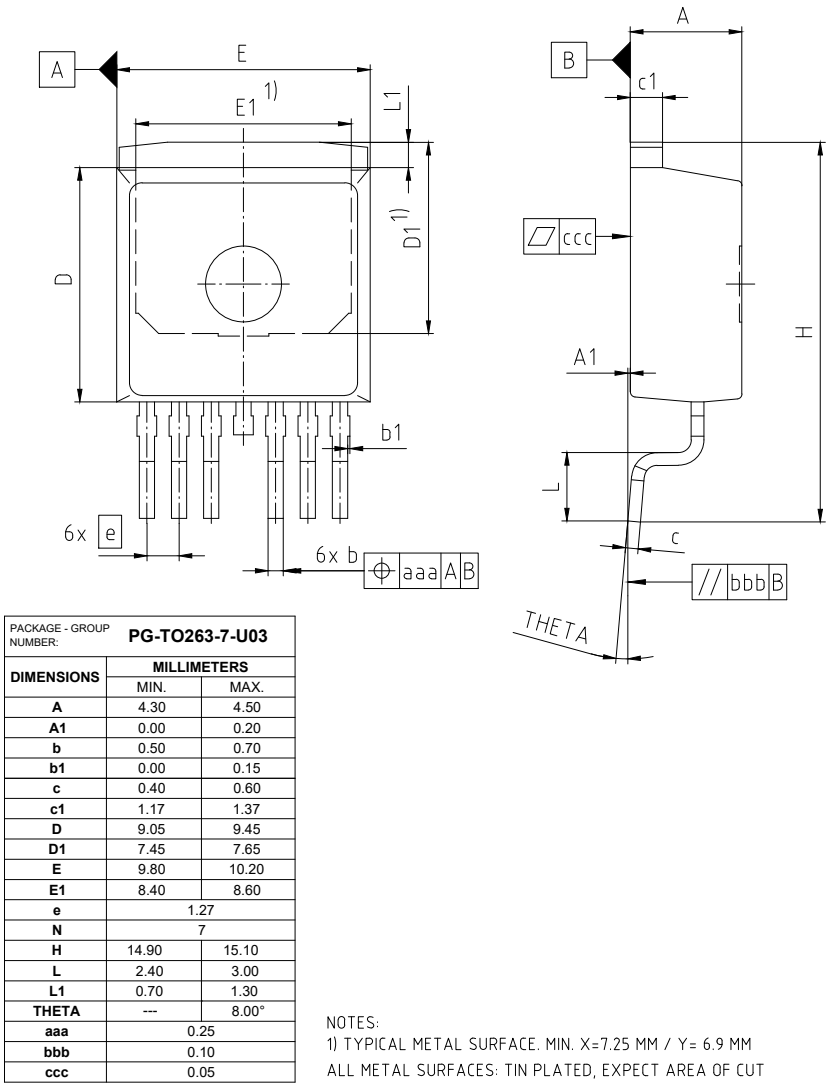
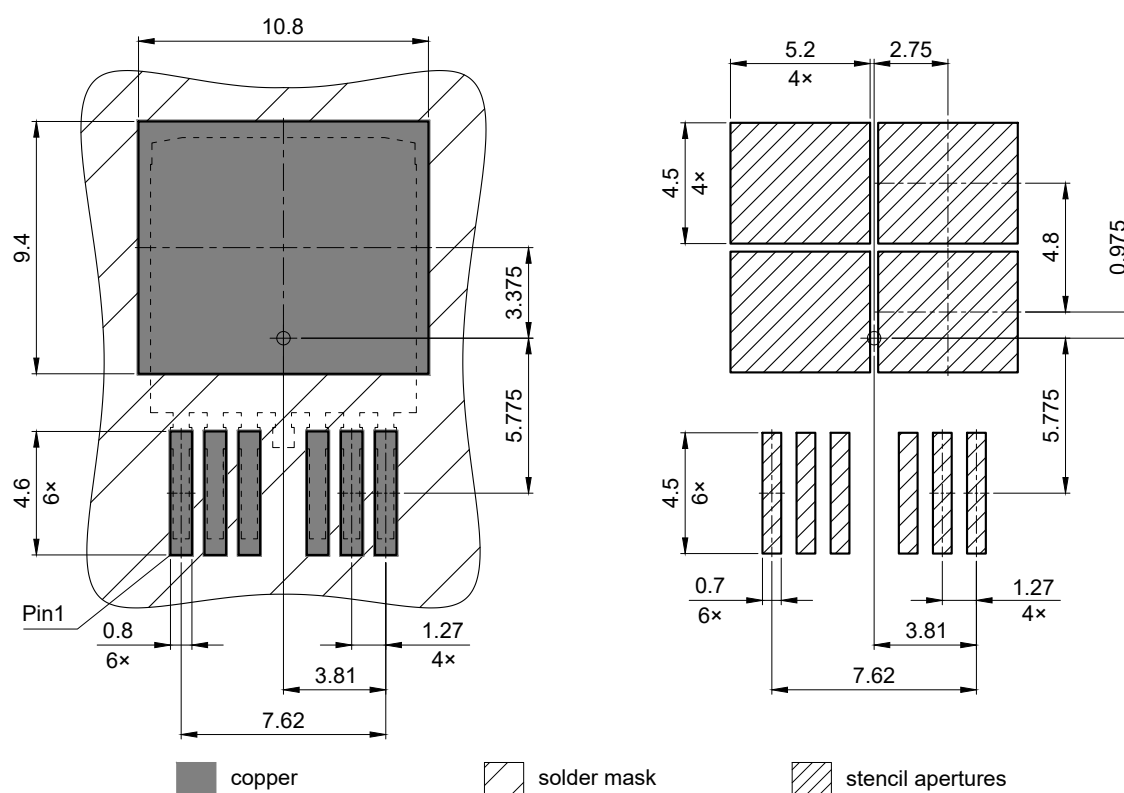


Figure 1 Outline PG-T0263-7, dimensions in mm



All dimensions are in units mm
 All pads are solder mask defined

Figure 2 Footprint drawing PG-T0263-7, dimensions in mm

Revision history

IPF129N20NM6

Revision 2025-11-27, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2023-12-07	Release of final version
2.1	2025-11-27	Update Rgext for timing and Qrr at di/dt=1000A/us

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