

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes to figures 1, 2, 3 and table I. Deleted vendor CAGE number 27014 from 5962-8953501KX and added to 5962-8953501LX. Editorial changes throughout.	90-11-06	W. Heckman
B	Changes IAW NOR 5962-R225-92. Replaced table I. - Itg	92-06-18	Tim Noh
C	Change paragraphs 3.1 and 3.5 to include QD statements. Upgrade document to reflect current requirements. Correct Test circuit on Figure 5. Editorial changes throughout. - les	02-01-30	Raymond Monnin
D	Update drawing to current requirements. Editorial changes throughout. - gap	09-03-18	Robert M. Heber

The original first sheet of this drawing has been replaced.

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PMIC N/A				PREPARED BY Larry T. Gauder					DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dscc.dla.mil																					
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE				CHECKED BY Tim H. Noh																										
				APPROVED BY William K. Heckman																										
				DRAWING APPROVAL DATE 89-09-12																										
				REVISION LEVEL D					SIZE A	CAGE CODE 67268		5962-89535																		
AMSC N/A									SHEET 1 OF 13																					

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89535	01	K	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F657	Octal bi-directional transceiver with 8-bit parity generator/checker and three state outputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or GDFP3-F24	24	Flat
L	GDIP3-T24 or GDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage	-0.5 V dc minimum to +7.0 V dc maximum
DC input voltage range	-0.5 V dc minimum to +7.0 V dc maximum
DC input current range	-30 mA minimum to +5.0 mA maximum
Voltage applied to output in high output state	-0.5 V dc to +5.5 V dc
Current applied to output in low output state:	
A ₀ - A ₇	40 mA
B ₀ - B ₇ PARITY, ERROR	96 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D) per device 2/	1.15 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ _{JC})	See MIL-STD-1835
Junction temperature (T _J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V _{CC})	+4.5 V dc to +5.5 V dc
Maximum input clamp current (I _{IC})	-18 mA
Minimum high level input voltage (V _{IH})	2.0 V dc
Maximum low level input voltage (V _{IL})	0.8 V dc
Case operating temperature range (T _C)	-55°C to +125°C

1/ Unless otherwise specified, all voltages are referenced to ground.

2/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer's QM plan, the "QD" certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE I. Electrical performance characteristics.

Test		Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	All outputs	V _{OH}	V _{CC} = 4.5 V, V _{IH} = 2.0 V, V _{IL} = 0.8 V	I _{OH} = -2.0 mA	1, 2, 3	2.4		V
				I _{OH} = -1.0 mA		2.5		
	B ₀ - B ₇ , PARITY, ERROR			I _{OH} = -12 mA	1, 2, 3	2.0		V
Low level output voltage	A ₀ - A ₇	V _{OL}	V _{CC} = 4.5 V, V _{IH} = 2.0 V, V _{IL} = 0.8 V	I _{OL} = 20 mA	1, 2, 3		0.50	V
	B ₀ - B ₇ , PARITY, ERROR			I _{OL} = 48 mA	1, 2, 3		0.55	V
Input clamp voltage		V _{IC}	V _{CC} = 4.5 V, I _{IC} = -18 mA		1, 2, 3		-1.2	V
High level input current	ODD/ $\overline{\text{EVEN}}$	I _{IH}	V _{CC} = 5.5 V	V _{IN} = 2.7 V	1, 2, 3		20	μA
	T/ $\overline{\text{R}}$, $\overline{\text{OE}}$						40	
	A ₀ - A ₇			V _{IN} = 5.5 V			2.0	mA
	B ₀ - B ₇						1.0	
	T/ $\overline{\text{R}}$, $\overline{\text{OE}}$, ODD/ $\overline{\text{EVEN}}$		V _{CC} = 0.0 V	V _{IN} = 7.0 V	1, 2, 3		100	μA
Low level input current	ODD/ $\overline{\text{EVEN}}$	I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V		1, 2, 3		-20	μA
	T/ $\overline{\text{R}}$, $\overline{\text{OE}}$						-40	
Off-state output high current	A ₀ - A ₇	I _{OZH}	V _{CC} = 5.5 V, V _{IH} = 2.0 V, V _{OUT} = 2.7 V		1, 2, 3		100	μA
	B ₀ - B ₇ , PARITY						70	
	ERROR						50	
Off-state output low current	A ₀ - A ₇	I _{OZL}	V _{CC} = 5.5 V, V _{IH} = 2.0 V, V _{OUT} = 0.5 V		1, 2, 3		-100	μA
	B ₀ - B ₇ , PARITY						-70	
	ERROR						-50	
Output short-circuit current	A ₀ - A ₇	I _{OS}	V _{CC} = 5.5 V <u>1/</u>		1, 2, 3	-60	-150	mA
	B ₀ - B ₇					-100	-225	
Supply current		I _{CC} H	V _{CC} = 5.5 V		1, 2, 3		125	mA
		I _{CC} L					150	
		I _{CC} Z					145	
Functional testing			See 4.3.1c		7, 8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, A _n to B _n , B _n to A _n	t _{PLH1}	C _L = 50 pF, R _L = 500 Ω, See figure 3	V _{CC} = 5.0 V	9	2.5	8.0	ns
			V _{CC} = 4.5 V to 5.5 V	10, 11	2.5	9.5	ns
	t _{PHL1}		V _{CC} = 5.0 V	9	3.0	7.5	ns
	V _{CC} = 4.5 V to 5.5 V		10, 11	3.0	8.5	ns	
Propagation delay time, A _n to PARITY	t _{PLH2}		V _{CC} = 5.0 V	9	6.5	14.5	ns
			V _{CC} = 4.5 V to 5.5 V	10, 11	5.5	18.0	ns
	t _{PHL2}		V _{CC} = 5.0 V	9	6.5	15.5	ns
			V _{CC} = 4.5 V to 5.5 V	10, 11	5.5	20.5	ns
Propagation delay time, ODD/ <u>EVEN</u> to PARITY, <u>ERROR</u>	t _{PLH3}	V _{CC} = 5.0 V	9	4.5	11.5	ns	
		V _{CC} = 4.5 V to 5.5 V	10, 11	4.0	14.0	ns	
	t _{PHL3}	V _{CC} = 5.0 V	9	4.5	12.5	ns	
		V _{CC} = 4.5 V to 5.5 V	10, 11	4.0	16.5	ns	
Propagation delay time, B _n to <u>ERROR</u>	t _{PLH4}	V _{CC} = 5.0 V	9	8.0	21.5	ns	
		V _{CC} = 4.5 V to 5.5 V	10, 11	7.0	26.0	ns	
	t _{PHL4}	V _{CC} = 5.0 V	9	8.0	22.5	ns	
		V _{CC} = 4.5 V to 5.5 V	10, 11	7.0	28.0	ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, PARITY to $\overline{\text{ERROR}}$	t _{PLH5}	C _L = 50 pF, R _L = 500 Ω, See figure 3	V _{CC} = 5.0 V	9	6.5	16.0	ns
			V _{CC} = 4.5 V to 5.5 V	10, 11	6.0	20.0	ns
	t _{PHL5}		V _{CC} = 5.0 V	9	7.5	17.0	ns
			V _{CC} = 4.5 V to 5.5 V	10, 11	6.5	21.5	ns
Output enable time, $\overline{\text{OE}}$ to A _n , B _n , PARITY, $\overline{\text{ERROR}}$	t _{PZH}		V _{CC} = 5.0 V	9	3.0	8.0	ns
			V _{CC} = 4.5 V to 5.5 V	10, 11	2.5	11.0	ns
	t _{PZL}		V _{CC} = 5.0 V	9	4.0	10.0	ns
			V _{CC} = 4.5 V to 5.5 V	10, 11	3.5	13.5	ns
Output disable time, $\overline{\text{OE}}$ to A _n , B _n , PARITY, $\overline{\text{ERROR}}$	t _{PHZ}	V _{CC} = 5.0 V	9	1.0	8.0	ns	
		V _{CC} = 4.5 V to 5.5 V	10, 11	1.0	9.5	ns	
	t _{PLZ}	V _{CC} = 5.0 V	9	1.0	7.5	ns	
		V _{CC} = 4.5 V to 5.5 V	10, 11	1.0	8.5	ns	

1/ Not more than one output should be shorted at a time and the duration of the short circuit conditions shall not exceed one second.

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Case outlines	K and L	3
Terminal number	Terminal symbols	
1	T/\overline{R}	NC
2	A_0	A_5
3	A_1	A_6
4	A_2	A_7
5	A_3	$\text{ODD}/\overline{\text{EVEN}}$
6	A_4	$\overline{\text{ERROR}}$
7	V_{CC}	PARITY
8	A_5	NC
9	A_6	B_7
10	A_7	B_6
11	$\text{ODD}/\overline{\text{EVEN}}$	B_5
12	$\overline{\text{ERROR}}$	B_4
13	PARITY	GND
14	B_7	GND
15	B_6	NC
16	B_5	B_3
17	B_4	B_2
18	GND	B_1
19	GND	B_0
20	B_3	\overline{OE}
21	B_2	T/\overline{R}
22	B_1	NC
23	B_0	A_0
24	\overline{OE}	A_1
25		A_2
26		A_3
27		A_4
28		V_{CC}

FIGURE 1. Terminal connections.

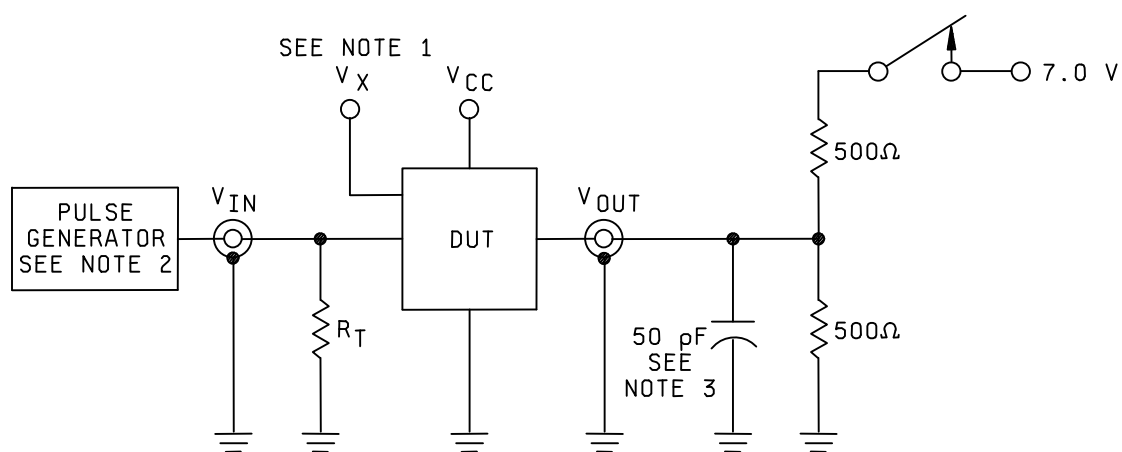
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Number of inputs that are high	Inputs			Input/output	Outputs	
	$\overline{\text{OE}}$	T/ $\overline{\text{R}}$	ODD/ $\overline{\text{EVEN}}$	PARITY	$\overline{\text{ERROR}}$	Outputs mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Irrelevant	H	X	X	Z	Z	Z

H = High voltage level
 L = Low voltage level
 Z = High impedance STATE
 X = Irrelevant

FIGURE 2. Truth table.

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Test	Switch Position
t_{PLZ}	Closed
t_{PZL}	Closed
All others	Open

NOTES:

1. V_X = Unused pins must be held at ≤ 0.8 , ≥ 2.7 V or open.
2. All input pulses have the following characteristics: PRR = 1.0 MHz, pulse width = 500 ns, duty cycle = 50%, $t_r = t_f \leq 2.5$ ns.
3. C_L includes probe and jig capacitance..
4. R_T = Termination resistance and should be equal to Z_{OUT} of the pulse generators.

FIGURE 3. Test circuit and switching waveforms.

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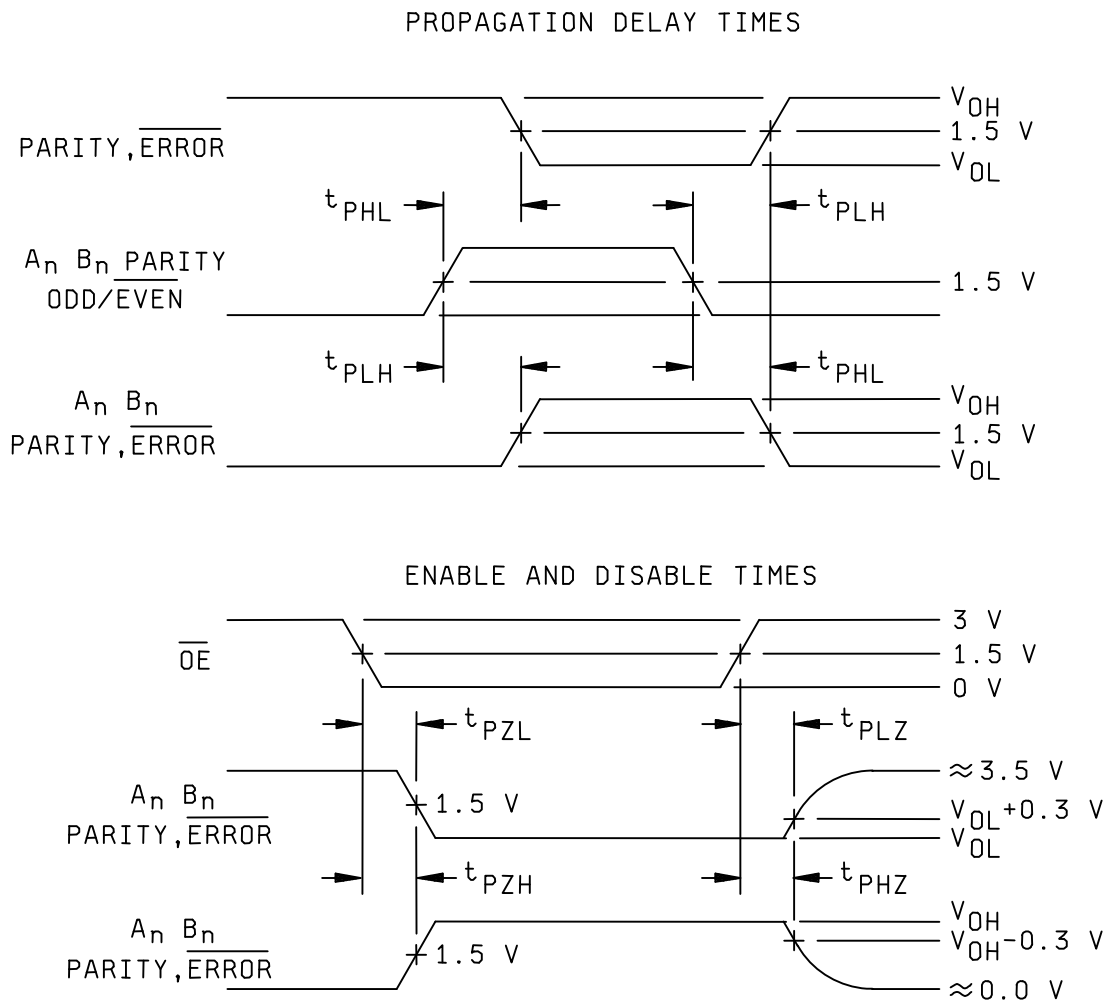


FIGURE 3. Test circuit and switching waveforms - Continued.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-03-18

Approved sources of supply for SMD 5962-89535 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8953501KA	0C7V7	54F657
	<u>3/</u>	54F657/BKA
5962-8953501LA	0C7V7	54F657
	<u>3/</u>	54F657/BLA
	<u>3/</u>	54F657/SDMQB
5962-89535013A	0C7V7	54F657
	<u>3/</u>	54F657/B3A

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE
number

Vendor name
and address

0C7V7

QP Semiconductor
2945 Oakmead Village Court
Santa Clara, CA 95051

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