USER GUIDE

UG499: Si828x-xW-GDB Gate Driver Boards

Introduction

The Si828x Gate Driver Boards (GDB) are ideal for driving Wolfspeed's XM3 1200 V and 1700 V Half Bridge Power Modules or other parallel combinations of discrete transistors. This two-channel isolated gate driver reference design in a half-bridge configuration features a differential digital interface, optimized on-board isolated power supply, DESAT protection, gate drive current boost, and user-configurable turn-on (RH) and turn-off (RL) gate resistors. Status indicator LEDs and test points make evaluation and prototyping easy. There are two variations of the gate driver boards that support SiC MOSFET modules with different gate terminal connections (parallel or cross-pin connections).

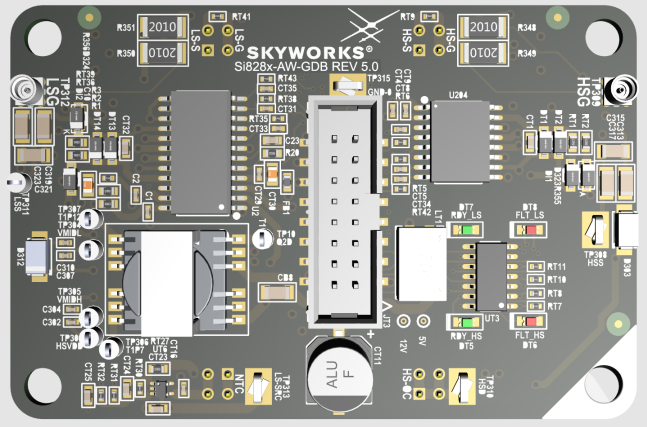


Figure 1. Si828x Gate Driver Board (GDB)

Key Features

- Two digital gate drivers for high-side/low-side operation
- Up to +20 A, -30 A peak output current with integrated boost circuit
- Independent control of turn on/turn off timing through gate resistor selection
- Isolated power supplies
- 5 kVRMS safety rated isolation
- 125 kV/µs common mode transient immunity (CMTI)
- Reverse polarity protection for 12 V input supply
- Differential inputs for increased noise immunity
- DESAT detection and soft-shutdown for short-circuit protection
- Gate supply ready indicator
- Module temperature (NTC) output as frequency modulated digital signal

Additional System Components

The Si828x GDB is highly versatile and can be combined with Wolfspeed's CIL boards and CGD12HB00D transceiver board to provide platforms to evaluate gate driver and SiC device combinations. The Si828x GDB is also designed to operate in Wolfspeed's 300 kW Three-Phase Inverter platform, where three Si828x-AW-GDB provide all gate drivers necessary to drive the XM3 power modules.

Tested Components (Not Included in KITs)

- **Evaluation Tool for the 1.2 kV XM3 Module Platform**
- **CAB450M12XM3 Power Module**
- **Evaluation Tool for the 1.7 kV Module Platform**
- **CAB320M17XM3 Power Module**
- **Differential Transceiver Daughter Board**

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1. System Overview

The Skyworks Si828x-xW-GDB are printed circuit reference designs suitable for interfacing to Wolfspeed XM3 power modules. The boards contain isolated gate drive functions for high-side and low-side transistors in a half-bridge module configuration, with gate biasing, isolated power supply, and fault indication. Figure 2 shows an Si828x-xW-GDB functional diagram. The Si828x-AW-GDB (1200 V compatible) is included in the Si828x-AAWB-KIT, and the Si828x-BW-GDB (1700 V compatible) is included in the Si828x-BAWB-KIT.

An I/O header (JT3) provides access to the differential high-side and low-side control signals as well as differential fault indicator and temperature sensor outputs. It also exposes single-ended inputs for power supply disable, transceiver enable, and driver reset.

A digital transceiver converts the differential high-side and low-side PWM control signal inputs to the single-ended high-side and low-side gate drive control signals. The transceiver also converts a frequency-encoded NTC (Negative Temperature Coefficient) sensor output into a differential RTD signal and a single-ended signal representing the combined fault signals and ready signals from the high-side low-side gate drivers into a differential fault signal.

There are two gate drivers on the Si828x-xW-GDB, and they both have complementary NPN/PNP transistor current booster circuits to drive the XM3 modules sufficiently. The Si8285 drives the high-side switching device, while the Si8284 drives the low-side. Both drivers have a DESAT sensing pin to detect switch desaturation. A soft shutdown circuit controls the rate of the switch turn-off if desaturation is detected to minimize the VDS voltage spike. Desaturation faults are indicated via the /FLT pin. Operation is restored by toggling the /RST pin via the Reset signal on the JT3 I/O header. The Si828x gate driver circuits include an enhanced Miller Clamp feature to maintain switch turn-off in the presence of high slew rate drain/collector or source/emitter signals.

Loss of gate drive supply results in a loss of the RDY signal both on the RDY pin and the combined differential /FLT output at the header, but RDY is restored when the gate drive supply is restored.

The Si8284x also has a dc-dc controller function. This controller drives an external NMOS switch on the primary side of the power transformer. The secondary side of the transformer forms both high and low-side driver supplies. These supplies are +15 Vdc and –3.5 Vdc with a return between them and provide a total of 5 W between high and low-side sections. The high side supplies are isolated from the low side supplies by the transformer. The dc-dc controller function may be shut down via the PS-DISb input on the I/O header.

High-side isolated gate drive is achieved by the Si8285 Isolated Gate Driver. This device and its associated circuit provide the same function as the Si8284 but without the dc-dc controller.

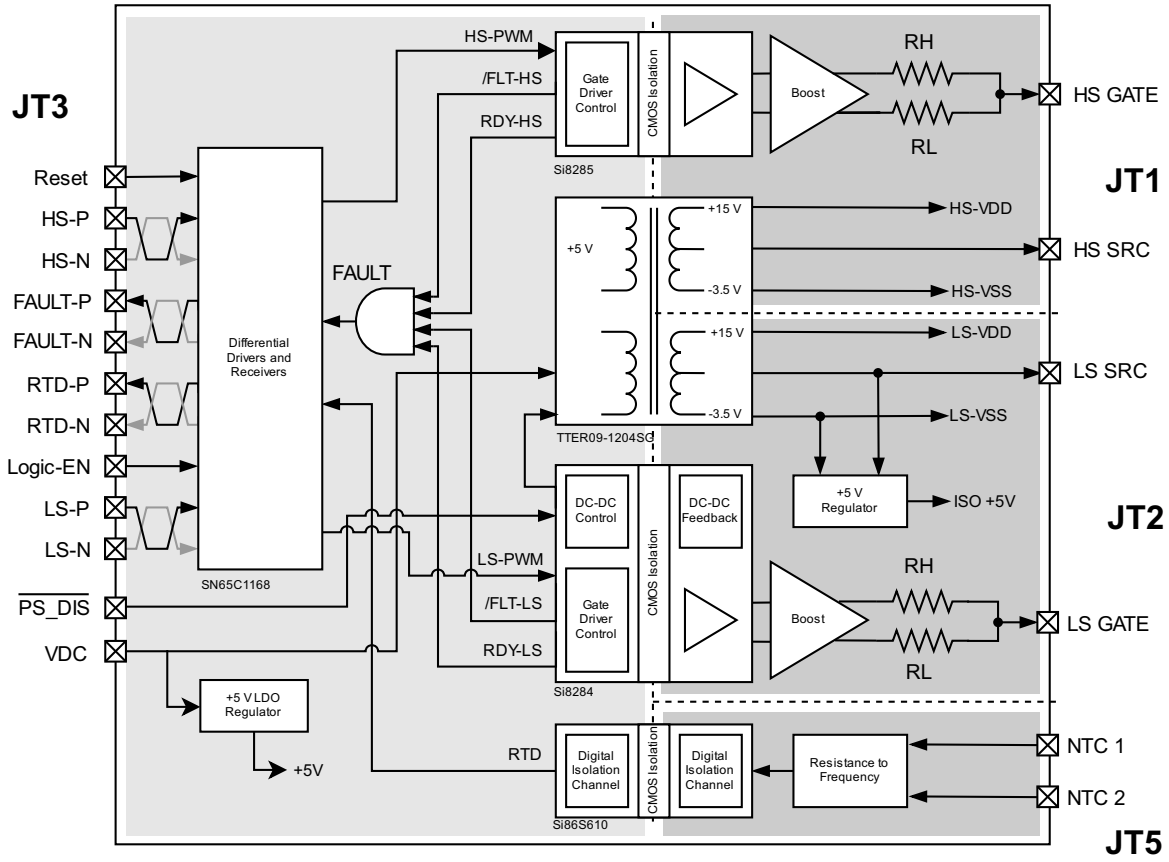
The dc power input to the board is protected from a reverse polarity connection via the P channel MOSFET gate biasing voltage UB2.

An RTD connector provides the connection to an external NTC (negative temperature coefficient) resistive sensor for measurement of switch module temperature. The RTD resistance is converted to a frequency that is then isolated and sent to the differential transceiver, which is converted to a differential signal accessed via the I/O header.

The **AN1362: Si828x XM3 Gate Driver Test Report** provides more detailed information and a complete schematic of the Si828x-xW-GDB. It also includes test setup and performance data of the operations between the Si828x gate drivers and the XM3 SiC modules on the **Evaluation Tool for the XM3 Module Platform.**

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Functional Block Diagram



To lab bench equipment: 12V power supply, single-end PWM, indication, and control signals



To JT3 Differential Signals

Figure 2. Functional Block Diagram and Differential Transceiver Daughter Card

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2. Pin Descriptions

2.1. Input I/O Connector (Low-Voltage JT3)

This connector is located in the center of the Si828x-xW-GDB. In the **XM3 Evaluation Tool** test setup, the JT3 connector provides the I/O interface connections across the **Differential Transceiver Daughter Board Companion Tool** to the lab bench instrumentations including power supply, function generator, control signals, etc. In the **XM3 Inverter Reference Design**, the JT3 connector provides direction connection to the control board, enabling the evaluation of the Si828x-xW-GDB in high power inverter applications. Table 1 provides a complete list of the signals in the JT3 connector.

Table 1: Input I/O Connector (Low Voltage JT3)

Pin Number	Parameter	Description
1	VDC	Power supply input pin (+12 V Nominal Input)
2	Common	Common
3	HS-P	Positive line of 5 V differential high-side PWM signal pair. Terminated Into 120 Ω
4	HS-N	Negative line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω
5	LS-P	Positive line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω
6	LS-N	Negative line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω
7	FAULT- P	Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA. A low state on FAULT indicates when a desaturation fault has occurred. The presence of a fault precludes the gate drive output from going high.
8	FAULT- N	Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA. A low state on FAULT indicates when a desaturation fault has occurred. The presence of a fault precludes the gate drive output from going high.
9	RTD-P	Positive line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via frequency.
10	RTD-N	Negative line of 5 V temperature dependent resistor output signal pair. Drive strength 20mA. Temperature measurement is encoded via frequency.
11	PS-DIS	Pull down to disable power supply. Pull up or leave floating to enable. Gate and source are connected with 10 kΩ when disabled.
12	Common	Common
13	PWM EN	Pull down to disable PWM input logic. Pull up or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled.
14	Common	Common
15	RESET	When a fault exists, bring this pin high to clear the fault.
16	Common	Common
Note: Inputs 3 to 10 are differential pair.		

- **PWM Signals:** High-side and low-side PWM are RS-422 compatible differential inputs. The termination impedance of the differential receiver is 120 Ω.
- **FAULT Signal:** The fault signal is an RS-422 compatible differential output with a maximum drive strength of 20mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. This signal will be low if an overcurrent fault or UVLO fault condition is detected on either channel. A red LED will indicate a fault condition. The LED, DT6, indicates a high-side fault and DT8 indicates a low-side fault.
- **UVLO Fault:** The UVLO circuit detects when the output rails of the isolated DC/DC converter fall below safe operating conditions for the gate driver. A UVLO fault indicates that the potential between the split output rails has fallen below the UVLO active level. The gate for the channel where the fault occurred will be pulled low through RG for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. There is hysteresis for this fault to ensure safe operating conditions. The UVLO faults for both channels are combined along with the over-current fault in the FAULT output signal. When there is no UVLO fault present, a green LED indicates a power good state. The LED, DT5, indicates a high-side power good status and DT7 indicates a low-side power good status.

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- **Over-Current Fault:** An over-current fault is an indication of an over-current event in the SiC power module. The over-current protection circuit measures the drain-source voltage, and the fault will indicate if this voltage has risen above a level corresponding to the safe current limit. When a fault has occurred the corresponding gate driver channel will be disabled, and the gate will be pulled down through a soft-shutdown resistor, RSS. The drain-source limit can be configured through on-board resistors. The over-current fault is latched upon detection and must be cleared by the user with a high pulse of at least 500 ns on the RESET signal.
- **RTD (NTC):** RTD output is a differential signal that returns the resistance of the temperature sensor (NTC) integrated into XM3 modules. The signal is a frequency modulated signal that encodes the resistance of the temperature sensor. The approximate temperature of the module can be determined from this resistance. See the section RTD (NTC) Temperature Feedback for further details.
- **PS-DISb:** The PS-DISb signal disables the output of the isolated DC/DC converters for the two channels. It is a single-ended input that must be pulled low to turn off the power supplies. With the power supplies disabled the gate will be held low with a 10 kΩ resistor. This signal can be used for startup sequencing.
- **PWM-EN:** This is a single-ended input that enables the PWM inputs for both channels. When this signal is pulled down the differential receivers for both channels are disabled and the gates will both be pulled low through R_G-OFF. All protection circuitry and power supplies will continue to operate including FAULT and RTD outputs.
- **RESET:** This single-ended input clears a desaturation-induced fault state, allowing PWM inputs to function as soon as RESET is released. When the signal is set high, FAULT will assume a high state if there are no UVLO conditions. The signal should be returned to low in order to operate the device.
- **Over-Voltage and Reverse Polarity Protection:** Power input on pin 1 is protected against connecting a power source with over-voltage or reverse polarity; there is a diode and a Zener diode across the power input, and a MOSFET in-line with the power input.

2.2. Module Connectors (High-Voltage)

These connectors are located at the bottom of the Si828x-xW-GDB and provide direct connections to the Wolfspeed XM3 SiC half-bridge modules. Table 2 lists the locations of signals on the module connectors. The main differences between the Si828x-AW-GDB and Si828x-BW-GDB are in the patterns of the pin connections on JT1 and JT6. These patterns correspond to the gate terminal connections of the CAB450M12XM3 and CAB320M12XM3, respectively.

Table 2: Module Connectors (High Voltage)

Connector Reference	Si828x-AW-GDB Connector Pin(s)	Si828x-BW-GDB Connector Pin(s)	Signal Name	Description
JT1	2, 4	2, 3	HS-Gate	High-side gate lead of switch module
JT1	1, 3	1, 4	HS-Source (LS-Drain)	High-side source lead of switch module; primary output
JT2	1, 2, 3, 4	1, 2, 3, 4	HS-Drain	High-side drain lead of switch module
JT6	2, 4	2, 3	LS-Gate	Low-side gate lead of switch module
JT6	1, 3	1, 4	LS-Source	Low-side source lead of switch module
JT5	1, 3	1, 3	RTD-1	Lead 1 of switch module resistive temperature sensor
JT5	2, 4	2, 4	RTD-2	Lead 2 of switch module resistive temperature sensor

- **HS-Gate:** The high-side gate pin is driven by the Si8285 Isolated Gate Driver IC and external BOM circuitry meant to enhance the drive, soft shutdown, and Miller clamp functions for higher gate capacitance switch devices / arrays.
- **HS-Source:** The high-side source pin is connected to the VMID-H supply and the low-side DESAT detection circuit.
- **HS-Drain:** The high-side drain pin is connected to the high-side DESAT detection circuit.
- **LS-Gate:** The low-side gate pin is driven by the Si8284 Isolated Gate Driver IC and external BOM circuitry meant to enhance the drive, soft shutdown, and Miller clamp functions for higher gate capacitance switch devices / arrays.
- **LS-Source:** The low-side source pin is connected to the VMID-L supply.
- **RTD-1 and RTD-2:** The RTD pins connect to a resistive temperature sensor in the switch device / module. The resistance is sensed and converted to a frequency which is then sent across an isolation barrier to the digital transceiver and out the I/O connector.

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3. Truth Table

Table 3 is the truth table of input-to-output signals under various operating conditions.

Table 3: Si828x-xW-GDB I/O Truth Table

HS-PWM	LS-PWM	PWM-EN[2]	PS-DIS[4]	Reset_Input[3]	Overcurrent UVLO	FAULT[8]	HS-Gate	LS-Gate	Output (HS-Source/LS-Drain)
L	L	H or Z	H or Z	L or Z	No	H	L	L	Z
L	H	H or Z	H or Z	L or Z	No	H	L	H	L
H	L	H or Z	H or Z	L or Z	No	H	H	L	H
H	H	H or Z	H or Z	L or Z	Yes[5]	L	H[9]	H[9]	Z[9]
X	X	L[6]	H or Z	L or Z	No	H	L	L	L
X	X	X	L7	X	No	L	L	L	Z
X	X	H or Z	H or Z	L or Z	Yes	L	L	L	Z[9]

Notes:
1. H = High | L = Low | X = Irrelevant | Z = High Impedance

2. PWM-EN is active high and has a pull up resistor on the input.

3. Reset_Input is active high and has a pull down resistor on the input.

4. PS-DIS\ is active low and has a pull up resistor on the input.

5. An Overcurrent condition is induced when both PWM inputs are high. This condition must be disallowed by external overlap protection.

6. A low on PWM-EN disables the outputs of the PWM receivers; they are pulled low by resistors in this case.

7. When PS-DIS\ is low, the gate driver output power supply is disabled. The HS-Gate and LS-Gate signals are pulled to their respective sources by resistors.

8. The FAULT output is active low; it goes low when there is an overcurrent / UVLO fault or a driver IC indicates a non-READY state.

9. When an overcurrent condition is induced, the gate signals are pulled low and the output becomes high-impedance after the fault condition is indicated by a driver chip.

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4. Gate Driver Connections

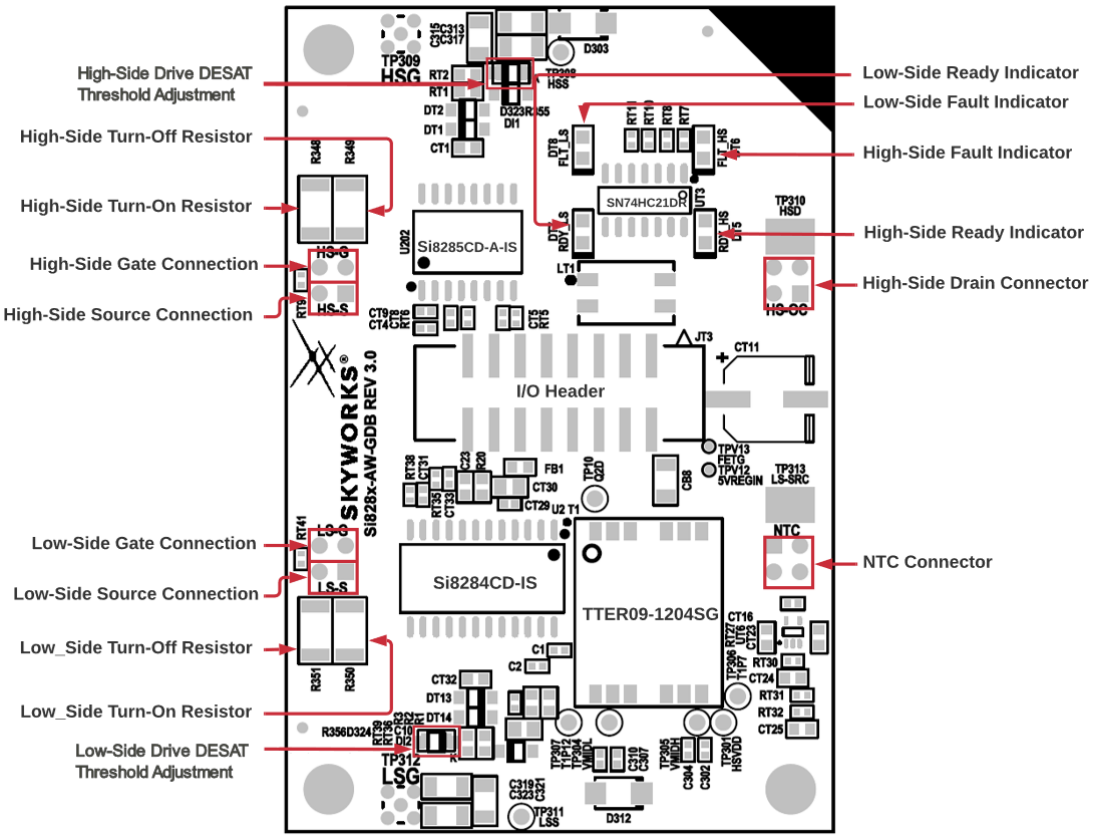


Figure 3. Si828x Gate Driver Board Top-Side Silkscreen

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5. Temperature Feedback

The XM3 power module uses a thermistor to provide temperature feedback to the controller. The resistance of the thermistor sensor is converted to a 50% duty cycle square wave with a frequency that varies inversely with the resistance. The resistance to frequency relationship is displayed in the Table 4 below. The resistance to frequency circuits is located on the high voltage side to provide direct connection to the XM3 thermistor sensor. Then, a digital isolator is used to transmit the frequency-encoded signal back to the primary side and its differential signals are connected to pin 9 and pin 10 of the JT3 low side connector.

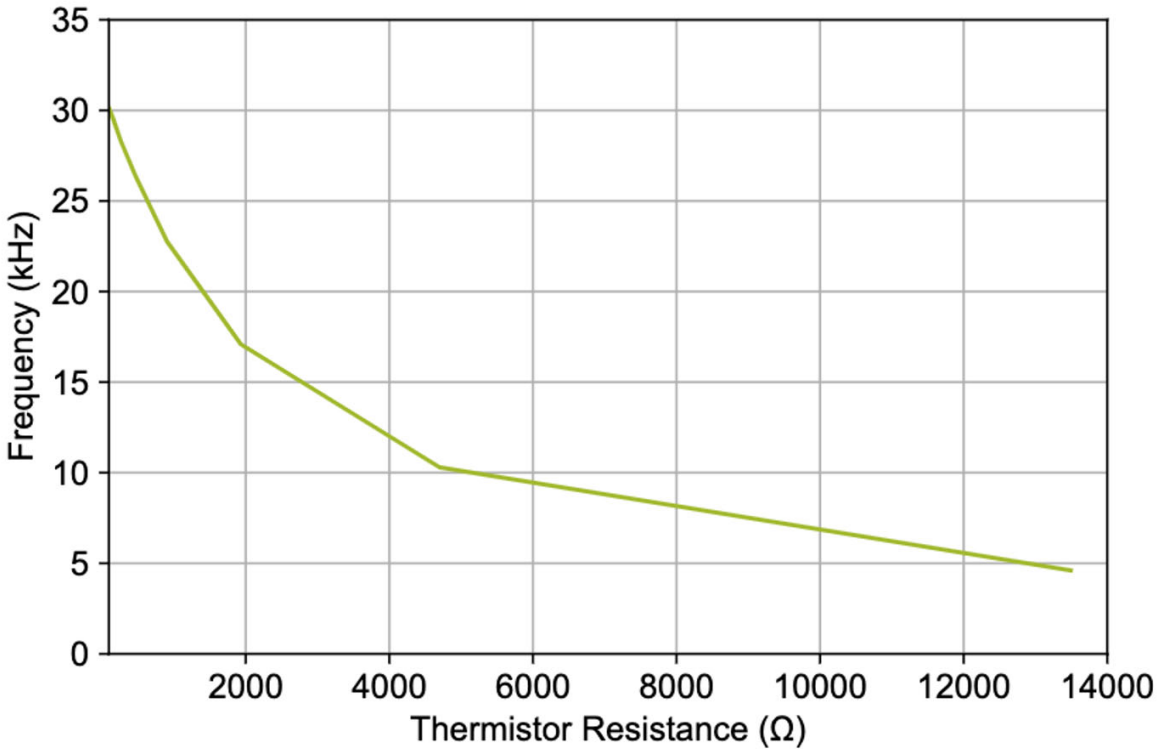


Figure 4. Thermistor Resistance vs Output Frequency

Table 4: Thermistor Resistance vs Output Frequency

Thermistor Resistance (Ω)	Frequency Output (kHz)
13491	4.6
4700	10.3
1928	17.1
898	22.8
464	26.4
260	28.3
156	29.5
99	30.1

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6. User Configuration Options

6.1. Series Gate Resistors

The Si828x-xW-GDB are populated at the factory with 1 Ω turn-on RH (R348, R350) and turn-off RL (R349, R351) to drive the XM3 module low-side and high-side switching devices. These gate resistors can be easily replaced to optimize the switching rate and minimize switching loss.

6.2. Negative Gate Bias

The default configuration of this driver board provides a gate drive signal that swings from +15 V to –4 V with respect to the VMID pin connection. Note that the VMID pin from the gate driver is connected to the Source terminals of the XM3 SiC devices, and since the Si828x are powered by the bipolar supplies, the gates of the XM3 SiC devices are driven positive to turn on and negative to turn off.

6.3. Isolated Driver Power Supply Voltage

The Si828x-xW-GDB uses a dc-dc converter integrated into the Si8284 gate driver. This converter regulates the output of one secondary of the transformer used in the application. The design of the transformer provides regulation of the other secondary winding to provide separate, isolated power supplies for both the high side and low side driver. The default configuration provides a driver power supply that is regulated to 19 V. Since the source pin of each channel is biased about 4 V above the converter's reference, the gate will see a voltage swing from +15 V to –4 V when measured with respect to the source pin.

The dc-dc converter may be operated with a different set of output voltages by changing the resistor divider (R1/R2+1) * 1.05V to obtain the desired supply voltage. The limit of VDDB - VSSB is 30V, and the VDDB/VSSB ratio is fixed by the turns ratios of transformer T1. Operating the device at a higher voltage may impair operation or damage the device.

6.4. Overcurrent/Desaturation Trip Level

The overcurrent (OC) fault detection circuit measures the on-state VDS voltage across each switch position and triggers a fault condition if the voltage rises above a set level. The internal comparator trip voltage in the Si828x gate driver IC is 7 V. Considering the forward voltage of the high-voltage blocking diodes and a tunable Zener diode, the overcurrent trip level is calculated with the following equation:

VOC-Trip = 7V - VZ - 2VF

where the forward voltage of the high-voltage diodes, VF, is approximately 0.5 V, and the Zener voltage, V_Z, included on the gate driver is 3.9 V (On Semi MMSZ4686T1G). As shipped, the Zener diode is replaced with a 0 Ohm resistor and the overcurrent trip level is 6 V. If it is desired to change the overcurrent trip level, the Zener diode should be in a SOD123 package such as the diodes in the MMSZ series from On Semi. The Zener diodes are labeled D323 and D324 on the PCB.

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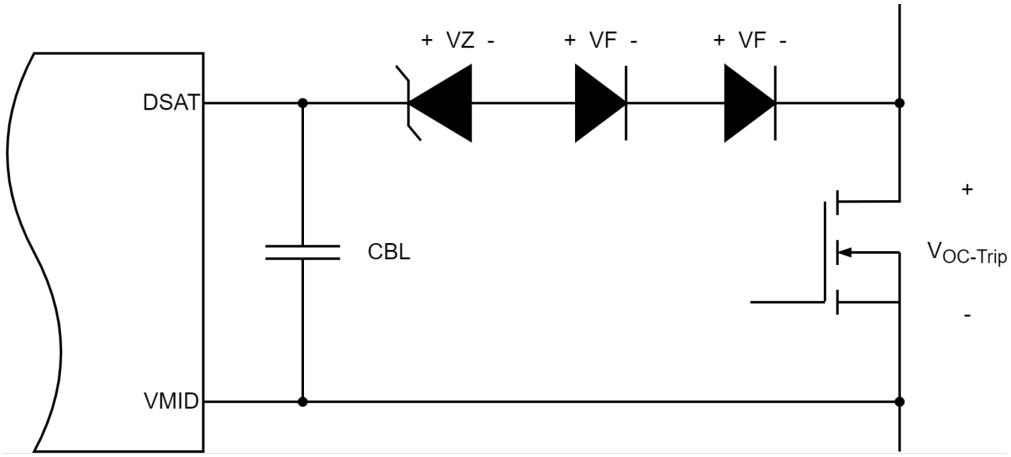


Figure 5. Over-Current Trip Level

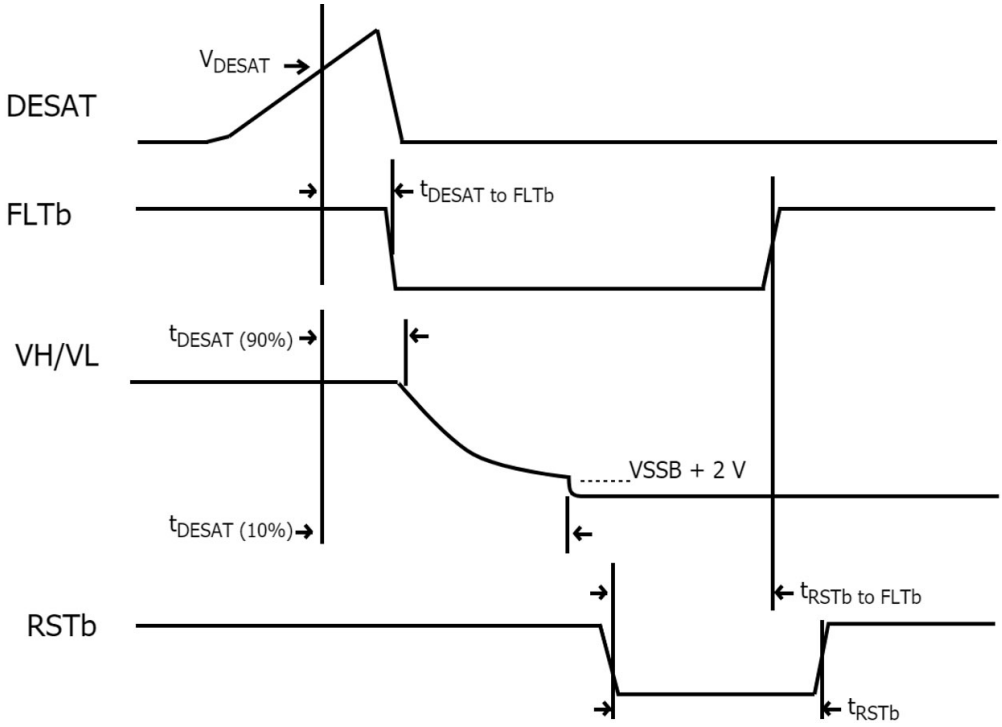


Figure 6. DESAT Behavior

To set an appropriate overcurrent trip level, see the module data sheet for the ID vs. VDS output characteristic curves. For example, the pulse-current rating of the CAB450M12XM3 is 900 A at TJ = 25 °C; it follows that an overcurrent trip point of 1000 A at 25 °C should be selected. The drain-to-source voltage at the 1000 A operating condition is approximately 3.0 V, as seen on the ID vs. VDS curve. From that, the overcurrent trip voltage, VOC-Trip, should be approximately 3.0 V. This trip voltage can be used to calculate the required Zener voltage, V_Z, with the equation above.

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Note that the HS-Drain connector, JT2, cannot be left floating because the over-current fault will trip immediately when the high-side gate is taken high. If bench testing of the gate driver is required without the XM3 module, one may short the HS-Drain connection to the high-side source to prevent the overcurrent fault from tripping. The low-side exhibits the same behavior, and one may short the high-side source (low-side drain) to the low-side source for bench testing. The Reset signal must be activated to acknowledge the over-current fault condition so as to return the gate driver to normal operation.

6.5. Si828x-xW-GDB - XM3 Test Circuits

The Si828x-xW-GDB is designed to operate with Wolfspeed's XM3 Evaluation Tool and the XM3 Three-Phase Inverter Demonstration Platform. The Si828x-xW-GDB was tested extensively with the XM3 module on the Wolfspeed's XM3 Evaluation Tool with excellent test results. The Si828x-AW-GDB fits directly to the gate driver slots of the XM3 Three Phase Demonstration Platform. The Si828x-BW-GDB is currently incompatible with Wolfspeed’s XM3 Three Phase Demonstration Platform. Below are the links to the documentation for test setup and test results.

- AN1362: Si828x XM3 Gate Driver Test Report
- 1.2 kV XM3 Evaluation Tool: KIT-CRD-CIL12N-XM3
- 1.7 kV XM3 Evaluation Tool: KIT-CRD-CIL12N-XM3
- Differential Transceiver Daughter Board
- XM3 Three-Phase Inverter Reference Design User Guide: AN30

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7. Dimensions

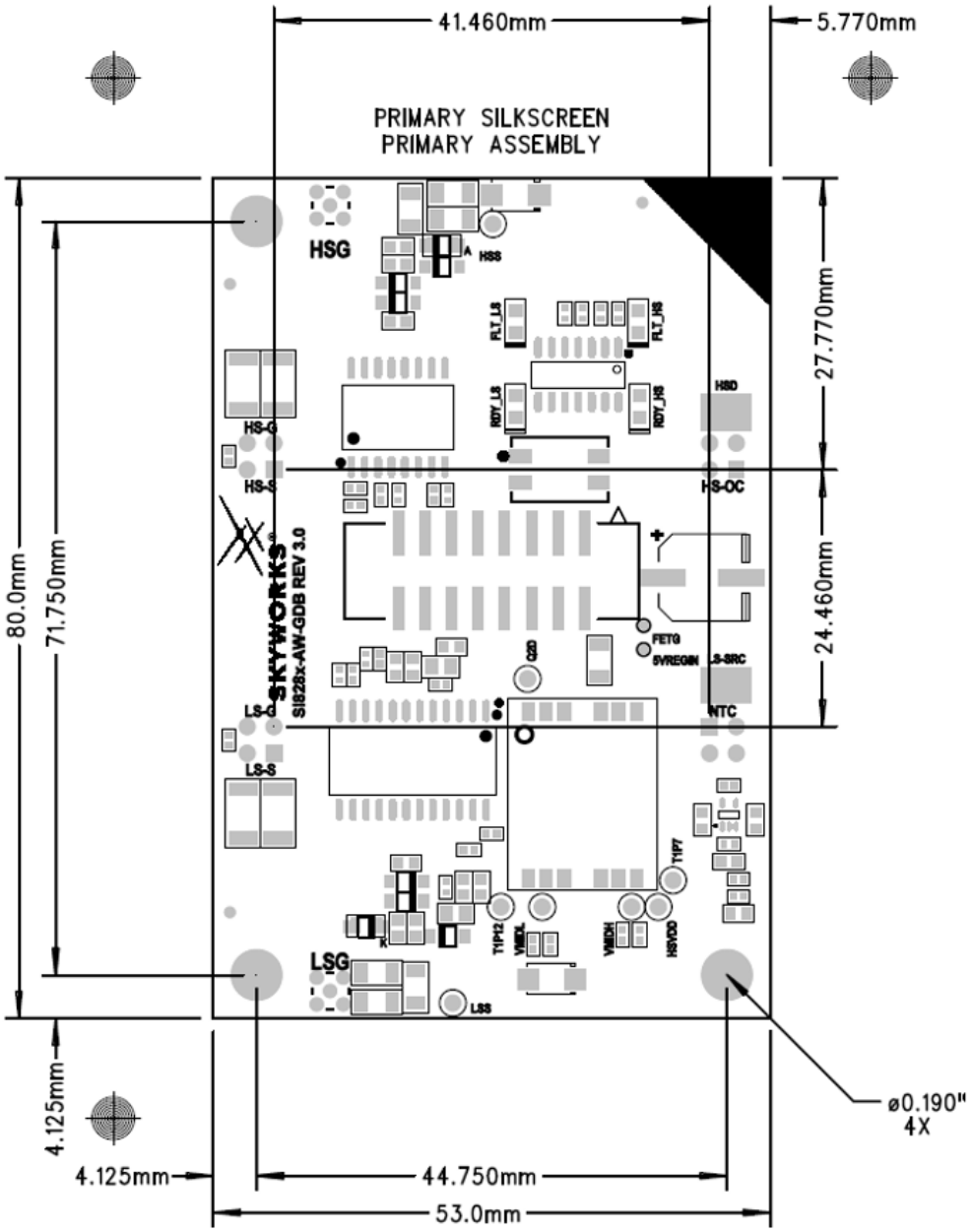


Figure 7. Si828x Gate Driver Board (GDB) Dimensions

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8. Ordering Information

Full schematic, BOM, and layout Gerber files are available for download at the KIT links listed below under Part Number.

Part Number	Part Description
Si828x-AAWB-KIT	KIT contains the 1200 V XM3 module compatible Si828x-AW-GDB evaluation board described in this document
Si828x-BAWB-KIT	KIT contains the 1700 V XM3 module compatible Si828x-BW-GDB evaluation board described in this document

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