Platform Manager 2 Evaluation Board User Guide

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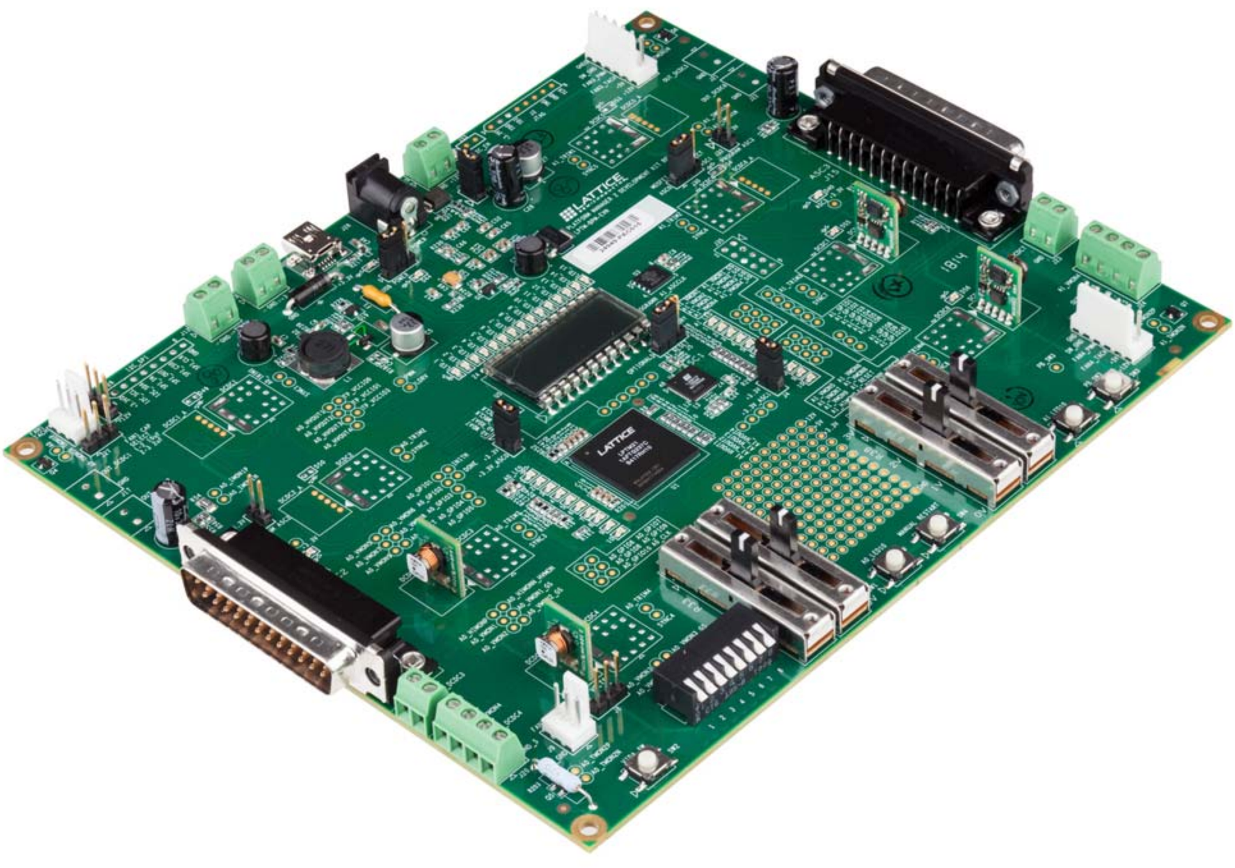


Introduction

Thank you for choosing the Lattice Semiconductor Platform Manager 2 Evaluation Board!

The Platform Manager 2 evaluation board is used to demonstrate, evaluate and design using the Platform Manager 2 (LPTM21) device and the Hardware Management Expander (L-ASC10) device. The board is pre-programmed with a demo design that highlights the features and flexibility of the LPTM21 and L-ASC10 devices. This demo operates on the board without any other software or hardware as described in the **QuickSTART Guide** that is included with the board. However, a more complete evaluation can be accomplished using the I^2C demo / debugging software which is available from the Lattice website. This software and the demo design can be used to evaluate the following features provided by the Platform Manager 2 devices: Power Management (Power Sequencing, Voltage Monitoring, Trimming, Margining), Thermal Management (Temperature Monitoring, Fan Control, Power Control) and Control Plane (Reset Control, Fault Logging). The use of the software with the demo design is fully described in the user guide which is included with the software zip file: UG59, *Platform Manager 2 I^2C Demo Design and GUI User's Guide*.

The QuickSTART Guide

Please use the Platform Manager 2 Board QuickSTART Guide to get started. The QuickSTART Guide provides a "fast path" for working with the Platform Manager 2 evaluation board and the pre-programmed demo. This user's guide augments the QuickSTART Guide by providing detailed descriptions of the on board circuits that support both the demo and customer evaluation designs.

Features

The Platform Manager 2 evaluation board has been designed to demonstrate and evaluate the following applications:

- Supply Voltage monitoring, sequencing, trimming, VID, and control.
- Current sensing, monitoring and control.
- Temperature sensing, monitoring and control.
- 3-Wire, 4 Wire Fan Control.
- Fault logging to internal UFM or external SPI Flash.
- Scalable monitoring and control of voltages, currents, temperatures.
- Field upgrades via background programming and dual boot.
- GPIO control and expansion.

The Platform Manager 2 evaluation board also allows the user to quickly learn, evaluate, develop and test their own designs using the LPTM21, L-ASC10 and surrounding circuits and components.

The Platform Manager 2 evaluation board contains the following on-board components and circuits to support the demo design and customer developed designs:

- **Integrated Circuits**
  - LPTM21 – FTBGA-237 – Platform Manager 2 [U1]
  - L-ASC10 – QFN-48 – Hardware Expander [U4]
  - AT25DF041AMH -SPI Flash Memory [U3]
  - FT2232HL- USB Driver [U6]
  - 93C46-WMN6TP –EEPROM Memory [U7]
  - NCP1117-LDO [U8]
  - LD6836-LDO [U9]
  - FSA4157 Analog Switch-SPDT [U10, U11]

- **Power Supplies, Connections and Switches**
  - External 12 V Supply Connector –Coaxial Power Jack [J28]
  - External 12 V Supply Connector – Two position Terminal [J25]
  - External 5 V Supply Connector – Two position Terminal [J12]
  - External 3 V Supply Connector – Two position Terminal [J13]
  - +5 V to 2.5 V Trim-able DCDC Converter [DCDC3, DCDC7]
  - +5 V to 1.2 V Trim-able DCDC Converter [DCDC4, DCDC8]
- **LEDs and LCD Display**
  - Blue USB Power LED [D42]
  - Green +3.3 V Power LED [D44]
  - Red LPTM21 (U1 ASC) Output LEDs [D3-D12]
  - Red LPTM21 (U1 FPGA) Output LEDs[D22-D36]
  - Red L-ASC10 (U4) Output LEDs [D13-D21]
  - 3-Digit LCD Display [U5]
  - Red ASC # 2 Interface Power LED [D39]
  - Red ASC # 3 Interface Power LED [D40]
  - Green DC-DC # 3 Power LED [D51]
  - Green DC-DC # 4 Power LED [D52]
  - Green DC-DC # 7 Power LED [D55]
  - Green DC-DC # 8 Power LED [D56]
- **Switches, Sliders, Buttons, Sensors and Jumper**s
  - VID_A 8-position DIP Switch [SW6]
  - Restart Push Button Switch [SW4]
  - Demo control Push Button Switch [SW1-SW3, SW5]
  - Slide Potentiometer [R34, R36, R39, R41]
  - Temperature Sensor [Q4, Q6, Q7]
  - Temperature Sensor [Q5-with artificial load power resistor]
  - 3.3 V supply select Jumper [J1, J3, J4]
  - Reset select Jumper [J5]
  - Fan Supply Select [J6, J8]
  - Enable ASC program Jumper [J31, J32]
  - MOSFET Drive Select [J30]
  - 5 V supply select jumper [J29]
- **Connectors and Interfaces**
  - JTAG connector [J2]
  - I^2C/SPI connector [J26]
  - External FAN connectors [J7, J9, J10, J11]
  - Two Position Screw connector for off board load for DCDC3 and DCDC7 [J19, J23]
  - Four position screw connector for off board load for DCDC4 and DCDC8 [J20, J24]
  - USB B-mini Connector [J16]
  - DSUB 25 Expandable Architecture Connectors for ASC Breakout Board [J14, J15]
  - Probe and Test Points
- **User Prototyping Area**
  - 12 x 10 through-Hole array with +12 V, +5 V, +3.3 V, and GND buses
  - 24 SMD 0805 footprints
  - 8 SMD SOT-23 footprints
  - 4 SMD 2512 footprints
  - 4 SMD SOIC-8 footprints
  - 2 SMD SOT-223 footprints

Mechanical Specifications

Dimensions: 7 in. [L] x 6 in. [W] x 1 in. [H]

Environmental Specifications

The evaluation board must be stored between –40 °C and 100 °C. The recommended operating temperature is between 0 °C and 55 °C.

Electrical Specifications

- 12 V Input +/– 15% @ 50 mA typical.
- 5 V Input +/– 10% @ 110 mA typical.
- 3.3 V Input +/– 5% @ 150 mA typical.
- 12 V Maximum Current 10 A when using an off board supply and load.
- 5 V Maximum Current 10 A when using an off board supply and load.
- 3.3 V Maximum Current 5 A when using an off board supply and load.

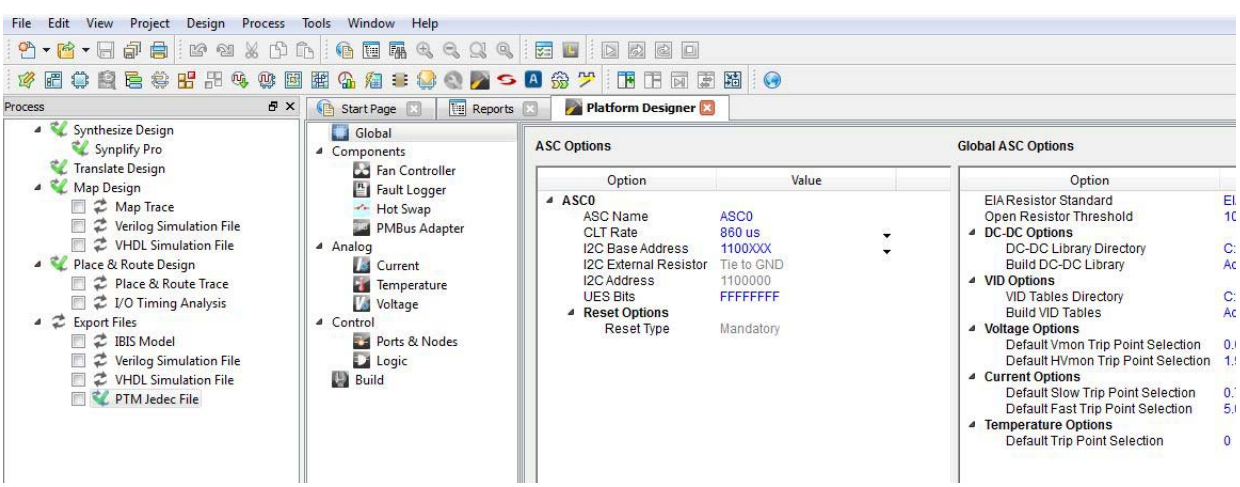
Software Requirements

The pre-loaded demo design on the Platform Manager 2 evaluation board can operate without the need to install any special software and can be powered using any standard USB port. All control and status information is available on the board using switches, push-buttons, potentiometers, LEDs and the LCD display, as described in the QuickSTART Guide that was mentioned in the introduction. In order to create and program custom designs or program reference or demo designs, Lattice Diamond 3.4 or later software is required along with a corresponding license. Within Lattice Diamond®, Platform Designer is a custom tool that is used to create, edit, and build Platform Manager 2 designs.

Platform Designer Tool-Software

The Platform Designer tool provides an integrated design environment that simplifies building and editing Platform Manager 2 designs. It supports all of the following and more: implement the hardware management algorithm, check design rules, compile the design, generate stimulus files, simulate the design, assign pins, and finally generate the JEDEC files used to program and configure the device on the circuit board. Platform Designer also supports the importing of an HDL file to integrate other desired functions.

Figure 1. Platform Designer Software



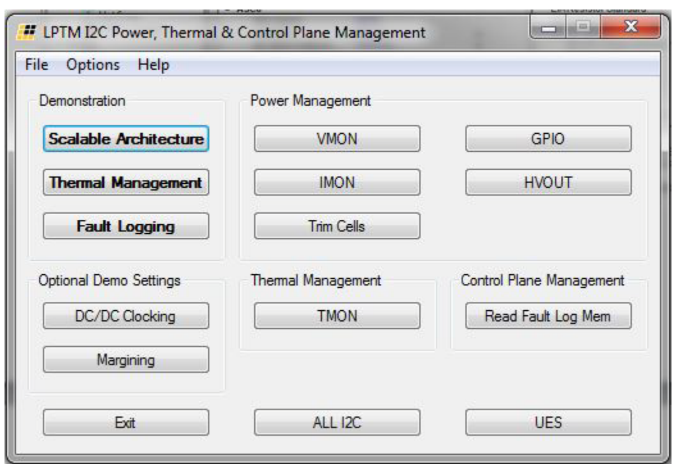
As shown in Figure 1, the Platform Designer tool contains five main sections: Global, Analog, Components, Control, and Build. Each of the five sections is briefly described below.

- **Global** – ASC Options and Device Options views are used for configuring global settings for the ASC and the device.
- **Analog** – Current, Temperature, and Voltage views are used for configuring the built-in monitoring circuits for these signals.
- **Components** – Fan Controller, Fault Logger, Hot Swap, and PMBus Adapter views are used to configure and instantiate built-in IPs for these functions.
- **Control** – Ports and Nodes and Logic views are used to name and assign I/O for the design; and to develop and/or import the control logic.
- **Build** – DRC, Compile, Pin Assignment, Generate Jedec, Generate Stimulus, and Export Configuration Report buttons are used for checking design rules, and building the design. A summary view shows the usage and consumption of the design resources available.

Platform Manager 2 I^2C GUI - Software

The Platform Manager 2 I^2C GUI software and User's Guide can be downloaded from the Lattice website. This software is provided license free and is used to enhance the demo experience and as a hardware debugging tool; the main interface is shown in Figure 2. The Demonstration buttons are used in conjunction with the default demo. The Power Management, Thermal Management, and Control Plane Management buttons can be used independently of the demo and can also be used with customer board designs (provided an FTDI based USB to I^2C interface is used).

Figure 2. Platform Manager 2 I^2C GUI Software



Platform Manager 2 Evaluation Board

LPTM21-Platform Manager 2-Device

As shown in Figure 3, the Lattice Platform Manager 2 device is a fast-reacting, programmable logic based hardware management controller. Platform Manager 2 is an integrated solution combining analog sense and control elements with scalable programmable logic resources. This unique approach allows Platform Manager 2 to integrate Power Management (Power Sequencing, Voltage Monitoring, Trimming and Margining), Thermal Management (Temperature Monitoring, Fan Control, Power Control), and Control Plane functions (System Configuration, I/O Expansion, etc.) as a single device.

Architecturally, the Platform Manager 2 device can be divided into two sections – Analog Sense and Control and FPGA. The Analog Sense and Control (ASC) section provides three types of analog sense channels: voltage (nine standard channels and one high voltage channel), current (one standard voltage and one high voltage) and temperature (two external and one internal).

Each of the analog sense channels is monitored through two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. In addition, each of the current sense channels provides a fast fault detect (one µs response time) for detecting short circuit events. The temperature sense channels can be configured to work with different external transistor or diode configurations.

The Analog Sense and Control section also provides ten general purpose 5 V tolerant open-drain digital input/output pins that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for general purpose logic interface functions. In addition, four high-voltage charge pumped outputs (HVOUT1-HVOUT4) may be configured as high-voltage MOSFET drivers to control high-side MOSFET switches. These HVOUT outputs can also be programmed as static output signals or as switched outputs (to support external charge pump implementation) operating at a dedicated duty cycle and frequency.

The ASC section incorporates four TRIM outputs for controlling the output voltages of DC-DC converters. Each power supply output voltage can be maintained typically within 0.5% tolerance across various load conditions using the Digital Closed Loop Control mode of the trimming block.

The internal 10-bit A/D converter can be used to measure the voltage and current through the I^{2}C bus. The ADC is also used in the digital closed loop control mode of the trimming block.

The ASC section also provides the capability of logging up to 16 status records into its nonvolatile EEPROM memory. Each record includes voltage, current and temperature monitor signals along with digital input and output levels.

The ASC section includes an output control block (OCB) which allows certain inputs and control signals a direct connection to the digital outputs or HVOUTs, bypassing the ASC-I/F for a faster response. The OCB is used to connect the fast current fault detect signal to an FPGA input directly. It also supports functions such as Hot Swap with a programmable hysteretic controller.

The FPGA section contains non-volatile low cost programmable logic of 1280 Look-Up Tables (LUTs). In addition to the LUT-based logic, the FPGA section features Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), flexible I/Os, and hardened versions of commonly used functions such as SPI controller, I^{2}C controller and Timer/counter. The FPGA I/Os offer enhanced features such as drive strength control, slew rate control, bus-keeper latches, internal pull-up or pull-down resistors, and open-drain outputs. These features are controllable on a “per-pin” basis.

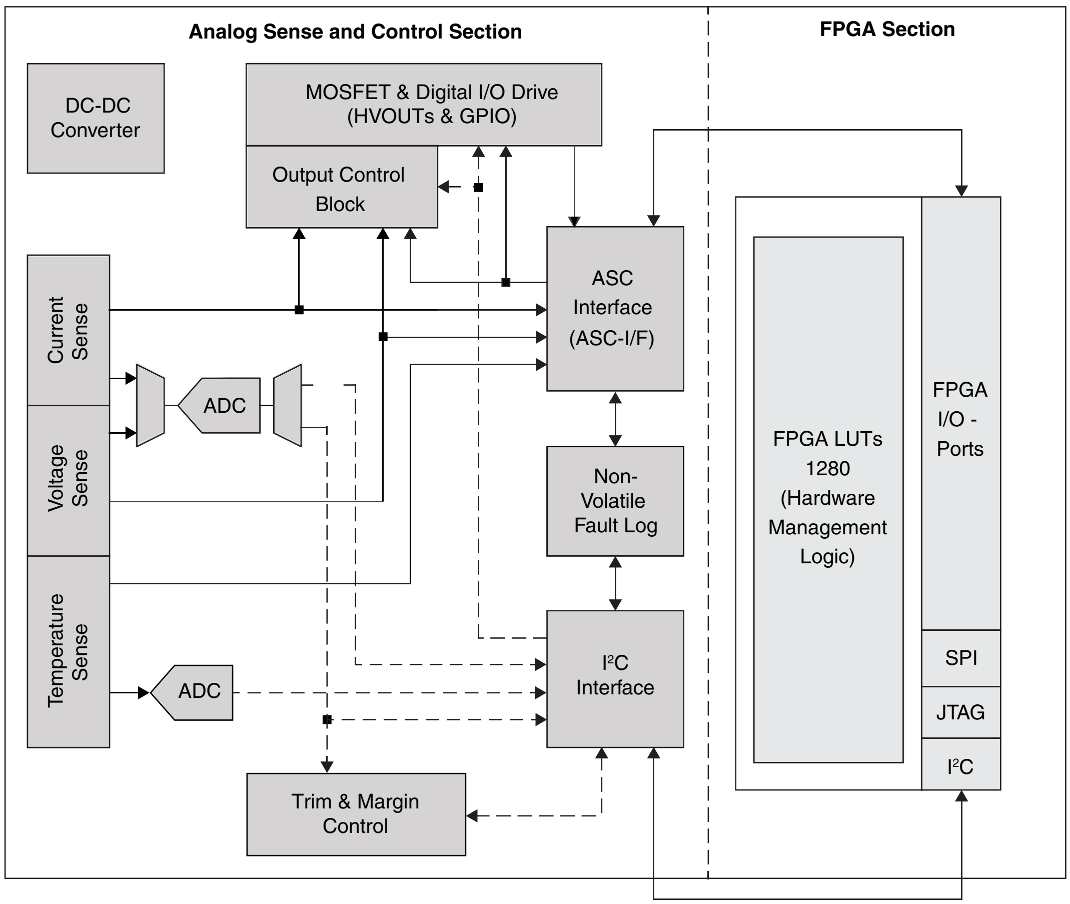
The power management, thermal management and control plane logic functions are implemented in the FPGA section of Platform Manager 2. The FPGA receives the analog comparator values and inputs from the ASC section and sends output commands to the ASC section through the dedicated ASC-interface (ASC-I/F) high-speed, reliable serial channel. The FPGA hardware management functions are implemented using the Platform Designer tool inside Lattice Diamond software. The Platform Designer tool includes an easy to use sequence and monitor logic builder tool and a set of pre-engineered components for functions like time-stamped fault logging, voltage by identification (VID), and fan control.

The Platform Manager 2 is designed to enable seamless scaling of the number of voltage, current and temperature sense channels in the system by adding external Analog Sense and Control (ASC) Hardware Management Expanders. The algorithm implemented within the FPGA can access and control these external ASCs through the dedicated ASC-I/F. Larger systems with up to eight ASC devices can be created by using a MachXO2 FPGA in place of the Platform Manager 2 device. The companion devices are connected in a scalable, star topology to Platform Manager 2 or MachXO2.

The Platform Manager 2 has an I²C interface which is used by the FPGA section for ASC interface configuration. The I²C interface also provides the mechanism for parameter measurement or I/O control or status. For example, voltage trim targets can be set over the I²C bus and measured voltage, current, or temperature values can be read over the I²C bus.

The Platform Manager 2 device can be programmed in-system through JTAG or I²C interfaces. The configuration is stored in on-chip non-volatile memory. Upon power-on, the FPGA section configuration is transferred to the on-chip SRAM and the device operates from SRAM. It is possible to update the non-volatile memory content in the background without interrupting the system operation. For additional details please see DS1043, Platform Manager 2 Data Sheet.

Figure 3. Platform Manager 2 Block Diagram



L-ASC10-Hardware Expander-Device

As shown in Figure 4, The L-ASC10 (Analog Sense and Control - 10 rail) is a Hardware Management (Power, Thermal, and Control Plane Management) Expander designed to be used with Platform Manager 2 or MachXO2 FPGAs to implement the Hardware Management Control function in a circuit board. The L-ASC10 (referred to as ASC) enables seamless scaling of power supply voltage and current monitoring, temperature monitoring, sequence and margin control channels. The ASC includes dedicated interfaces supporting the exchange of monitor signal status and output control signals with these centralized hardware management controllers. Up to eight ASC devices can be used to implement a hardware management system.

The ASC provides three types of analog sense channels: voltage (nine standard channels and one high voltage channel), current (one standard voltage and one high voltage), and temperature (two external and one internal) as shown in Figure 2.

Each of the analog sense channels is monitored through two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. The current sense channels feature a programmable gain amplifier and a fast fault detect (<1 µs response time) for detecting short circuit events. The temperature sense channels can be configured to work with different external transistor or diode configurations.

Nine general purpose 5 V tolerant open-drain digital input/output pins are provided that can be used in a system for controlling DC-DC converters, low-drop-out regulators (LDOs) and optocouplers, as well as for supervisory and general purpose logic interface functions. Four high-voltage charge pumped outputs (HVOUT1-HVOUT4) may be configured as high-voltage MOSFET drivers to control high-side MOSFET switches. These HVOUT outputs can also be programmed as static output signals or as switched outputs (to support external charge pump implementation) operating at a dedicated duty cycle and frequency.

The ASC device incorporates four TRIM outputs for controlling the output voltages of DC-DC converters. Each power supply output voltage can be maintained typically within 0.5% tolerance across various load conditions using the Digital Closed Loop Control mode.

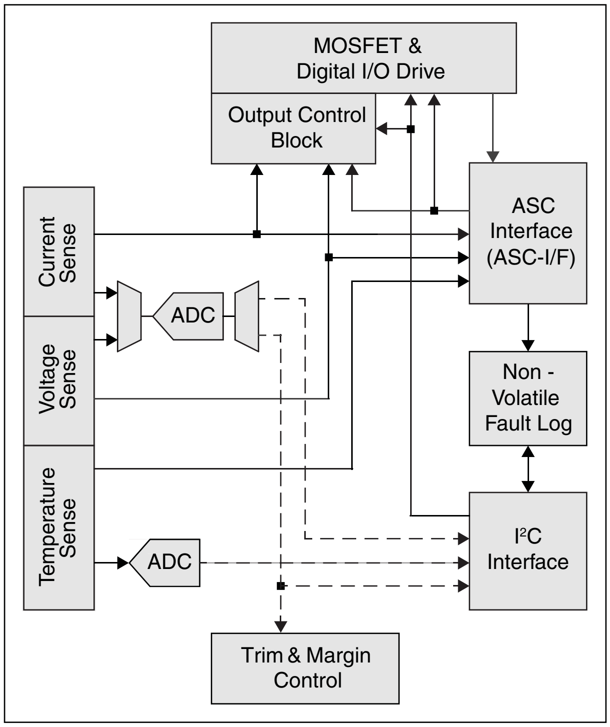
The internal 10-bit A/D converter can be used to monitor the voltage and current through the I^2C bus. The ADC is also used in the digital closed loop control mode of the trimming block.

The ASC also provides the capability of logging up to 16 status records into the on-chip nonvolatile EEPROM memory. Each record includes voltage, current and temperature monitor signals along with digital input and output levels.

The dedicated ASC Interface (ASC-I/F) is a reliable serial channel used to communicate with a Platform Manager 2 or a MachXO2 FPGA in a scalable star topology. The centralized control algorithm in the FPGA monitors signal status and controls output behavior via this ASC-I/F. The ASC I^2C interface is used by the FPGA or an external microcontroller for ASC background programming, interface configuration, and additional data transfer such as parameter measurement or I/O control or status. For example, voltage trim targets can be set over the I^2C bus and measured voltage, current, or temperature values can be read over the I^2C bus.

The ASC also includes an on-chip output control block (OCB) which allows certain alarms and control signals a direct connection to the GPIOs or HVOUTs, bypassing the ASC-I/F for a faster response. The OCB is used to connect the fast current fault detect signal to an FPGA input directly. It also supports functions like Hot Swap with a programmable hysteretic controller. For additional details please see DS1042, L-ASC10 Data Sheet.

Figure 4. Hardware Management Expander L-ASC10 Block Diagram



Platform Manager 2 Board Photos

Photographs of the top and bottom of Platform Manager 2 Board are shown in Figure 5 and Figure 6 below. Component location references are relative to the top of the board with the silk screen text in the readable orientation (as shown in the photo).

Figure 5. Platform Manager 2 Evaluation Board – Top View

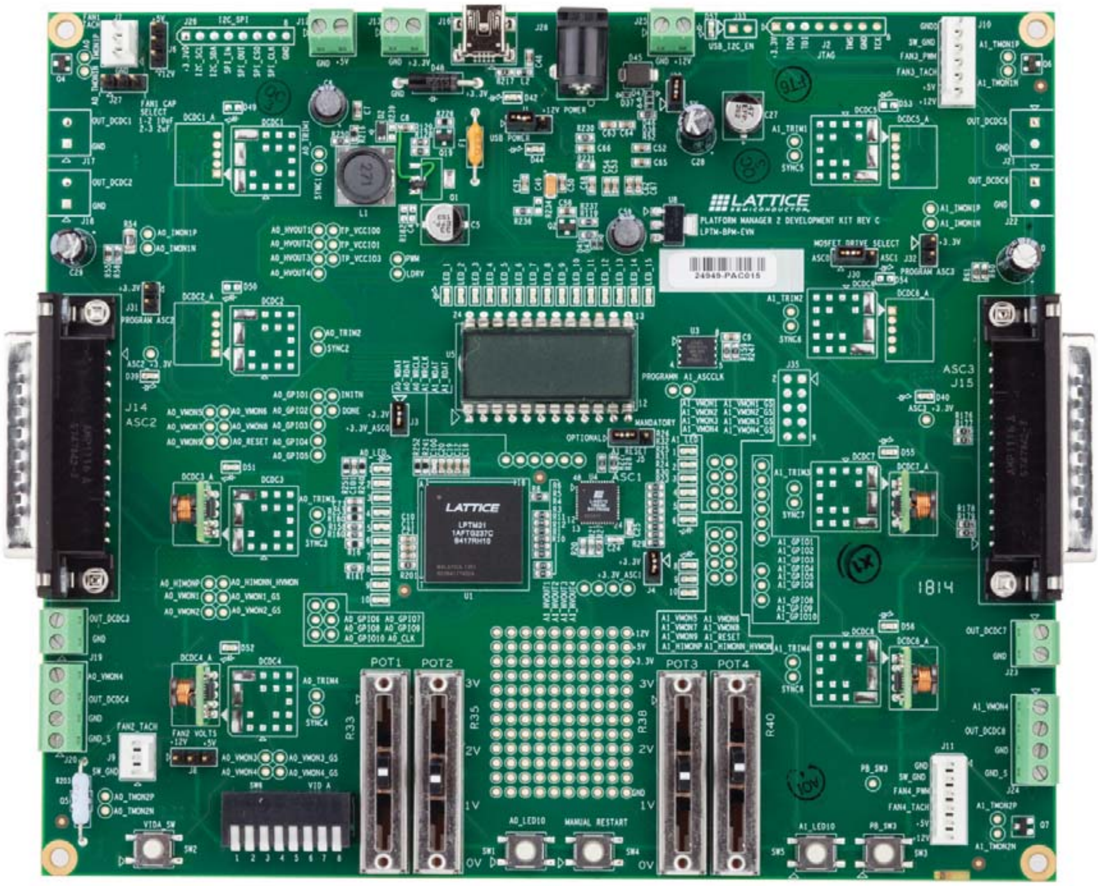
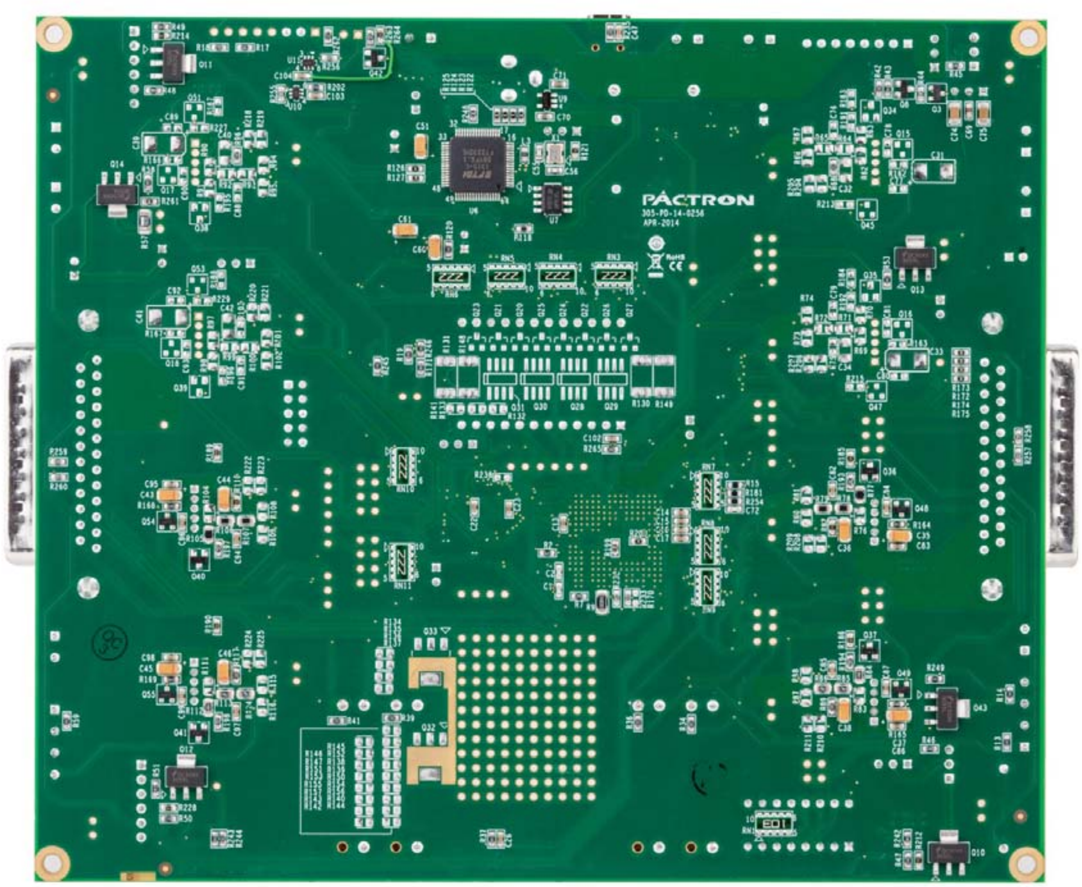


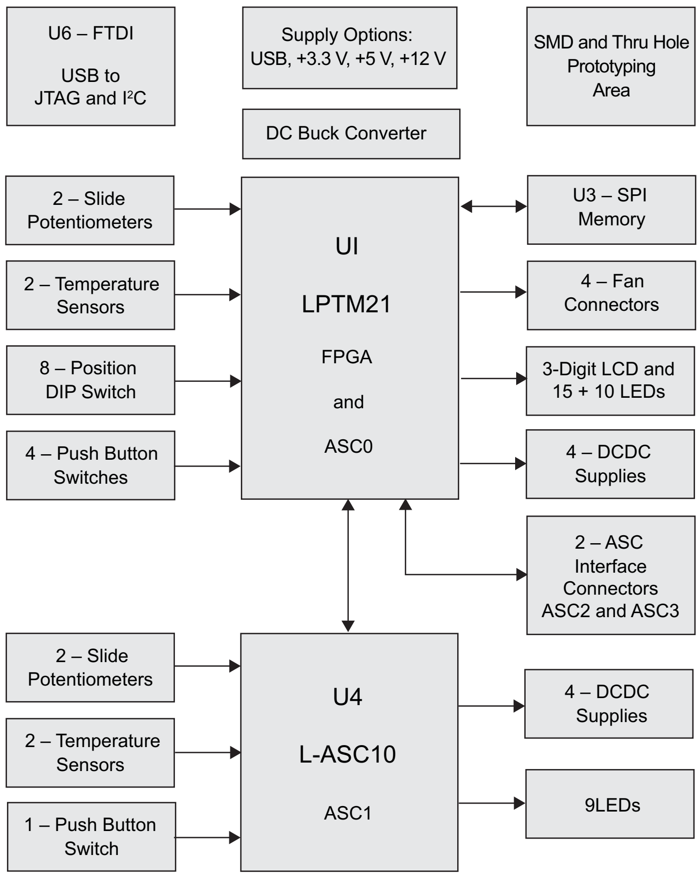
Figure 6. Platform Manager 2 Evaluation Board – Bottom View



Platform Manager 2 Board – Architecture Overview

In this section, the Platform Manager 2 evaluation board is described at the top level. It identifies the main hardware components on the board and briefly describes their functions. Because many of these elements are described in much more detail in the various Operational Description sections that follow, this section is just a short overview. Refer to the appropriate Operational Description Section for more details on each block. A block diagram of the overall system architecture of the Platform Manager 2 evaluation board is shown in Figure 7. Not all blocks are used by the demo but are provided to evaluate other features of the Platform Manager devices.

Figure 7. Platform Manager 2 Evaluation Board – Block Diagram



As discussed earlier the LPTM21 (U1) and L-ASC10 (U4) are the Platform Manager 2 devices that are highlighted on this board. Both are connected to a variety of input and output circuits that can be used in demos and customer evaluations.

LPTM21 (U1) is the primary Platform Manager 2 device. It is referred to as ASC0 in this document when discussing the analog features and as LPTM21 or FPGA when the focus is on the programmable logic.

L-ASC10 (U4) is the secondary Platform Manager 2 device that expands the hardware control and monitoring of LPTM21 (U1).

SPI Memory (U3) is used for Dual Boot and fault logging.

FTDI USB Interface (U6) is used for programming the Platform Manager devices and to access the I²C bus from USB.

DC Buck Converter is used to power the board from an optional +12 V supply.

Slide Potentiometers are used to demonstrate voltage monitoring; they simulate power supplies and can be used to generate either over or under voltage faults.

Temperature Sensors are used to demonstrate temperature monitoring.

8-Position DIP Switch interfaces with the FPGA and can be used for a variety of uses.

Push Button Switches are connected to ASC GPIO and FPGA pins for a variety of uses.

Fan Connectors are used with off board fans.

LCD Display is a three digit seven segment display that is connected to the FPGA for a variety of uses.

LED Indicators are distributed to the ASC GPIO pins and some FPGA pins for user defined functions.

DC-DC Supplies can be enabled, monitored, trimmed, and controlled be VID.

ASC Interface Connectors are provided to connect additional ASC Evaluation boards to expand the level of hardware control and monitoring.

Operational Description

Platform Manager 2 evaluation board supports the demonstration of multiple features, the details of which are described in this part of user guide. Each of the following sections covers a specific Platform Manager 2 feature with a focus on the associated circuitry and signals. Some sections are independent while others are combined to implement the complete Platform Manager 2 solution. The operational sections are organized as follows:

- Voltage Monitor
- Temperature Sense
- Current Monitor
- Hot Swap
- Fan Control
- Fault Logging
- Closed Loop Trim
- VID
- Programming and Configuration
- Dual Boot
- 12 V Buck Converter
- Power Supplies
- ASC Interface
- I^2C Bus
- Miscellaneous

Voltage Monitor Operation

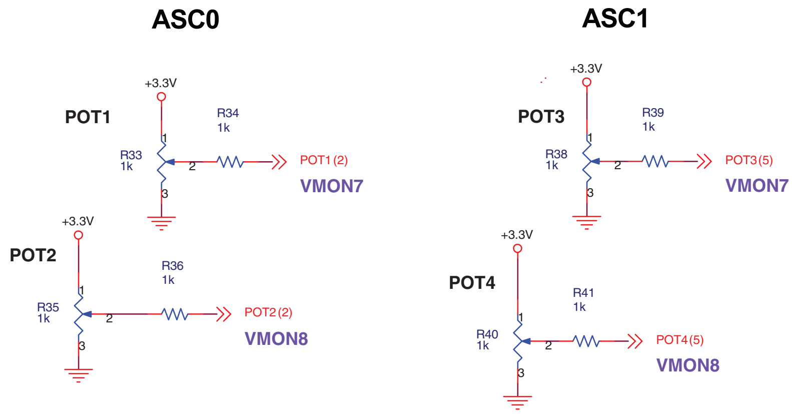
One of the key features of the Platform Manager 2 device is the ability to accurately monitor Voltages. The evaluation board has four slide potentiometers connected to Voltage Monitor inputs (VMONs). These potentiometers function as pseudo power supplies for the demo design and for evaluation of Voltage Monitoring. Most of the VMONs on the evaluation board have a low value series resistors connected to the on board source such as the DC-DC outputs, on-board supplies, and the potentiometers. These series resistors are only needed for the evaluation board so that the VMON test points can be driven from off-board sources without damage to either the on-board circuits or the off-board source and without the need to modify the board. Table 1 lists the components and signals associated with Voltage Monitoring.

Table 1. Components and Signals for Voltage Monitoring

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components			
Slider Potentiometers[1] (POT1 and POT2)	R33, R35	6	1 kOhm slider potentiometer: provides a variable Voltage from zero to 3.3 V. Connected to VMON7 and VMON8 of U1 with a 1 kOhm series resistor.
Series Resistors[2]	R34, R36	6	1 kOhm resistor.
Slider Potentiometers[1] (POT3 and POT4)	R39, R41	6	1 kOhm slider potentiometer: provides a variable Voltage from zero to 3.3 V. Connected to VMON7 and VMON8 of U4 with a 1 kOhm series resistor.
Series Resistors[2]	R39, R41	6	1 kOhm resistor.
Series Resistors[2]	R1, R2, R3, R4, R6, R7, R8	2	270 Ohm resistor.
Series Resistor[2]	R9	2	680 Ohm resistor.
Ground Sense Resistors[2]	R10, R11, R12	2	100 Ohm resistor.
Ground Sense Resistor[2]	R13	9	100 Ohm resistor.
Series Resistors[2]	R23, R24, R25, R26, R28, R29	5	270 Ohm resistor.
Ground Sense Resistors[2]	R29, R30, R31	5	100 Ohm resistor.
Ground Sense Resistor[2]	R32	9	100 Ohm resistor.
Signals			
A0_VMON1 – A0_VMON9		2	ASC0 VMON inputs (9)
A0_GS_VMON1 – A0_GS_VMON4		2	ASC0 VMON Ground Sense inputs (4) pulled to ground with 100 Ohm resistors. Can be connected to low side of a differential source.
A0_HVMON		2	ASC0 High Voltage VMON input.
A1_VMON1 – A1_VMON9		5	ASC1 VMON inputs (9)
A1_GS_VMON1 – A1_GS_VMON4		5	ASC1 VMON Ground Sense inputs (4) pulled to ground with 100 Ohm resistors. Can be connected to low side of a differential source.
A1_HVMON		5	ASC1 High Voltage VMON input.

1. Not required for customer designs; this is only needed to support demonstrations on the evaluation board.
2. Not required for customer designs; allows driving test points with an off-board Voltage source without adding or removing components or damaging on board circuitry.

Figure 8. Voltage Monitor POT Circuits



The four slide potentiometers shown in Figure 8 provide a variable Voltage source from zero to +3.3 V. POT1 and POT2 are connected to LPTM21 (U1) while POT3 and POT4 are connected to L-ASC10 (U4).

Temperature Monitor Operation

Another key feature of the Platform Manager 2 device is the ability to sense and monitor temperatures. Each device can support up to two external temperature sensors and one internal. The external sensors are diode configured bipolar transistors that are connected to the TMON (temperature monitor) inputs of LPTM21 and L-ASC10 (U1 and U4). Table 2 lists the components and signals on the Platform Manager 2 evaluation board to demonstrate temperature sensing and monitoring operation.

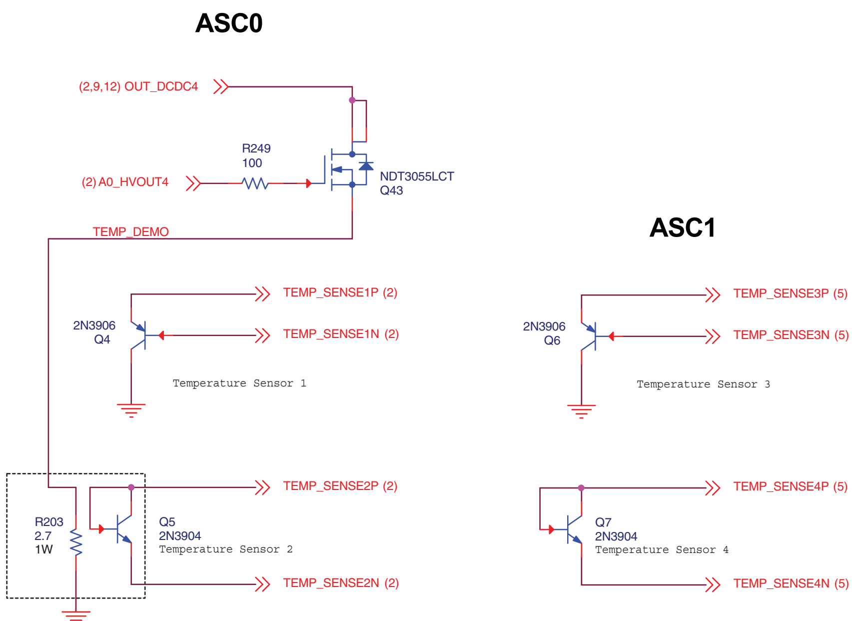
Table 2. Components and Signals for Temperature Sense and Monitor

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components			
Temperature Sensor 1	Q4	9	2N3906 PNP Transistor, Diode-configured (Beta Compensated) differential temperature sensor. Connected to TMON1 inputs of LPTM21 U1.
Temperature Sensor 2	Q5	9	2N3904 NPN Transistor, Diode- configured (Differential NPN) temperature sensor. Connected to TMON2 inputs of LPTM21 U1.
Temperature Sensor 3	Q6	9	2N3906 PNP Transistor Diode- configured (Beta Compensated) differential temperature sensor. Connected to TMON1 inputs of L-ASC10 U4.
Temperature Sensor 4	Q7	9	2N3904 NPN Transistor Diode- configured (Differential NPN) temperature sensor. Connected to TMON2 inputs of L-ASC10 U4.
Heater (Pseudo IC)[1]	R203	9	2.7 Ohm 1 W power resistor is mounted over Q5 for demo purposes. The amount of heat generated depends on the output of DCDC4 and the state of Q43.
Heater Power Switch[1]	Q43	9	Connects the output of DCDC4 to the heater (R203) when A0_HVOUT is active.
Sensor Filter Capacitors	C1, C2, C24, C25	2 and 5	150 pF Input filter capacitors for temperature monitoring signals to reject external noise. Located near U1 and U4.

Component / Signals	Ref. Des.	Schematic Sheet	Description
Signals			
TEMP_SENSE1P / TEMP_SENSE1N		2 and 6	Differential temperature sensor inputs to TMON1 of LPTM21 U1.
TEMP_SENSE2P / TEMP_SENSE2N		2 and 6	Differential temperature sensor inputs to TMON2 of LPTM21 U1.
TEMP_SENSE3P / TEMP_SENSE3N		5 and 6	Differential temperature sensor inputs to TMON1 of L-ASC10 U4.
TEMP_SENSE4P / TEMP_SENSE4N		5 and 6	Differential temperature sensor inputs to TMON2 of L-ASC10 U4.
A0_HVOUT4		2 and 6	HVOUT output from LPTM21 to turn on/off transistor (Q43) in order to control the current flowing into resistor (R203) which provides temperature for demo purpose.

1. Not required for customer designs; this is only needed to support demonstrations on the evaluation board.

Figure 9. Temperature Monitor Circuits



On the Platform Manager 2 evaluation board there are four external temperature sensors as shown in Figure 9. Two sensors (Q4 and Q5) are connected to LPTM21 (U1) and two sensors (Q6 and Q7) are connected to L-ASC10 (U4). The evaluation board demonstrates two different configurations for the temperature sensors. Q5 and Q7 are configured as *Differential NPN* diodes while; Q4 and Q6 are configured as *Beta Compensated PNP* diodes. The *Beta Compensated PNP* configuration is similar to a substrate diode connection and is able to take advantage of the Platform Manager 2 built-in beta compensation for more accurate temperature monitoring. All of the temperature sensors have filter capacitors connected across the differential signals to improve noise-immunity and they are located close to the Platform Manager 2 devices (U1 and U4). All of the temperature sensors have test points nearby to support off-board sensors after the on-board sensor has been removed.

The circuit in Figure 9 shows a power resistor (R203) mounted thermally close to sensor 2 (Q5). This 1-watt power resistor is a pseudo IC load to demonstrate thermal management in the demo design. The resistor is powered when both the MOSFET switch (Q43) is biased ON and DCDC4 is enabled. Q43 is turned on when HVOUT4 of LPTM21 (U1) is turned ON; HVOUT4 needs to be in Charge Pump mode with the following settings: 8 V, 100 uA source, 3000 uA sink, and static mode. Using the Platform Manager 2 I^{2}C GUI with the demo, the output of DCDC4 can be adjusted or fan #2 can be controlled (or both) in order to reduce the power and lower the temperature of the sensor. For details on using the demo and GUI please refer to the Platform Manager 2 I²C Demo Design and GUI User's Guide. For additional information regarding temperature monitoring please refer to TN1278, Temperature Monitoring and Fan Control with Platform Manager 2.

Current Monitoring Operation

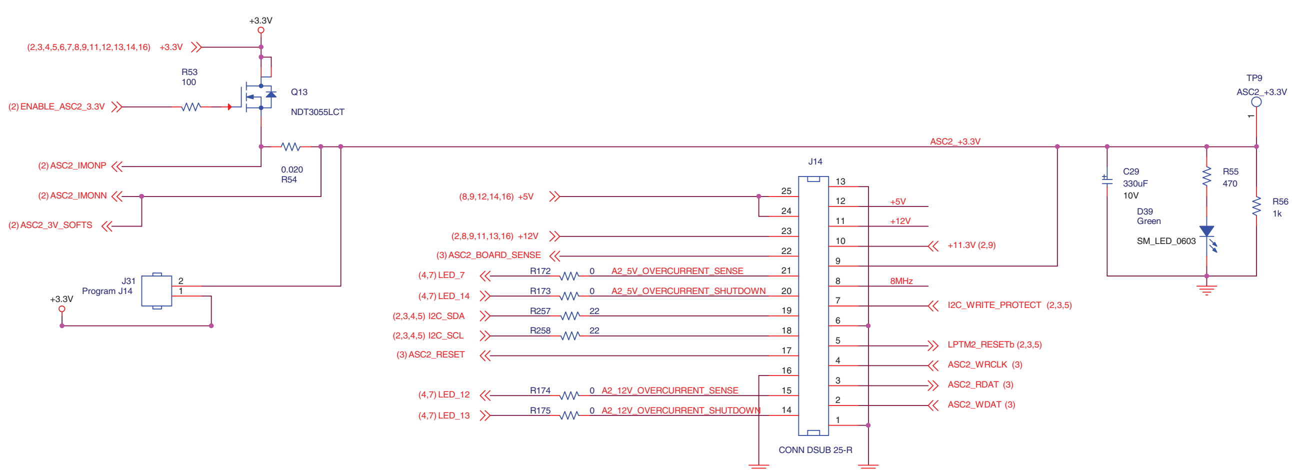
Another key feature of the Platform Manager 2 device is the ability to monitor current. Each device has two current monitoring (IMON) inputs and each input has two pins that connect to an external current sensing resistor. One current sensing input is designed to monitor current at high voltage (12 V typical) and shares a pin with the high voltage VMON (HIMONN_HVMON). The second current sensing input is designed to monitor lower voltage (5 V typical or lower) currents. Table 3 lists the components and signals associated with current monitoring operation on the Platform Manager 2 board.

Table 3. Components and Signals for Current Monitoring Operation

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components			
Current sense resistor	R54	10	20 milli-Ohm ¼ W Resistor for load side current monitoring with IMON1 inputs of LPTM21 (U1).
Current sense resistor	R57	10	20 milli-Ohm ¼ W Resistor for supply side current monitoring with IMON1 inputs of L-ASC10 (U4).
Isolation Resistor	R261	10	Zero Ohm Resistor isolates the ASC3_IMONP net from the +3.3 V supply net to support Kelvin layout.
Test Connector[1]	J31, J32	10	Connect an external load resistor between pin 2 and ground to provide a measurable current.
Power Switch MOSFET[1]	Q13, Q14	10	N-Channel Power MOSFET, used to enable power to loads either on/off or Hot Swap mode.
Signals			
ASC2_IMONP ASC2_IMONN		2, 10	The current monitoring signals to LPTM21 (U1) connected across the current sense resistor R54.
ASC3_IMONP ASC3_IMONN		5, 10	The current monitoring signals to L-ASC10 (U4) connected across the current sense resistor R57.

1. Not required for customer designs; this is only needed to support demonstrations on the evaluation board.

Figure 10. ASC0 IMON1 Monitors ASC2 Current and Supports Hot Swap Circuits

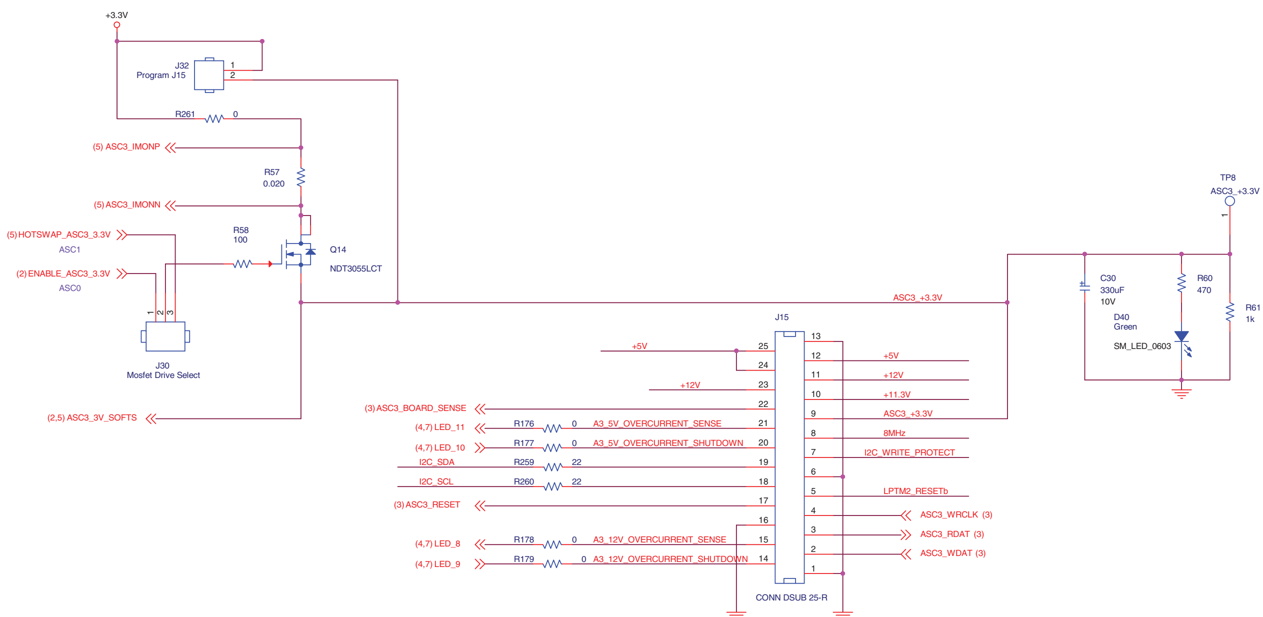


The current sense resistor (R54) shown in Figure 10 is used to monitor the current through power switch MOSFET (Q13). When Q13 is turned on, +3.3 V is supplied to loads both on and off board and R54 is used to monitor the combined load current. The signals ASC2_IMONP and ASC2_IMONN are connected to R54 using Kelvin connections and differential signaling layout techniques to maximize the current sensing accuracy at the IMON1 inputs of U1 (sheet 2). The signals are named because they can be used to monitor off board current drawn by the ASC2 interface connector J14.

The N-channel MOSFET (Q13) is controlled by the HVOUT2 of U1 (sheet 2) either on/off control or Hot Swap based on the design. The gate resistor (R53) is mounted physically close to Q13 to minimize parasitic oscillations. The programming jumper (J31) by-passes Q13 when installed to support programming ASC2 via J14; the jumper should be removed for Hot Swap operation.

The on-board loads consist of the following components: C29, D39, R55, and R56. While they provide a path to ground for Q13 and R54, they are not designed to provide a significant load. Alternatively, an external load resistor can be attached between pin 2 of J31 and ground to provide a more significant load to be measured. The external load resistor should draw less than 200 mA when the board is powered by USB and less than 3 A when the board is powered from a bench supply connected to J12 (sheet 9). The function of LED D39 and bias resistor R55 is to indicate that +3.3 V is available for the ASC2 interface connector. R56 is designed to discharge the Hot Swap load capacitor C29 when power is removed. The Hot Swap load capacitor C29 only draws current when it is charging up which is discussed in the Hot Swap Operation section.

Figure 11. ASC1 IMON1 Monitors ASC3 Current and Supports Hot Swap Circuits



The current sense resistor (R57) shown in Figure 11 is used to monitor the current through the power switch MOSFET (Q14). When Q14 is turned on, +3.3 V is supplied to loads both on and off board and R57 is used to monitor the combined load current. The signals ASC3_IMONP and ASC3_IMONN are connected to R57 using Kelvin connections and differential signaling layout techniques to maximize the current sensing accuracy at the IMON1 inputs of U4 (sheet 5). The signals ASC3_IMONP and ASC3_IMONN are named because they can be used to monitor off board current drawn by the ASC3 interface connector J15. Since R57 is used to monitor the current on the high (or supply side), a zero Ohm jumper (R261) is used to generate a sensing net that is isolated from the power net. This separate net supports differential signal layout from the sensing resistor to the IMON inputs.

The N-channel MOSFET (Q14) can be controlled by either HVOUT3 of U1 (sheet 2) for simple on/off control or HVOUT3 of U4 (sheet 5) for Hot Swap control, based on the position of a jumper (J30). Hot Swap is only supported when the current sense and MOSFET control are connected to the same ASC; in this case ASC1 (U4). The gate resistor (R58) is mounted physically close to Q14 to minimize parasitic oscillations. The programming jumper (J32) by-passes Q14 when installed to support programming ASC3 via J15; the jumper should be removed for Hot Swap operation.

The on-board loads consist of the following components: C30, D40, R60, and R61. While they provide a path to ground for Q14 and R57, they are not designed to provide a significant load. Alternatively, one can attach a load resistor between pin 2 of J32 and ground to provide a load to be measured. The resistor should draw less than 200 mA when the board is powered by USB and less than 3 A when the board is powered from a bench supply connected to J12 (sheet 9). The function of LED D40 and bias resistor R60 is to indicate that +3.3 V is available for the ASC3 interface connector. R61 is designed to discharge the Hot Swap load capacitor C30 when power is removed. The Hot Swap load capacitor C30 only draws current when it is charging up which is discussed in the Hot Swap Operation section.

Hot Swap Operation

The Hot Swap operation can be demonstrated on the Platform Manager 2 evaluation board using the IMON1 current sense inputs and the HVOUT MOSFET driver outputs. The default demo does not include Hot Swap operation. However, this section is provided for future demos and customer evaluations. Table 4 lists the components and signals associated with the Hot Swap operation on the Platform Manager 2 evaluation board

Table 4. Components and Signals for Hot Swap Operation

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components			
Current sense resistor	R54	10	20 milli-Ohm ¼ W Resistor for load side current monitoring with IMON1 inputs of LPTM21 (U1).
Current sense resistor	R57	10	20 milli-Ohm ¼ W Resistor for supply side current monitoring with IMON1 inputs of L-ASC10 (U4).
Isolation Resistor	R261	10	Zero Ohm Resistor isolates the ASC3_IMONP net from the +3.3V supply net to support Kelvin layout.
Gate Resistors	R53, R58	10	100 Ohm Resistor to reduce parasitic MOSFET oscillations on Q13 and Q14.
LED Bias Resistors	R55, R60	10	470 Ohm Resistors to limit the current in LEDs D39 and D40.
MOSFET Switch	Q13	10	N-Channel MOSFET Supply-side hot-swap switch supplies power to load capacitor C29 and ASC2 interface connector (J14).
MOSFET Switch	Q14	10	N-Channel MOSFET Load-side hot-swap switch supplies power to load capacitor C30 and ASC3 interface connector (J15).
LEDs	D39, D40	10	LEDs Green, indicate when hot-swap power is on or programming jumpers are in place.
Load Capacitors[1]	C29, C30	10	330 uF 10 V Bulk capacitance emulates a hot-swap load.
Discharge Resistors[1]	R56, R61	10	1 kOhm Resistor discharges load capacitor between hot-swaps.
Three-Pin Header[1]	J30	10	
2-Pin Header[1]	J31, J32	10	Install jumper to bypass hot-swap circuits and provide power during programming of ASC2 and/or ASC3.

Component / Signals	Ref. Des.	Schematic Sheet	Description
Signals			
ENABLE_ASC2_3.3V		2, 10	HVOUT2 signal from LPTM21 (U1) to control Q13. Can be used in hot-swap or simply as on/off control.
ENABLE_ASC3_3.3V		2, 10	HVOUT3 signal from LPTM21 (U1) to control Q13. For use as on/off control when L-ASC10 (U4) is powered down.
HOTSWAP_ASC3_3.3V		5, 10	HVOUT3 signal from L-ASC10 (U4) to control Q14. Can be used in hot-swap or simply as on/off control.
ASC2_IMONP			
ASC2_IMONN		2, 10	The current monitoring signals to LPTM21 (U1) connected across the current sense resistor R54.
ASC3_IMONP			
ASC3_IMONN		5, 10	The current monitoring signals to L-ASC10 (U4) connected across the current sense resistor R57.
ASC2_3V_SOFTS		2, 10	Voltage monitoring signal for Hot Swap or sequencing connected to VMON6 of LPTM21 (U1).
ASC3_3V_SOFTS		5, 10	Voltage monitoring signal connected to VMON9 of LPTM21 (U1) for sequencing and VMON9 of L-ASC10 (U4) for Hot Swap.
ASC2_+3.3V	TP9	10	Hot-swap power bus for ASC2 interface connector (J14) and loads. Test point on board is labeled with the signal name.
ASC3_+3.3V	TP8	10	Hot-swap power bus for ASC3 interface connector (J15) and loads. Test point on board is labeled with the signal name.

1. Not required for customer designs; this is only needed to support demonstrations on the evaluation board.

There are two Hot Swap circuits provided on the Platform Manager 2 evaluation board; one is controlled LPTM21 U1 and the other is controlled by L-ASC10 U4. The supporting Hot Swap circuitry for U1 is shown in Figure 10 and for U4 in Figure 11. Neither Hot Swap circuit is used in the default demo but, they are described for future demos and customer evaluations.

The circuit in Figure 10 illustrates a Supply based Hot Swap with the MOSFET Q13 connected between the supply and the current sensing resistor R54. The N type MOSFET Q13 is controlled by HVOUT2 of LPTM21 (sheet 2) and the gate resistor R53 is located physically close to Q13 to reduce turn on oscillations. The signals ASC2_IMONP and ASC2_IMONN are connected to R54 using Kelvin connections and differential signaling layout techniques to maximize the current sensing accuracy at the IMON1 inputs of LPTM21 (sheet 2). The signal ASC2_3V_SOFTS can be used by the Hot Swap function to monitor the load capacitor C29 voltage and is connected to VMON6 of LPTM21 using R7 (sheet 2). The Hot Swap function monitors the load capacitor C29 voltage for the following reasons: 1) to see that C29 is charging up and there is not a short or open in the circuit, 2) see that C29 has reached a voltage where a higher current limit can be used, 3) to know when C29 is close to the supply value – Hot Swap is complete. When Hot Swap is disabled R56 provides a discharge path for C29 to prepare the circuit for a subsequent Hot Swaps. LED D39 and bias resistor R55 gives a visual indication that the Hot Swap process is complete.

The circuit In Figure 11 illustrates a Load based Hot Swap with the MOSFET Q13 connected between the current sensing resistor R74 and the load. The N type MOSFET Q14 is controlled by HVOUT3 of L-ASC10 (sheet 5) and the gate resistor R58 is located physically close to Q14 to reduce turn on oscillations. The signals ASC3_IMONP and ASC3_IMONN are connected to R57 using Kelvin connections and differential signaling layout techniques to maximize the current sensing accuracy at the IMON1 inputs of L-ASC10 (sheet 5). The signal ASC3_3V_SOFTS is used by the Hot Swap function to monitor the load capacitor C30 voltage and is connected to VMON9 of L-ASC10 using R28 (sheet 5). The Hot Swap function monitors the load capacitor C30 voltage for the following reasons: 1) to see that C30 is charging up and there is not a short or open in the circuit, 2) see that C30 has reached a voltage where a higher current limit can be used, 3) to know when C30 is close to the supply value – Hot Swap is complete. When Hot Swap is disabled R61 provides a discharge path for C30 to prepare the circuit for a subsequent Hot Swaps. LED D40 and bias resistor R60 gives a visual indication that the Hot Swap process is complete.

Note the series resistors R7 (sheet 2) and R28 (sheet 5) are not required for Hot Swap or VMON operation; in a typical design the VMON input is connected directly to the Voltage source being monitored. The value of the series resistor (270 Ohms) is a compromise; it is low enough that the voltage sensing accuracy during Hot Swap is not affected but, it is also high enough that another supply can be connected directly to VMON test point without significant current flowing between the supplies. The function of R7 and R28 is to support prototype circuits that may be built using the Platform Manager 2 evaluation board without having to remove components or cut traces.

For Hot Swap operation the Platform Designer tool must be used to configure ASC0 and ASC1 (U1 and U4) so that the HVOUT output is controlled by the status of the IMON1 inputs. This internal connection provides hysteretic control such that the MOSFET is modulated to restrict the current below the IMON1 trip point. If the sensed current is below the trip point then the MOSFET bias is increased; and if the sensed current exceeds the trip point then the MOSFET bias is reduced. For additional information please see the Hot Swap Application Note.

Note that for the Hot Swap operation to work properly, no significant off board load should be enabled or attached to J31 or J32 or the ASC interface connectors J14 and J15. A significant load would draw more than 20% of the Hot Swap current. Also J30 should be in the ASC1 position.

Fan Control Operation

The Platform Manager 2 evaluation board provides four channels of fan control for a variety of thermal management demos and the kit includes a loose un-mounted 5 V 3-wire fan. Table 5 lists the components and signals associated with fan control operation of the Platform Manager 2 board.

Table 5. Components and Signals for Fan Control Operation

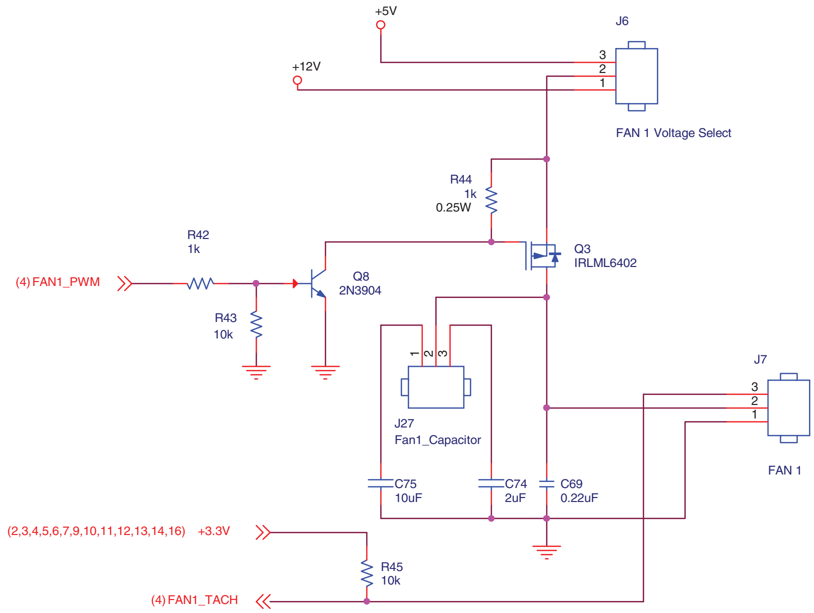
Component / Signals	Ref. Des.	Schematic Sheet	Description
Components			
5V 3-Wire Fan			Not mounted on the board but, included with the kit for various demos. Has a 3x1 connector for use with FAN1 or FAN2.
3x1 Header	J7, J9	8	Headers to connect external 3 Wire fans. (FAN1 and FAN2). Supports both +5 V and +12 V fans.
6x1 Header	J10, J11	8	Headers to connect external fans (FAN3 and FAN4). Supports both +5 V and +12 V also 3-wire and 4-wire fans.
3x1 Header1	J6, J8	8	Headers to select from either +5 V or +12 V supply for FAN1 and FAN2.
3x1 Header1	J27	8	Provides options to connect various filter capacitors to the supply pin of FAN1.
High-Side Drive Filter Capacitor2	C69	8	0.22 uF capacitor – Default filter for PWM frequencies 40 kHz or more. No jumper on J27.
High-Side Drive Filter Capacitor2	C74	8	2.0 uF capacitor – Optional filter for PWM frequencies between 10 kHz and 26 kHz. Jumper pins 2-3 on J27.
High-Side Drive Filter Capacitor2	C75	8	10 uF capacitor – Optional filter for PWM frequencies below 10 kHz. Jumper pins 1-2 on J27.
NPN Transistor – SOT-23	Q8	8	2N3904 NPN Transistor inverts the FAN1_PWM signal from LPTM21 U1 and shifts the drive level up to +12 V.
P-Channel MOSFET – SOT-23	Q3	8	IRLML6402 P-Channel MOSFET provides high-side switching for FAN1 based on the inverted (by Q8) FAN1_PWM signal.

Component / Signals	Ref. Des.	Schematic Sheet	Description
N-Channel MOSFET – SOT-235	Q10, Q11, Q12	8	NDT3055LCT – N-Channel MOSFET provides low-side drive based on PWM signal from LPTM21 U1.
Gate Resistor	R212, R214, R228	8	470 Ohm resistor to isolate the MOSFET input capacitance from the LPTM21 I/O bank to minimize ground and supply bounce. Also suppresses MOSFET turn-on oscillations.
Gate Pull Down Resistor	R47, R49, R51	8	10k Ohm resistor to keep MOSFETs turned off by default.
Gate Pull Up Resistor	R44	8	1 kOhm ¼ W Resistor to provide a fast turn-off of Q3. The power rating is required for operation at +12 V.
Tach Pull Up Resistor	R45, R46, R48, R50	8	10 kOhm resistor to bias the open-drain tachometer feedback signal from the fans.
Base Pull Down Resistor	R43	8	10 kOhm resistor to keep Q8 turned off by default.
Base Bias Resistor	R42	8	1 kOhm resistor to limit the current from the LPTM21 U1 output when turning on Q8.
Signals			
FAN1_PWM,			
FAN2_PWM,			
FAN3_PWM,			
FAN4_PWM		4, 8	The PWM signals to control the fan speed, FPGA output from LPTM21 U1.
FAN1_TACH,			
FAN2_TACH,			
FAN3_TACH,			
FAN4_TACH		4, 8	The Tachometer or fault signal from fan to FPGA input of LPTM21 U1.

1. Not required for customer designs; this is only needed to support demonstrations on the evaluation board.
2. Actual values may vary for customer designs; several values are provided to support demonstrations on the evaluation board.

The control circuit shown in Figure 12 for Fan 1 is the most complex fan drive circuit on the board. This is to support a wide variety of design evaluations. High-side drive is implemented for Fan 1 using Q3 to modulate the supply to the fan. The FAN1_PWM signal from LPTM21 (U1) is inverted and level shifted by Q8. The low impedance (1 kOhm) of R44 is needed to turn Q3 off quickly and because of operation at +12 V the ¼ watt package is required. The high-side drive benefits from having a filter capacitor in the circuit and J27 provides the means to change the filter value based on the PWM frequency. The PWM frequency is selected in Platform Designer Fan Component view. A jumper needs to be installed on J6 to select the fan supply voltage. +5 V can be provided by the USB cable to power the included fan. Alternatively +5 V can be supplied from J12, J14, or J15 (sheets 9 and 10) based on type of evaluation being done. If a +12 V fan is used the voltage must be supplied from an off-board supply via J28, J25, J14, or J15 (sheets 9 and 10) because +12 V is not generated from the USB +5 V. The 10k pull-up resistor (R45) is connected to +3.3 V to provide bias for fans that have an open-drain tachometer or fault output and to interface with the LPTM21 (U1) FPGA inputs.

Figure 12. Fan 1 PWM Control Circuit



FAN 1 - 3 WIRE HIGH SIDE DRIVE

The control circuit shown in Figure 13 for Fan 2 provides a low-side drive circuit where Q10 modulates the ground connection to the fan. The signal FAN2_PWM comes from the FPGA output of LPTM21 (U1) through a series resistor (R212). The series resistor minimizes both the capacitive loading on the LPTM21 outputs and the tendency for Q10 to oscillate during turn-on; it is located physically close to Q10 on the board. The pull-down resistor R17 keeps the MOSFET Q10 turned off by default. A jumper needs to be installed on J8 to select the fan supply voltage. +5 V can be provided by the USB cable to power the included fan. Alternatively +5 V can be supplied from J12, J14, or J15 (sheets 9 and 10) based on type of evaluation being done. If a +12 V fan is used the voltage must be supplied from an off-board supply via J28, J25, J14, or J15 (sheets 9 and 10) because +12 V is not generated from the USB +5 V. The 10 kOhm pull-up resistor (R47) is connected to +3.3 V to provide bias for fans that have an open-drain tachometer or fault output and to interface with the LPTM21 (U1) FPGA inputs.

Figure 13. Fan 2 PWM Control Circuit

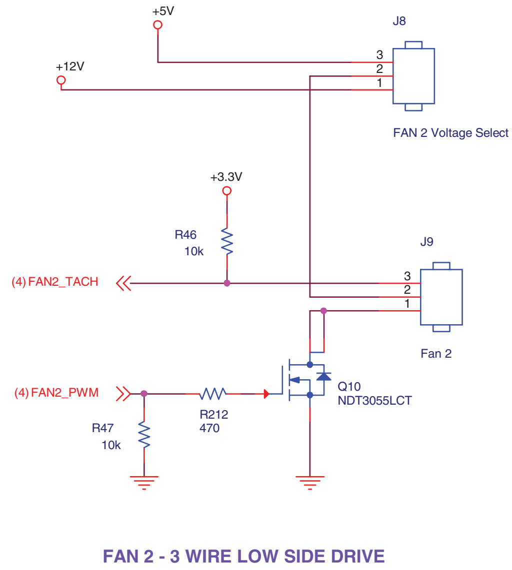
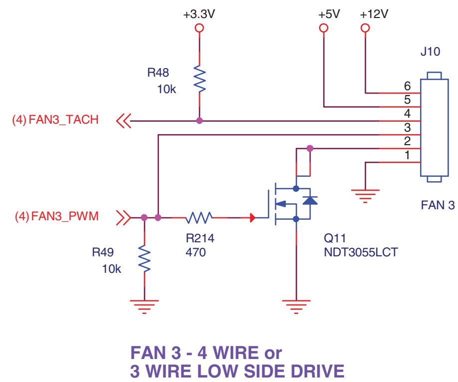
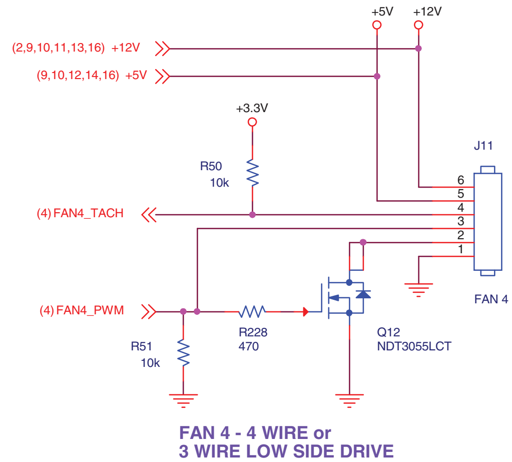


Figure 14. Fans 3 and 4 PWM Control Circuits





The control circuits shown in Figure 14 for Fan 3 and 4 provide low-side drive for both fans; Q11 modulates the ground connection for Fan 3 based on the FAN3_PWM signal and Q12 modulates the ground connection for Fan 4 based on the FAN4_PWM signal. Both signals come from LPTM21 (U1) FPGA outputs and use series resistors of 470 Ohms (R214 and R228) to minimize the capacitive loading. The series resistors are also mounted physically close to the MOSFETs (Q11 and Q12) to minimize parasitic oscillations. Both circuits have 10 kOhm pull-down resistors to keep the MOSFETs turned off by default. Unlike Fans 1 and 2 there is not a separate jumper to select the fan supply voltage; both the +5 V and +12 V supplies are available on the six-pin headers (J10 and J11) so that the fan connector can be wired to select the supply voltage. The six-pin headers also provide the PWM signals directly on pin three to support 4-wire fans. Both fan circuits have 10 kOhm pull-up resistors to +3.3 V on the TACH signals to support fans with open-drain tachometer outputs and to interface with the LPTM21 (U1) FPGA inputs.

The Platform Designer tool has a configurable Fan Controller component which can be implemented within the LPTM21 (U1). The fan controller can be configured to work with 2-wire, 3-wire, or 4-wire fans, and a maximum of sixteen fans can be controlled. The fan controller IP generates a pulse width modulated (PWM) signal, which is used to control the speed of the fan. It also monitors the tachometer input from the fan to detect a faulty condition. For additional information regarding fan control please refer to TN1278, Temperature Monitoring and Fan Control with Platform Manager 2.

Fault Logging Operation

One of the main features of any Platform Manager is the ability to log faults in non-volatile memory for later retrieval and analysis. The Platform Manager 2 evaluation board supports three methods of fault logging: 1) internal L-ASC10 storage only, 2) internal LPTM21 storage, and 3) external storage in SPI flash memory. The board also provides hold-up circuits so the Platform Manager 2 has time to log faults in the event of a primary supply failure. Table 6 lists the components and signals associated with Fault Logging operation of the Platform Manager 2 evaluation board.

Table 6. Components and Signals for Fault Logging OperationComponents and Signals for Fan Control Operation

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components			
4 MB Flash Memory	U3	3	SPI Flash memory to store Fault log data from LPTM21. LPTM21 has built-in SPI master which enables data transfer. This is the same memory that is used for Dual Boot.
5 V Blocking Diode	D41	15	Schottky Diode. Prevents external loads or supply from draining the hold-up capacitor.
5 V Passing Diode	D43	15	Schottky Diode. Allows the hold-up capacitor to provide full current to down-stream supply.
5 V Hold-up Capacitor	C59	15	47uF Capacitor. Keeps U1, U3, and U4 alive after +5 V power outage to store faults.
5 V Charging Resistor	R120	15	100 Ohm Resistor. Prevents large in-rush current charging the hold-up capacitor at power up.
12 V Blocking Diode	D37	9	Schottky Diode. Prevents external loads or supply from draining the hold-up capacitor.
12 V Passing Diode	D38	9	Schottky Diode. Allows the hold-up capacitor to provide full current to down-stream supply.
12 V Hold-up Capacitor	C27, C28	9	47 uF and 220 uF Capacitors. Keeps U1, U3, and U4 alive after +12 V power outage to store faults.
12 V Charging Resistor	R52	9	100 Ohm Resistor. Prevents large in-rush current charging the hold-up capacitor at power up.

Figure 15 shows the hold-up circuit for the USB +5 V supply. If the USB +5 V supply suddenly fails, this hold-up circuit will power the Platform Manager 2 and flash memory long enough to store the fault. The USB +5 V can fail for several of the following reasons: the USB cable is unplugged, the USB hub is powered down, the FTDI (U6) device is told to power down and Q2 is turned off. The signal +5V_USB_SW is connected to VMON5 of LPTM21 (U1 on sheet 2) for early detection of a 5 V fault. Small signal Schottky diodes are used for the blocking and passing diodes as the power required for the Platform Manager 2 and flash memory is fairly low. The size of the hold-up capacitor (C59) should be increased for fault logging support if significant loads are added to the +3.3 V supply. The charging resistor (R120) prevents large in-rush currents when the supply is connected or turned on.

Figure 15. Fault Log Hold-Up Circuit for 5 V

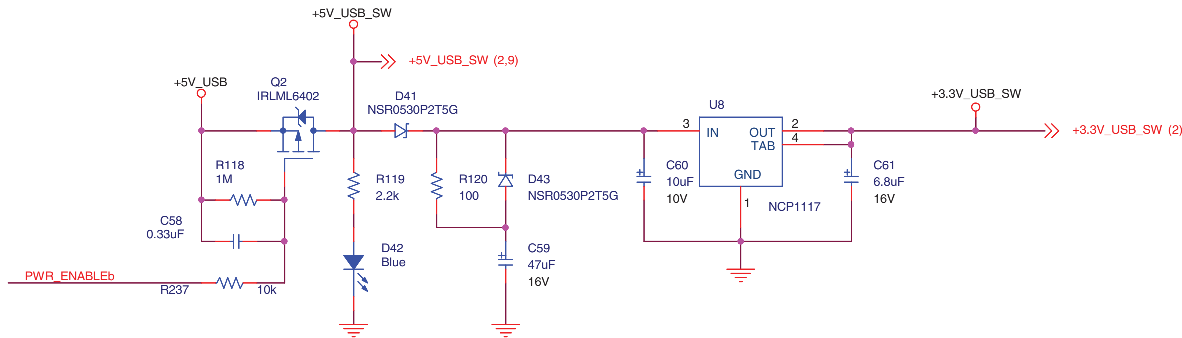
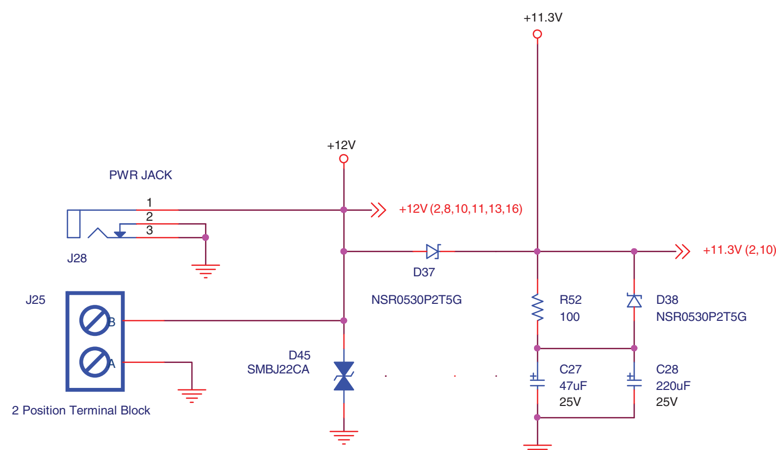


Figure 16 shows the hold-up circuit for the +12 V supply; it is similar to the 5 V circuit described above. The +12 V supply is monitored by the HIMONN_HVMON pin of the LPTM21 (U1 on sheet 2) for early detection of supply failure. The small signal Schottky diodes are used for blocking and passing the charge on the hold-up capacitors (C27 and C28). The charging resistor R52 prevents large in-rush currents when the supply is connected or turned on.

Figure 16. Fault Log Hold-Up Circuit for 12V



Both the LPTM21 and L-ASC10 devices have non-volatile EEPROM and volatile registers available to store fault log data. In addition, the LPTM21 device can store fault log data either internally in the User Flash Memory (UFM) of the FPGA section of U1 or externally in the SPI Flash Memory (U3). The Platform Manager 2 evaluation board has an external SPI 4 MB flash (U3) connected to the LPTM21 SPI interface to communicate with the memory as shown in Figure 21. This memory can be used for both Dual Boot and Fault Logging. The Platform Designer tool has a Fault Logging component which is used to configure what is logged and how it is stored. For additional information regarding fault logging please refer to TN1277, Fault Logging Using Platform Manager 2.

Close Loop Trim Operation

A differentiating feature of the Platform Manager 2 is the Closed Loop Trim (CLT) feature which is used to accurately trim and margin power supplies. The Platform Manager 2 evaluation board provides CLT circuits for up to eight DC-DC power supplies; four (DCDC1 – DCDC4) are controlled by LPTM21 (U1) and four (DCDC5 – DCDC8) are controlled by L-ASC10 (U4). Table 7 lists the installed components and signals associated with CLT operation on the Platform Manager 2 evaluation board.

Table 7. Installed Components and Signals for Closed Loop Trim Operation

Component / Signals	Ref. Des.	Schematic Sheet	Description
Components			
DC-DC Converter	DCDC3, DCDC4	12	Dual-footprint +5 V input adjustable output power supply. NQR002A0X4Z SIP installed.
DC-DC Converter	DCDC7, DCDC8	14	Dual-footprint +5 V input adjustable output power supply. NQR002A0X4Z SIP installed.
N-Channel MOSFET – SOT-23	Q48,Q49, Q54,Q55	12, 14	FDV301N N-Channel MOSFET. Inverts the DC-DC enable signal from ASC GPIO for SIP.
Green LED	D51, D52, D55, D56	12, 14	LED to indicate output of DC-DC is active.
LED Bias Resistor	R185,R186, R189, R190	12, 14	470 Ohm resistor limits the LED current.
NPN Transistor – SOT-23	Q36,Q37,Q40, Q41	12, 14	2N3904 NPN Transistor drives LED on when DC-DC output is active.
NPN Bias Resistor	R193, R194, R197, R198	12, 14	4.7 kOhm resistor limits the base current of NPN transistor.
Tantalum Cap 1	C35, C37, C43, C45	12, 14	22 uF, 10 V capacitor +5 V DC-DC input filter.
Ceramic Bypass Cap	C83, C84, C86, C87,C95,C96, C98,C99	12, 14	100 nF 16 V capacitor +5 V DC-DC input and output filter.
Tantalum Cap[1]	C36, C38, C44, C46	12, 14	22 uF, 10 V capacitor +5 V DC-DC output filter.
DC-DC Output Load Resistor[1]	R82, R89, R110,R117	12, 14	470 and 330 Ohm resistors pull DC-DC output down to zero when disabled.
DC-DC 3 Trim Resistors[1]	R76 – R81	12	Resistor values based on Platform Designer Trim Calculator. Three installed.
DC-DC 4 Trim Resistors[1]	R83 – R88	12	Resistor values based on Platform Designer Trim Calculator. Three installed.
DC-DC 7 Trim Resistors[1]	R104 – R109	14	Resistor values based on Platform Designer Trim Calculator. Three installed.
DC-DC 8 Trim Resistors[1]	R111 – R116	14	Resistor values based on Platform Designer Trim Calculator. Three installed.
Ceramic Cap[1]	C82, C85, C94, C97	12, 14	10 nF 10 V capacitor: trim network filter.
Phoenix 2-Terminal Connector DC-DC 3 and 7	J19, J23	9	Wire to board connectors to apply off-board loads to DC-DC.
Phoenix 4-Terminal Connector DC-DC 4 and 8	J20, J24	9	Wire to board connectors to apply off-board loads to DC-DC with remote sensing.
Ground Sense Resistor	R13, R32	9	100 Ohm resistor: default ground sense connection when off-board sensing is not used.
VMON Series Resistor	R14, R59	9	100 Ohm resistor: default VMON connection when off-board sensing is not used.

Component / Signals	Ref. Des.	Schematic Sheet	Description
2x5 Header	J35	12	Header to connect PM bus controller for DC-DC convertors (DOSA supplies).
1x2 Header	J29	9	Jumper to provide +5 V to the DC-DCs from USB.
Signals			
A0_LED5		2, 11	DCDC1 enable signal from ASC0_GPIO5. Safe state is low.
A0_LED6		2, 11	DCDC2 enable signal from ASC0_GPIO6. Safe state is low.
A0_LED3		2, 12	DCDC3 enable signal from ASC0_GPIO3. Safe state is low.
A0_LED4		2, 12	DCDC4 enable signal from ASC0_GPIO4. Safe state is low.
A1_LED5		2, 13	DCDC5 enable signal from ASC1_GPIO5. Safe state is low.
A1_LED6		2, 13	DCDC6 enable signal from ASC1_GPIO6. Safe state is low.
A1_LED8		2, 14	DCDC7 enable signal from ASC1_GPIO8. Safe state is high.
A1_LED9		2, 14	DCDC8 enable signal from ASC1_GPIO9. Safe state is high.
TRIM_DCDC1		2, 11	DCDC1 Trim signal from ASC0_TRIM1.
TRIM_DCDC2		2, 11	DCDC2 Trim signal from ASC0_TRIM2.
TRIM_DCDC3		2, 12	DCDC3 Trim signal from ASC0_TRIM3.
TRIM_DCDC4		2, 12	DCDC4 Trim signal from ASC0_TRIM4.
TRIM_DCDC5		5, 13	DCDC5 Trim signal from ASC1_TRIM1.
TRIM_DCDC6		5, 13	DCDC6 Trim signal from ASC1_TRIM2.
TRIM_DCDC7		5, 14	DCDC7 Trim signal from ASC1_TRIM3.
TRIM_DCDC8		5, 14	DCDC8 Trim signal from ASC1_TRIM4.
OUT_DCDC1		2, 11	DCDC1 Output connected to ASC0_VMON1 via R1.
OUT_DCDC2		2, 11	DCDC2 Output connected to ASC0_VMON2 via R2.
OUT_DCDC3		2, 12	DCDC3 Output connected to ASC0_VMON3 via R3.
OUT_DCDC4		2, 9, 12	DCDC4 Output connected to ASC0_VMON4 via R4.
OUT_DCDC5		5, 13	DCDC5 Output connected to ASC1_VMON1 via R23.
OUT_DCDC6		5, 13	DCDC6 Output connected to ASC1_VMON2 via R24.
OUT_DCDC7		5, 14	DCDC7 Output connected to ASC1_VMON3 via R25.
OUT_DCDC8		5, 9, 14	DCDC8 Output connected to ASC1_VMON4 via R26.
DCDC4_SENSE		9, 12	DCDC4 Sense input connected to DCDC4 output via R14.
DCDC8_SENSE		9, 14	DCDC8 Sense input connected to DCDC8 output via R59.
DCDC1_SYNC – DCDC8_SYNC		4, 11 - 14	DOSA DC-DC Synchronization signals: support for operating the supplies at different phases to minimize switching noise from the primary supply.
PMBUS_SDA, PMBUS_SCL, SMB_ALERT		11 - 14	PM Bus control signals for DOSA DC-DC convertors.

1. Value is subject to change and/or may not be required based on customer design.

Generic Overview of Trim and Margin Operation

The Platform Manager 2 evaluation board can support up to eight DC-DC modules. All eight are similarly designed and laid out so we will detail the generic similarities rather than provide a separate section for each DC-DC. The Platform Manager 2 evaluation board provides two footprints for each DC-DC: one is for a Single Inline Package (SIP) and the other is for the Distributed Open Source Alliance (DOSA) compliant package. The SIP footprint is populated for DCDC3, DCDC4, DCDC7, and DCDC8. The other DCDC locations are unpopulated to support user evaluation of other DC-DC supplies of either footprint. In addition, all of the surrounding components are also unpopulated for DCDC1, DCDC2, DCDC5, and DCDC6 to support the design and evaluation of different devices and values with Platform Manager 2.

ASC0 (U1) is used to enable, monitor, and trim DCDC1 – DCDC4 which are located on the left side of the board and ASC1 (U4) is used to enable, monitor, and trim DCDC5 – DCDC8 which are located on the right side of the board. The top four DC-DC supplies are powered by +12 V (DCDC1, DCDC2, DCDC5, and DCDC6) while the bottom four DC-DC supplies are powered by +5 V (DCDC3, DCDC4, DCDC7, and DCDC8). The installed DC-DC supplies can only be powered and demonstrated using an off board +5 V source. For light loads the +5 V from the USB cable can be used by installing a jumper on J29, while heavier loads may require a bench supply connected to J12.

The Platform Manager 2 evaluation board provides footprints and circuit connections for six trimming resistors for each DCDC. These six resistors are shared by both the SIP and DOSA footprints because only one supply can be populated at a time. The resistors are organized in an “H” pattern both in the schematic and on the board layout. The resistors are named in the schematic to match the names used in the Platform Designer Trim-view calculator. The names are listed and described in Table 8 below. Typically only three resistors are suggested by the calculator; a pull up, a pull down, and a series resistor. The exact population of the “H” pattern depends on many factors that the calculator takes into account such as type of DC-DC, output voltage, and range of trim. The Platform Manager 2 evaluation board provides pads and connections to support any result from the Trim Calculator. However, with certain supplies and by adjusting the options, the calculator can produce a result that only uses two resistors: a pull down and a series resistor. The DC-DCs on the Platform Manager 2 Evaluation board are populated with the two resistor solution. A key requirement for the calculator to produce a two resistor solution is the Bi-Polar Zero (BPZ) voltage of the Trim Cell has to match the DC-DC’s internal reference voltage. Otherwise the calculator will add a pull up or pull down resistor in attempt to offset the imbalance and still keep the Trim DAC code near 80h (the BPZ value, halfway between –127 and +128). For more information on the Trim interface and Calculator please see AN6074 Interfacing the Trim Output of Power Manager II Devices to DC-DC Converters and the Platform Designer User Guide.

The Platform Manager 2 evaluation board uses two resistors for Rseries, Rs1 and Rs2, and places a 10nF capacitor in between them to form a low pass filter. The sum of Rs1 and Rs2 should equal the Rseries value calculated by Platform Designer. This filter network is recommended by some DOSA supply data sheets however, other supplies can also benefit from the additional filtering.

Table 8. Trim Resistor "H-Network" Names.

Schematic Name	Calculator Name	Description
RpupS	RpupSupply	Pull up resistor at DC-DC Trim input
RpdnS	RpdnSupply	Pull down resistor at DC-DC Trim input
Rs1	Rseries	Series resistor (½ between Trim DAC output and filter)
Rs2	Rseries	Series resistor (½ between filter and DC-DC Trim input)
RpupD	RpupDAC	Pull up resistor at Trim DAC output
RpdnD	RpupDAC	Pull down resistor at Trim DAC output

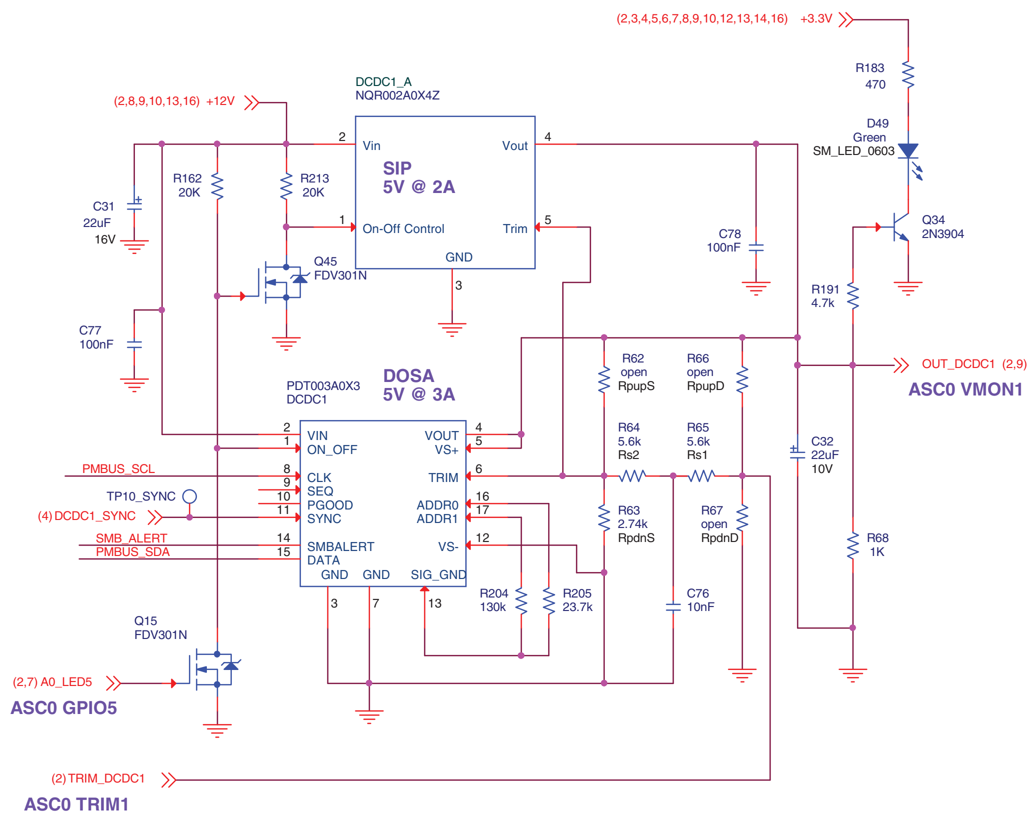
In order for the CLT circuits within the ASC to operate properly the output of the supply needs to be monitored by the correct VMON input. The Platform Manager 2 evaluation board illustrates the correct trimming connections by using TRIM1 with VMON1, TRIM2 with VMON2, all the way to TRIM4 with VMON4. As discussed in the Voltage Monitor Operation section, the DCDC outputs are connected to the VMON inputs using a series resistor with a value of 270 Ohms (see sheets 2 and 5). The series resistor is not required in customer designs; the only function on the evaluation board is to isolate the DCDC outputs from the VMON test points. The VMON series resistor allows another voltage source to be applied to the VMON test point directly. If the voltage source has a high output impedance, the VMON series resistor should be removed for accurate operation.

Each of the DCDC supplies has a dummy load resistor connected to the output. The dummy load resistor is not required in customer designs as the supply is connected to a real load. The dummy load resistor is only used on the evaluation board to prevent the output of the supply from “creeping up” when the supply is disabled. Without the dummy load resistor, an output of around 1 V can appear at the output of disabled supplies. The dummy load resistors are sized based on the target DCDC supply output voltage; lower values for lower voltages and higher values for higher voltages. In all circuits they are 1/10 watt packages because there is minimal heat generated.

DCDC1 – Enable and Trim Operation

In this section we will analyze the specific circuits that support DCDC1. The circuits for DCDC2, DCDC5, and DCDC6 are similar to DCDC1 and therefore will not be discussed in detail. In Figure 17 the control signal A0_LED5, which comes from ASC0’s GPIO5 output, is inverted and level shifted by a small signal N-channel MOSFET (Q15 FDV301N). For +12 V supplies a buffer or inverter is needed because the ASC GPIOs can only be pulled up to +5.5 V. All the GPIOs of the ASC have a “safe state” which defines the behavior independent of configuration during Power-On-Reset (POR) or during programming; the safe state of GPIO5 is low. The DOSA supply is enabled when the On-Off pin is low (negative enable logic), so the inverter Q15 prevents the supply from turning on during POR or programming. Similarly, the SIP supply is enabled when the On-Off pin is high (positive enable logic) so, the second MOSFET inverter Q45 prevents the SIP from turning on during POR or programming. Both MOSFETs use a 20k pull-up resistor to +12 V to insure a full logic swing at the enable inputs of the supplies.

Figure 17. Power On Indication, Enable, and Trim Circuits for DCDC1



The control signal A0_LED5 is also used to turn on a red LED (D7) when it is low and is pulled up to +3.3 V by a 2.2k Ohm resistor (RN11B see sheet 7). Because the installed supply could use either positive or negative enable logic, the illumination of LED D7 may not correspond to the supply being enabled. A separate green LED (D49) is used to indicate when the supply is enabled. An NPN transistor (Q34) is used to turn the green LED on when the supply has enough voltage to bias the emitter-base junction (slightly more than 0.7 V).

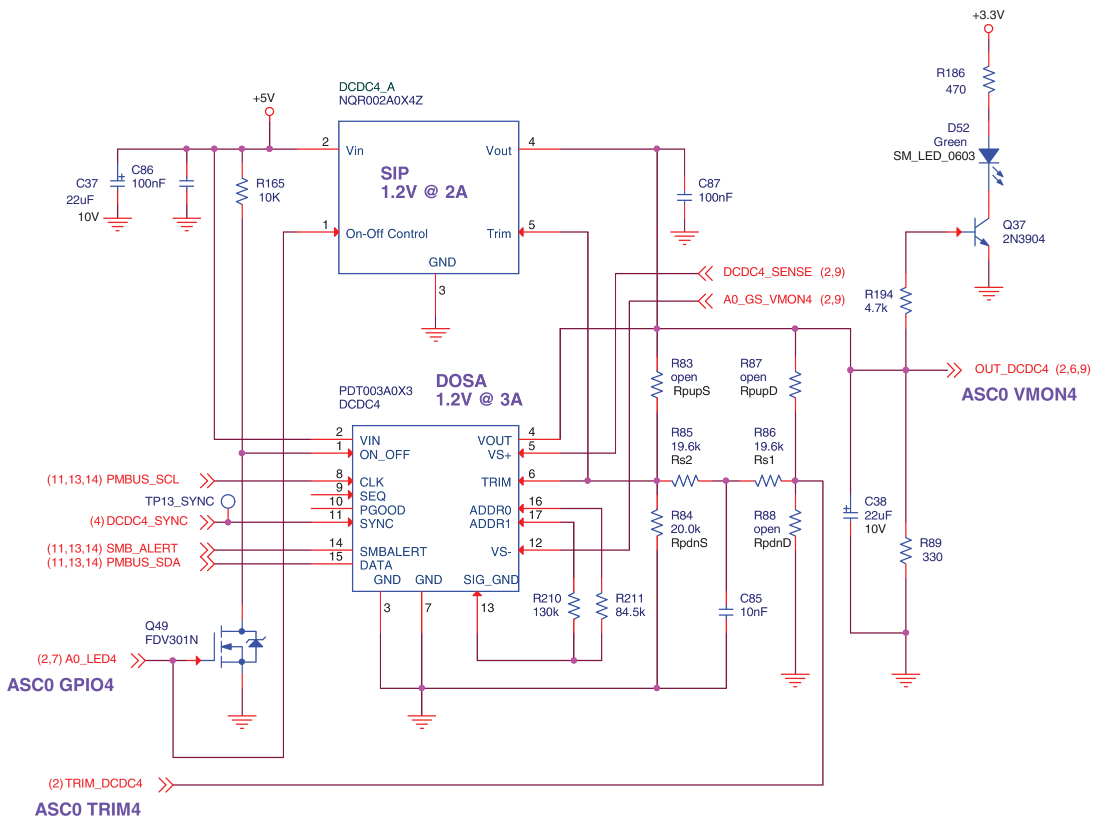
Supply filtering is provided by a 22 uF and 100 nF pair of capacitors, both at the input and output, that are located close to both DC-DC footprints to be effective for either. For DCDC1 the input capacitors are C31 and C77 while the output capacitors are C32 and C78. A load resistor (R68) is used to pull the DCDC output low when it is disabled. Note, these values may not be optimal for all supplies and loading conditions; specific filtering requirements should be followed from the supply data sheet.

All the DOSA supply footprints on the Platform Manager 2 evaluation board have provision to set the PMBus address with pull-down resistors; for DCDC1 these are R204 and R205. The PMBus signals (PMBUS_SDA, PMBUS_SCL, SMB_ALERT) are bussed to all the DCDCs and are brought out on connector J35. Each DOSA supply footprint also has a SYNC connection to demonstrate the PMBus feature of DC-DC phasing; where the switching circuits of different DC-DCs is synchronized out-of-phase to minimize the peak power requirements of the power source.

DCDC4 – Enable and Trim Operation

In this section we discuss the circuits for the +5 V input supplies with a focus on DCDC4. The circuitry for all the DCDCs is very similar, so this discussion will be limited to the key differences from the +12 V input supplies described in the previous section (DCDC1). The support circuits with DCDC4 are shown in Figure 18.

Figure 18. Power On Indication, Enable, and Trim Circuits for DCDC4



The circuits for DCDC3, DCDC7, and DCDC8 are similar to DCDC4 and therefore will not be discussed in detail. The significant difference from the circuit for DCDC1 shown in Figure 17 is the +5 V input supply power for DCDC4 instead of +12 V. At this voltage level the On-Off pin of the SIP can be connected directly to the GPIO4 output of ASC0 without the need for a buffer. The inverter (Q49) is still used to keep the DOSA supply turned off during POR and programming.

One other unique feature of DCDC4 (and DCDC8) is the support for remote sensing when the DOSA supply is installed after removing the SIP. The V+ and V- pins of the DOSA are routed to a four pin screw connecter (J20 and J24 on sheet 9) instead of directly to the output and ground. Resistors with the value of 100 Ohms (R13, R14 and R32, R59 on sheet 9) are used to connect the sense pins to the output and ground when off-board connections are not used. When a four-wire off board load is used, the 100 Ohms is bypassed by a direct short and the V+ and V- pins sense the voltage at the load.

One difference from Figure 18 for DCDC7 and DCDC8 is the connections for the enable inverter. Since the safe state for GPIO8 and GPIO9 is high-impedance, the inverter transistors are used on the SIPs for DCDC7 and DCDC8 instead of the DOSAs (see sheet 14).

Table 9 provides a summary of the installed DCDCs, the connections, logic levels, and voltages for a quick reference for designers.

Table 9. Summary of DCDC Trim Circuits.

DCDC	Package	Vin	Vout	Control Signal	ASC	GPIO	On Logic Level	VMON	RpdnS	Rseries
1[1]	n/a	12 V	n/a	A0_LED5	ASC0	GPIO5	n/a	1	n/a	n/a
2[1]	n/a	12 V	n/a	A0_LED6	ASC0	GPIO6	n/a	2	n/a	n/a
3	SIP	5 V	2.5 V	A0_LED3	ASC0	GPIO3	1	3	6.34k	22k
4	SIP	5 V	1.2 V	A0_LED4	ASC0	GPIO4	1	4	20k	39.2k
5[1]	n/a	12 V	n/a	A1_LED5	ASC1	GPIO5	n/a	1	n/a	n/a
6[1]	n/a	12 V	n/a	A1_LED6	ASC1	GPIO6	n/a	2	n/a	n/a
7	SIP	5 V	2.5 V	A1_LED8	ASC1	GPIO8	0	3	6.34k	22k
8	SIP	5 V	1.2 V	A1_LED9	ASC1	GPIO9	0	4	20k	39.2k

1. Values shown in the schematic for these DC-DC converters is for example only – they are not installed.

The Platform Manager 2 evaluation board has four DC-DC trim circuits that are unpopulated to allow customization and evaluation of different circuits and devices, Table 10 lists the un-installed components to support custom designs.

Table 10. Un-Installed Components for Closed Loop Trim Operation[1]

Components	Ref. Des.	Schematic Sheet	Description
DC-DC Converter	DCDC1, DCDC2	11	Dual-footprint +12 V input adjustable output power supply.
DC-DC Converter	DCDC5, DCDC6	13	Dual-footprint +12 V input adjustable output power supply.
N-Channel MOSFET – SOT-23	Q15 – Q18	11, 13	FDV301N N-Channel MOSFET. Inverts the DC-DC enable signal from ASC GPIO and shifts the level up to +12 V.
N-Channel MOSFET – SOT-23	Q45,Q47,Q51,Q53	11, 13	FDV301N N-Channel MOSFET. Inverts the DC-DC enable signal from DOSA to SIP.
Green LED	D49,D50,D53,D54	11, 13	LED to indicate output of DC-DC is active.
LED Bias Resistor	R183,R184,R187,R188	11, 13	470 Ohm resistor limits the LED current.
NPN Transistor – SOT-23	Q34,Q35,Q38,Q39	11, 13	2N3904 NPN Transistor drives LED on when DC-DC output is active.
NPN Bias Resistor	R191,R192,R195,R196	11, 13	4.7k Ohm resistor limits the base current of NPN transistor.
Tantalum Cap[2]	C31,C33,C39,C41	11, 13	22 uF, 16 V capacitor +12 V DC-DC input filter.
Ceramic Bypass Cap	C77,C78,C80,C81,C89, C90,C92,C93	11, 13	100 nF 16 V capacitor +12 V DC-DC input and output filter.
Tantalum Cap[2]	C32,C34,C40,C42	11, 13	22 uF, 10 V capacitor +12 V DC-DC output filter.
DC-DC Output Load Resistor[2]	R68,R75,R96,R103	11, 13	1k and 680 Ohm resistors pull DC-DC output down to zero when disabled.
DC-DC PMBus Address Setting Resistor[2]	R204 – R211, R218 – R225	11, 12,13, 14	Various resistor values to set PMBus address based on DOSA DC-DC data sheet.
DC-DC 1 Trim Resistors[2]	R62 – R67	11	Resistor values based on Platform Designer Trim Calculator. None installed.
DC-DC 2 Trim Resistors[2]	R69 – R74	11	Resistor values based on Platform Designer Trim Calculator.
DC-DC 5 Trim Resistors[2]	R90 – R95	13	Resistor values based on Platform Designer Trim Calculator.
DC-DC 6 Trim Resistors[2]	R97 – R102	13	Resistor values based on Platform Designer Trim Calculator.
Ceramic Cap[2]	C76, C79, C88, C91	11, 13	10 nF 10 V capacitor: trim network filter.
Phoenix 2-Terminal Connector DCDC 1, 2, 5, and 6	J17,J18,J21,J22	9	Wire to board connectors to apply off-board loads to DC-DC.

1. Not installed to allow customer development on the evaluation board.
2. Value is subject to change and/or may not be required based on customer design.

VID Operation

Voltage Identification (VID) is supported by Platform Designer and the Platform Manager 2 evaluation board. In the Platform Designer Voltage view, VID can be configured and added to any Trim output. The Platform Manager 2 evaluation board has DC-DC supplies, switches, and connections to support VID operation. Table 11 lists the components and signals associated with VID operation on the Platform Manager 2 board.

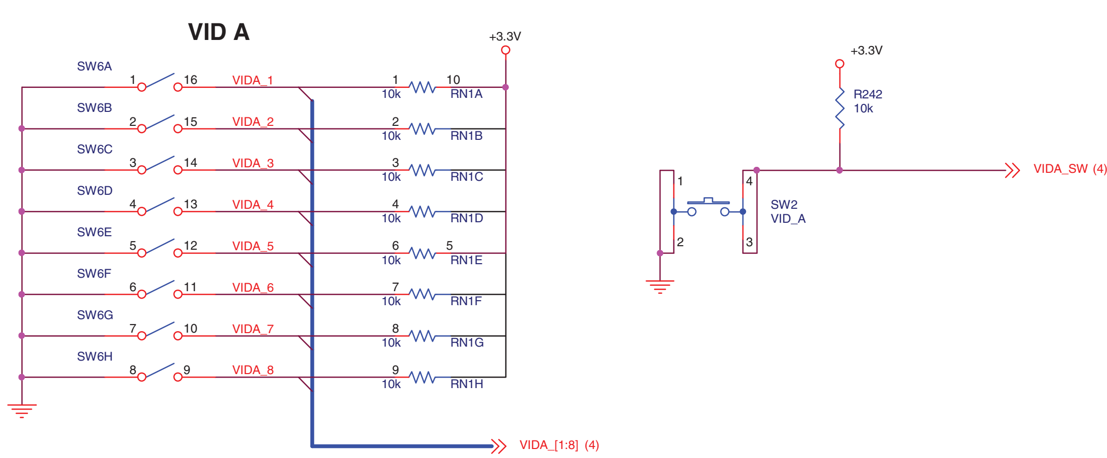
Table 11. Components and Signals for VID Operation

Components / Signals	Ref. Des.	Schematic Sheet	Description
Components			
DC-DC Convertor	DCDC3, DCDC4	12	Dual-footprint +5V input adjustable output power supply. NQR002A0X4Z SIP installed.
DC-DC Convertor	DCDC7, DCDC8	14	Dual-footprint +5V input adjustable output power supply. NQR002A0X4Z SIP installed.
DC-DC Trim Resistors [2]	R76 – R81, R83 – R88	12	Resistor values based on Platform Designer Trim Calculator. Three installed.
DC-DC Trim Resistors [2]	R104-R109, R111-R116	14	Resistor values based on Platform Designer Trim Calculator. Three installed.
8- position DIP switch[1]	SW6	6	Switch is used to change the VID Select Bus.
Push Button Switch[1]	SW2	6	Switch is used to create a VID strobe signal.
Signals			
VIDA_1 to VIDA_8		4, 6	Signals used as the VID Select Bus.
VIDA_SW		4, 6	Signal used to strobe the VID Select Bus into the VID IP.

1. Installed to allow demos and development on the evaluation board customer designs can use other methods.
2. Value is subject to change and/or may not be required based on customer design.

When VID is added to a Trim channel in Platform Designer the software adds the VID IP to the design. The function of the VID IP is to read the Select Bus when the strobe signal is active and then send the target voltage to the corresponding ASC via I^{2}C. The VID IP translates the Select Bus value to the target voltage using a look-up table that is defined in the Platform Designer software. The Closed Loop Trim (CLT) circuits within the ASC then drive the Trim DAC output pin which adjusts the DC-DC output to the target voltage as read by the VMON input pin. For a more complete explanation of VID operation please see AN6092, Implementing VID Function with Platform Manager 2.

Figure 19. Switches for VID



Two switches are provided on the Platform Manager 2 evaluation board as shown in Figure 19; one is an eight position piano-style DIP switch (SW6) and the other is a momentary push button switch (SW2). As seen in Figure 5, SW6 is located in the lower right of the board. When the switch lever is up the signal is high (1) and when the switch lever is down the signal is low (0). It is up to the design as to the number and order of the switch positions used to generate the VID Select Bus. The eight position switch can easily support two VID channels of four bits each or a slightly more complex design could use three bits to multiplex the strobe signal to eight VID channels and use the other five bits as a common VID Select Bus. The push button switch SW2 can be used to generate a falling edge “VID Strobe” signal which triggers the VID IP to sample the VID Select Bus and update the target voltage. For design support the VID signals are defined in the preference file listing in Appendix B.

Programming and Configuration

The two featured devices on the Platform Manager 2 evaluation board are the LPTM21 and L-ASC10 (U1 and U4). Both devices have non-volatile memory that can be erased and reprogrammed numerous times to support demos, development, and testing. They can also be configured from the SPI memory (U3). The primary method of reprogramming U1, U3, and U4 is with Diamond Programmer using a USB cable. Table 12 lists the components and signals associated with programming and configuring the LPTM21, L-ASC10, and SPI devices on the Platform Manager 2 evaluation board.

Table 12. Components and Signals for Programming.

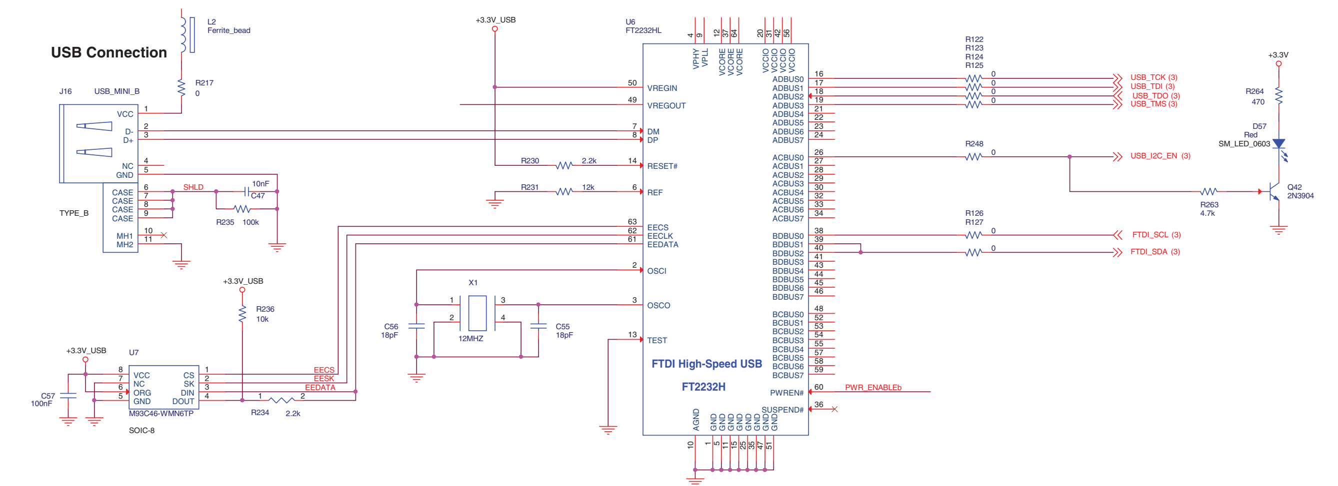
Components / Signals	Ref. Des.	Schematic Sheet	Description
Components			
USB connector	J16	15	USB Mini connector for connecting with USB cable (included).
FT2232H	U6	15	FTDI chip converts USB to JTAG signal for programming U1 directly and U4 via the JTAG to I^2C bridge within U1; also ASC2 and ASC3 if connected. The FTDI device also converts USB to I^2C for software utilities.
JTAG Enable Pull-up Resistor	R158	3	4.7k Ohm Resistor. Connected between +3.3 V and JTAGENAB pin of LPTM21.
Zero Ohm Jumper1	R122 – R125	15	Zero Ohm Resistor. Connects FTDI to JTAG signals. Remove to disconnect U6 from JTAG.
Zero Ohm Jumper1	R126 – R127	15	Zero Ohm Resistor. Connects FTDI to I^2C bus. Remove to disconnect U6 from I^2C bus.
Zero Ohm Jumper1	R248	15	Zero Ohm Resistor. Connects I^2C-Enable signal to FTDI. Remove to use J33 in manual mode.
Red LED	D57	15	Red LED indicates when FTDI U6 is the I^2C master.
LED Bias Resistor	R264	15	470 Ohm Resistor. Limits the current in D57 when Q42 is on.
LED Drive Transistor	Q42	15	2N3904 NPN Transistor. Drives LED D57 on when USB_I2C_EN signal is active.
Transistor Bias Resistor	R263	15	4.7k Ohm Resistor. Sets the base current of Q42.
I^2C MUX1	U10, U11	3	FSA4157 Analog Switch. Used to disconnect the FTDI I^2C ports from the bus when FTDI is not the master.
I^2C Address Resistor	R27	5	A pull down resistor of 2.2K connected to I2C_ADDR pin of L-ASC10. This sets the LSBs for I^2C slave (L-ASC10) address to ”001”.
Atmel 4MB Flash Memory1	U3	3	SPI Flash memory to store “Golden Bitstream” for Dual Boot Programming operation.
2 x 1 Header	J33	3	Unpopulated header provides manual control of USB_I2C_EN.

Components / Signals	Ref. Des.	Schematic Sheet	Description
8 x 1 Header	J2	3	Unpopulated header provides JTAG access for optional programming with JTAG cable (not included).
8 x 1 Header	J26	3	Unpopulated header provides access to I²C and SPI signals.
Signals			
USB_TCK, USB_TMS, USB_TDO, USB_TDI		3, 15	The 4 JTAG signals for programming LPTM21 and ASC devices via the JTAG to I²C bridge within U1.
USB_I2C_EN		3, 15	Controls the I²C MUX. When this signal is high the I²C pins of the FTDI device U6 are connected to the I²C bus.
FTDI_SDA, FTDI_SCL		3, 15	Branch off the main I²C bus connected using a MUX.
SPI_CS0, SPI_CLK, SPI_IN, SPI_OUT		3	Bus between memory and SPI port of LPTM21 for Dual boot programming operation.

1. Not required for customer designs; this is only needed to support demonstrations on the evaluation board.

The Platform Manager 2 evaluation board provides both a JTAG and I²C programming interface for LPTM21 and L-ASC10. A portion of the schematic which supports programming is shown in Figure 20 below.

Figure 20. USB Programming Interface



The mini-USB connector (J28) provides the USB connection to a computer running Lattice Diamond Programmer software. The FTDI device (U6) provides the interface between USB and JTAG signals (on AD BUS) and I²C signals (on BD BUS). The FPGA within the LPTM21 device is programmed directly from the JTAG signals. All the ASC devices are programmed over the I²C bus using the LPTM21 built in JTAG to I²C bridge. When the LPTM21 device is the I²C master the MUX is needed to disconnect the I²C pins of the FTDI device (U6) from the bus. This is because the FTDI pins do not support multi-master mode and will load down the bus and prevent proper operation. The MUX can be controlled either by the FTDI device (U6 - bit 0 on the AC BUS) or the jumper J33 setting the level of USB_I2C_EN. The Platform Manager I²C Software Utility controls the MUX automatically. When other software is used that does not drive the USB_I2C_EN signal, the user must control the MUX manually with J33. When the signal USB_I2C_EN is high the I²C pins of the FTDI device (U6) are connected to the I²C bus and the red LED (D57) is illuminated.

The zero Ohm resistors (R122 – R127) connected to the FTDI device (U6) pins are installed to support the on board connections. If off-board JTAG or I^2C sources are used the zero Ohm resistors should be removed to prevent the I/O pins of the FTDI device (U6) from loading down the signals.

To support dual boot the 4Mbit SPI Flash Memory device (U3) is connected to the SPI pins of the LPTM21 device (U1). The memory is programmed using Diamond Programmer and the JTAG to SPI interface built into the FPGA of U1. The SPI signals are also brought out to the unpopulated header J26 to support alternate programming sources.

On sheet 5 the LSBs of the I^2C slave address for the L-ASC10 device (U4) are determined by the value of resistor R27 connected between the I2C_ADDR pin and ground. The 2.2k Ohm resistor value corresponds to ASC1 and LSBs of “001”.

For additional information regarding programming the LPTM21 and L-ASC10 please refer to AN6091, Powering Up and Programming Platform Manager 2 and L-ASC10.

Dual Boot Operation

The Platform Manager 2 devices are designed to support field updates. In the event that an update is terminated prematurely either by power outage or communication interruption, a back-up boot image can be recalled from the SPI flash memory. This back-up boot image is called the default or “Golden” bit-stream and is used to boot the LPTM21 and L-ASC10 devices. Thus the system can operate from this default design at a basic support level until another field update can be completed. Table 13 lists the components and signals associated with the dual boot operation.

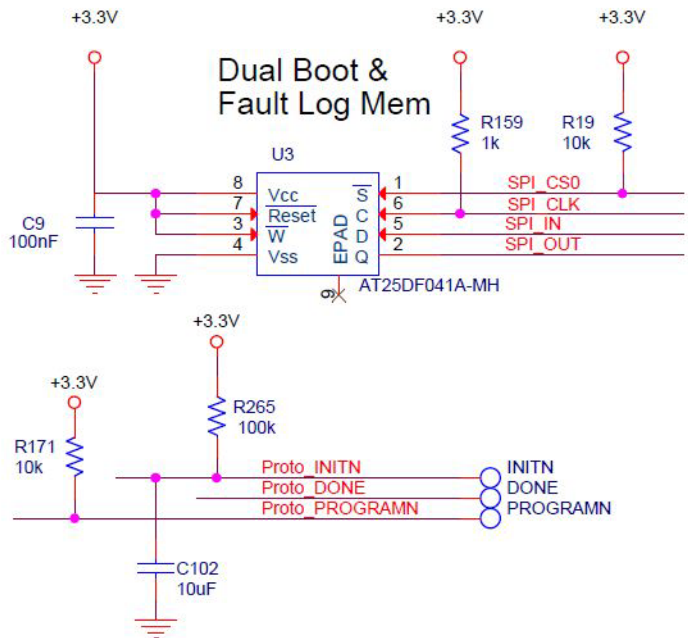
Table 13. Components and Signals for Dual Boot Operation.

Components / Signals	Ref. Des.	Schematic Sheet	Description
Components			
Atmel 4MB Flash Memory	U3	3	SPI Flash memory to store “Golden” bit-stream for Dual Boot Programming operation. This is the same memory that is used for Fault Logging.
Pull-up Resistor	R159	3	1k Ohm Resistor. Strong pull-up is required for SPI Clock.
Pull-up Resistor	R19	3	10k Ohm Resistor. Weak pull-up is required for SPI Chip Select.
RC Delay Resistor	R265	3	100k Ohm Resistor. Used to delay INITN pin of LPTM21 during power up.
RC Delay Capacitor	C102	3	10 uF Capacitor. Used to delay INITN pin of LPTM21 during power up.
Signals			
SPI_CS0, SPI_CLK, SPI_IN, SPI_OUT		3	SPI signals to read the “Golden” bit-stream from the external memory into the LPTM21 and L-ASC10 devices.
Proto_INITN		3	Signal used to delay the external boot process of the LPTM21.

Dual boot support requires two key circuits which are shown in Figure 21; 1) a memory device to store the “Golden” bit-stream and 2) a delay circuit to prevent reading data from the SPI memory at power-on when the supply is still ramping up. A simple RC delay circuit is all that is needed to prevent the LPTM21 from reading the “Golden” bit-stream from the SPI memory until the supply is stable. The Platform Manager 2 evaluation board is built with the RC delay circuit attached to the INITN pin. However, either the INITN pin or the PROGRAMN pin can be used to delay the configuration. Without the delay the LPTM21 and SPI memory may come out of power-on-reset (POR) at different voltage levels and the data transfer between them can be corrupted causing the configuration to fail. The

SPI memory (U3) should be connected to the SPI pins of the LPTM21 (U1) with short and similar length traces as the clock frequency is around 25 MHz. Because the drive strength of the clock and chip select pins on the LPTM21 are similar, the SPI_CLK signal has a more substantial pull-up (R159) than the SPI_CS0 signal (R19) in order to improve the reliability of the interface with the SPI memory. For more information on the dual boot operation please see TN1284, Dual Boot and Background Programming with Platform Manager 2.

Figure 21. Dual Boot Circuitry



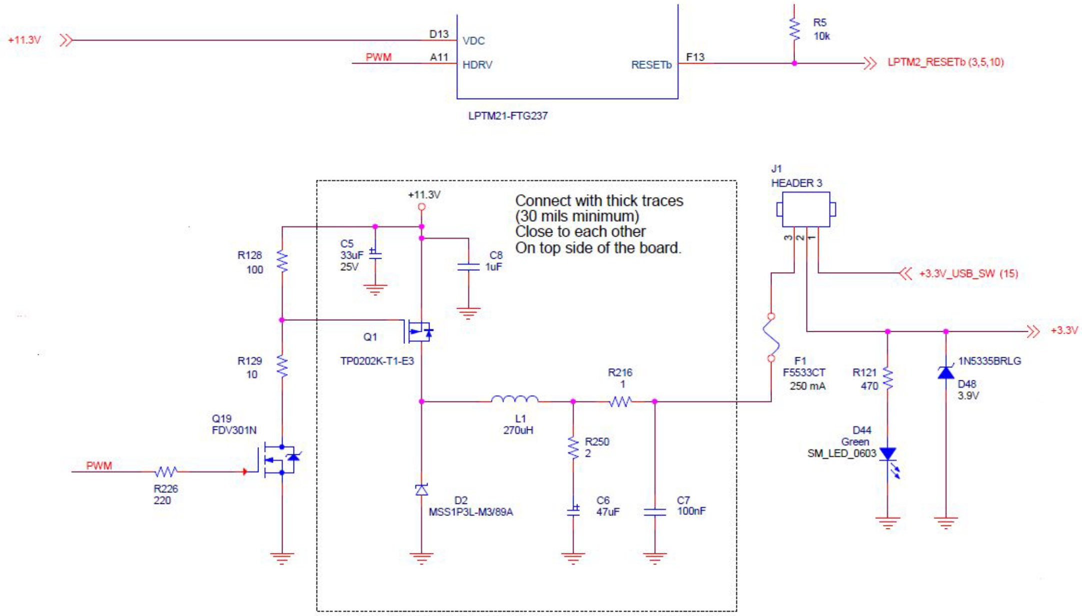
12 V Buck Converter Operation

A key feature of the LPTM21 (U1) device is the built-in control circuitry to implement a DC-DC Buck converter. It only takes a few external components connected to the LPTM21 to implement a regulated step-down DC-DC Buck converter with an output of +3.3 V. The Buck converter can operate with an input voltage ranging from 13.2 V down to 4.5 V. The components used on the Platform Manager 2 evaluation board are designed for a typical load of 200 mA; this is more than enough power for the on-board devices and one L-ASC10 evaluation board. The components and signals associated with a Buck converter operation on the Platform Manager 2 evaluation board are listed in Table 14 below.

Table 14. Components and Signals for 12 V Buck Converter.

Components / Signals	Ref. Des.	Schematic Sheet	Description
Components			
Fast MOSFET Switch	Q1	2	TP0202K-T1-E3 P-Channel MOSFET power switch for Buck converter operation.
Q1 Driver MOSFET	Q19	2	IRLML2803TRPBF N-Channel MOSFET signal switch that drives Q1.
Schottky Diode	D2	2	Schottky Diode for Buck converter operation.
Power Inductor	L1	2	270 uH Inductor for Buck converter operation.
Q1 Drive Resistor	R129	2	10 Ohms Resistor, Limits peak drain current for Q19 and sets bias voltage for Q1.
Q1 Drive Resistor	R128	2	100 Ohms Resistor, Sets bias voltage and turns Q1 off quickly.
Filter Capacitor	C6	2	47 uF Capacitor, output low-pass filter.
Filter Capacitor	C7	2	100 nF Capacitor, output low-pass filter.
RC Filter Resistor	R250	2	2 Ohms Resistor, output low-pass filter.
RC Filter Resistor	R216	2	1 Ohm Resistor, output low-pass filter.
Capacitor	C5	2	35 uF Capacitor, input filter.
Filter Capacitor	C8	2	1 uF Capacitor, input filter.
Q19 Gate Resistor	R226	2	220 Ohms Resistor, limits drive current for PWM signal and reduces Q19 parasitic oscillations.
Fuse	F1		250mA Fast-blow Fuse, Protects Buck converter from short and +3.3 V loads from over-voltage.
Zener Diode	D48	2	3.9V Zener Diode, protects all 3.3V devices in the event of short across Q1 or other malfunction where too high a voltage is applied to the +3.3V bus.
3 x1 Header	J1	2	Jumper to select the board's +3.3 V source; The Buck converter output (2-3), The USB regulator (1-2), off board supply (open).
2 x 1 Header	J3	4	Jumper to connect the +3.3 V Buck converter output to the LPTM21 supply pins for feedback control of the PWM. This jumper can also be replaced with an Ammeter to measure the U1 current during operation.
Signals			
PWM		2	215 kHz Buck converter PWM drive signal output from the HDRV pin of LPTM21 U1
+11.3 V		2, 9, 10	Diode OR'd supply from various +12 V sources. Provides power for Buck converter operation and VDC pin of LPTM21 U1.
+3.3 V		2, 4, (All)	The output of the Buck converter is monitored by the supply pins of U1 to close the feedback loop and adjust the PWM duty cycle.

Figure 22. +12V Buck Converter Circuit



The Buck converter circuit shown in Figure 22 shows how a 12V source can be used to provide the 3.3 V required for the LPTM21 and supporting circuits (external ASC and SPI memory). The circuit is designed to provide approximately 200mA which is more than enough for most Platform Manager 2 demonstrations using this board.

Because this is an evaluation board, and it is likely that component values may be changed, the +3.3 V bus is protected using a 250 mA fast-blow fuse (F1) and 3.9V Zener diode (D48). If the wrong device is installed for Q1 or a short from drain to source occurs then 11 V or more would be applied to the +3.3 V bus. In such a case, the Zener diode will limit the voltage and cause the current to exceed the rating of the fuse and the devices on the +3.3 V supply bus will be protected. It is recommended that customer designs include these protection devices (F1 and D48) at least for prototypes; then in production the fuse could be replaced with a zero Ohm jumper (a resistor in parallel with the fuse) and the Zener could be left off the board, if cost is an issue. Note that a 3.6V Zener has significant leakage at 3.3 V which is why the 3.9 V Zener diode is used.

The Buck converter in Figure 22 is powered by +11.3 V because there are numerous +12 V sources on the board which may or may-not be used as part of a demo design. Thus, all the +12 V sources connect to the +11.3 V bus with a small diode so the Buck converter can be active no matter where the +12 V is supplied from. The VDC pin of LPTM21 U1 is powered by the +11.3 V and enables the Buck converter control circuits to drive the external power-switch (Q1) and monitor the +3.3 V supply pins.

As in most DC-DC converters one design goal is to minimize turn-on and turn-off times of the N-channel power MOSFET (Q1). This is accomplished in a cost effective manner using low impedance resistors and a P-channel driver MOSFET (Q19). The 100 Ohms of R128 rapidly drains the charge from the gate of Q1 when Q19 is turned off which will quickly turn Q1 off. Similarly the 10 Ohms of R129 quickly charges the gate of Q1 for a fast turn on time. The divider ratio of the two resistors is 1:10. This provides ample bias voltage for Q1 to reach saturation, which is also a desirable goal in DC-DC converters. By minimizing the turn-on and turn-off times and by driving Q1 into saturation the power loss is low enough that a SOT-23 device can be used as the Buck converter power-switch.

The rest of the Buck converter components (L1, D2, C6, and C7) perform their standard functions. The inductor L1 stores energy when Q1 is on. The ‘catch diode’ D2 provides a low-loss path for the inductor L1 to dump the energy when Q1 is off. The output filter C6 and C7 hold the energy for the load to use. The unique feature of this output filter is the integration of a two pole low-pass filter. R250 with C6 form a low-pass filter with a corner frequency around 1.7 kHz and R216 with C7 form a low pass filter with a corner frequency around 1.6 MHz. The net effect of the combined filters is a very low ripple (typically less than 30 mV-pp) on the output which is most desirable when powering the analog circuits within LPTM21 and L-ASC10.

When J1 has the shorting jumper installed on pins 2-3 then the green LED (D44) will indicate that the Buck converter is operational.

Power Supplies

The Platform Manager 2 evaluation board has multiple options to power the board. The power provided over the USB cable is sufficient for most demos, programming, and evaluation. However, USB is typically only able to supply 5 V at 500 mA. To support evaluations that require more current or higher voltage a variety of connections are available around the board for other power sources and loads. Table 15 lists the components and signals associated with the power supplies and connections on the Platform Manager 2 evaluation board.

Table 15. Components and Signals for the Power Supplies

Components / Signals	Ref. Des.	Schematic Sheet	Description
Components			
USB mini interface	J16	15	USB connecter to provide +5 V for the board operation. Board is functional with this interface.
Low Drop Out (LDO) Linear Regulator	U8	15	Generates +3.3 V supply for the board from the USB +5 V power.
12 V Buck Regulator	n/a	2	Circuit and components described in DC-DC Converter section.
3 x 1 Header	J1	2	Jumper to select either Buck converter output or LDO output for +3.3 V supply or neither when using J13.
Phoenix 2-Terminal Screw Connector 1	J13	9	Wire to board connector. For use with a bench supply for +3.3 V.
2 x 1 Header1	J3	4	Jumper to provide +3.3 V to LPTM21 (U1). Can also be used as test points to measure current drawn by U1.
2 x 1 Header1	J4	5	Jumper to provide +3.3 V supply for L-ASC10 (U4). Can also be used as test points to measure current drawn by U4.
Coaxial PWR Jack 1	J28	9	External +12 V supply from wall adapter.
Phoenix 2-Terminal Screw Connector 1	J25	9	Dual function. For off-board +12 V hot-swap load or to provide +12 V from a bench supply to power the board.
Phoenix 2-Terminal Screw Connector 1	J12	9	Dual function. For off-board +5 V hot-swap load or to provide +5 V from a bench supply to power the board.
Phoenix 2-Terminal Screw Connector 1	J13	9	To provide +3.3 V from a bench supply to power the board.
Transient Suppressor	D45	9	Transient Voltage suppressor to protect the board from inductive spikes.
Schottky Diodes	D37,D46	9	To implement Power Supply OR-ing between +12 V and +5 V supplies with a minimal voltage drop (typically 0.4 V).
2 x 1 Header 1	J29	9	Jumper to connect USB +5 V to DCDC3, DCDC4, DCDC7, DCDC8, ASC Interface, and Fan connectors.
Signals			
+3.3 V		2 - 16	3.3 V supply to the whole board
+3.3V_UB_SW		2, 15	3.3 V generated by LDO from USB power.

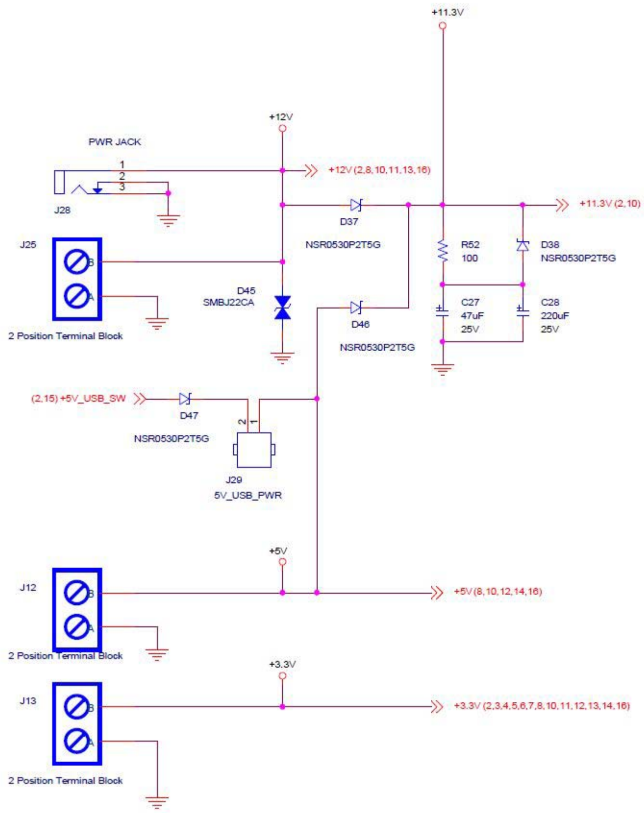
Components / Signals	Ref. Des.	Schematic Sheet	Description
+5 V		8,10,12, 14,16	Supply for DCDC3, DCDC4, DCDC7, DCDC8, ASC Interface and Fan connectors. Can be the supply for built in Buck Converter. Also the load side of the ASC evaluation board +5 V in a hot swap demo.
+11.3 V		2, 10	Supply to VDC pin of LPTM21 for Buck Converter operation.
+12 V		2,8,10,11, 13, 16	Supply for DCDC1, DCDC2, DCDC5, and DCDC6. Also supply for built in Buck Converter. Also the load side of ASC evaluation board +12 V hot swap demo.

1. Not required for customer designs; this is only needed to support demonstrations on the evaluation board.

For most applications the Platform Manager 2 board can simply be powered by the +5 V supply from the USB connection. J29 can be installed to provide power to the DC-DCs for low power loads. D47 is a protection diode for the USB interface in the event that +5 V is supplied to the board from another source. The Buck Regulator (described in the previous section) should not be powered from the USB through the series of diodes (D47 and D46). The combined diode drops with a marginal USB supply may provide too low a Voltage for proper Buck Regulator operation. The Buck Regulator can operate with single Schottky diode drop (D46) when the +5 V bus is powered by J12 or the ASC Interface connectors (discussed in the next section).

When additional power or operation from a bench power supply is required several connectors and jumpers are available on the Platform Manager 2 board. A variety of options are available for operation from +12 V. Power can be supplied from J28, J25, or the ASC interface connectors. J25 can also be used to attach an off board load when +12 V is supplied from the ASC Interface connectors. As shown in Figure 23 a Transient Voltage suppressor [D45] is mounted on the board to absorb high voltage spikes from either the +12 V supply itself or from inductive spikes produced from an over-current shut-down by the hot swap circuits on the ASC evaluation board connected to the ASC Interface connector.

Figure 23. Platform Manager 2 Evaluation Board Power Supply Connections



To ensure reliable operation of the board, power supply ORing is implemented using diodes D37 and D46 between +5 V and +12 V supply. The +11.3 V after diode drop from +12 V is connected to VDC input of LPTM21 for Buck Regulator operation. The Hot swap demonstration might require high current therefore external +5 V should be used, the +5 V from USB should be disconnected by removing jumper J29.

ASC Interface Connectors

The Platform Manager 2 evaluation Board has two DB25 connectors that are designed to interface with L-ASC10 evaluation Boards. Table 16 lists the components and signals associated with the interface connectors.

Table 16. Components and Signals for ASC Interface Connectors

Components / Signals	Ref. Des.	Schematic Sheet	Description
Components			
DB 25 Pin Connector	J14	10	DSUB 25 pin connector to plug-in ASC2 evaluation board.
DB 25 Pin Connector	J15	10	DSUB 25 pin connector to plug-in ASC3 evaluation board.
2 x 1 Header	J31	10	Jumper to bypass the hot swap / soft start circuits and provide +3.3 V supply for programming ASC2 evaluation board.
2 x 1 Header	J32	10	Jumper to bypass the hot swap / soft start circuits and provide +3.3 V supply for programming ASC3 evaluation board.
Zero Ohm Jumper	R172 – R179	10	Zero Ohm Resistor. Allows the LED drive signals to support the ASC evaluation board hot swap signals.
I^2C Series Resistor	R257 – R260	10	22 Ohm Resistor. Passive buffer to isolate the ASC evaluation board and connector from the I^2C bus.
Signals			
(See Table 18 for the signal names and descriptions)			

The ASC2 interface connector J14 and associated circuitry are shown in Figure 10. The ASC3 interface connector J15 and associated circuitry are shown in Figure 11. Both circuits include a two pin jumper (J31 and J32) that must be installed to provide +3.3 V to the interface ASC boards for programming. During programming the HVOUT pins of U1 and U4 will be in safe state (weak pull down) so Q13 and Q14 will be turned off. Also the jumper must be in place if the +3.3 V power is provided from an ASC evaluation board; such as in a +12 V hot swap demo. The ASC Breakout Boards are programmed via the I^2C signals on the DB25 connector. The ASC devices are integrated into the system using the ASC-I/F signals that connect to the FPGA of U1, also on the DB25 connector. The +12 V and +5 V signals use multiple pins for handling higher currents. Further details of the interface connector pins and signals are provided in Table 17. The ASC interface connectors help demonstrate the concept of scalable architecture using In-System Programmable Hardware Management Expanders (L-ASC10 devices).

Table 17. ASC Interface Connector Pin Descriptions

Pin #	Name	Description
1	GND	Common ground for all boards.
2	ASC_WDAT	ASC-I/F Signal – is connected to FPGA PIO and must be assigned in Diamond
3	ASC_RDAT	ASC-I/F Signal – is connected to FPGA PIO and must be assigned in Diamond
4	ASC_WRCLK	ASC-I/F Signal – is connected to FPGA PIO and must be assigned in Diamond
5	MANDATORY_RESET	RESETb signal from ASC evaluation board. Wire-ORed with ASC0 and other mandatory ASC's RESETb pins and is connected to FPGA PIO pin and must be assigned Diamond.
6	GND	Common ground for all boards.
7	I2C_WRITE_EN	Connected to GPIO1 on ASC evaluation board for optional ASC Write Protect feature. It is connected to FPGA PIO and must be assigned in Diamond if this feature is used.
8	ASC_CLK	8 MHz Clock Output from ASC0. Not used on Platform Manager 2 evaluation board; LPTM21 uses the 8 MHz clock from internal ASC0.
9	+3.3V	Common +3.3 V supply rail. Can be provided by either ASC evaluation board or Platform Manager 2 evaluation board.
10	+11.3V	Common +11.3 V supply. It is the pre hot swap supply from ASC evaluation board and is used by LPTM21 Buck converter. It is generated from multiple diode ORing supplies both on ASC evaluation board and Platform Manager 2 evaluation board.
11	+12V_HS	Common +12 V supply rail. Output from 12 V hot swap circuit or input for DCDC1 and DCDC2 on ASC evaluation board.
12	+5V_HS	Common +5 V supply rail. Output from 5 V hot swap circuit or input for DCDC3 and DCDC4 on ASC evaluation board.
13	GND	Common ground for all boards.
14	ASC_12V_OC_SHUTDOWN	Connected to fast shutoff transistor of 12 V hot swap circuit on ASC evaluation board. Driven from an output of the FPGA.
15	12V_OC_SENSE	Output from ASC HIMONN_HVMON on ASC evaluation board. Used as fast shutdown alarm for 12 Volt hot swap demo. Connected to an input of the FPGA.
16	GND	Common ground for all boards.
17	OPTIONAL_RESET	RESETb signal from ASC evaluation board. Is connected to individual FPGA PIO and must be assigned in Diamond.
18	I2C_SCL	I^2C Clock Signal.
19	I2C_SDA	I^2C Data Signal.
20	ASC_5V_OC_SHUTDOWN	Connected to fast shutoff transistor of 5V hot swap circuit on ASC evaluation board. Driven from an output of the FPGA.
21	5V_OC_SENSE	Output from ASC IMON1 on ASC evaluation board. Used as fast shutdown alarm for 5 Volt hot swap demo. Connected to an input of the FPGA.
22	ASC_BOARD_PRESENT	Grounded on ASC evaluation board and connected to an input of the FPGA to sense when the board is attached or removed.
23	+12V_HS	Common +12 V supply rail. Output from 12V hot swap circuit or input for DCDC1 and DCDC2 on ASC evaluation board.
24	+5V_HS	Common +5 V supply rail. Output from 5V hot swap circuit or input for DCDC3 and DCDC4 on ASC evaluation board.
25	+5V_HS	Common +5 V supply rail. Output from 5V hot swap circuit or input for DCDC3 and DCDC4 on ASC evaluation board.

I²C Bus

The Platform Manager 2 evaluation board supports an I²C bus with multiple masters, slaves, and connectors. This bus is used to program the ASC devices, dynamically reconfigure the ASC devices, customize the sequence, and monitor status and signals. Table 18 lists the components and signals associated with I²C bus on the Platform Manager 2 evaluation board.

Table 18. Components and Signals of I²C Bus.

Components / Signals	Ref. Des.	Schematic Sheet	Description
Components			
LPTM21	U1	2, 3, 4	**Master:** JTAG to I²C bridge is used to program the ASC devices; also the FPGA logic can read and control the ASC devices from here. **Analog Slave:** Programming connection for ASC0. **Logic Slave:** Soft I²C interface to the FPGA control logic.
FT2232H	U6	15	FTDI chip converts USB to either JTAG or I²C based on the software being used. The ACBUS0 pin can be used to automatically connect the FTDI pins to the I²C bus.
Pull Up Resistors	R15, R16	3	2k Ohm Resistors. Slightly stronger than typical pull-up to match the series and filter resistors used by U1.
Filter Resistors	R180,R181	3	150 Ohm Resistors. Provide an RC low-pass glitch filter with C73 and C72.
Filter Capacitor	C72	3	120 pF Capacitor. About 18 ns delay with R181 for primary SDA of U1. Slightly shorter delay on Data than Clock to prevent false re-starts.
Filter Capacitor	C73	3	150 pF Capacitor. About 22.5 ns delay with R180 for primary SCL of U1. Slightly longer on Clock than Data to prevent false re-starts.
Series Resistor	R253,R254	3	50 Ohm Resistors. Isolates the filter capacitor from the I²C pins when U1 is driving the bus, and provides secondary noise filter when U1 receiving from the bus.
Filter Resistors	R240,R241	4	150 Ohm Resistors. Provide an RC low-pass glitch filter with C100 and C101.
Filter Capacitor	C100	4	120 pF Capacitor. About 18 ns delay with R241 for secondary SDA of U1. Slightly shorter delay on Data than Clock to prevent false re-starts.
Filter Capacitor	C101	4	150 pF Capacitor. About 22.5 ns delay with R240 for secondary SCL of U1. Slightly longer on Clock than Data to prevent false re-starts.
Series Resistor	R251, R252	4	50 Ohm Resistors. Isolates the filter capacitor from the I²C pins when U1 is driving the bus, and provides secondary noise filter when U1 receiving from the bus.
Series Resistors	R20, R21, R232, R233, R255, R256, R257, R258, R259, R260	2, 3, 5, 6	22 Ohm Resistor. Isolates the bus capacitance from the I²C pins, provides minor noise filtering, and can be removed to disconnect selected devices from the bus; either for development or debugging.
Analog Mux	U10, U11	3	Used to disconnect the FTDI I²C pins from the bus during programming.
2- pin header	J33	3	When installed enables FTDI I²C interface.

Components / Signals	Ref. Des.	Schematic Sheet	Description
NPN Transistor – SOT-23	Q42	15	2N3904 NPN Transistor drives LED (D57) on when FTDI pins are connected to the I^2C bus.
Red LED	D57	15	Illuminates to indicate the FTDI pins are connected to the I^2C bus.
LED Bias Resistor	R264	15	470 Ohm Resistor. Limits the current in D57.
NPN Bias Resistor	R263	15	4.7k Ohm Resistor. Limits the base current of Q42.
Signals			
USB_I2C_EN		3, 15	FTDI I^2C MUX control signal. High to connect the FTDI I^2C pins to the bus; Low to isolate the FTDI I^2C pins from the bus. Controlled by U6 and software or J33.
FTDI_SDA,			
FTDI_SCL		3, 15	FTDI I^2C bus signals.
I2C_SCL,			
I2C_SDA		2, 3, 5, 10	I^2C bus signals.

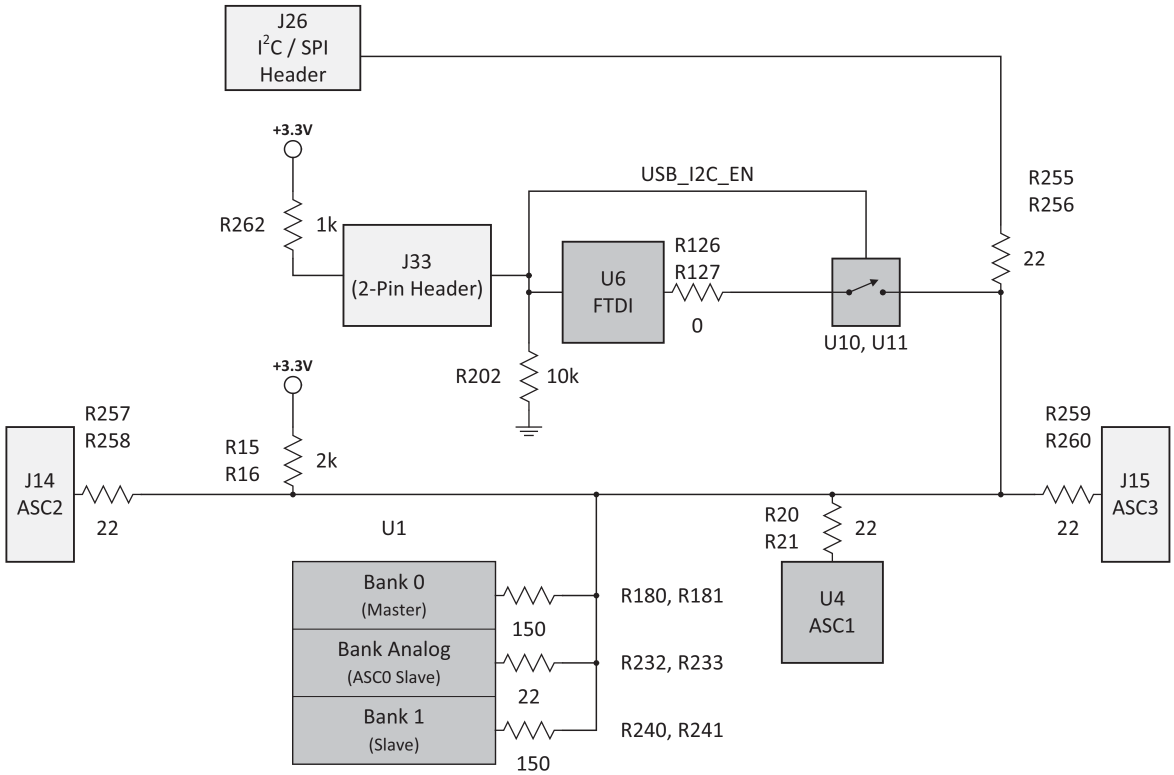
Programming the ASC Devices

The primary function of the I^2C bus on the Platform Manager 2 evaluation board is to program the on-board and off-board ASC devices. Diamond Programmer will send the programming data over the USB connection (J16) to the FTDI (U6) device which drives the JTAG signals into the LPTM21 (U1). The LPTM21 device has a JTAG to I^2C bridge that translates the data from the JTAG connections to the I^2C Master in Bank 0 (note JTAG signals are not shown in Figure 22 to place focus on the I^2C Bus route). The following ASC devices can be programmed Via I^2C: ASC0 within U1, ASC1 (U4), ASC2 via J14, and ASC3 via J15. The I^2C pins of the FTDI (U6) device are not fully I^2C compliant. Specifically they do not support multi-master mode and must be disconnected from the bus when not in use. That is the function of two solid state switches U10 and U11; they only connect the FTDI I^2C pins to the bus when U6 is the master.

Demo and Debugging Software

The I^2C Demo and Debugging Software for the Platform Manager 2 evaluation board is available for download from the Lattice website. This software automatically drives the USB_I2C_EN signal to connect the FTDI I^2C pins to the bus. The software configures the FTDI (U6) device to translate USB to I^2C. The LED (D57) illuminates when the software is actively driving the I^2C bus. Using the FTDI (U6) as the I^2C master the software can read and write the ASC registers and communicate with the slave port in Bank 1 of the LPTM21 (U6) device as shown in Figure 24. Customer based software that does not automatically drive the USB_I2C_EN can still be supported by installing J33 to force the MUX to connect the I^2C pins to the bus. Alternatively, an off board I^2C master can be connected to the bus using J26. Note that neither J33 nor an off board I^2C master should be active when programming the board via USB / JTAG.

Figure 24. I²C Bus Route



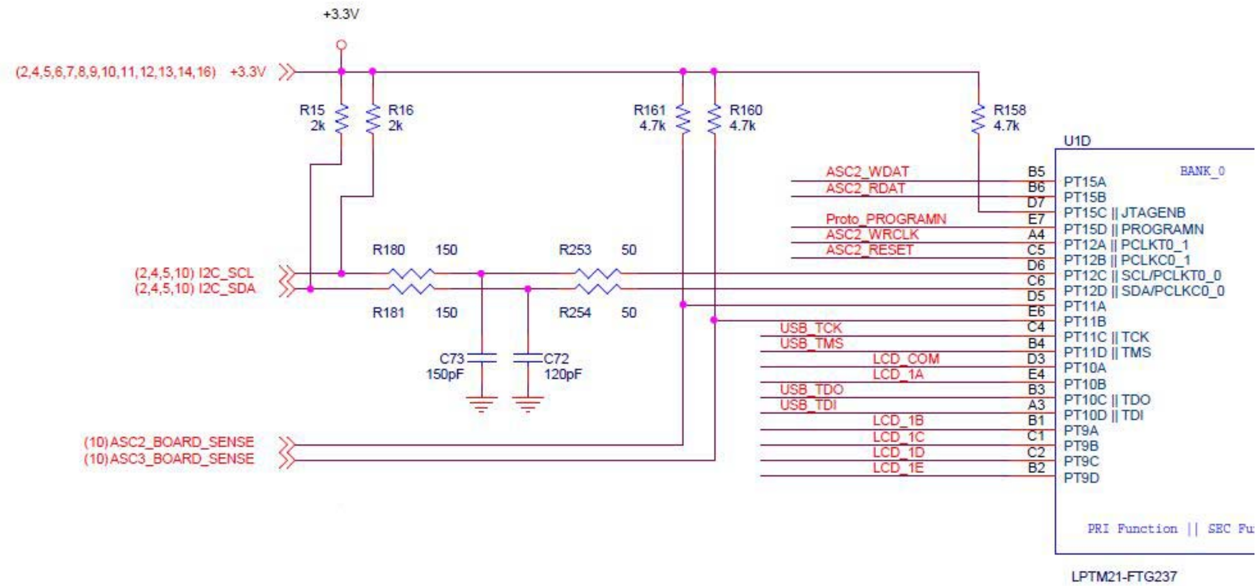
VID Control

Another function of the I²C bus is to support the VID feature of the Platform Manager 2 system. The VID feature (described in the VID Section above) uses the I²C port in Bank 0 of U1 as the master to send target voltage data to the respective ASC devices. Note that when using the VID feature J33 should not be installed and the I²C Demo Debugging software should not be used as bus contentions may occur.

Dual Boot Control

The I²C bus can also be used to support the Dual Boot feature of the Platform Manager 2 system. The Dual Boot feature uses the I²C port in Bank 0 of U1 as the master to send configuration information to all the ASC devices in the system. Note that when using the Dual Boot feature J33 should not be installed and the I²C Demo Debugging software should not be used as bus contentions may occur.

Figure 25. I²C Noise Filter Circuit



Filters and Series Terminations

Throughout the I²C bus route shown in Figure 24 most of the devices are connected to the I²C bus either by a filter or series termination resistor. The noise filter is shown in Figure 25 and is an effective compromise to the 50 ns glitch filter called for in the I²C specification. This is because a full 50 ns low-pass filter results in too slow a rise time for the signals at the inputs of the FPGA. The 150 Ohm resistors with the capacitors values correspond to 18 ns to 22.5 ns which is enough filtering to block most of the high frequency noise. The data (I2C_SDA) has a shorter delay than the clock (I2C_SCL) by design to prevent false re-starts. False re-starts can occur when the rising edge of the data and clock happen at the same time with certain data patterns. The I²C pins of the FTDI (U6) device and external software based interfaces tend to drive the clock and data transitions at the same time, so the offset in delays prevents false re-starts. The 50 Ohm series resistors provide a second low-pass filter of about 0.8 ns using the input capacitance of the FPGA pins. More importantly the 50 Ohm resistor isolates the filter capacitor and limits the current when the FPGA is driving the bus. All of the slave devices and connectors also have a 22 Ohm series resistor on both the data and clock lines. These series resistors have multiple benefits. First, they isolate the slave device from having to drive the capacitance of the bus and they also minimize the effect of adding more pin capacitance to the bus; so it works both ways. Furthermore, series resistors are easier to remove than a slave device when debugging an I²C issue.

Miscellaneous

The Platform Manager 2 evaluation board has other significant components used for indication, status information, and control in various designs by the user. These components and signals are listed in Table 19 below.

Table 19. Components and Signals for Miscellaneous Operation.

Components / Signals	Ref. Des.	Schematic Sheet	Description
Components			
LCD	U5	7	LCD 3-Digit display driven by LPTM21 (U1) for demonstration purpose. See Appendix D and E for connections.
LED_1 to LED_15	D22 – D36	7	LEDs Red (15) for demonstration purpose connected to LPTM21 (U1 BANK1 and BANK3) on the board. See Appendix D and E for connections.
A0_LED1 to A0_LED10	D3 – D12	7	LEDs Red (10) for demonstration purpose connected to LPTM21 (U1 ASC section) on the board.
A1_LED1 to A1_LED10	D13 – D21	7	LEDs Red (9) for demonstration purpose connected to L-ASC10 (U4) on the board. Note A1_LED7 and GPIO7 do not exist.
Push Button Switches	SW4, SW3	6	Switches push button (2) connected to LPTM21 on BANK2. The nets have pull-up resistors. See Appendix D and E for connections.
Push Button Switch	SW1	6	Switch push button connected to GPIO10 of ASC0 (ASC section of LPTM21 U1). The net is shared by A0_LED10 and has a pull-up resistor.
Push Button Switch	SW5	6	Switch push button connected to GPIO10 of ASC1 (U4). The net is shared by A1_LED10 and has a pull-up resistor.
Signals			

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
Platform Manager 2 Evaluation Board	LPTM-BPM-EVN	

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
June 2015	1.0	Initial release.

Appendix A. Bill of Materials (Installed)

Table 20. Bill of Materials - Populated on Evaluation Board

Quantity	Reference Designator	Description	Package	Manufacturer	Part Number
ICs					
1	U1	Platform Manager 2 Device	FTBGA-237	Lattice Semiconductor	LPTM21-1AFTG237C
1	U3	4 Mbit Flash Device	UDFN-8	Adesto Technologies	AT25DF041A-MH-T
1	U4	ASC Device	TQFN-48	Lattice Semiconductor	L-ASC10-1SG48I
1	U5	LCD 3 Digit	LCD_301	Lumex Opto	LCD-S301C31TR
1	U6	High Speed USB Interface	TQFP-64	FTDI	FT2232HL-REEL
1	U7	1 Kbit EEPROM	SOIC-8	ST Microelectronics	M93C46-WMN6TP
1	U8	3.3 V LDO Regulator 1 A	SOT223	On Semi	NCP1117ST33T3G
1	U9	3.3 V LDO Regulator 0.3 A	5STOP	NXP	LD6836TD/33P
2	U10,U11	Dual Analog Switch	6-TSSOP	Fairchild	FSA4157P6X
Capacitors					
2	C55,C56	18 pF 50 V 5% NP0	SM_C_0603	Kemet	C0603C180J5GACTU
2	C73,C101	120 pF 50 V 5% NP0	SM_C_0603	Samsung	CL10C121JB8NNNC
6	C1,C2,C24, C25,C72,C100	150 pF 50 V 5% NP0	SM_C_0603	Murata	GRM1885C1H151JA01D
9	C26,C47,C48, C82,C85,C94, C97,C103,C104	10 nF 50 V 10% X7R	SM_C_0603	Kemet	C0603C103K5RACTU
36	C4,C9,C10,C11,C12, C13,C14, C15,C16,C17, C18,C19,C20, C21,C22,C23, C50,C52,C53, C54,C57,C62, C63,C64,C65, C66,C67,C68, C83,C84,C86, C87,C95,C96, C98,C99	100 nF 16 V 10% X7R	SM_C_0603	Murata	GRM188R71C104KA01D
1	C69	220 nF 16 V 10% X7R	SM_C_0603	Murata	GRM188R71C224KA01D
1	C58	330 nF 16 V 10% X7R	SM_C_0603	Murata	GRM188R71C334KA01D
3	C8,C70,C71	1 uF 16 V 10% X5R	SM_C_0603	Murata	GRM188R61C105KA93D
1	C74	2.2 uF 16 V 10% X7R	SM_C_1206	Kemet	C1206C225K4RACTU
1	C51	3.3 uF 10 V 10% Tantalum	SM_C_1206	Kemet	T491A335K010AT
1	C49	4.7 uF 10 V 10% Tantalum	SM_C_1206	Kemet	T491A475K010AT
1	C61	6.8 uF 16 V 10% Tantalum	SM_C_1206	Kemet	T491A685K016AT
1	C102	10 uF 10 V 10% X7R	SM_C_0603	Kemet	C0603C104K8RACTU
1	C75	10 uF 16 V 10% X5R	SM_C_1206	Kemet	C1206C106K4PACTU
1	C60	10 uF 10 V 10% Tantalum	SM_C_1206	Kemet	T491A106K010AT
8	C35,C36,C37, C38,C43,C44, C45,C46	22 uF 10 V 20% Tantalum	SM_C_1206	Kemet	T491A226M010AT
1	C5	33 uF 25 V 20% Aluminum	SM_C_Can	Panasonic	EEE-FP1E330AP
2	C6,C59	47 uF 16 V 20% Aluminum	Thru Hole	Panasonic	ECE-A1CKS470
1	C27	47 uF 25 V 20% Aluminum	SM_C_Can	Panasonic	EEE-FP1E470AP
1	C28	220 uF 25 V 20% Aluminum	SM_C_Can	Rubycon	25YXG220MEFC6.3X11
2	C29,C30	330 uF 10 V 20% Aluminum	SM_C_Can	Rubycon	10ZLH330MEFC6.3X11

Quantity	Reference Designator	Description	Package	Manufacturer	Part Number
Diodes					
1	D2	Schottky 30 V 1 A	MicroSMP	Vishay	MSS1P3L-M3/89A
35	D3,D4,D5,D6,D7,D8, D9,D10,D11,D12, D13,D14,D15,D16, D17,D18,D19,D20, D21,D22,D23,D24, D25,D26,D27,D28, D29,D30,D31,D32, D33,D34,D35,D36, D57	Red LED Clear	SM_LED_0603	Lite-On	LTST-C190KRKT
7	D39,D40,D44, D51,D52,D55, D56	Green LED Clear	SM_LED_0603	Lite-On	LTST-C190GKT
1	D42	Blue LED Clear	SM_LED_0603	Lite-on	LTST-C191TBKT
1	D45	22 V 600 W 5% TVS	DO-214AA	Bourns	SMBJ22CA
6	D37,D38,D41, D43,D46,D47	Schottky 30 V 0.5 A	SOD_923	On Semiconductor	NSR0530P2T5G
1	D48	3.9 V 5W Zener	Thru Hole	ON Semiconductor	1N5335BRLG
Jumpers					
6	J1,J5,J6,J8,J27,J30	3 Pin Header	Header_3X1	Molex	22-28-4364
4	J3,J4,J29,J31, J32	2 Pin Header	Header_2X1	Molex	22-28-4364
2	J7,J9	3 Pin Connector	Header_3X1	Molex	22272031
2	J10,J11	6 Pin Connector	Header_6X1	Molex	22272061
2	J14,J15	25 Pin D-SUB PLUG R/A	Thru Hole	TE Connectivity	5747842-3
1	J16	Mini USB RCPT RA Type B	SMD	TE Connectivity	1734035-2
5	J12,J13,J19,J23,J25	2 Pin Terminal Block	Thru Hole	Phoenix Contact	1727010
2	J20,J24	4 Pin Terminal Block	Thru Hole	Phoenix Contact	1727036
1	J28	Power Jack 2.1 mm X 5.5 mm High Cur.	Thru Hole	CUI Inc	PJ-102AH
11	J1,J3,J4,J5,J6,J8, J27,J29,J30,J31,J32	Shorting Jumper	N/A	3M	929957-08
Transistors					
1	Q1	MOSFET P-CH 30 V 385 mA	SOT-23	Vishay Siliconix	TP0202K-T1-E3
2	Q2,Q3	MOSFET P-CH 20 V 3.7 A	SOT-23	IR	IRLML6402TRPBF
2	Q4,Q6	PNP	SOT-23	Fairchild	MMBT3906
8	Q5,Q7,Q8,Q36,Q37, Q40,Q41,Q42	NPN	SOT-23	Fairchild	MMBT3904
6	Q10,Q11,Q12,Q13, Q14,Q43	MOSFET N-CH 60 V 4 A	SOT-23	Fairchild	NDT3055L
4	Q48,Q49,Q54,Q55	MOSFET N-CH 25 V 220 mA	SOT-23	Fairchild	FDV301N
Resistors					
20	R122,R123,R124, R125,R126,R127, R172,R173,R174, R175,R176,R177, R178,R179,R199, R200,R201,R217, R248,R261	Zero Ohm jumper	SM_R_0603	Panasonic	ERJ-3GEY0R00V
2	R54,R57	0.02 Ohm 1/4 W 1%	SM_R_1206	Yageo	PF1206FRF070R02L
1	R216	1.0 Ohm 1/10 W 1%	SM_R_0603	Panasonic	ERJ-3RQF1R0V
3	R182,R239,R250	2.0 Ohm 1/10 W 1%	SM_R_0603	Panasonic	ERJ-3RQF2R0V
1	R203	2.7 Ohm 1 W 5%	Thru Hole	Panasonic	ERX-1SJ2R7A
1	R129	10 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ100V
10	R20,R21,R232,R233, R255,R256,R257, R258,R259,R260	22 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ220V
4	R251,R252,R253, R254,	50 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ500V

Quantity	Reference Designator	Description	Package	Manufacturer	Part Number
19	R10,R11,R12,R13, R14,R29,30,R31, R59,R120,R128, R245,R246,R247, R249	100 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ101V
4	R180,R181,R240, R241	150 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ151V
1	R226	220 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ221V
12	R1,R2,R3,R4,R6, R7,R8,R23,R24,R25, R26,R28	270 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ271V
2	R89,R117	330 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ331V
13	R55,R60,R82,R110, R121,R185,R186, R189,R190,R212, R214,R228,R264	470 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ471V
1	R9	680 Ohm 0.5 W 1%	SM_R_1206	Vishay Dale	CRCW1206680RFKEAHP
12	R34,R36,R39,R41, R42,R56,R61,R68, R96,R159,R244, R262	1 kOhm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ102V
1	R44	1 kOhm 1/4 W 5%	SM_R_0603	Rohm	ESR03EZPJ102
4	R33,R35,R38,R40	1 kOhm Slide Pot	Thru Hole	Taiwan Alpha Elect.	RA2043F-20-10EB1-B1K
2	R15,R16	2 kOhm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ202V
4	R27,R34,R119,R230	2.2 kOhm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ222V
9	RN3,RN4,RN5,RN6, RN7,RN8,RN9,RN10, RN11	2.2 kOhm Array	SM_ 2512	CTS	745C101222JP
10	R17,R18,R158,R160, R161,R193,R194, R197,R198,R263	4.7 kOhm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ472V
2	R77,R105	6.34 kOhm 1/8 W 1%	SM_R_0805	Panasonic	ERJ-6ENF6341V
22	R5,R19,R22,R37, R43,R45,R46,R47, R48,R49,R50,R51, R164,R165,R168, R169,R171,R202, R236,R237,R242, R243	10 kOhm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ103V
1	RN1	10 kOhm Array	SM_ 2512	CTS	745C101103JP
4	R78,R79,R106,R107	11.0 kOhm 1/8 W 1%	SM_R_0805	Panasonic	ERJ-6ENF1102V
1	R231	12 kOhm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ123V
4	R85,R86,R113,R114	19.6 kOhm 1/8 W 1%	SM_R_0805	Panasonic	ERJ-6ENF1962V
2	R84,R112	20.0 kOhm 1/8 W 1%	SM_R_0805	Panasonic	ERJ-6ENF2002V
2	R235,R265	100 kOhm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ104V
1	R118	1M Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ105V
DC-DC Converters					
4	DCDC3,DCDC4, DCDC7,DCDC8	5V In, 0.6 V-5.5 V Out 2 A	Thru Hole	GE Critical Power	NQR002A0X4Z
Fuse					
1	F1	FAST ACT 125 V 0.25 A	Thru Hole	Littelfuse Inc.	F5533CT
Inductors					
1	L1	270 uH 0.4 A 10%	SM 10 mm x 10 mm	Bourns Inc.	PM105SB-271K-RC
2	L2,L3	Ferrite Bead 600 Ohm	SM_FB_0603	TDK Corp.	MPZ1608S601A
Switches					
5	SW1,SW2,SW3, SW4,SW5	Tactile SPST-NO 0.02 A 15 V	SMT_SW	Panasonic	EVQ-Q2K03W
1	SW6	8 Pos Dip Sw	Thru Hole	CTS	195-8MST
Crystal					
1	X1	12 MHz	SM_XTAL	TXC	7M-12.000MAAJ-T

Appendix B: Bill of Materials (Not installed)

Table 21. Bill of Materials – Not Populated on Evaluation Board

Quantity	Reference Designator	Description	Package	Manufacturer	Part Number
Capacitors					
4	C76,C79,C88,C91	10 nF 50 V 10% X7R	SM_C_0603	Kemet	C0603C103K5RACTU
8	C77,C78,C80,C81, C89,C90,C92,C93	100 nF 16 V 10% X7R	SM_C_0603	Murata	GRM188R71C104KA01D
4	C31,C33,C39,C41	22 uF 16 V 20% Tantalum	SM_C_2413	Kemet	T491C226M016ZT
4	C32,C34,C40,C42	22 uF 10 V 20% Aluminum	SM_C_1206	Kemet	T491A226M010AT
Diodes					
4	D49,D50,D53,D54	Green LED Clear	SM_LED_0603	Lite-On	LTST-C190GKT
Jumpers					
1	J33	2 Pin Header	Header_2X1	Molex	22-28-4364
2	J2,J26	8 Pin Header	Header_8X1	Molex	22-28-4364
1	J35	10 Pin Header	Header_5X2	Molex	22-28-4364
Transistors					
4	Q34,Q35,Q38,Q39	NPN	SOT-23	Fairchild	MMBT3904
9	Q15,Q16,Q17,Q18, Q19,Q45,Q47,Q51, Q53	MOSFET N-CH 25 V 220 mA	SOT-23	Fairchild	FDV301N
8	Q20,Q21,Q22,Q23, Q24,Q25,Q26,Q27	Prototype[1]	SOT-23		
2	Q32,Q33	Prototype[1]	SOT-223		
4	Q28,Q29,Q30,Q31	Prototype[1]	SOIC-8		
Resistors					
2	R170,R238	Zero Ohm jumper	SM_R_0603	Panasonic	ERJ-3GEY0R00V
4	R183,R184,R187, R188	470 Ohm 1/10 W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ471V
2	R75,R103	680 Ohm 1/10 W 1%	SM_R_0603	Panasonic	ERJ-3GEYJ681V
24	R132,R133,R134, R135,R136,R137, R138,R139,R140, R141,R142,R143, R144,R145,R146, R147,R150,R151, R152,R153,R154, R155,R156,R157	Prototype[1]	SM_R_0805		
4	R130,R131,R148, R149	Prototype[1]	SM_R_2512		
4	R191,R192,R195, R196	4.7 kOhm 1/10W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ472V
8	R162,R163,R166, R167,R213,R215, R227,R229	20 kOhm 1/10W 5%	SM_R_0603	Panasonic	ERJ-3GEYJ203V
24	R62,R66,R67,R69, R73,R74,R76,R80, R81,R83,R87,R88, R90,R94,R95,R97, R101,R102,R104, R108,R109,R111, R115,R116	Open[2]	SM_R_0805		
2	R63,R91	2.74 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF2741V
2	R70,R98	4.42 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF4421V
4	R64,R65,R92,R93	5.60 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF5601V
4	R71,R72,R99,R100	8.02 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF8061V
2	R205,R219	23.7 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF2372V
2	R207,R221	36.5 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF3652V
2	R209,R223	54.9 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF5492V
2	R211,R225	84.5 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF8452V
4	R204,R206,R208, R210	130 kOhm 1/8 W 1%[2]	SM_R_0805	Panasonic	ERJ-6ENF1303V

4	R218,R220,R222, R224	200 kOhm 1/8 W 1% 2	SM_R_0805	Panasonic	ERJ-6ENF2003V
DC-DC Converters					
4	DCDC1,DCDC2, DCDC5,DCDC6	12 V In – User selected	5 Pin SIP		

1. Prototype mounting pads for "blue wire" connections to user defined transistors, resistors, inductors, capacitors, and diodes.
2. Values subject to user selected DC-DC type and output; use Platform Designer to calculate values based on output voltage.

Appendix C: Predefined Preference File Listing

```
// These names are generated by the software and can be copied into the
// preference file

// ASC0 Connections
LOCATE COMP "ASC0_RSTN" SITE "M8" ;

// ASC1 Connections
LOCATE COMP "ASC1_RSTN_I" SITE "C8" ;
LOCATE COMP "rdat_1"  SITE "B7" ;
LOCATE COMP "wdat_1"  SITE "C7" ;
LOCATE COMP "wrclk_1" SITE "A7" ;

// ASC2 Connections
LOCATE COMP "ASC2_RSTN_I" SITE "C5" ;
LOCATE COMP "rdat_2"  SITE "B6" ;
LOCATE COMP "wdat_2"  SITE "B5" ;
LOCATE COMP "wrclk_2" SITE "A4" ;

// ASC3 Connections
LOCATE COMP "ASC3_RSTN_I" SITE "N5" ;
LOCATE COMP "rdat_3"  SITE "T2" ;
LOCATE COMP "wdat_3"  SITE "P3" ;
LOCATE COMP "wrclk_3" SITE "R4" ;
```

Appendix D: User Defined Preference File Listing

```
// These names follow the Platform Manager 2 Evaluation Board schematic but,
// they may be defined by the user. Thus, they can be copied into the preference
// file and edited to match a different naming convention if needed.

// LED Connections
LOCATE COMP "LED1"  SITE "B10" ;
LOCATE COMP "LED2"  SITE  "N9" ;
LOCATE COMP "LED3"  SITE  "E9" ;
LOCATE COMP "LED4"  SITE "E10" ;
LOCATE COMP "LED5"  SITE "D11" ;
LOCATE COMP "LED6"  SITE "C11" ;
LOCATE COMP "LED7"  SITE "C10" ;
LOCATE COMP "LED8"  SITE "D10" ;
LOCATE COMP "LED9"  SITE  "M2" ;
LOCATE COMP "LED10" SITE  "N2" ;
LOCATE COMP "LED11" SITE  "N1" ;
LOCATE COMP "LED12" SITE  "M1" ;
LOCATE COMP "LED13" SITE  "L2" ;
LOCATE COMP "LED14" SITE  "L3" ;
LOCATE COMP "LED15" SITE  "L1" ;

// LCD Connections
LOCATE COMP "LCD_COM" SITE "D3" ;
LOCATE COMP "LCD_1E"  SITE "B2" ;
LOCATE COMP "LCD_1D"  SITE "C2" ;
LOCATE COMP "LCD_1C"  SITE "C1" ;
LOCATE COMP "LCD_DP1" SITE "P4" ;
LOCATE COMP "LCD_2E"  SITE "R5" ;
LOCATE COMP "LCD_2D"  SITE "P5" ;
LOCATE COMP "LCD_2C"  SITE "T4" ;
LOCATE COMP "LCD_DP2" SITE "M7" ;
LOCATE COMP "LCD_3E"  SITE "P7" ;
LOCATE COMP "LCD_3D"  SITE "P8" ;
LOCATE COMP "LCD_3C"  SITE "N8" ;
LOCATE COMP "LCD_3B"  SITE "E8" ;
LOCATE COMP "LCD_3A"  SITE "D8" ;
LOCATE COMP "LCD_3F"  SITE "R7" ;
LOCATE COMP "LCD_3G"  SITE "T7" ;
LOCATE COMP "LCD_2B"  SITE "P6" ;
LOCATE COMP "LCD_2A"  SITE "N6" ;
LOCATE COMP "LCD_2F"  SITE "R6" ;
LOCATE COMP "LCD_2G"  SITE "N7" ;
LOCATE COMP "LCD_1B"  SITE "B1" ;
LOCATE COMP "LCD_1A"  SITE "E4" ;
LOCATE COMP "LCD_1F"  SITE "R1" ;
LOCATE COMP "LCD_1G"  SITE "P1" ;

// VID Connections
LOCATE COMP "VIDA_1"  SITE "K2" ;
LOCATE COMP "VIDA_2"  SITE "K3" ;
LOCATE COMP "VIDA_3"  SITE "J3" ;
LOCATE COMP "VIDA_4"  SITE "J2" ;
```

```
LOCATE COMP "VIDA_5"  SITE "H2" ;
LOCATE COMP "VIDA_6"  SITE "H3" ;
LOCATE COMP "VIDA_7"  SITE "G3" ;
LOCATE COMP "VIDA_8"  SITE "G2" ;
LOCATE COMP "VIDA_SW" SITE "K1" ;


// FAN Connections
LOCATE COMP "FAN1_TACH" SITE "E2" ;
LOCATE COMP "FAN1_PWM"  SITE "D2" ;
LOCATE COMP "FAN2_TACH" SITE "D1" ;
LOCATE COMP "FAN2_PWM"  SITE "E1" ;
LOCATE COMP "FAN3_TACH" SITE "F2" ;
LOCATE COMP "FAN3_PWM"  SITE "F3" ;
LOCATE COMP "FAN4_TACH" SITE "F1" ;
LOCATE COMP "FAN4_PWM"  SITE "G1" ;

// DCDC Connections
LOCATE COMP "DCDC1_SYNC” SITE “N10” ;
LOCATE COMP "DCDC2_SYNC” SITE “P10” ;
LOCATE COMP "DCDC3_SYNC” SITE “P9” ;
LOCATE COMP "DCDC4_SYNC” SITE “R10” ;
LOCATE COMP "DCDC5_SYNC” SITE “L10” ;
LOCATE COMP "DCDC6_SYNC” SITE “T10” ;
LOCATE COMP "DCDC7_SYNC” SITE “M9” ;
LOCATE COMP "DCDC8_SYNC” SITE “M10” ;


// ASC2 Hot-Swap Connections
LOCATE COMP “ASC2_BOARD_SENSE” SITE “D5” ;
// Note: Overcurrent signals share the LED I/O.
LOCATE COMP “A2_5V_OVERCURRENT_SENSE”     SITE “C10” ; // LED_7
LOCATE COMP “A2_5V_OVERCURRENT_SHUTDOWN”  SITE  “L3” ; // LED_14
LOCATE COMP “A2_12V_OVERCURRENT_SENSE”    SITE  “M1” ; // LED_12
LOCATE COMP “A2_12V_OVERCURRENT_SHUTDOWN” SITE  “L2” ; // LED_13

// ASC3 Hot-Swap Connections
LOCATE COMP “ASC3_BOARD_SENSE” SITE “E6” ;
// Note: Overcurrent signals share the LED I/O.
LOCATE COMP “A3_5V_OVERCURRENT_SENSE”     SITE  “N1” ; // LED_11
LOCATE COMP “A3_5V_OVERCURRENT_SHUTDOWN”  SITE  “N2” ; // LED_10
LOCATE COMP “A3_12V_OVERCURRENT_SENSE”    SITE “D10” ; // LED_8
LOCATE COMP “A3_12V_OVERCURRENT_SHUTDOWN” SITE  “M2” ; // LED_9

// Misc Connections
LOCATE COMP "PIO3_PB_SW3" SITE "T9" ;
LOCATE COMP "MANUAL_RESTART_SW4" SITE "M6" ;
LOCATE COMP “I2C_WRITE_PROTECT” SITE “M5” ;
```

Appendix E: Schematics

Figure 26. System Block Diagram and Table of Contents

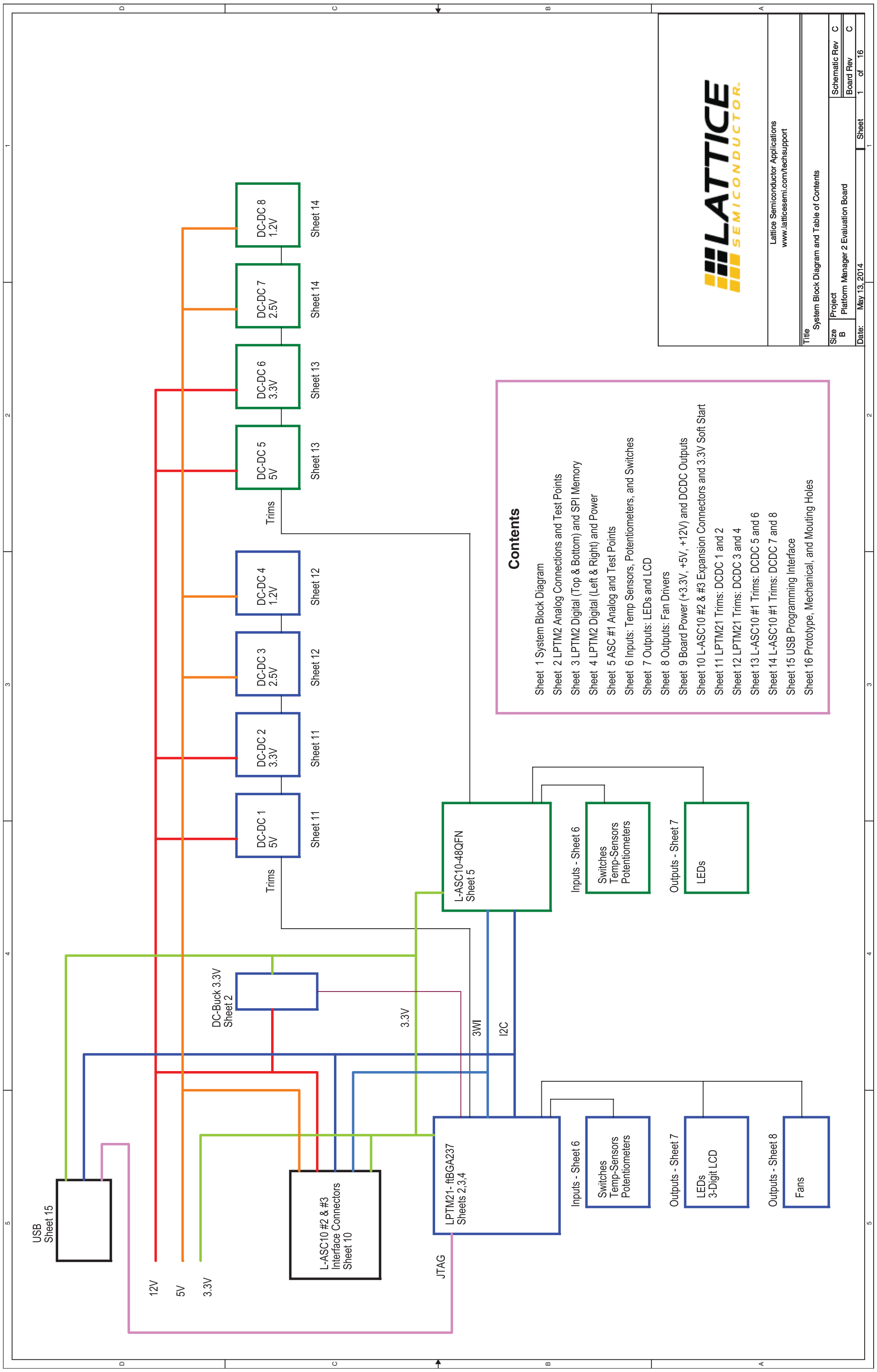


Figure 27. LPTM21 Analog Connections

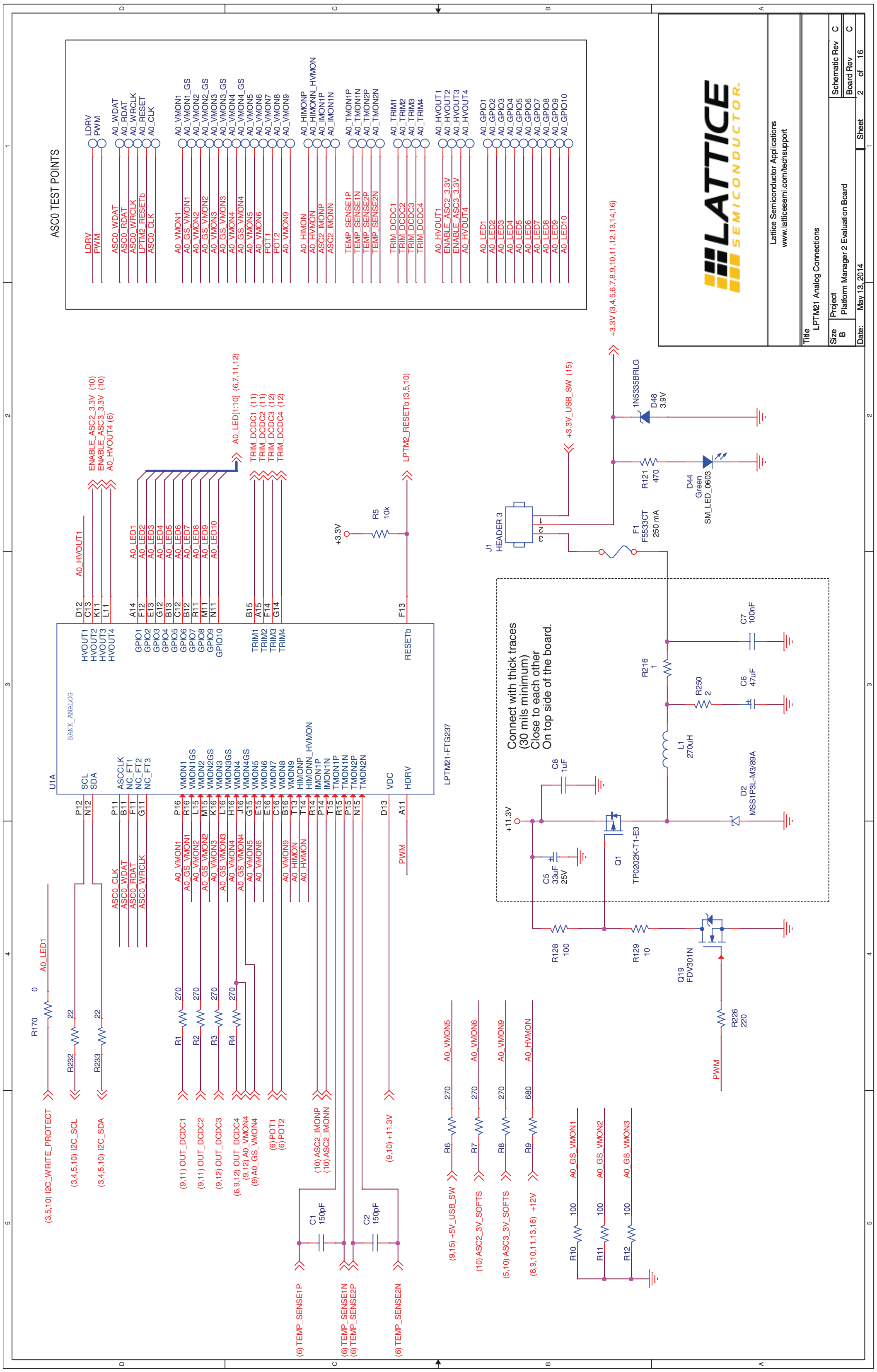


Figure 28. LPTM21 Top and Bottom Bank Digital Connections and SPI Memory

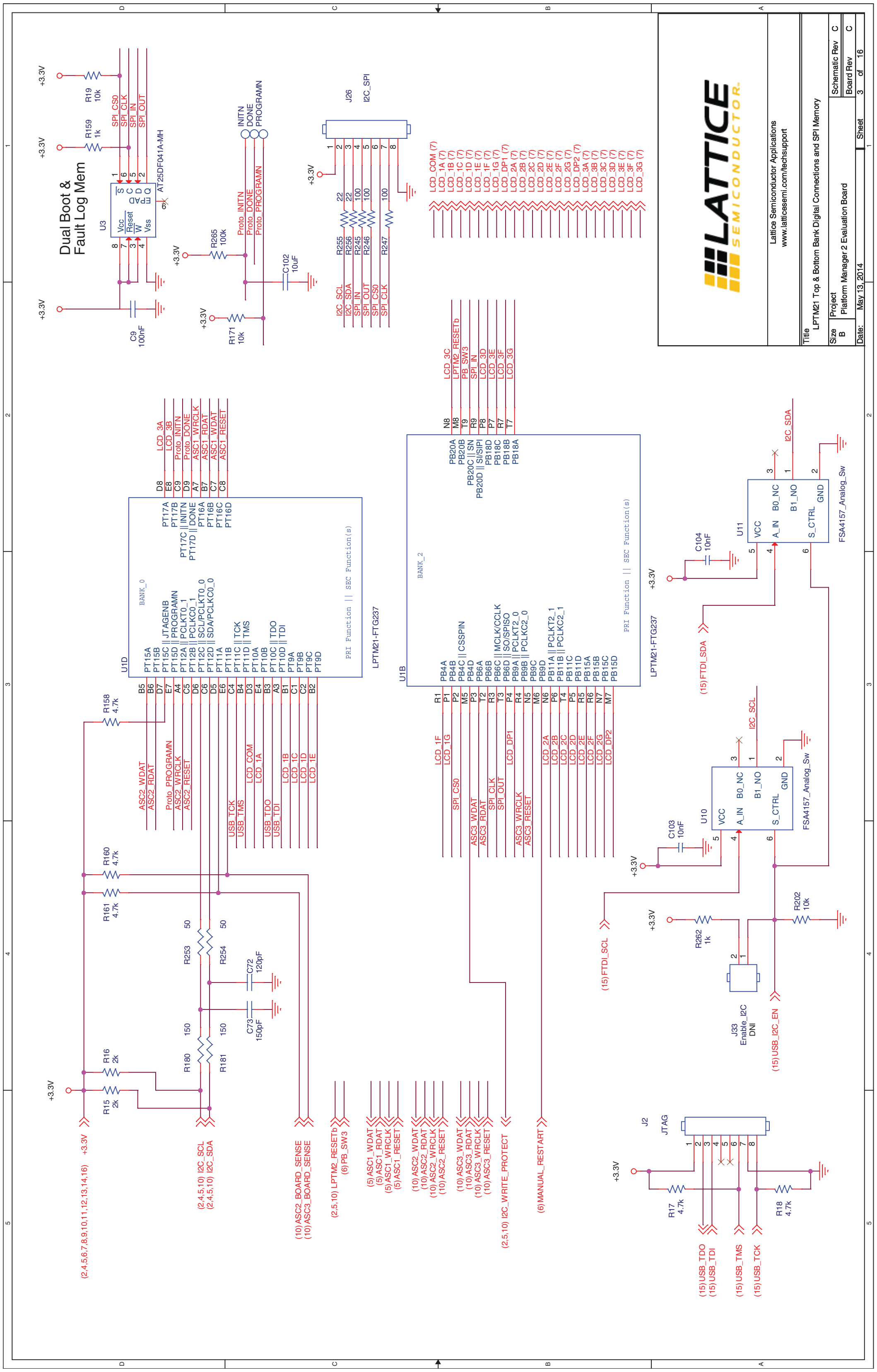


Figure 29. LPTM21 Left and Right Bank Digital and Power Connections

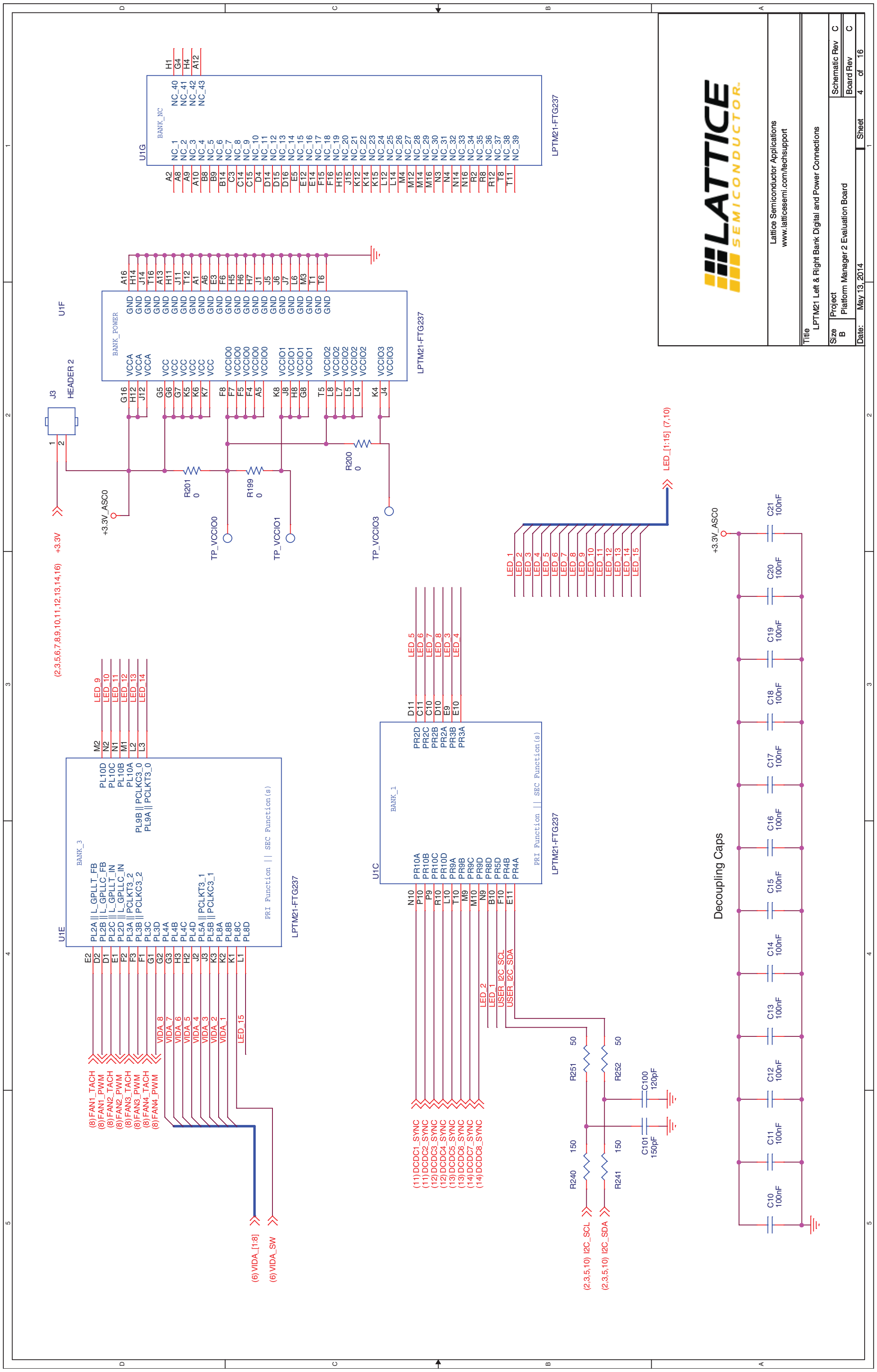


Figure 30. L-ASC10 Connections and Test Points

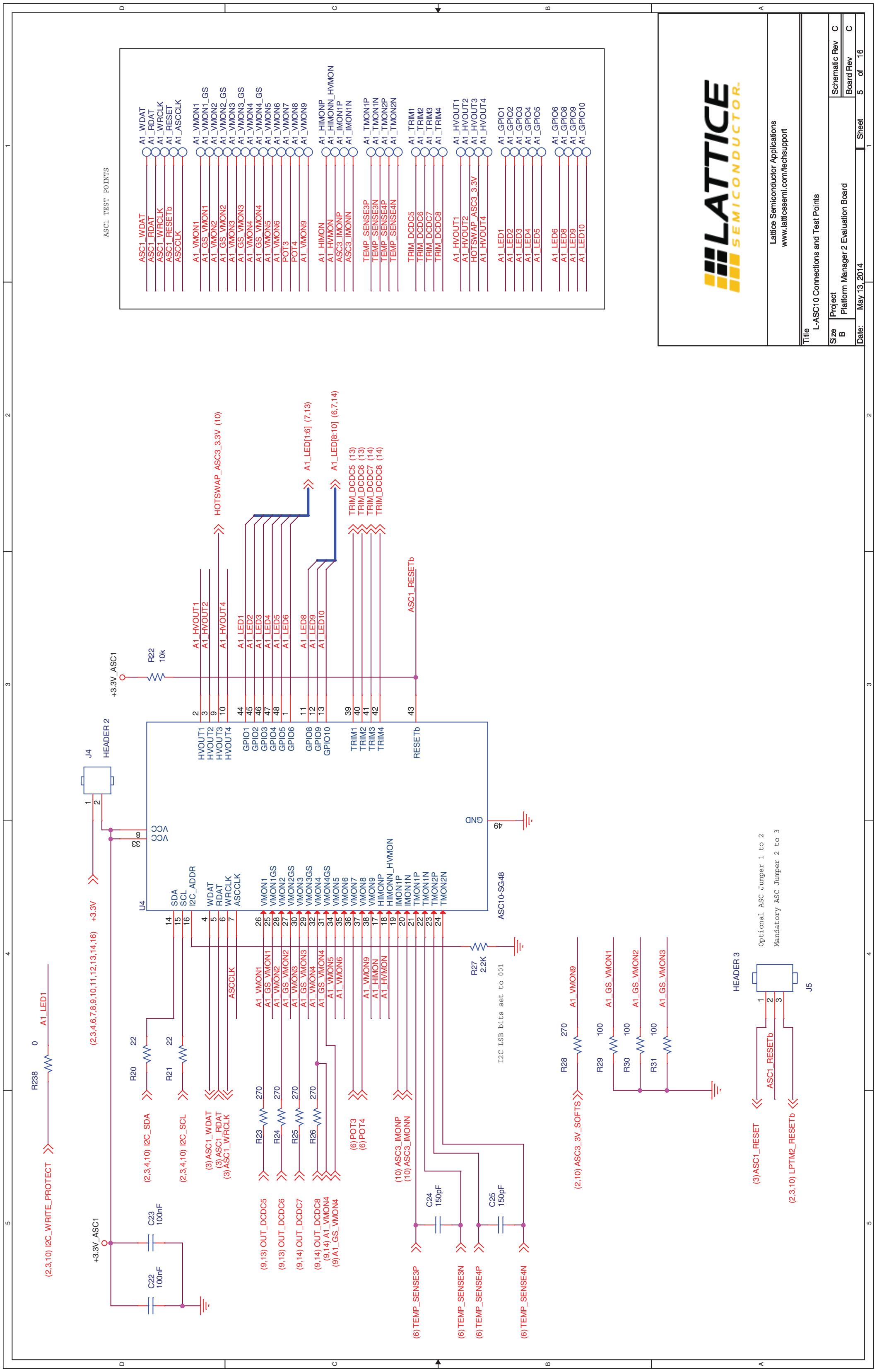


Figure 31. Inputs: Temperature Sensors, Slide Pots, and Switches

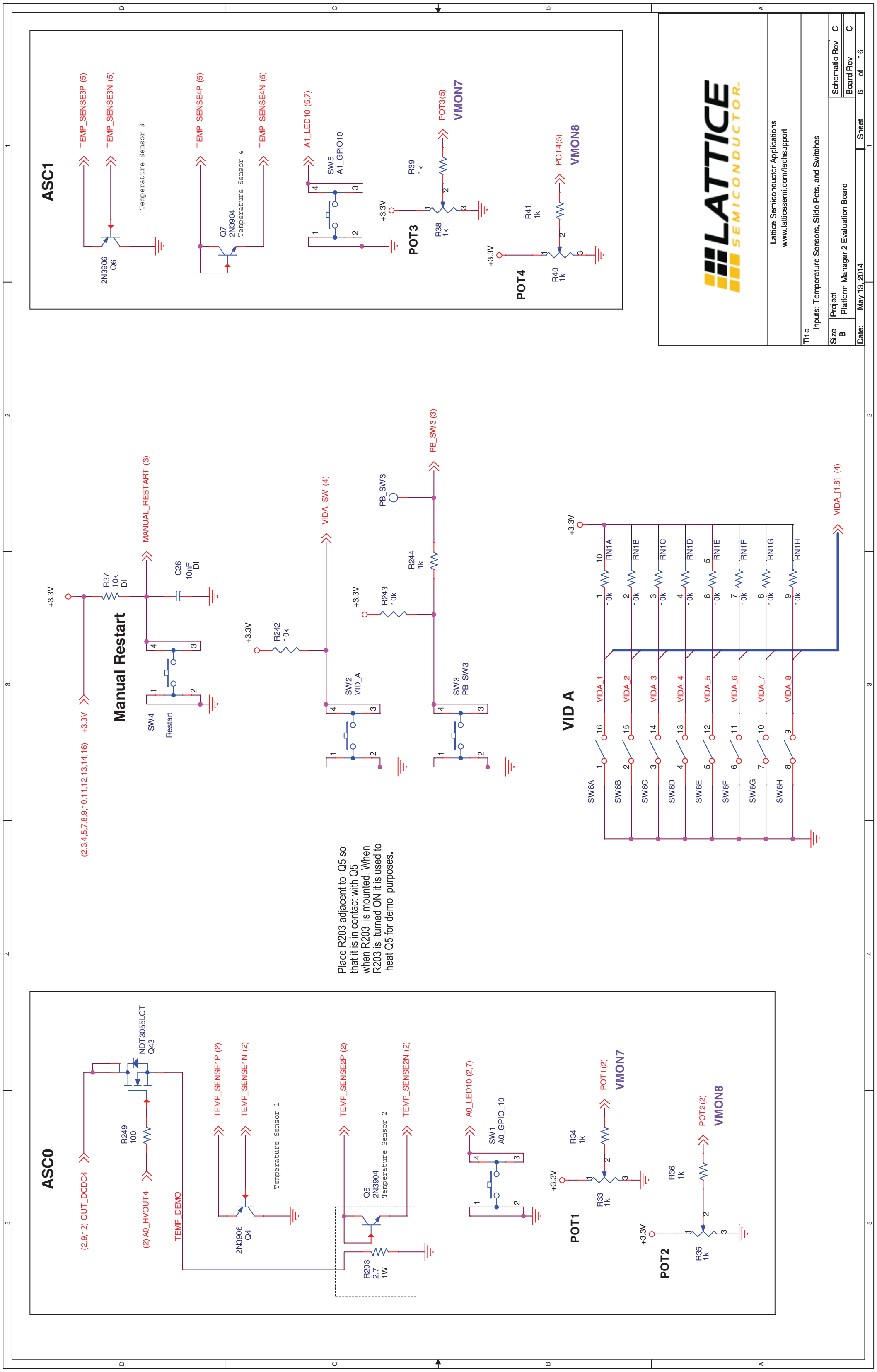


Figure 32. Outputs: LCD and LEDs

Figure 33. Fan Connectors

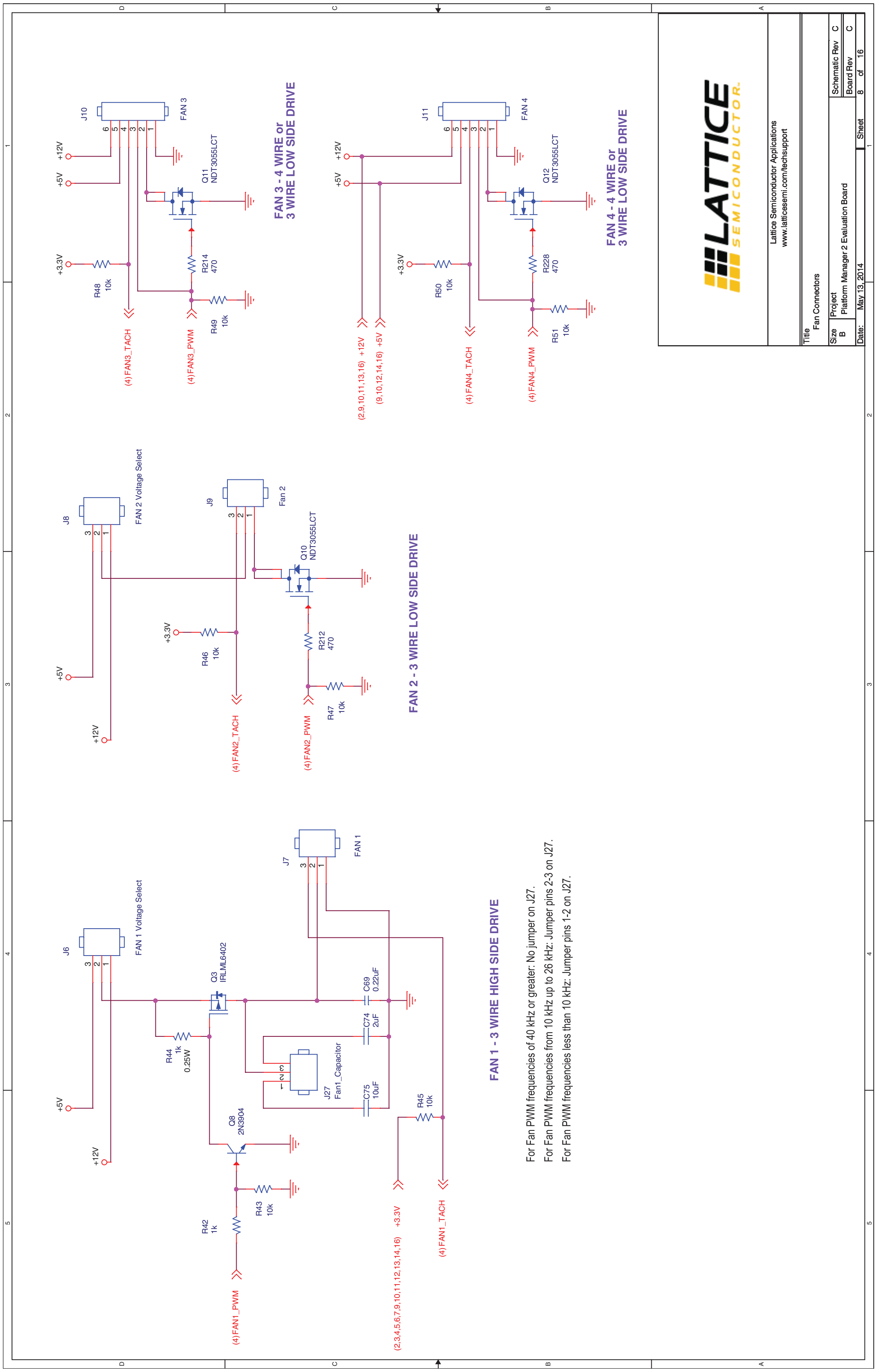


Figure 34. Board Power Connections

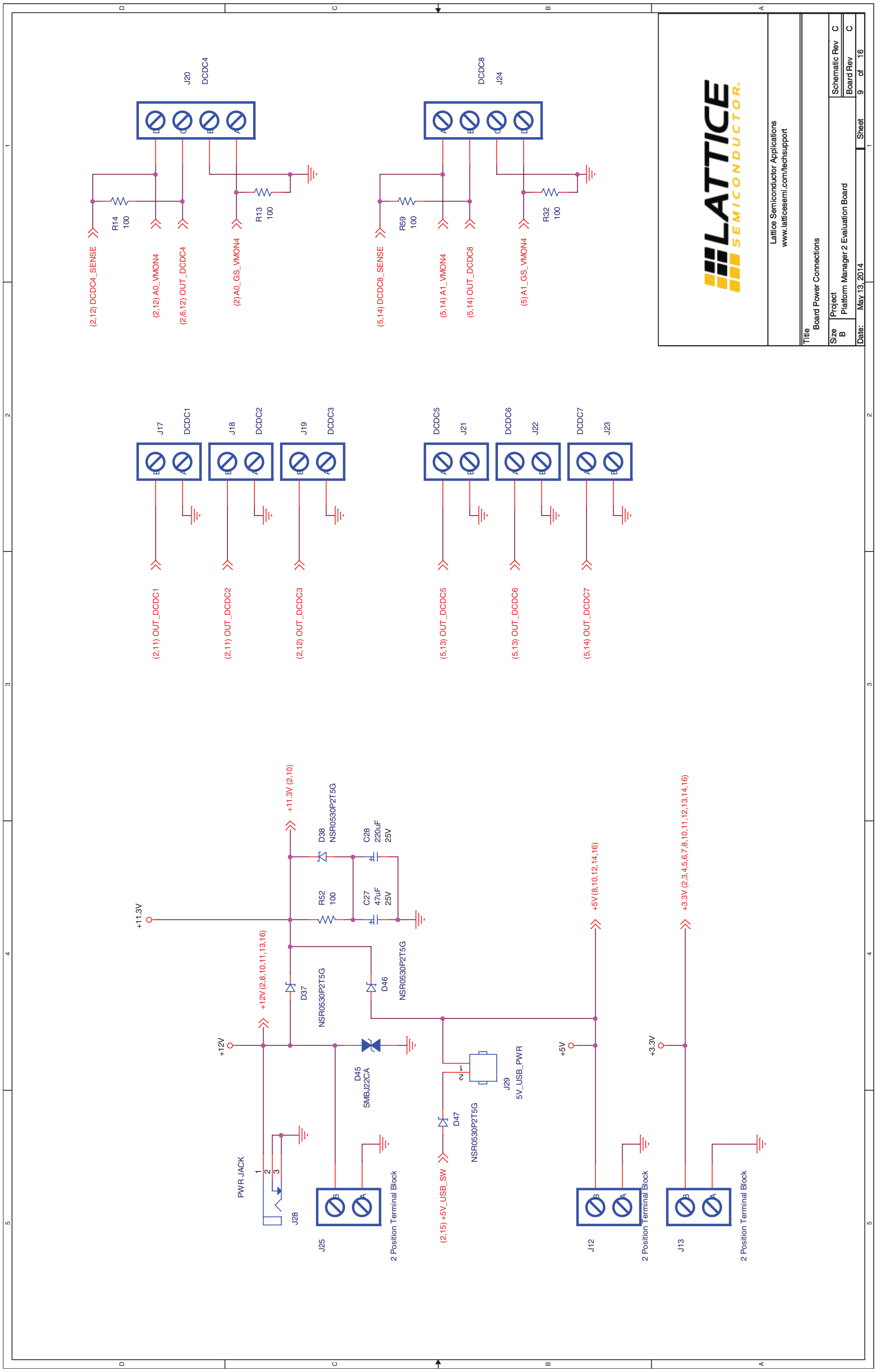


Figure 35. L-ASC10 #2 and #3 Expansion Connectors and 3.3 V Soft Start

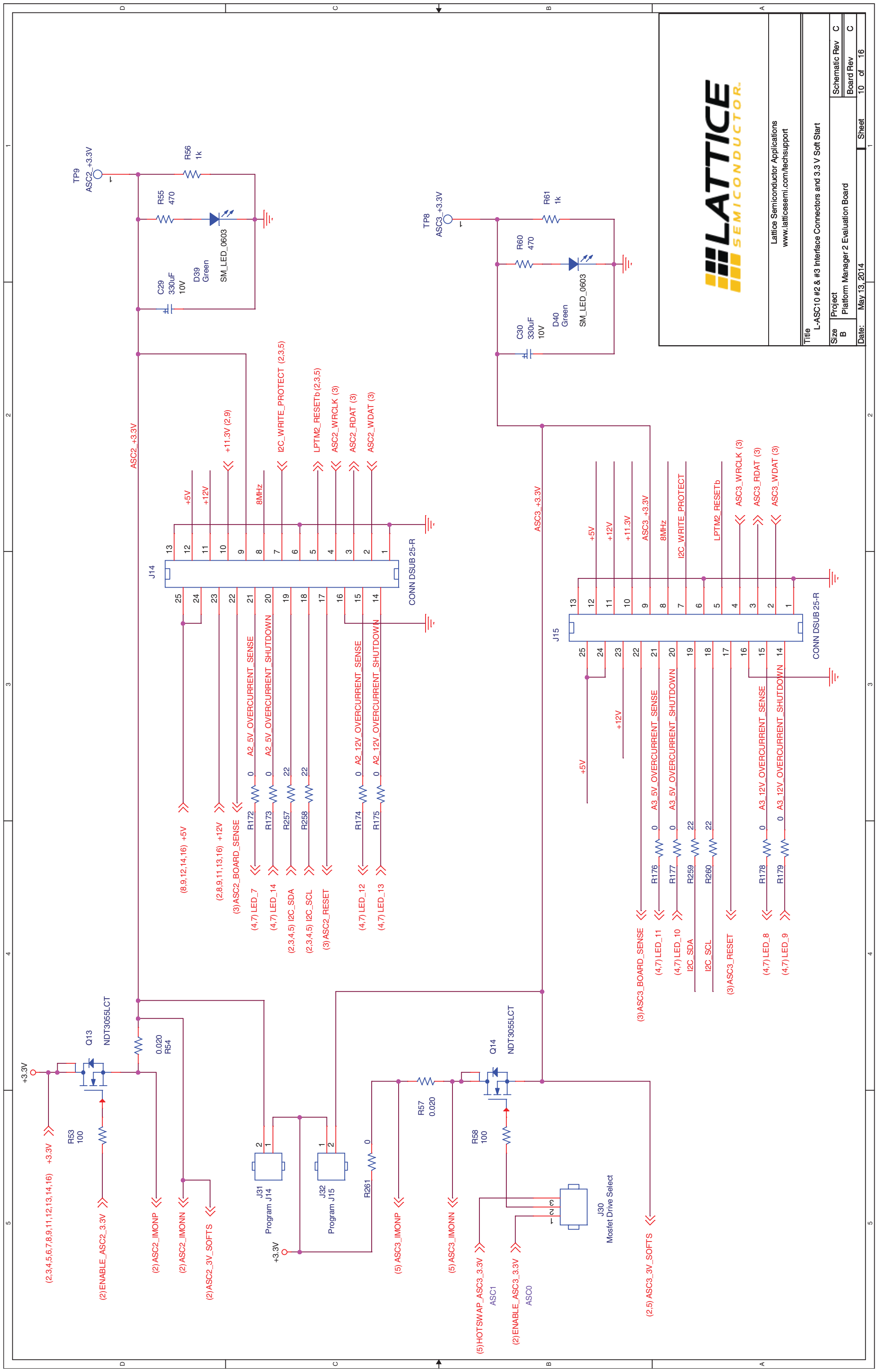


Figure 36. LPTM21 Trims: DCDC1 and DCDC2

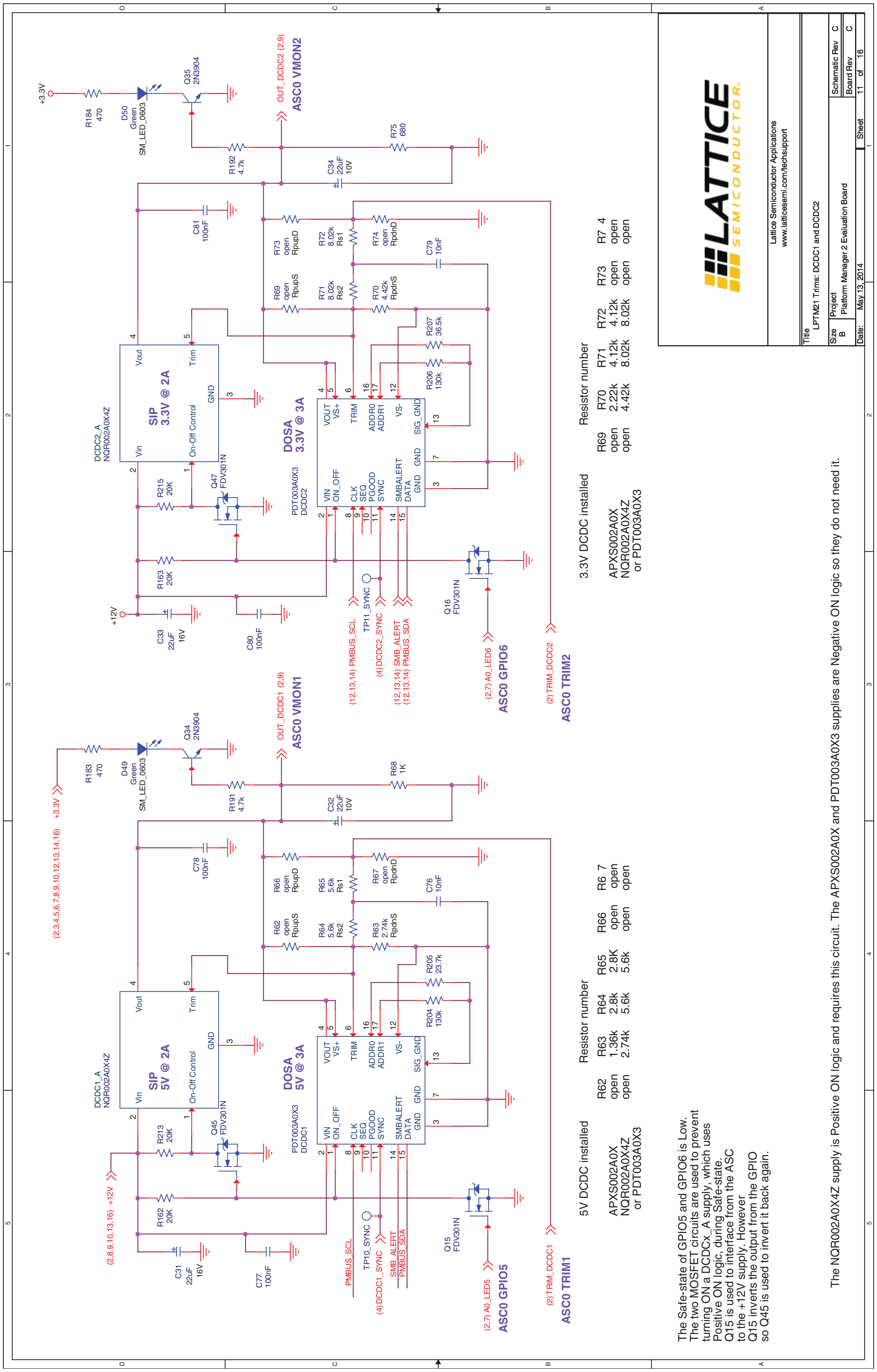


Figure 37. LPTM21 Trims: DCDC3 and DCDC4

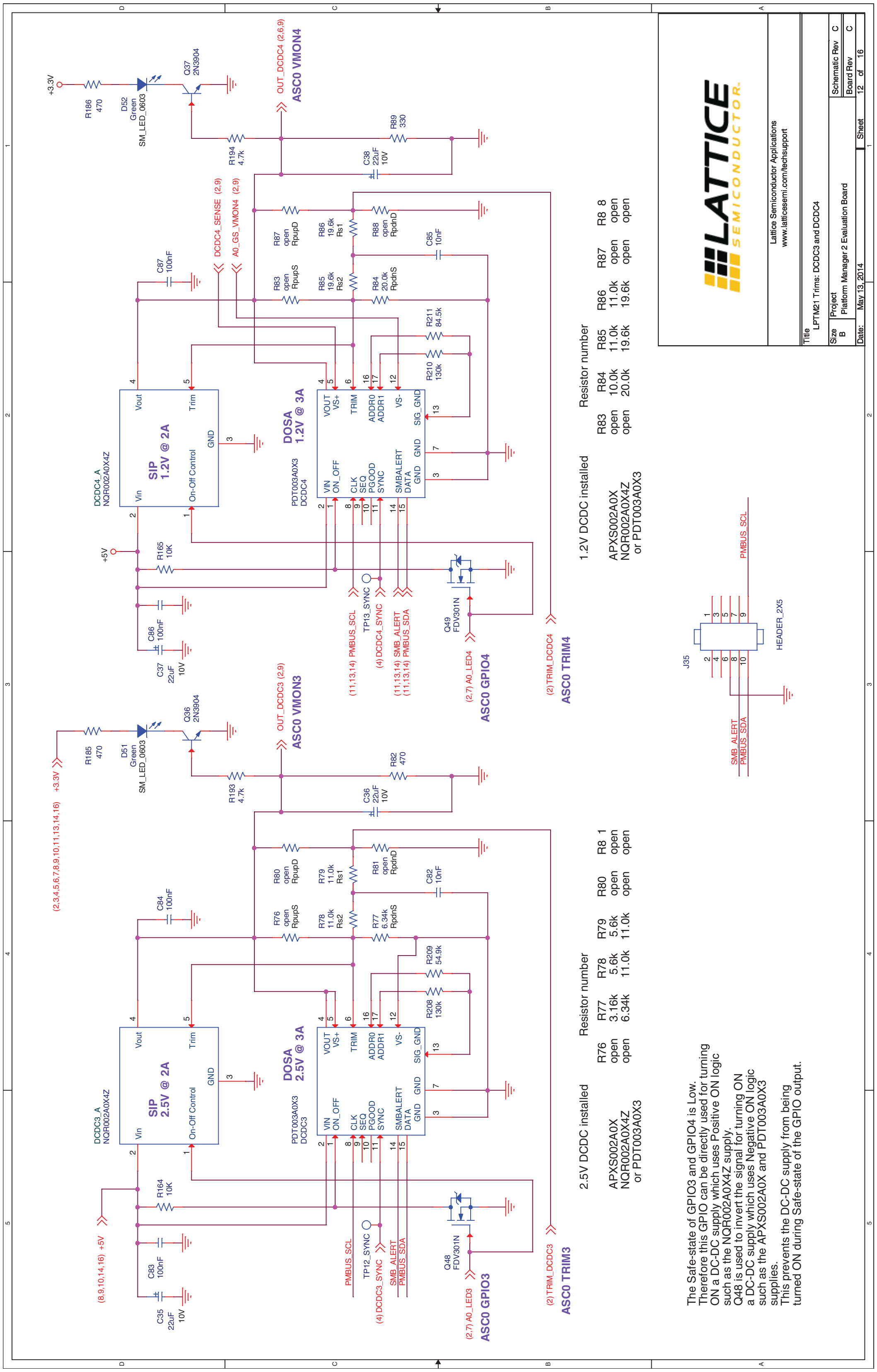


Figure 38. L-ASC10 #1 Trims: DCDC5 and DCDC6

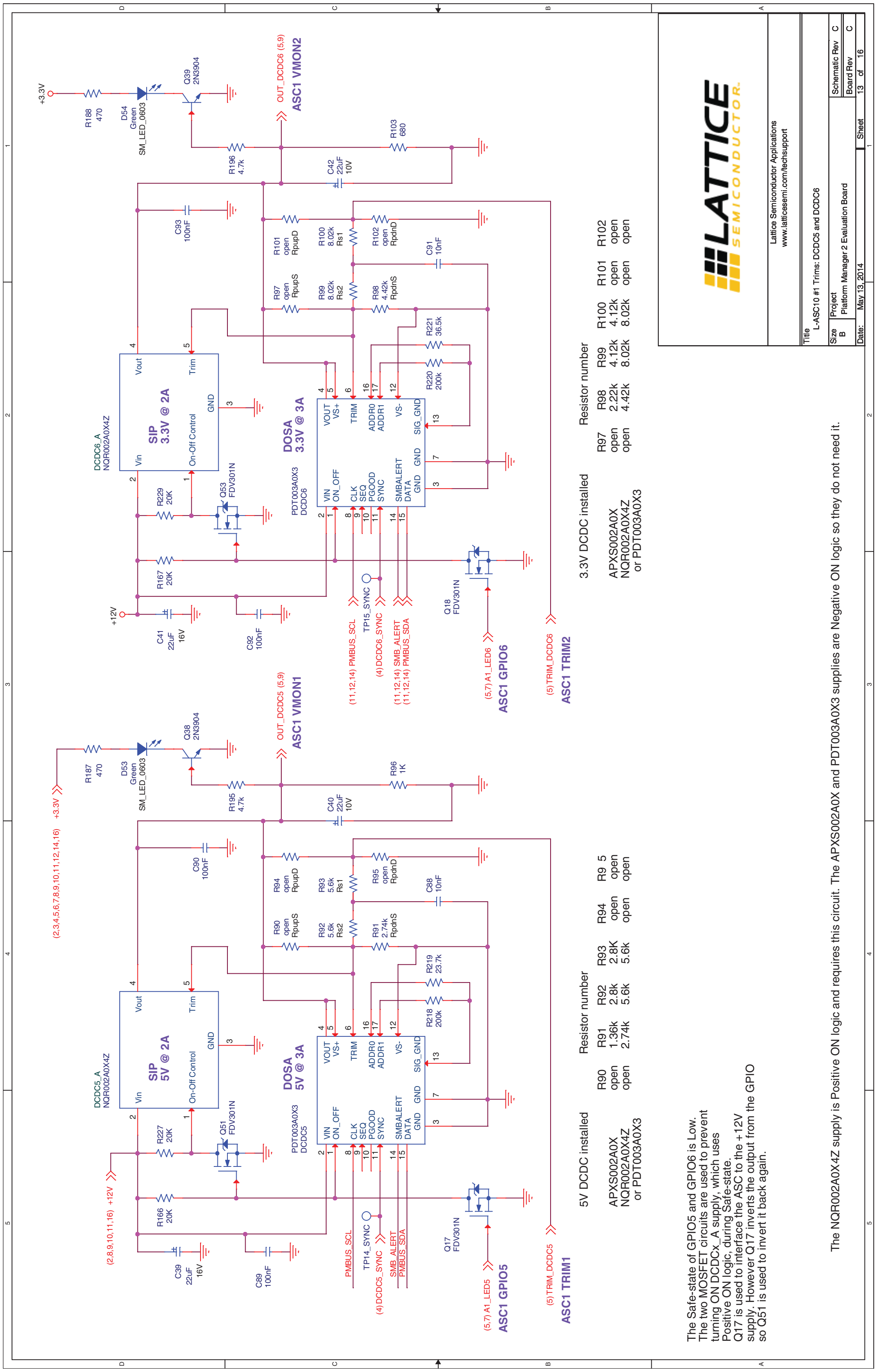


Figure 39. L-ASC10 #1 Trims: DCDC7 and DCDC8

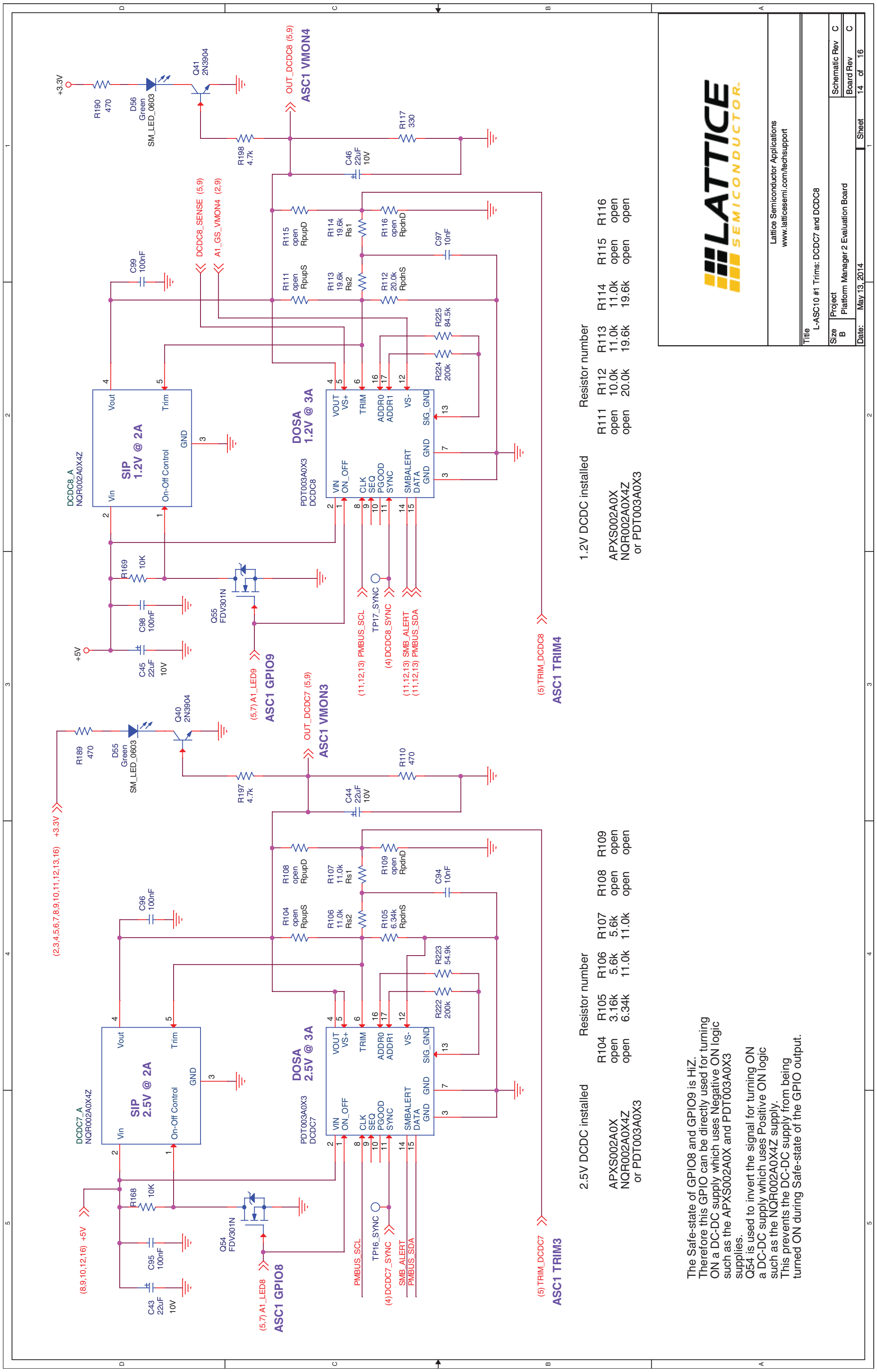


Figure 40. USB Programming Interface

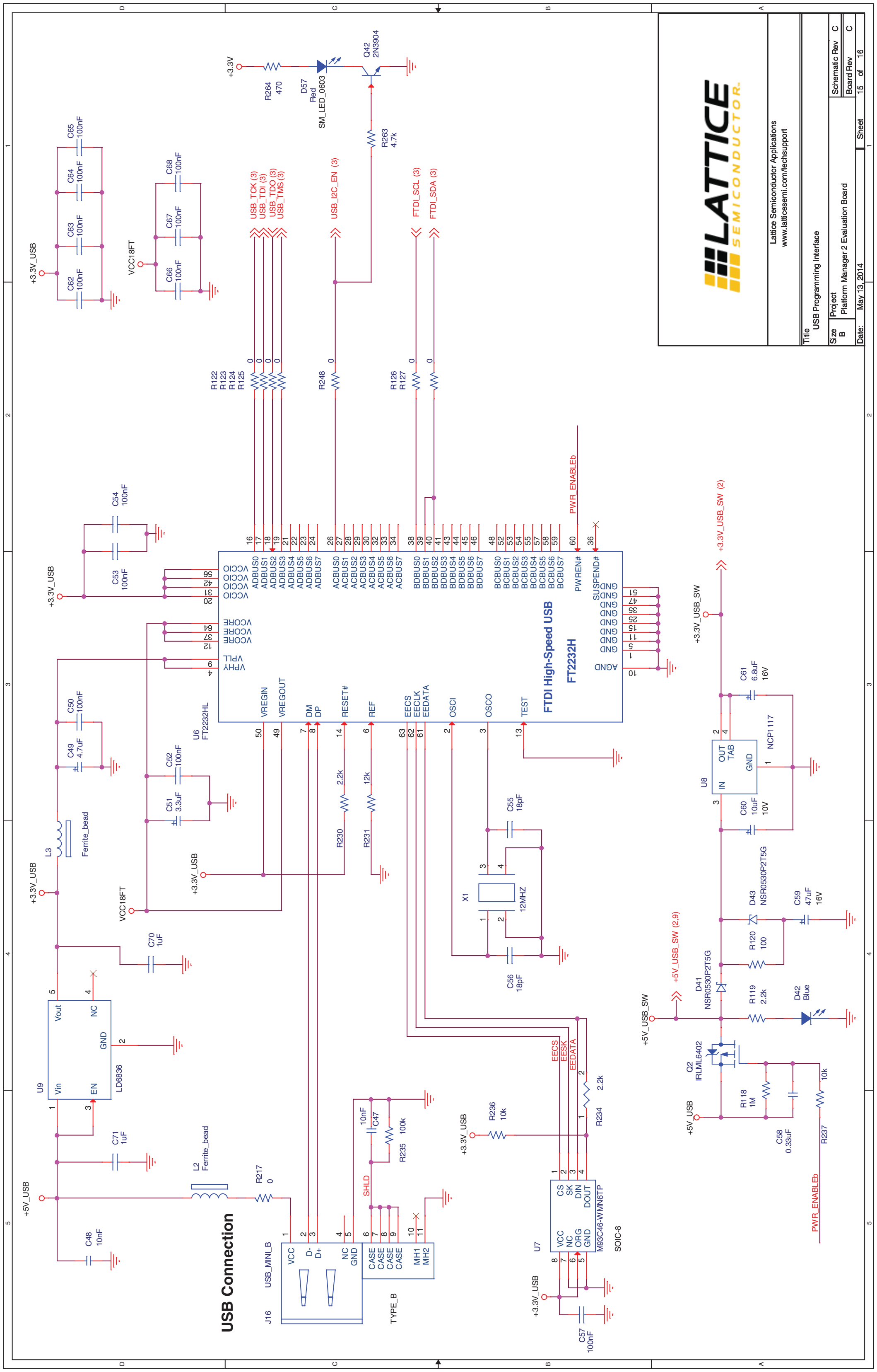
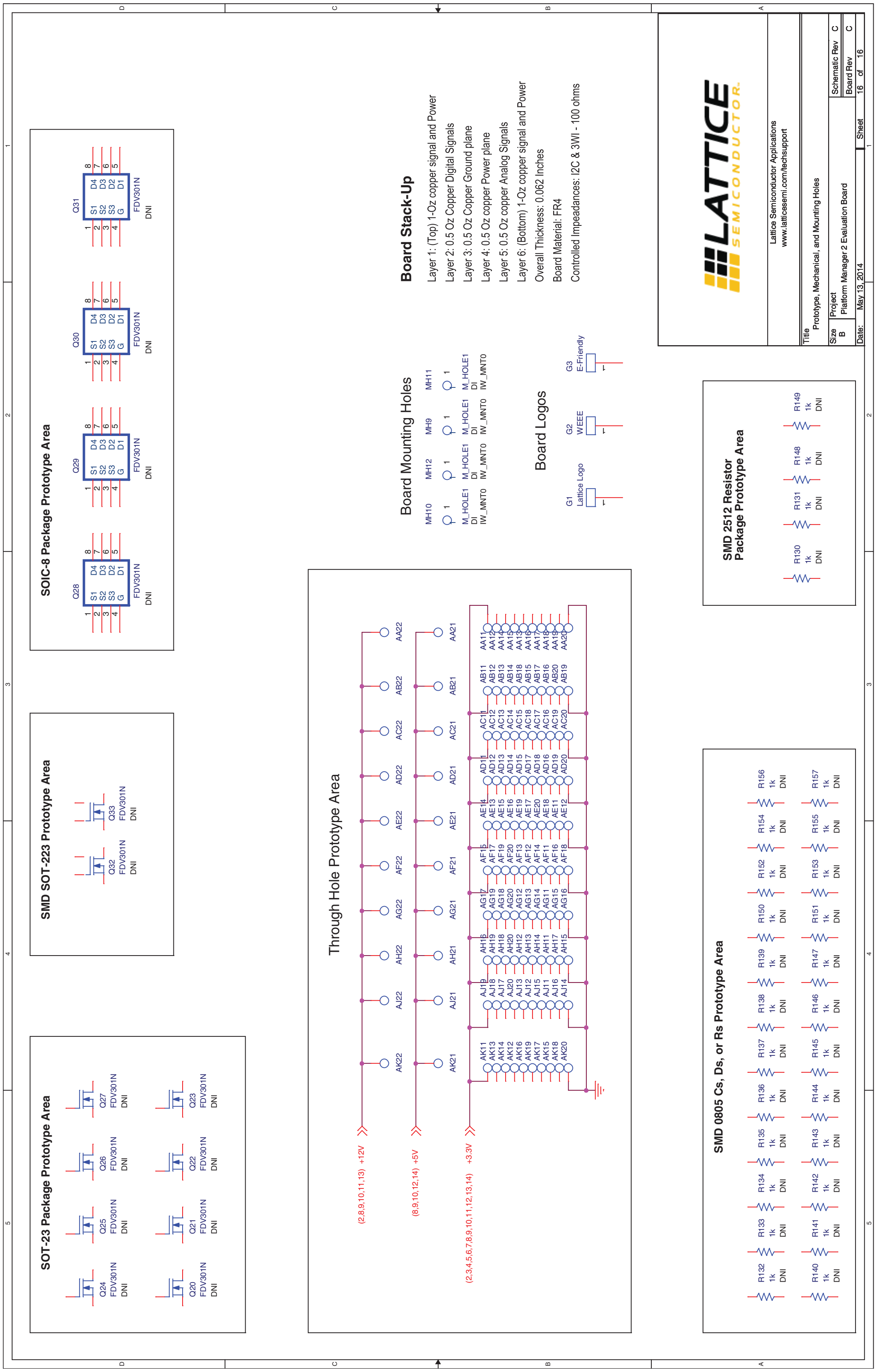


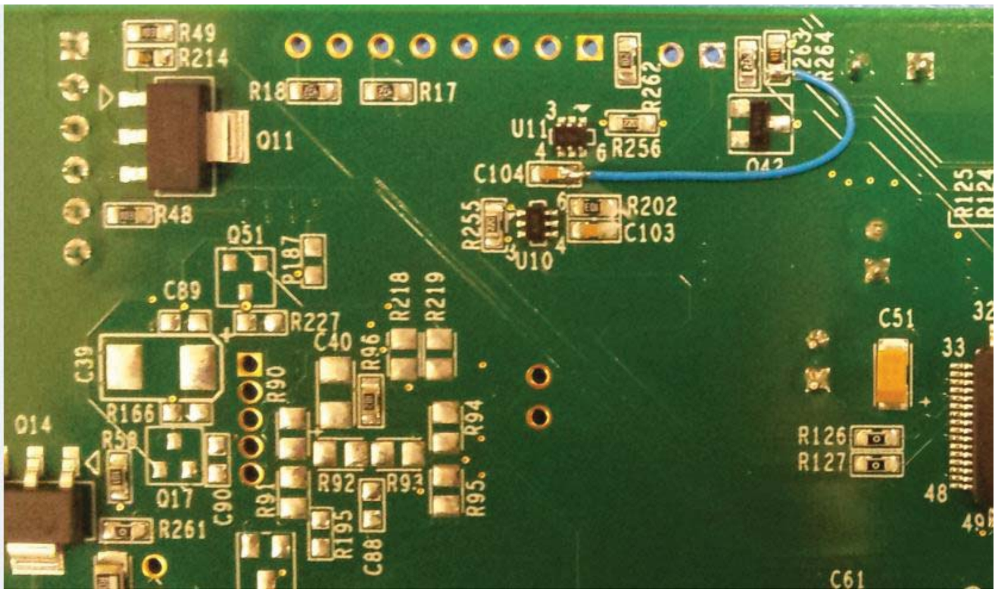
Figure 41. Prototype, Mechanical, and Mounting Holes



Appendix F. Known Issues

R264 is not connected to the +3.3 V plane on the board. A *blue* wire jumper is added to the bottom of the board to make the required connection for LED D57 to operate as shown in Figure 42.

Figure 42. Connecting R264 to the +3.3 V Plane



For the +12 V DC Buck Converter the package for Q1 was changed from the SOT-223 to the SOT23. The device is soldered down to pins 2 and 3 of the SOT-223 footprint and jumper wires are attached to the SOT-23 source and gate pins as shown in Figure 43.

Figure 43. Q1 Package Change and Connections