REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 07 through 09. Update boilerplate. Editorial changes throughout.	95-12-07	M. A. Frye
B	Add device type 10. Editorial changes throughout.	96-08-09	Raymond Monnin
C	Boilerplate update, part of 5 year review. ksr	06-08-16	Raymond Monnin

REV																				
SHEET																				
REV	C																			
SHEET	15																			

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
89-02-02

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 4K X 1 AND 1K X 4 STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87513**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87513	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		4096 x 1 CMOS static RAM	25 ns
02		4096 x 1 CMOS static RAM	35 ns
03		4096 x 1 CMOS static RAM	45 ns
04		1024 x 4 CMOS static RAM	25 ns
05		1024 x 4 CMOS static RAM	35 ns
06		1024 x 4 CMOS static RAM	45 ns
07		1024 x 4 CMOS static RAM	25 ns
08		1024 x 4 CMOS static RAM	35 ns
09		1024 x 4 CMOS static RAM	45 ns
10		1024 x 4 CMOS static RAM	35 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18 or CDIP2-T18	18	dual-in-line
X	See figure 1	18	flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Voltage on any pin relative to V_{SS} .....-2.0 V dc to +7.0 V dc
Voltage applied to outputs:
  devices 01-06, 10 .....-1.0 V dc to V_{CC} + 0.5 V dc
  devices 07-09 .....-0.5 V dc to +7.0 V dc
Storage temperature range.....-65°C to +150°C
Maximum power dissipation (P_D):
  devices 01-06 .....1.0 W
  devices 07-09 .....0.605 W
  device 10 .....0.660 W
Lead temperature (soldering, 10 seconds) .....+260°C
Thermal resistance, junction-to-case (θ_{JC}):
  Case V.....See MIL-STD-1835
  Case X.....15°C/W
Junction temperature (T_J) .....+175°C

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... 4.5 V dc to 5.5 V dc
Supply voltage (V_{SS}) ..... 0 V
Input high voltage (V_{IH}) ..... 2.0 V dc to V_{CC} + 0.5 V dc
Input low voltage (V_{IL}):
devices 01-06, 10 ..... -1.0 V dc to 0.8 V dc
devices 07-09 ..... -3.0 V dc to 0.8 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V_{CC} power supply current (average) 2/	I_{CC1}	$t_{AVAV} = t_{AVAV}$ (minimum)	1, 2, 3	01-03		80	mA
				04-09		110	
				10		120	
V_{CC} power supply current (standby, stable TTL input levels) 2/	I_{CC2}	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$	1, 2, 3	01-06, 10		15	mA
				07-09		10	
V_{CC} power supply current (standby, stable CMOS input levels) 2/	I_{CC3}	$\overline{CE} \ge (V_{CC} - 0.2\ V)$, all other inputs ≤ 0.2 V or $\ge (V_{CC} - 0.2\ V)$	1, 2, 3	01-06		6.0	mA
				10		10	
V_{CC} power supply current (standby, cycling CMOS input levels) 2/	I_{CC4}	$\overline{CE} \ge (V_{CC} - 0.2\ V)$, all other inputs ≤ 0.2 V or $\ge (V_{CC} - 0.2\ V)$	1, 2, 3	01-06		10	mA
				10		20	
Input leakage current, any input	I_{ILK}	V_{CC} = 5.5 V, V_{IN} = 0.0 V to 5.5 V	1, 2, 3	01-06		±5.0	µA
				07-10		±10	
Off state output leakage current	I_{OLK}	V_{CC} = 5.5 V, V_{IN} = 0.0 V to 5.5 V	1, 2, 3	01-06, 10		±10	µA
				07-09		±50	
Output high voltage	V_{OH}	I_{OUT} = -4.0 mA, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	I_{OUT} = 12 mA, V_{IL} = 0.8 V	1, 2, 3	01-03		0.4	V
		I_{OUT} = 8.0 mA, V_{IL} = 0.8 V	1, 2, 3	04-10		0.4	
Input capacitance	C_{IN}	V_{IN} = 0.0 V to 3.0 V, f = 1.0 MHz, T_A = +25°C, See 4.3.1c	4	01-06		4.0	pF
				07-10		8.0	
Output capacitance	C_{OUT}	V_{IN} = 0.0 V to 3.0 V, f = 1.0 MHz, T_A = +25°C, See 4.3.1c	4	01-06		4.0	pF
				07-10		8.0	
Functional tests		See 4.3.1d	7, 8A, 8B	All			
Chip enable access time	t_{ELQV}	See figures 4 and 5	9, 10, 11	01,04, 07		25	ns
				02,05, 08,10		35	
				03,06,09		45	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}	See figures 4 and 5 3/	9, 10, 11	01,04, 07	25		ns
				02,05, 08,10	35		
				03,06, 09	45		
Address access time	t_{AVQV}	See figures 4 and 5 4/	9, 10, 11	01,04, 07		25	ns
				02,05, 08,10		35	
				03,06, 09		45	
Output hold after address change	t_{AVQX}	See figures 4 and 5	9, 10, 11	01-06, 09	5.0		ns
				10	3.0		
				07,08	0		
Chip enable to output active	t_{ELQX}	See figures 4 and 5 5/	9, 10, 11	01-06	5.0		ns
				07	8		
				08,09	10		
				10	2.0		
Chip disable to output inactive	t_{EHQZ}	See figures 4 and 5 5/ 6/	9, 10, 11	01,05, 06, 08-10	0	20	ns
				02,03	0	30	
				04,07	0	15	
Chip enable to power up	t_{ELPU}	See figures 4 and 5 5/	9, 10, 11	All	0		ns
Chip enable to power down	t_{EHPD}	See figures 4 and 5 5/	9, 10, 11	All		30	ns
Input rise and fall times	t_T	5/ 7/	9, 10, 11	01-09		50	ns
				10		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle time	t_{AVAV}	See figures 4 and 6	9, 10, 11	01,04, 07	25		ns
				02,05, 08,10	35		
				03,06, 09	45		
Write pulse width	t_{WLWH}	See figures 4 and 6	9, 10, 11	01,04	15		ns
				02,07	20		
				03,05, 10	25		
				08	30		
				06,09	35		
Chip enable to end of write	t_{ELEH}	See figures 4 and 6	9, 10, 11	01,04, 07	20		ns
				02,05, 08,10	30		
				03,06, 09	40		
Data setup to end of write	t_{DVWH}	See figures 4 and 6	9, 10, 11	01,05, 06,10	15		ns
				02,03, 08,09	20		
				04	10		
				07	12		
Data hold after end of write	t_{WHDX}	See figures 4 and 6	9, 10, 11	All	0		ns
Address setup to end of write	t_{AVWH}	See figures 4 and 6	9, 10, 11	01,04, 07	20		ns
				02,05, 08,10	30		
				09	35		
				03,06	40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V V_{SS} = 0 V unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address setup to beginning of write	t_{AVWL}	See figures 4 and 6	9, 10, 11	All	0		ns
Address hold after end of write	t_{WHAV}	See figures 4 and 6	9, 10, 11	All	0		ns
Write enable to output disable	t_{WLQZ}	See figures 4 and 6	9, 10, 11	01,04	0	15	ns
				02,03, 05,06, 10	0	20	
				07-09	0	8	
Output active after end of write	t_{WHQX}	See figures 4 and 6 5/ 8/	9, 10, 11	All	0		ns

1/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0.0 V to 3.0 V and output loading of 30 pF load capacitance. Output timing reference is 1.5 V.

2/ I_{CC} is dependent upon output loading and cycle rate. The specified values apply with output(s) unloaded.

3/ For read cycles 1 and 2, $\overline{WE}$ is high for entire cycle.

4/ Device is continuously selected, $\overline{CE}$ low.

5/ Parameter may not be tested, but shall be guaranteed to the limits specified in table I.

6/ This parameter is measured ±200 mV from steady state output voltage for device types 01 through 06. For device types 07 through 10, this is measured ±500 mV from steady state output voltage. Load capacitance is 5.0 pF.

7/ Measured between V_{IL} maximum and V_{IH} minimum.

8/ If $\overline{WE}$ is low when $\overline{CE}$ goes low, the output remains in the high impedance state.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

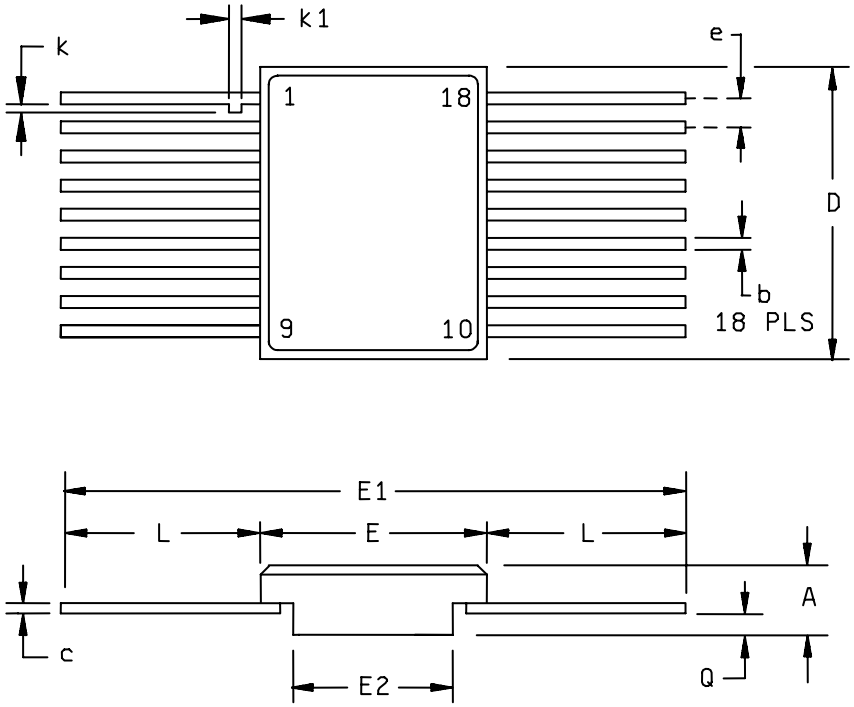
b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

Case X



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.08	2.54	.082	.100
b	0.38	0.48	.015	.019
c	0.10	0.18	.004	.007
D	10.72	11.23	.422	.442
E	7.67	8.08	.302	.318
E1	22.35 REF		.880 REF	
E2	5.67	5.99	.224	.236
e	1.19 REF	1.35 REF	.047 REF	.053 REF
k	0.20 Nom.		.008 Nom.	
k1	0.25 Nom.		.010 Nom.	
L	6.86	7.62	.270	.300
Q	0.66	---	.026	---
S2	0.64 Nom.		.025 Nom	

FIGURE 1. Case outline.

Device types	01-03	04-10
Case outlines	X, Y	X, Y
Terminal number	Terminal symbol	
1	A_0	A_6
2	A_2	A_5
3	A_6	A_4
4	A_8	A_3
5	A_{10}	A_0
6	A_5	A_1
7	Q	A_2
8	$\overline{WE}$	$\overline{CE}$
9	V_{SS}	V_{SS}
10	$\overline{CE}$	$\overline{WE}$
11	D	I/O_4
12	A_7	I/O_3
13	A_{11}	I/O_2
14	A_9	I/O_1
15	A_4	A_9
16	A_3	A_8
17	A_1	A_7
18	V_{CC}	V_{CC}

FIGURE 2. Terminal connections.

Device types 01 through 03

$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

H = Logic "1" state
L = Logic "0" state
X = Don't care

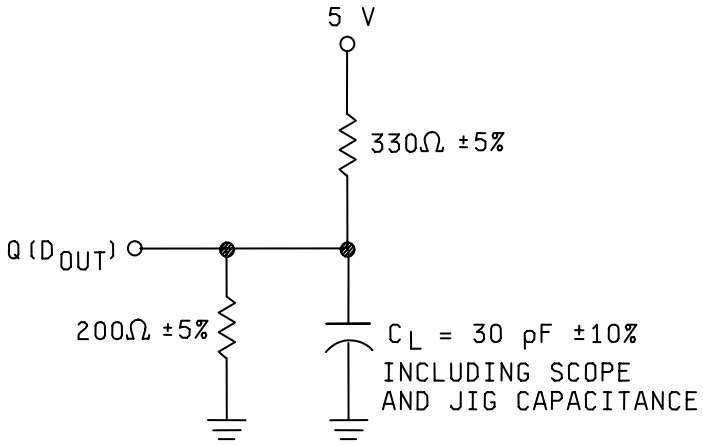
Device types 04 through 10

$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

H = Logic "1" state
L = Logic "0" state
X = Don't care

FIGURE 3. Truth tables.

DEVICE TYPES 01 THRU 03



DEVICE TYPES 04 THRU 10

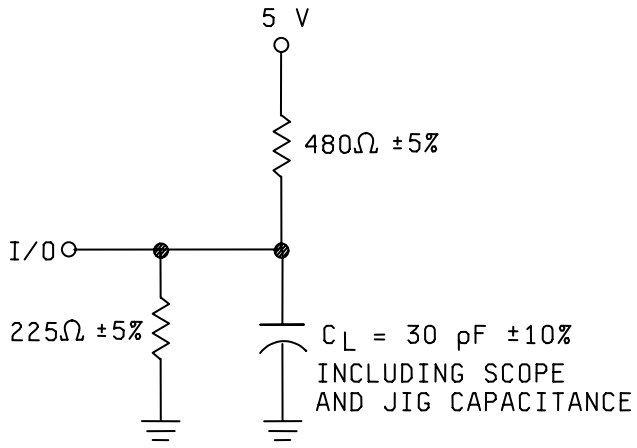
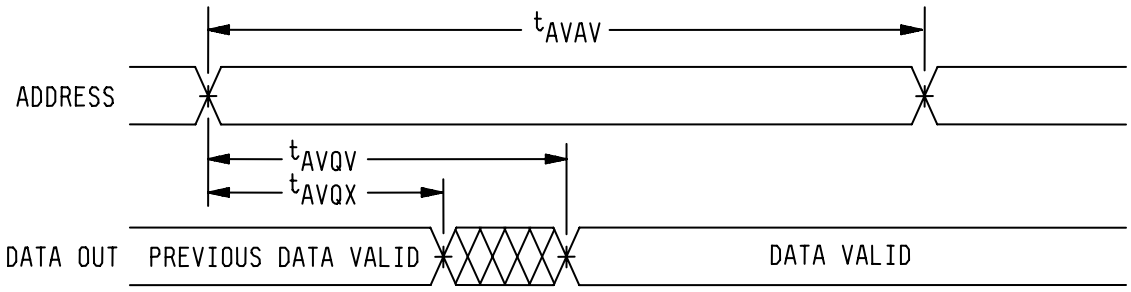
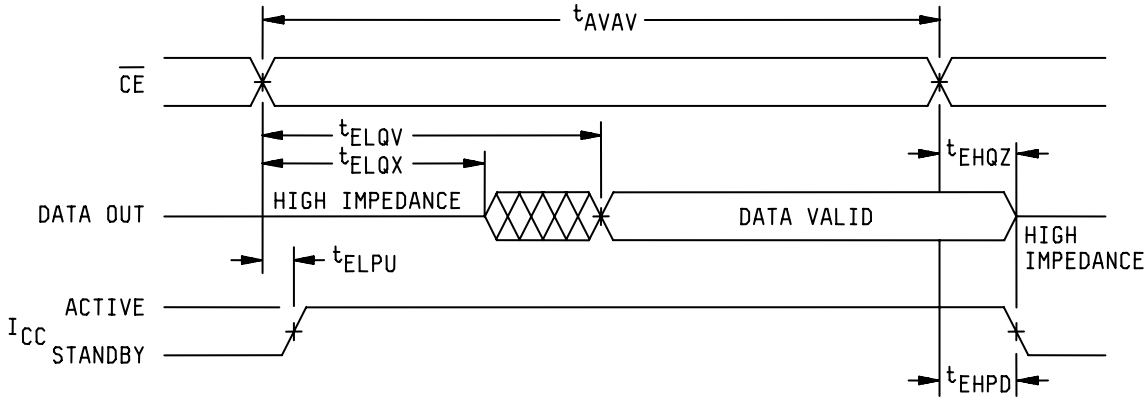


FIGURE 4. Output load circuit.

Read cycle no. 1: $\overline{WE}$ high, $\overline{CE}$ low (see notes 1, 2, and 3)



Read cycle no. 2 : $\overline{WE}$ high (see notes 1 and 2)

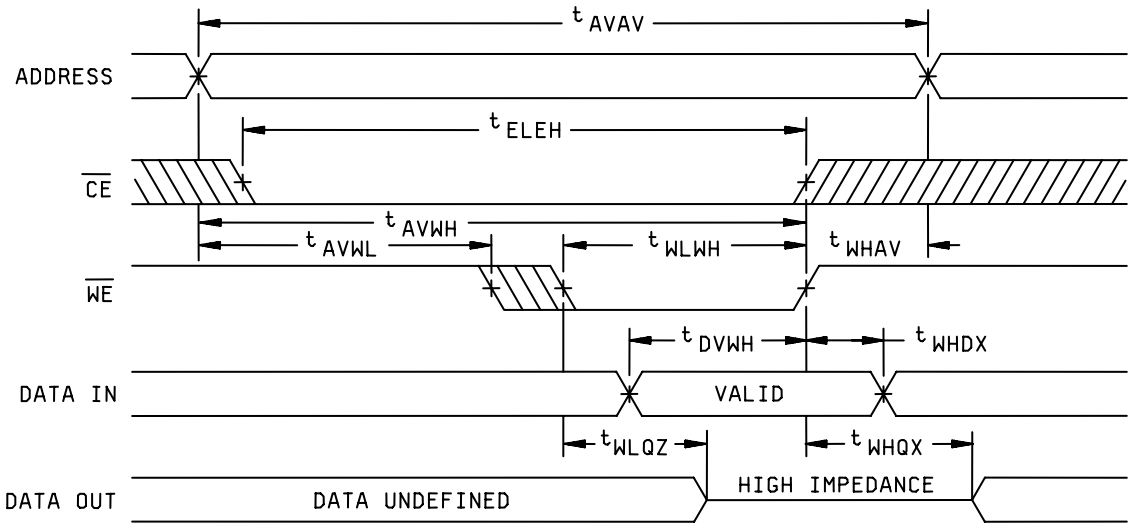


NOTES:

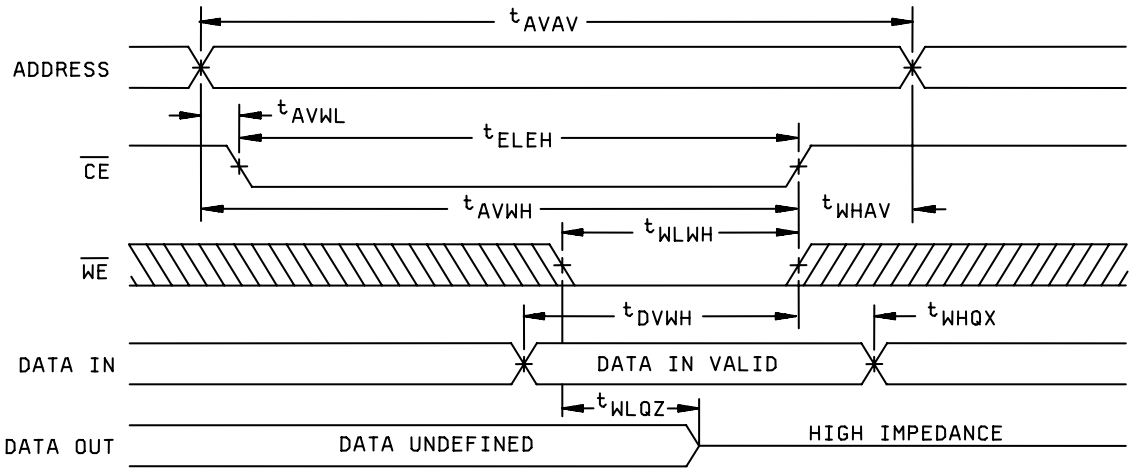
1. $\overline{WE}$ is high for entire cycle.
2. $\overline{CE}$ and $\overline{WE}$ must transition between V_{IH}(min) to V_{IL}(max) or V_{IL}(max) to V_{IH}(min) in a monotonic fashion.
3. Device is continuously selected, $\overline{CE}$ low.

FIGURE 5. Read cycle timing diagrams.

Write cycle no. 1: $\overline{WE}$ controlled (see notes 1 and 2)



Write cycle no. 2: $\overline{CE}$ controlled (see notes 1 and 2)



NOTES:

1. $\overline{CE}$ and $\overline{WE}$ must transition between V_{IH}(min) to V_{IL}(max) or V_{IL}(max) to V_{IH}(min) in a monotonic fashion.
2. $\overline{CE}$ and $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

FIGURE 6. Write cycle timing diagrams.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1,2,3,4**,7*,8A,8B, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2, 3

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-08-16

Approved sources of supply for SMD 5962-87513 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8751301VA	3/	IMS1203S-25M
5962-8751301XA	3/	IMS1203Y-25M
5962-8751302VA	3/	IMS1203S-35M
5962-8751302XA	3/	IMS1203Y-35M
5962-8751303VA	3/	IMS1203S-45M
5962-8751303XA	3/	IMS1203Y-45M
5962-8751304VA	3/	IMS1223S-25M
5962-8751304XA	3/	IMS1223Y-25M
5962-8751305VA	3/	IMS1223S-35M
5962-8751305XA	3/	IMS1223Y-35M
5962-8751306VA	3/	IMS1223S-45M
5962-8751306XA	3/	IMS1223Y-45M
5962-8751307VA	0C7V7 3DTT2	CY7C148-25DMB P4C148-25CMB
5962-8751308VA	0C7V7 3DTT2	CY7C148-35DMB P4C148-35CMB
5962-8751309VA	0C7V7 3DTT2	CY7C148-45DMB P4C148-45CMB
5962-8751310VA	3DTT2	P4C148-35DMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
3DTT2	Pyramid Semiconductor Corporation 1340 Bordeaux Drive Sunnyvale, CA 94089

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