



# Infineon® MUNICH512/256

## Multi-channel Network Interface Controller for 512/256 Channels with PCI

MUNICH512/256 is a highly integrated protocol controller that implements HDLC (High-Level Data Link Control), PPP (Point-to-Point Protocol), SS7 (Signalling System 7) protocol and Transparent Mode (TMA) processing for up to 512/256 bi-directional channels. An on-chip data management unit is optimized to transfer data packets via PCI interface by minimizing the bus load.

The MUNICH512/256 perfectly fits in voice or data control applications in the wireless 2G/3G infrastructure or low end E1/T1 router. As a stand-alone HDLC controller with PCI, the MUNICH512/256 is ready for current and next generation interconnect requirements.

### Applications

- Wireless 2G/3G Infrastructure
- Central Office (CO) switches/routers
- E1/T1-line cards
- Central D-channel controller for 512/256 ISDN basic access
- Multiplexer for terminals and other peripherals
- Frame relay switches

### Features

- PCI 2.1 compliant interface
- Protocol processing on up to 16 T1, E1, channelized 4-Mbit/s, channelized 8-Mbit/s or unchannelized links for frame relay, router or DSLAM applications with a maximum aggregate data rate of up to 131.072 Mbit/s per direction
- Support for 512/256 bi-directional channels; channels may be assigned arbitrarily to a maximum of 16 links, for HDLC, PPP, SS7, or TMA processing
- Enhanced SS7 protocol processing with support for ITU-T Q.703 including Annex A
- Concatenation of time slots to logical channels on each physical link; assignment need not be consecutive. Supports DSO, fractional T1/E1, or T1/E1 channels

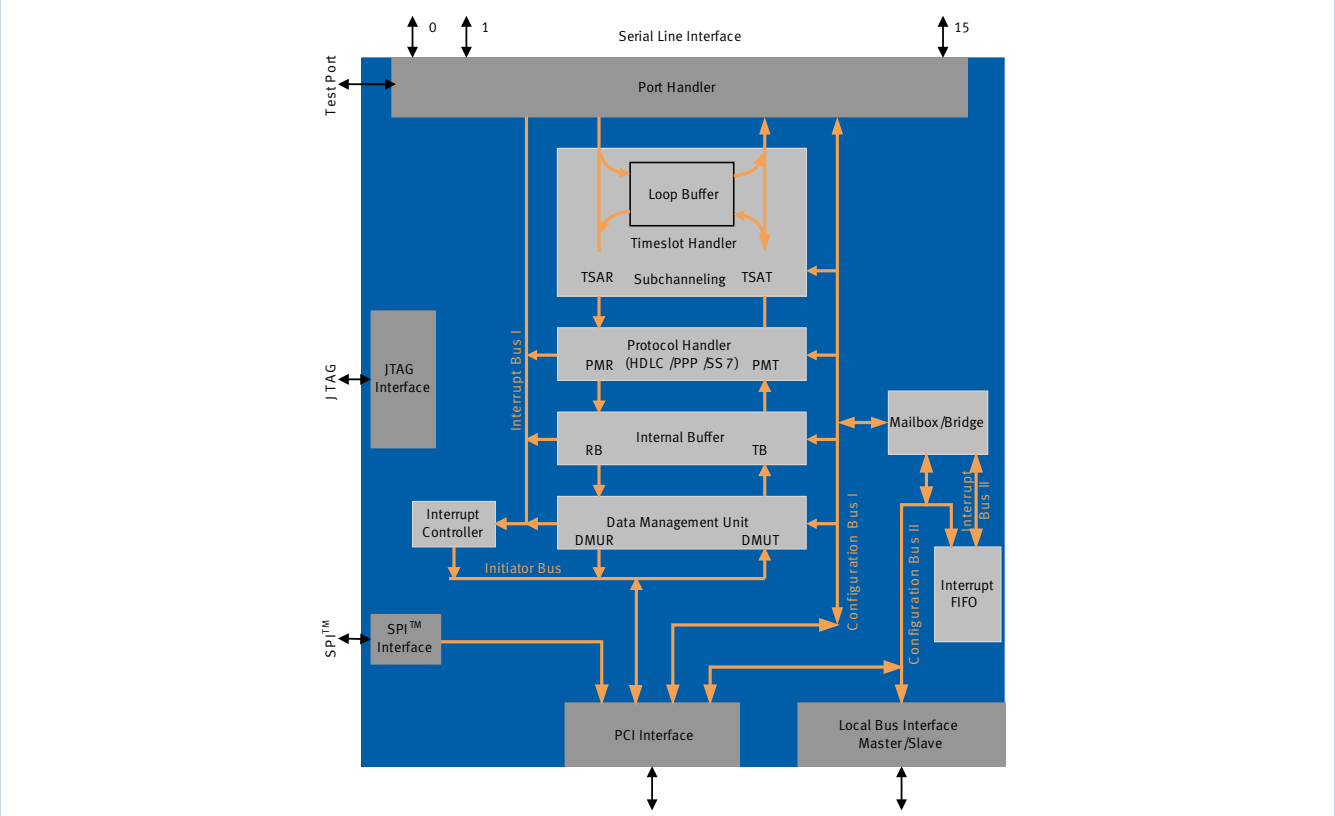
### Features

- Support for up to 4 sub-channels per time slot, each sub-channel supports a data rate from 8 kbit/s up to 56 kbit/s
- Additional support for unchannelized modes with data rates of up to 45 Mbit/s on Port 0 and 8.192 Mbit/s on each of the other ports
- Data buffers of 64 kB in the transmit direction & 24 kB in the receive direction
- Payload loops for each port are selectable independently
- Test function supports the assignment of one of 16 ports as a test port
- Support for Message Signaled Interrupt (MSI) and legacy INTx emulation
- Integration of local microprocessor master and slave interface (demultiplexed 16-bit address and data bus in Intel Mode or Motorola Mode) for access to the local bus via PCI Express or for communication with a PCI Express host processor through an on-chip mailbox
- JTAG boundary scan according to IEEE1149.1 (5 pins)
- 3.3 V LVTTTL I/Os
- Package SG-FCLBGA-323-1 (18 mm x 20 mm, 1 mm pitch)
- Full scan path and BIST of on-chip RAM for production test
- Performance: 131.072 Mbit/s data throughput per direction
- Power consumption 0.7W
- Extended temperature range -40 to +85°C

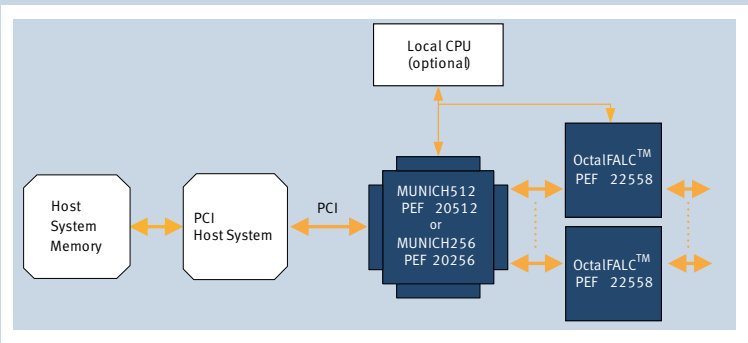
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## Multi-channel Network Interface Controller for 512/256 Channels

Block Diagram of MUNICH512/256



System Diagram of MUNICH512/256



Product Summary

Sales Code	Description	Package
PEF 20512E	Multichannel Network Interface Controller for 512 channels	SG-FCLBGA-323-1, 18 x 20mm
PEF 20256	Multichannel Network Interface Controller for 256channels	SG-FCLBGA-323-1, 18 x 20mm
EASY 512/256 PCI	MUNICH512/256 Reference Design	Board, Software and Documentation

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