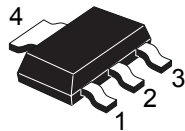
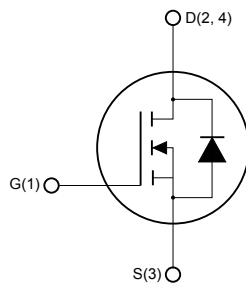


N-channel 600 V, 7.3 Ω typ., 0.4 A SuperMESH Power MOSFET in a SOT-223 package



SOT-223



Int_schem_nTnZ_SOT_223

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STN1HNK60	600 V	8.5 Ω	0.4 A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized

Applications

- Switching applications

Description

This high voltage device is an N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link

[STN1HNK60](#)

Product summary

Order code	STN1HNK60
Marking	N1HNK60
Package	SOT-223
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_A = 25\text{ }^{\circ}\text{C}$	0.4	A
I_D	Drain current (continuous) at $T_A = 100\text{ }^{\circ}\text{C}$	0.25	A
$I_{DM}^{(1)}$	Drain current (pulsed)	1.6	A
P_{TOT}	Total dissipation at $T_A = 25\text{ }^{\circ}\text{C}$	3.3	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	3	V/ns
T_J	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 0.4\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	38	$^{\circ}\text{C}/\text{W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	0.4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	25	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.25	3	3.7	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.5\text{ A}$		7.3	8.5	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	156		pF
C_{oss}	Output capacitance		-	23.5		pF
C_{rss}	Reverse transfer capacitance		-	3.8		pF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	7	$10^{(1)}$	nC
Q_{gs}	Gate-source charge		-	1.1		nC
Q_{gd}	Gate-drain charge		-	3.7		nC

1. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 0.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	6.5	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	19	-	ns
t_f	Fall time		-	25	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		1.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 0.4 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 1.0 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 25 \text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	140		ns
Q_{rr}	Reverse recovery charge		-	240		nC
I_{RRM}	Reverse recovery current		-	3.3		A
t_{rr}	Reverse recovery time	$I_{SD} = 1.0 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 25 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	229		ns
Q_{rr}	Reverse recovery charge		-	377		nC
I_{RRM}	Reverse recovery current		-	3.3		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area

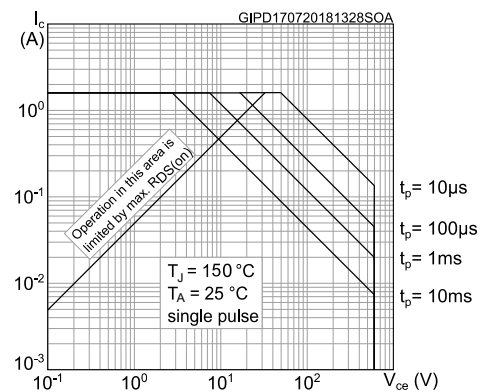


Figure 2. Normalized transient thermal impedance

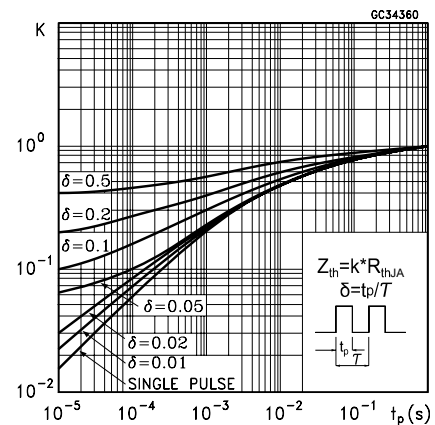


Figure 3. Typical output characteristics

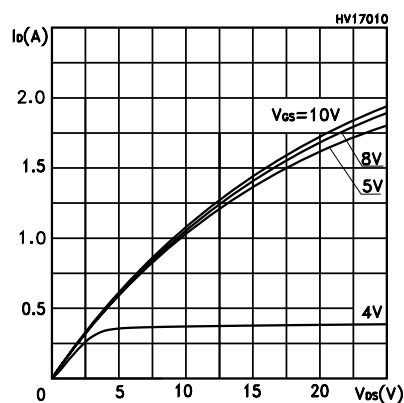


Figure 4. Typical transfer characteristics

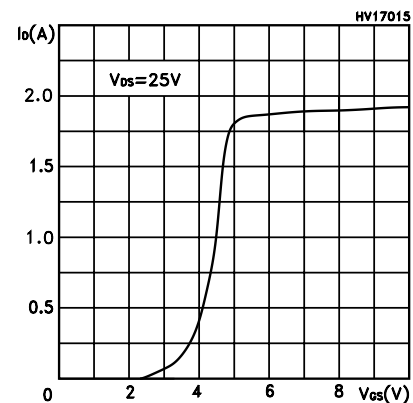


Figure 5. Typical gate charge characteristics

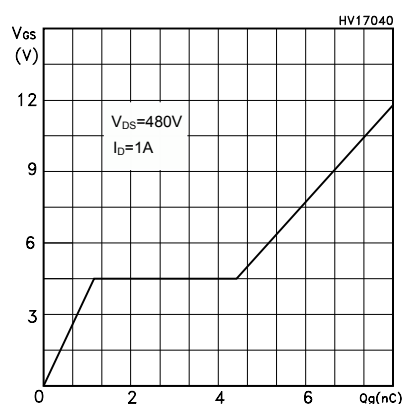


Figure 6. Typical capacitance characteristics

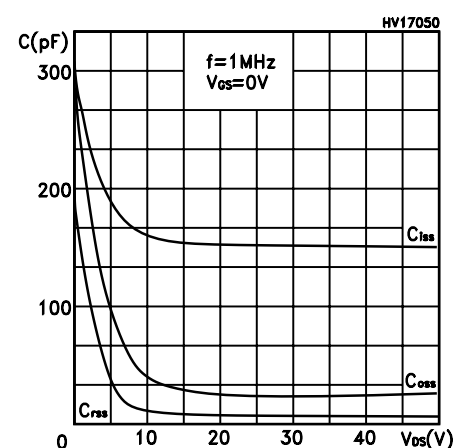


Figure 7. Typical static drain-source on-resistance

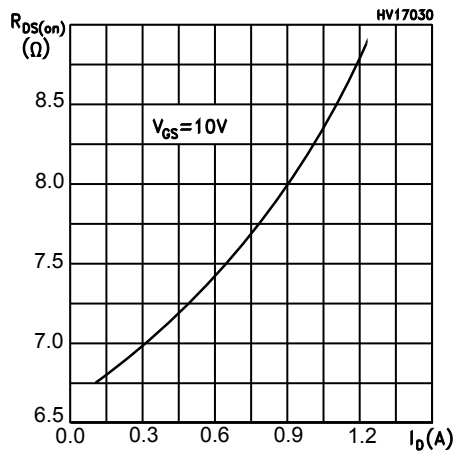


Figure 8. Normalized gate threshold vs temperature

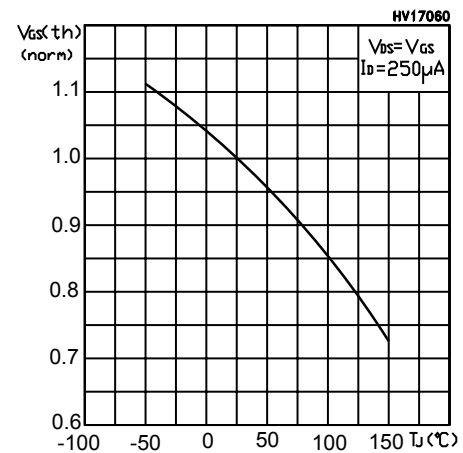


Figure 9. Normalized on-resistance vs temperature

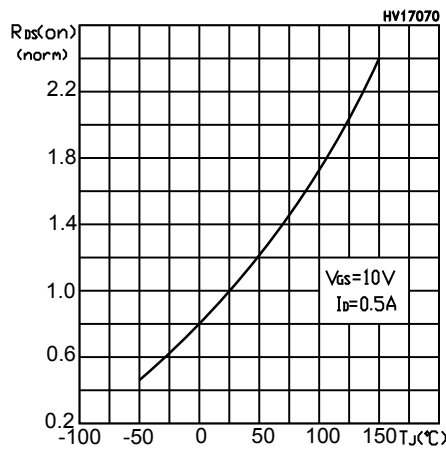


Figure 10. Typical reverse diode forward characteristics

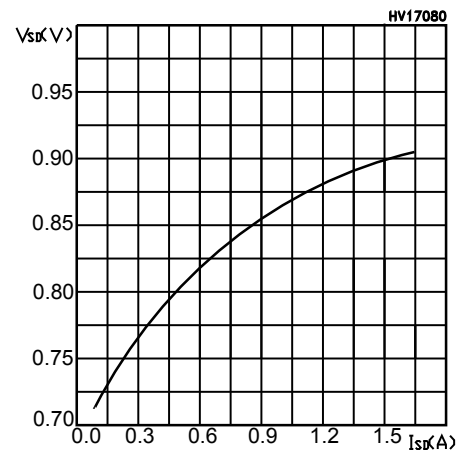


Figure 11. Normalized breakdown voltage vs temperature

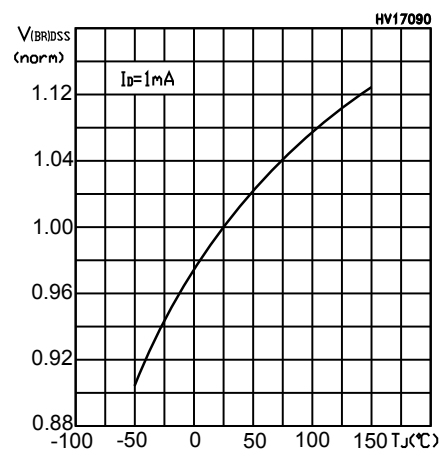
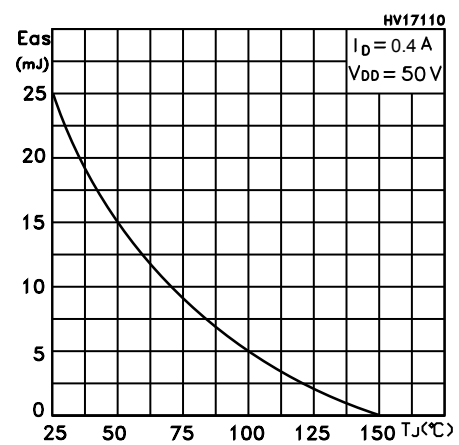
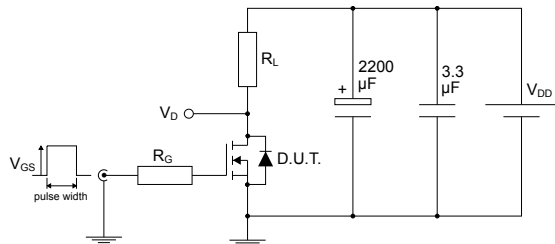


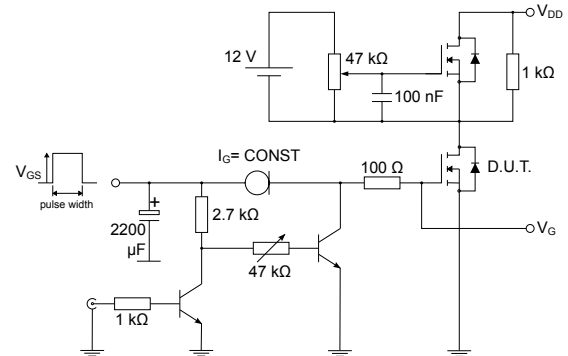
Figure 12. Maximum avalanche energy vs temperature



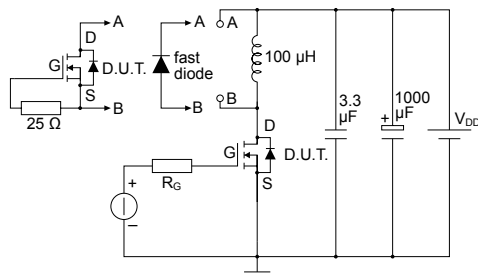
3 Test circuits

Figure 13. Test circuit for resistive load switching times


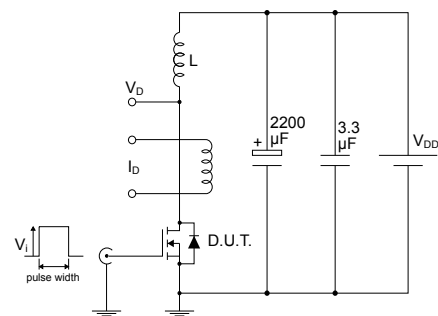
AM01468v1

Figure 14. Test circuit for gate charge behavior


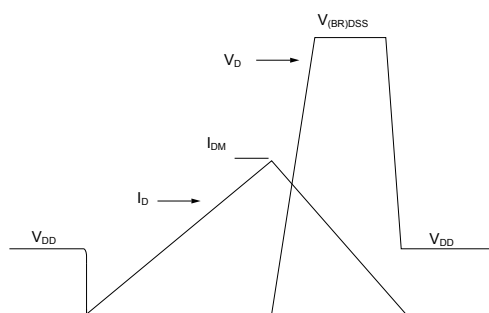
AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times


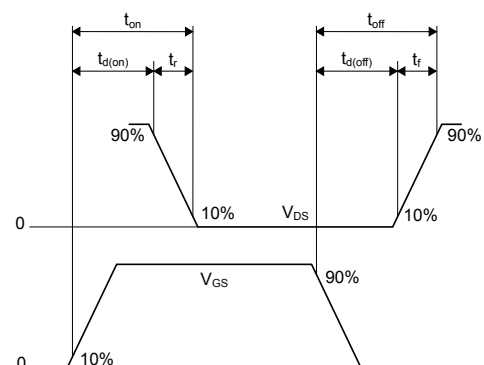
AM01470v1

Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


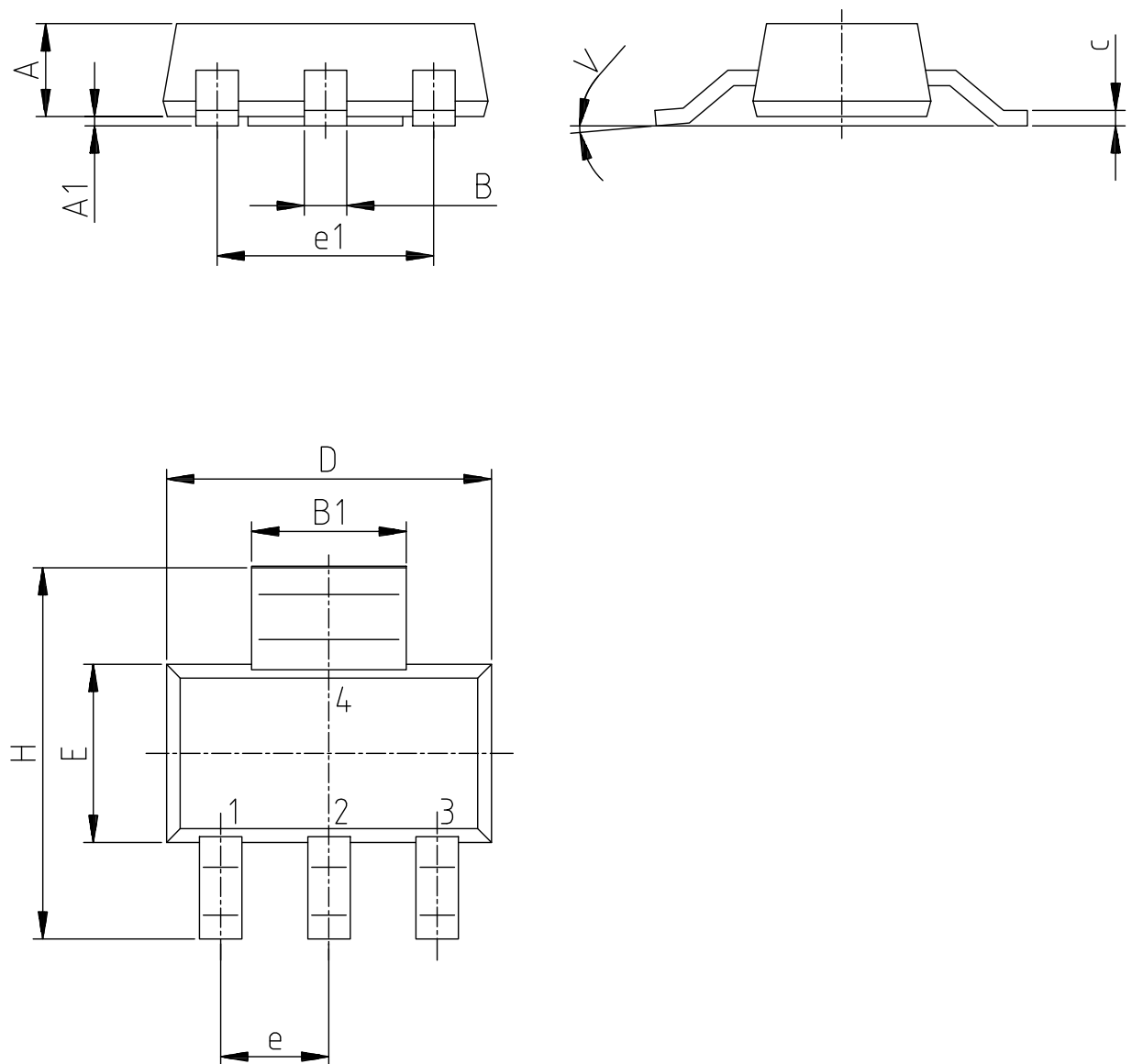
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SOT-223 package information

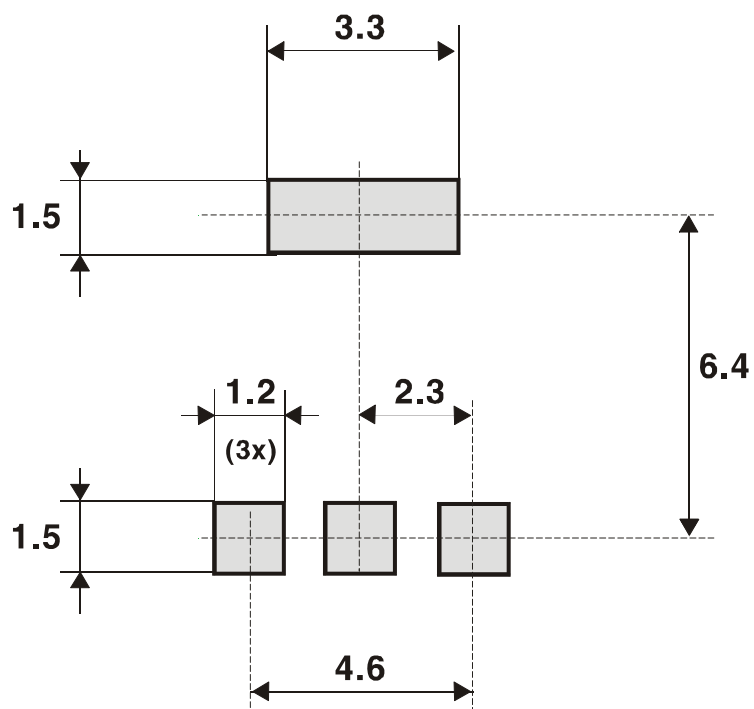
Figure 19. SOT-223 package outline



0046067_15

Table 8. SOT-223 package mechanical data

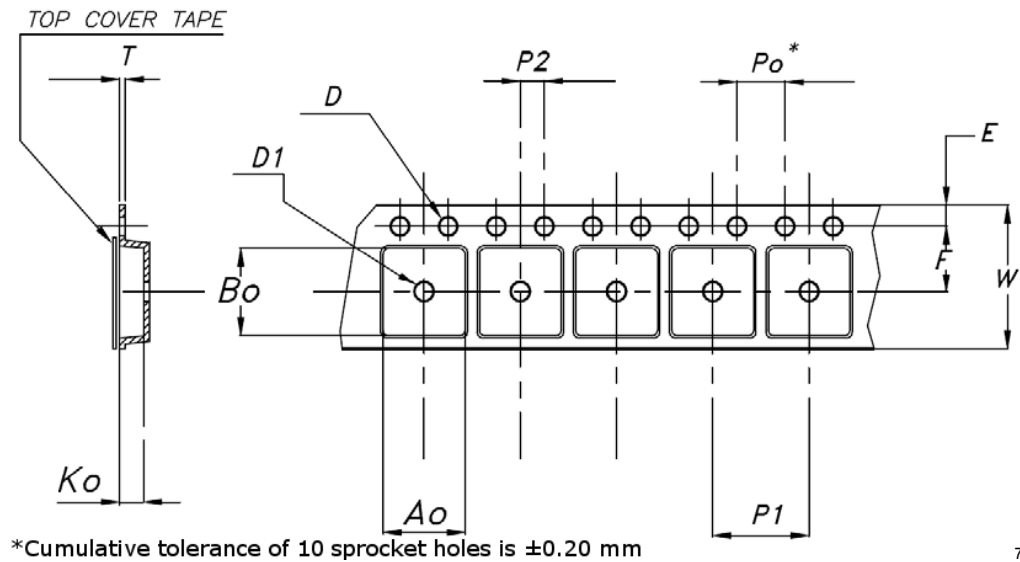
Dim.	mm		
	Min.	Typ.	Max.
A			1.8
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7	7.3
V			10 deg
A1	0.02		0.1

Figure 20. SOT-223 recommended footprint (dimensions are in mm)


0046067_15

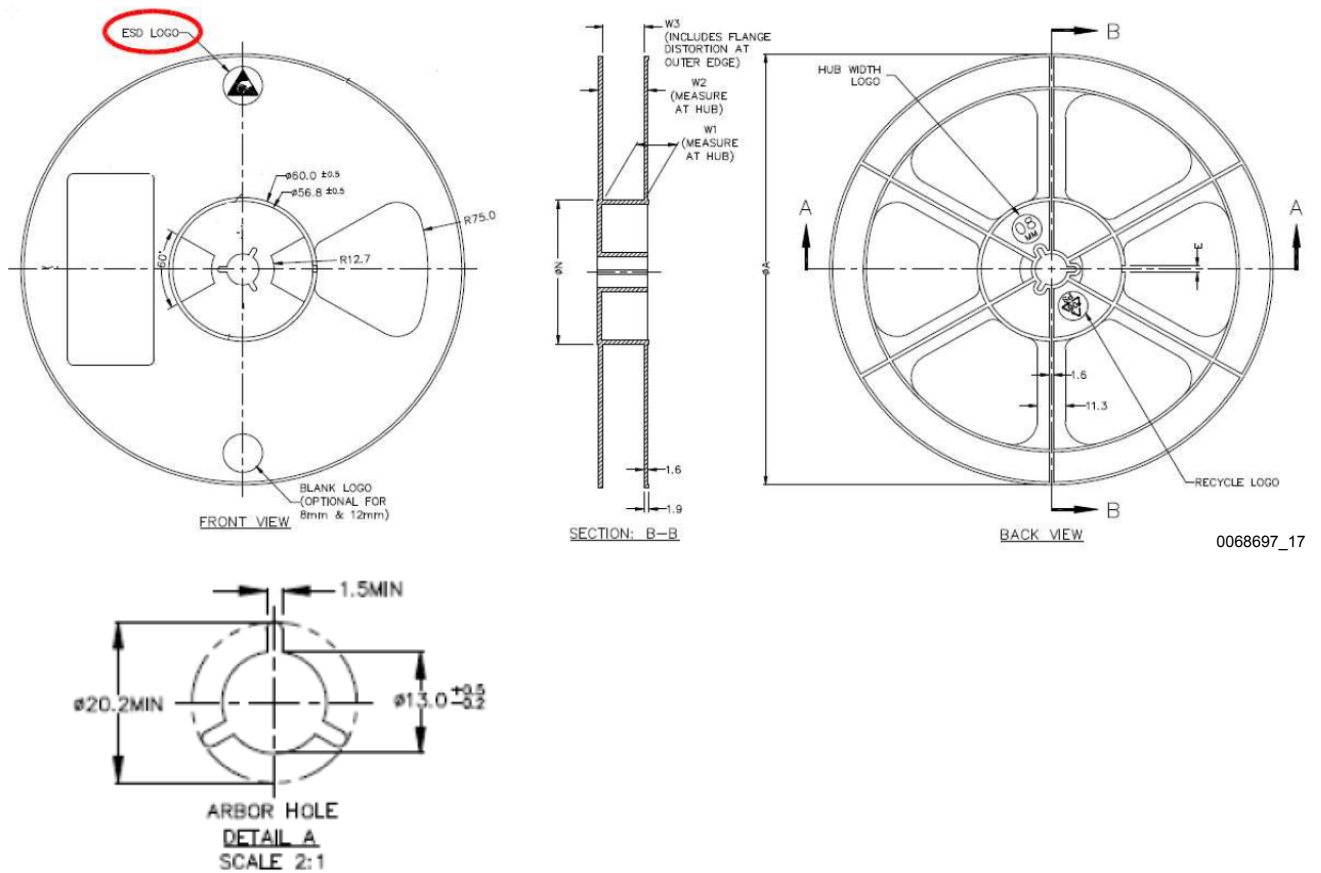
4.2 SOT-223 packing information

Figure 21. SOT-223 tape outline



7737436_3

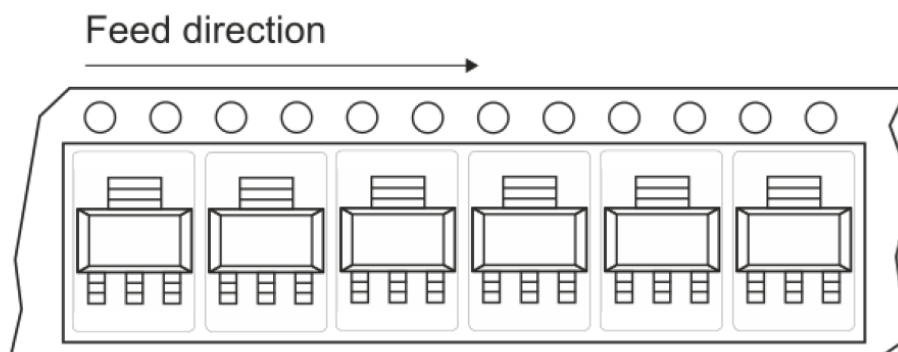
Figure 22. SOT-223 reel outline



0068697_17

Table 9. SOT-223 tape and reel mechanical data

Tape				Tape		
Dim.	mm			Dim.	mm	
	Min.	Typ.	Max.		Min.	Max.
A0	6.75	6.85	6.95	A		180
B0	7.30	7.40	7.50	N	60	
K0	1.80	1.90	2.00	W1		12.4
F	5.40	5.50	5.60	W2		18.4
E	1.65	1.75	1.85	W3	11.9	15.4
W	11.7	12.0	12.3			
P2	1.90	2.00	2.10	Base quantity pcs		1000
P0	3.90	4.00	4.10	Bulk quantity pcs		1000
P1	7.90	8.00	8.10			
T	0.25	0.30	0.35			
DΦ	1.50	1.55	1.60			
D1Φ	1.50	1.60	1.70			

Figure 23. SOT-223 package orientation in carrier tape


0050115_20

Revision history

Table 10. Document revision history

Date	Version	Changes
20-Aug-2018	1	Initial release.
14-Jul-2026	2	The part number STQ1HNK60R-AP has been moved to a separate datasheet and the document has been updated accordingly. Added Section 4.2: SOT-223 packing information . Minor text changes.

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