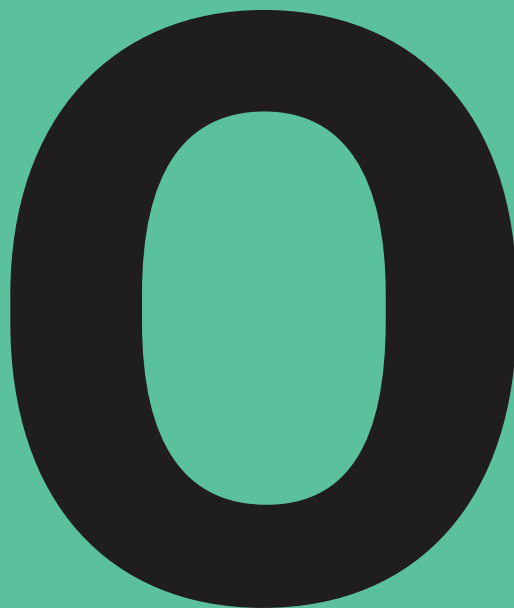
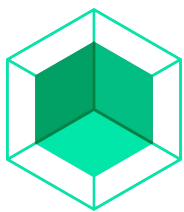




Samsung  
**ARTIK**<sup>™</sup> Modules



**030 Data Sheet**



# ARTIK 030 Mesh Networking Module

## Data Sheet

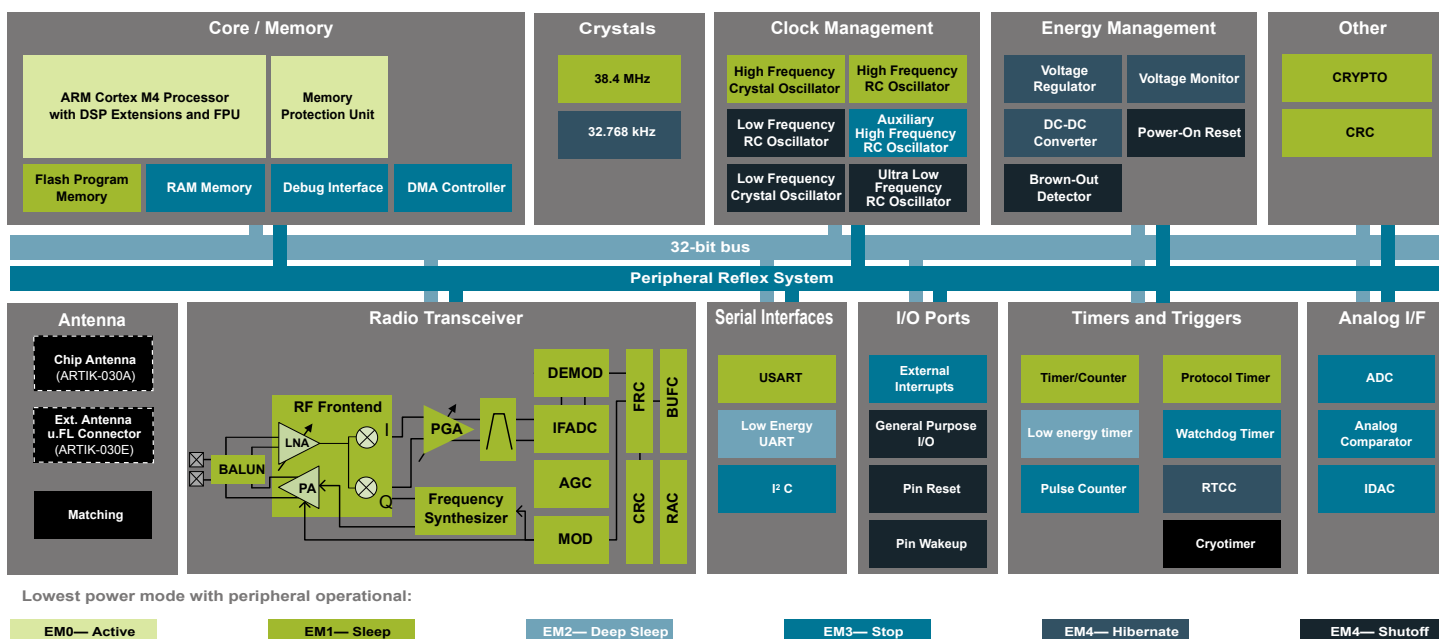
The ARTIK 030 is a fully-integrated, pre-certified module, enabling rapid development of wireless mesh networking solutions. The ARTIK 030 combines an energy-efficient, multi-protocol wireless SoC with a proven RF/antenna design and industry-leading wireless software stacks. This integration accelerates time-to-market and saves months of engineering effort and development costs.

ARTIK 030 can be used in a wide variety of applications:

- Connected Home
- Building Automation
- Lighting
- Security and Monitoring
- Smart Grid / Metering
- Industrial Automation
- Others

### KEY FEATURES

- Industry-leading mesh networking (ZigBee/Thread) software and development tools
- Antenna: internal chip and U.FL variants
- TX power: up to +10 dBm
- RX sensitivity: down to -99 dBm
- 32-bit ARM® Cortex®-M4 at 40 MHz
- Flash memory: 256 kB
- RAM: 32 kB
- Autonomous Hardware Crypto Accelerator and Random Number Generator
- Integrated DC-DC Converter



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## 1. Feature List

### MCU Features

- ARM Cortex®-M4 + Floating Point Unit
- Up to 40 MHz Clock Speed
- Low Active Mode Current: 63  $\mu$ A/MHz
- 256 kB flash, 32 kB SRAM
- Advanced hardware cryptographic engine with support for AES-128/-256, ECC, SHA-1, SHA-256, and a Random Number Generator
- 8 Channel DMA Controller

### Digital Peripherals

- 2 x USART (UART, SPI, IrDA, I<sup>2</sup>S)
- Low Energy UART (LEUART™)
- I<sup>2</sup>C peripheral interface (address recognition down to EM3)
- Timers: RTCC, Low Energy Timer, Pulse Counter
- 12-channel Peripheral Reflex System (PRS)
- Up to 25 GPIO with interrupts

### Analog Peripherals

- ADC (12-bit, 1 Msps, 326  $\mu$ A)
- Current-mode Digital to Analog Converter (IDAC)
- 2 x Analog Comparator (ACMP)

### Energy Efficient Low Power Modes

- Energy Mode 2 (Deep Sleep) Current: 2.5  $\mu$ A  
(Full RAM retention and RTCC running from LXFO)
- Ultra-fast wake up: 3  $\mu$ S down to EM3
- Wide Supply Voltage range of 1.85 to 3.8 V

### Environmental & Regulatory

- Operating Temperature: -40 to +85°C
- FCC, IC, CE, Aus/NZ, Korea certifications (pending)

### Dimensions

- W x L x H: 12.9 x 15.0 x 2.2 mm

### Radio Features

- 2.4 GHz with integrated balun
- Support for wireless mesh networking (ZigBee/Thread)
- Integrated PA (up to +10 dBm TX power)
- Packet Trace Interface (PTI) for non-intrusive packet trace with Simplicity Studio development tools
- Antenna interface: integrated high-performance chip antenna or u.FL variant for external antenna

### ZigBee and Thread Features

- IEEE 802.15.4
- Data Rate / Modulation: 250 kbps DSSS-OQPSK
- +10 dBm Programmable TX Power
- -99 dBm RX Sensitivity
- 9.8 mA RX current
- 8.2 mA TX current (at +0 dBm)
- Support for SoC and Network Co-Processor (NCP) architectures with SPI/UART host support
- Serial and Over-The-Air (OTA) bootloaders

## 2. Ordering Information

| Ordering Code  | Description                                                                 | Max TX Power | Antenna                 | Packaging          | Production Status                                                     |
|----------------|-----------------------------------------------------------------------------|--------------|-------------------------|--------------------|-----------------------------------------------------------------------|
| ARTIK-030-AV1  | ARTIK 030 Mesh Networking Module                                            | +10 dBm      | Integrated chip antenna | Cut Reel (100 pcs) | Initial Production / Engineering Samples (non-certified)              |
| ARTIK-030-AV1R | ARTIK 030 Mesh Networking Module                                            | +10 dBm      | Integrated chip antenna | Reel (1000 pcs)    | Initial Production / Engineering Samples (non-certified)              |
| ARTIK-030-EV1  | ARTIK 030 Mesh Networking Module                                            | +10 dBm      | External (U.FL)         | Cut Reel (100 pcs) | Initial Production / Engineering Samples (non-certified) <sup>1</sup> |
| ARTIK-030-EV1R | ARTIK 030 Mesh Networking Module                                            | +10 dBm      | External (U.FL)         | Reel (1000 pcs)    | Initial Production / Engineering Samples (non-certified) <sup>1</sup> |
| ARTIK-030-AV2  | ARTIK 030 Mesh Networking Module                                            | +10 dBm      | Integrated chip antenna | Cut Reel (100 pcs) | Full Production (certified) <sup>1</sup>                              |
| ARTIK-030-AV2R | ARTIK 030 Mesh Networking Module                                            | +10 dBm      | Integrated chip antenna | Reel (1000 pcs)    | Full Production (certified) <sup>1</sup>                              |
| ARTIK-030-EV2  | ARTIK 030 Mesh Networking Module                                            | +10 dBm      | External (U.FL)         | Cut Reel (100 pcs) | Full Production (certified) <sup>1</sup>                              |
| ARTIK-030-EV2R | ARTIK 030 Mesh Networking Module                                            | +10 dBm      | External (U.FL)         | Reel (1000 pcs)    | Full Production (certified) <sup>1</sup>                              |
| SIP-KITSZG001  | ARTIK 030 Mesh Networking Kit (includes 3 x ARTIK-030-A development boards) | —            | —                       | Development Kit    | —                                                                     |

**Note:**

1. Contact [sales@artik.io](mailto:sales@artik.io) for availability and certification timelines.
2. ARTIK 030 development kit and IAR license required for ZigBee® and Thread software development.

## 3. System Overview

### 3.1 Introduction

This section provides a brief overview of the ARTIK 030 module architecture including both MCU and RF sub-systems. A detailed functional description of the Silicon Lab's EFR32MG1 SoC used inside the module is available in the *EFR32MG1 Mighty Gecko Datasheet* and *EFR32xG1 Wireless Gecko Reference Manual* and a block diagram of the EFR32MG1 SoC is shown in the figure below.

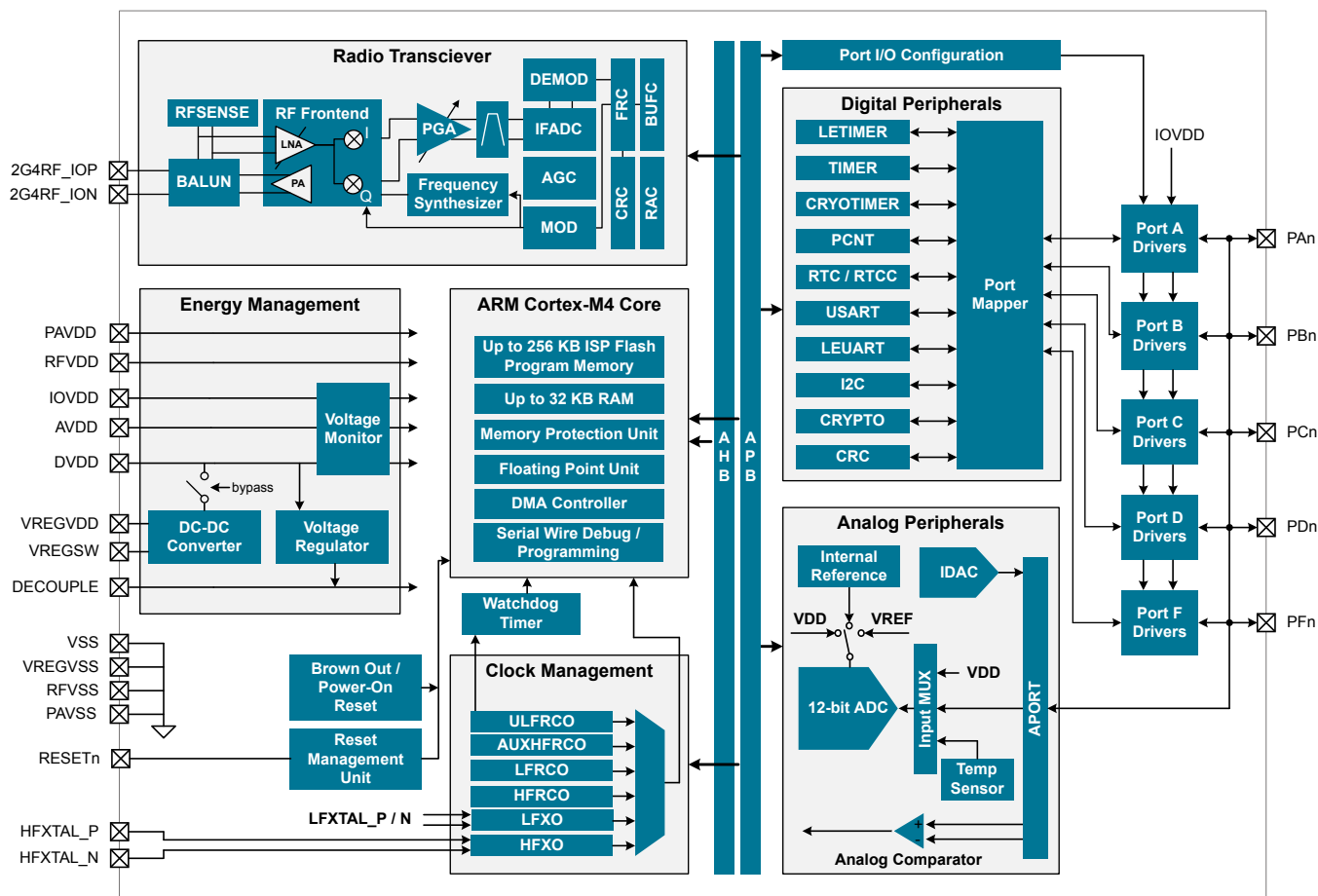


Figure 3.1. Detailed EFR32MG1 Block Diagram

### 3.2 Radio

The ARTIK 030 features a flexible, multi-protocol radio that supports wireless mesh networking (ZigBee® / Thread) protocols.

#### 3.2.1 Antenna Interface

The ARTIK 030 module family includes options for either a high-performance, integrated chip-antenna (ARTIK-030-A) or external antenna (ARTIK-030-E) via a U.FL connector. The table below includes performance specifications for the integrated chip antenna.

Table 3.1. Antenna Efficiency and Peak Gain (ARTIK-030-A)

| Parameter  | With optimal layout | Note                                                                                                                                                                                                                                                      |
|------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Efficiency | -2 dB to -3 dB      | Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Chapter 6. <a href="#">Layout Guidelines</a> for PCB layout and antenna integration guidelines for optimal performance. |
| Peak gain  | 1.0 dBi             |                                                                                                                                                                                                                                                           |

### 3.2.2 Packet and State Trace

The ARTIK 030 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

### 3.2.3 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

### 3.3 Power

The ARTIK 030 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption.

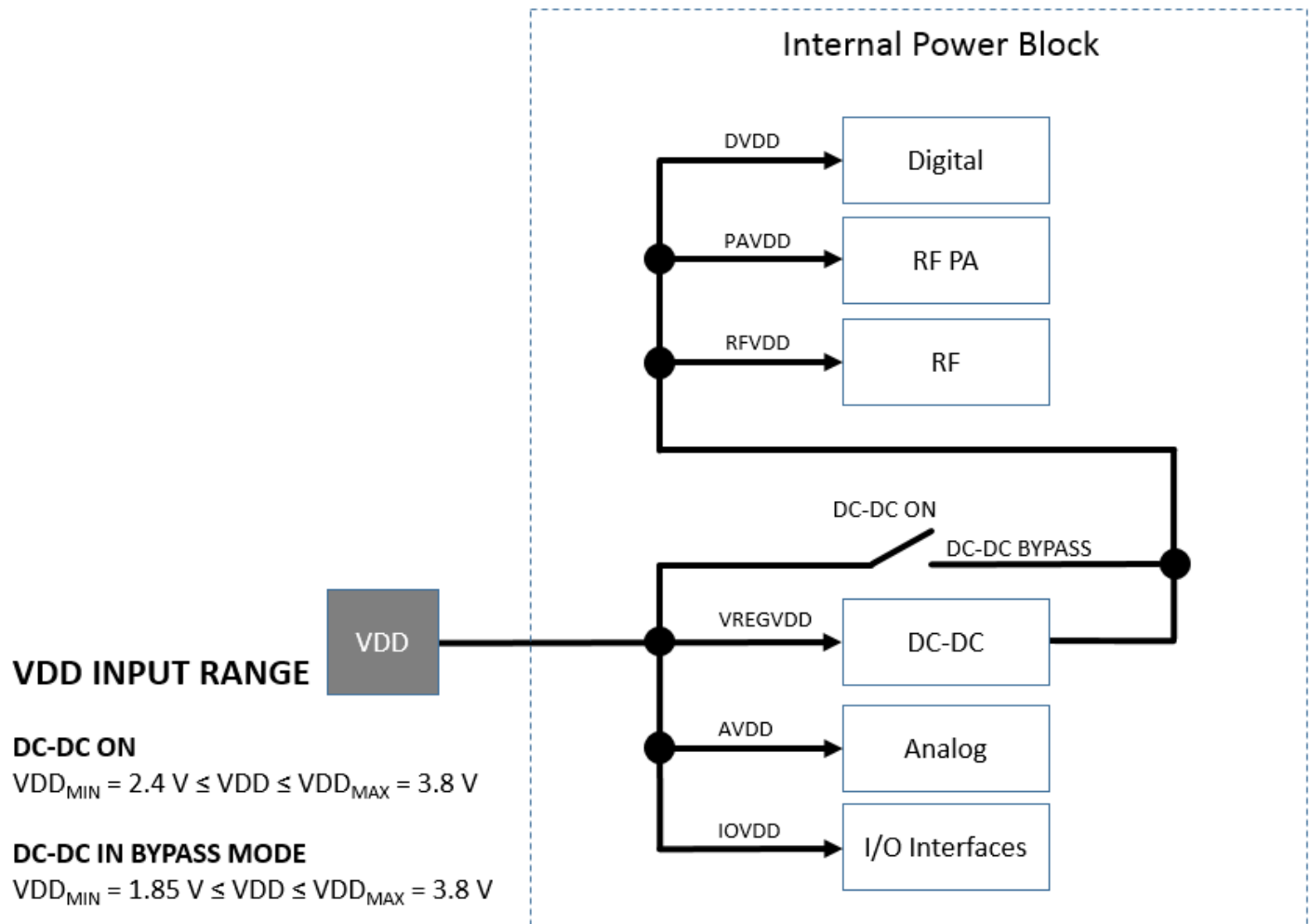


Figure 3.2. ARTIK 030 Power Block

#### 3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

#### 3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

### 3.4 General Purpose Input/Output (GPIO)

ARTIK 030 has up to 25 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

### 3.5 Clocking

#### 3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the ARTIK 030. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

#### 3.5.2 Internal Oscillators

The ARTIK 030 fully integrates two crystal oscillators and four RC oscillators, listed below.

- A 38.4MHz high frequency crystal oscillator (HFXO) provides a precise timing reference for the MCU and radio.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

### 3.6 Counters/Timers and PWM

#### 3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER\_0 only.

#### 3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

#### 3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

### 3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

### 3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTn\_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

### 3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

## 3.7 Communications and Other Digital Peripherals

### 3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I<sup>2</sup>S

### 3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART<sup>TM</sup> provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

### 3.7.3 Inter-Integrated Circuit Interface (I<sup>2</sup>C)

The I<sup>2</sup>C module provides an interface between the MCU and a serial I<sup>2</sup>C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I<sup>2</sup>C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

### 3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

## 3.8 Security Features

### 3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

### 3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. It supports AES encryption and decryption with 128- or 256-bit keys and ECC over both GF(P) and GF(2<sup>m</sup>), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

## 3.9 Analog

### 3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules ADC, ACMP, and IDAC on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

### 3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

### 3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 MSamples/s. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

### 3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The current is programmable between 0.05  $\mu$ A and 64  $\mu$ A with several ranges with various step sizes.

## 3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the ARTIK 030. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

## 3.11 Core and Memory

### 3.11.1 Processor Core

The ARM Cortex-M4F processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4F RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- 256 KB flash program memory
- 32 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

### 3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

### 3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The ARTIK 030 memory map is shown in the figures below.

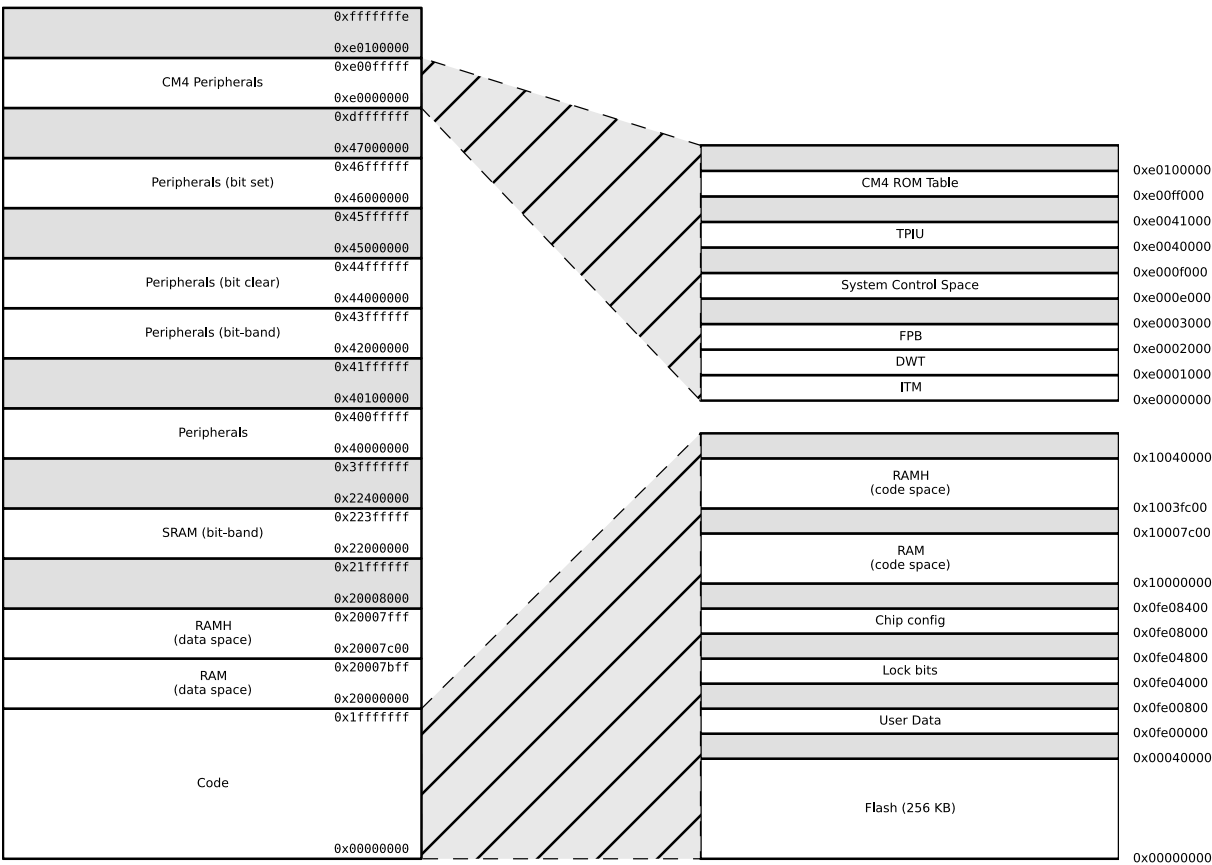


Figure 3.3. ARTIK 030 Memory Map — Core Peripherals and Code Space

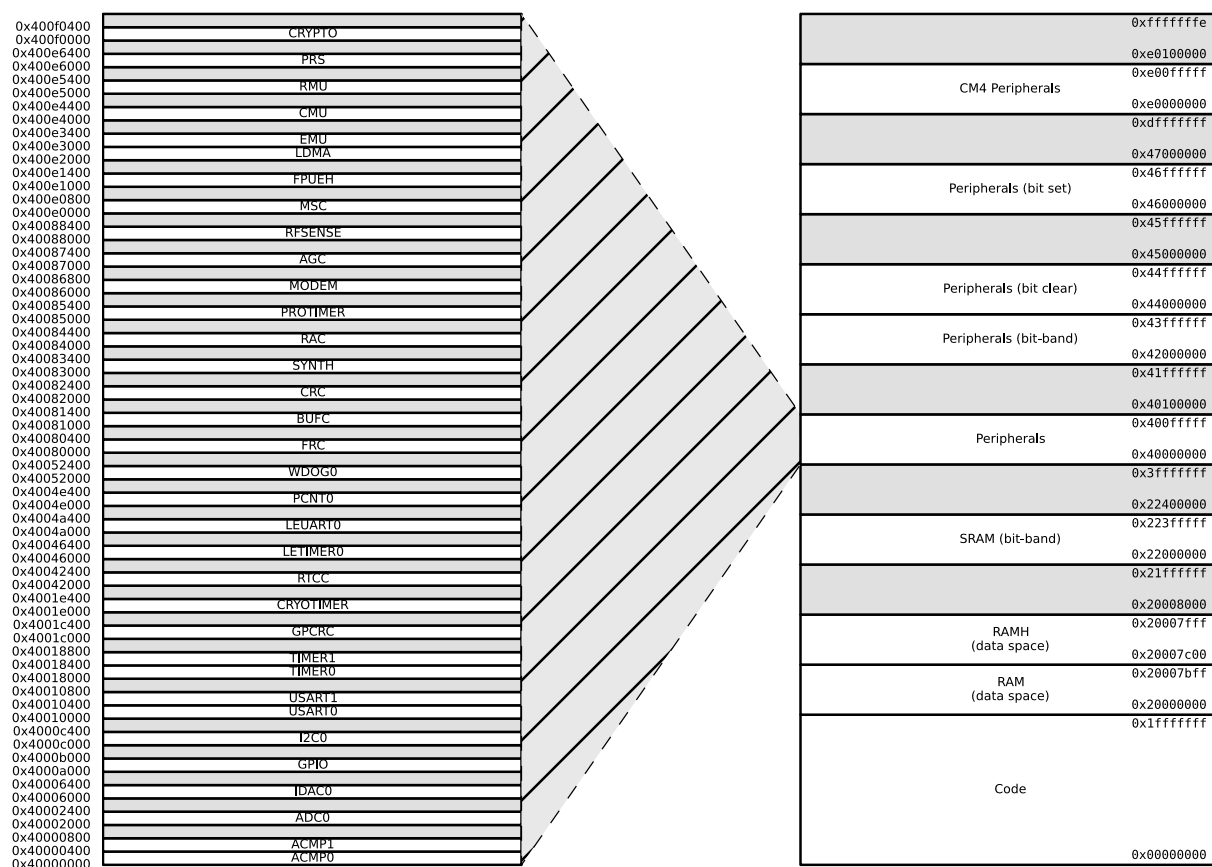


Figure 3.4. ARTIK 030 Memory Map — Peripherals

### 3.13 Configuration Summary

The features of the ARTIK 030 are a subset of the feature set described in the *EFR32xG1 Wireless Gecko Reference Manual*. The Pin Definitions section describes device specific implementation of the features.

## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on  $T_{AMB}=25^{\circ}\text{C}$  and  $V_{DD}=3.3\text{ V}$ , by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a  $50\ \Omega$  antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation and operating temperature.

Refer to [Table 4.2 General Operating Conditions on page 13](#) for more details about operational supply and temperature limits.

#### 4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 4.1. Absolute Maximum Ratings**

| Parameter                                        | Symbol           | Test Condition | Min  | Typ | Max                        | Unit               |
|--------------------------------------------------|------------------|----------------|------|-----|----------------------------|--------------------|
| Storage temperature range                        | $T_{STG}$        |                | -40  | —   | +85                        | $^{\circ}\text{C}$ |
| External main supply voltage                     | $V_{DDMAX}$      |                | 0    | —   | 3.8                        | V                  |
| External main supply voltage ramp rate           | $V_{DDRAMP MAX}$ |                | —    | —   | 1                          | V / $\mu\text{s}$  |
| Voltage on any 5V tolerant GPIO pin <sup>1</sup> | $V_{DIGPIN}$     |                | -0.3 | —   | Min of 5.25 and $V_{DD}+2$ | V                  |
| Voltage on non-5V tolerant GPIO pins             |                  |                | -0.3 | —   | $V_{DD}+0.3$               | V                  |
| Input RF level                                   | $P_{RFMAX2G4}$   |                | —    | —   | 10                         | dBm                |
| Current per I/O pin (sink)                       | $I_{IOMAX}$      |                | —    | —   | 50                         | mA                 |
| Current per I/O pin (source)                     |                  |                | —    | —   | 50                         | mA                 |
| Current for all I/O pins (sink)                  | $I_{IOALLMAX}$   |                | —    | —   | 200                        | mA                 |
| Current for all I/O pins (source)                |                  |                | —    | —   | 200                        | mA                 |

**Note:**

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage =  $V_{DD}$ .

## 4.1.2 General Operating Conditions

Table 4.2. General Operating Conditions

| Parameter                       | Symbol            | Test Condition                          | Min  | Typ  | Max | Unit |
|---------------------------------|-------------------|-----------------------------------------|------|------|-----|------|
| Operating temperature range     | T <sub>OP</sub>   | Ambient Temperature                     | -40  | 25   | 85  | °C   |
| VDD supply voltage <sup>1</sup> | V <sub>VDD</sub>  | DCDC in regulation                      | 2.4  | 3.3  | 3.8 | V    |
|                                 |                   | DCDC in bypass, 50mA load               | 1.85 | 3.3  | 3.8 | V    |
| VDD Current                     | I <sub>VDD</sub>  | DCDC in bypass                          | —    | —    | 200 | mA   |
| HFCLK frequency                 | f <sub>CORE</sub> | 0 wait-states (MODE = WS0) <sup>2</sup> | —    | —    | 26  | MHz  |
|                                 |                   | 1 wait-states (MODE = WS1) <sup>2</sup> | —    | 38.4 | 40  | MHz  |

**Note:**

1. The minimum voltage required in bypass mode is calculated using R<sub>BYP</sub> from the DCDC specification table. Requirements for other loads can be calculated as  $V_{VDD\_min} + I_{LOAD} * R_{BYP\_max}$
2. in MSC\_READCTRL register

### 4.1.3 DC-DC Converter

Test conditions:  $V_{\text{DCDC\_I}}=3.3$  V,  $V_{\text{DCDC\_O}}=1.8$  V,  $I_{\text{DCDC\_LOAD}}=50$  mA, Heavy Drive configuration,  $F_{\text{DCDC\_LN}}=7$  MHz, unless otherwise indicated.

**Table 4.3. DC-DC Converter**

| Parameter                                      | Symbol                 | Test Condition                                                                                                                             | Min  | Typ | Max                   | Unit          |
|------------------------------------------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------|-----|-----------------------|---------------|
| Input voltage range                            | $V_{\text{DCDC\_I}}$   | Bypass mode, $I_{\text{DCDC\_LOAD}} = 50$ mA                                                                                               | 1.85 | —   | $V_{\text{VDD\_MAX}}$ | V             |
|                                                |                        | Low noise (LN) mode, 1.8 V output, $I_{\text{DCDC\_LOAD}} = 100$ mA, or Low power (LP) mode, 1.8 V output, $I_{\text{DCDC\_LOAD}} = 10$ mA | 2.4  | —   | $V_{\text{VDD\_MAX}}$ | V             |
|                                                |                        | Low noise (LN) mode, 1.8 V output, $I_{\text{DCDC\_LOAD}} = 200$ mA                                                                        | 2.6  | —   | $V_{\text{VDD\_MAX}}$ | V             |
| Output voltage programmable range <sup>1</sup> | $V_{\text{DCDC\_O}}$   |                                                                                                                                            | 1.8  | —   | $V_{\text{VREGVDD}}$  | V             |
| Max load current                               | $I_{\text{LOAD\_MAX}}$ | Low noise (LN) mode, Heavy Drive <sup>3</sup>                                                                                              | —    | —   | 200                   | mA            |
|                                                |                        | Low noise (LN) mode, Medium Drive <sup>3</sup>                                                                                             | —    | —   | 100                   | mA            |
|                                                |                        | Low noise (LN) mode, Light Drive <sup>3</sup>                                                                                              | —    | —   | 50                    | mA            |
|                                                |                        | Low power (LP) mode, $\text{LPCMPBIAS}^2 = 0$                                                                                              | —    | —   | 75                    | $\mu\text{A}$ |
|                                                |                        | Low power (LP) mode, $\text{LPCMPBIAS}^2 = 3$                                                                                              | —    | —   | 10                    | mA            |

**Note:**

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage,  $V_{\text{VDD}}$
2. In EMU\_DCDCMISCCTRL register
3. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

## 4.1.4 Current Consumption

### 4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VDD = 3.3 V, DC-DC enabled. T<sub>OP</sub> = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T<sub>OP</sub> = 25 °C.

**Table 4.4. Current Consumption 3.3V with DC-DC**

| Parameter                                                                                                       | Symbol              | Test Condition                                                   | Min | Typ  | Max | Unit   |
|-----------------------------------------------------------------------------------------------------------------|---------------------|------------------------------------------------------------------|-----|------|-----|--------|
| Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>1</sup> . | I <sub>ACTIVE</sub> | 38.4 MHz crystal, CPU running while loop from flash <sup>2</sup> | —   | 88   | —   | μA/MHz |
|                                                                                                                 |                     | 38 MHz HFRCO, CPU running Prime from flash                       | —   | 63   | —   | μA/MHz |
|                                                                                                                 |                     | 38 MHz HFRCO, CPU running while loop from flash                  | —   | 71   | —   | μA/MHz |
|                                                                                                                 |                     | 38 MHz HFRCO, CPU running CoreMark from flash                    | —   | 78   | —   | μA/MHz |
|                                                                                                                 |                     | 26 MHz HFRCO, CPU running while loop from flash                  | —   | 76   | —   | μA/MHz |
| Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise CCM mode <sup>3</sup> . | I <sub>ACTIVE</sub> | 38.4 MHz crystal, CPU running while loop from flash <sup>2</sup> | —   | 98   | —   | μA/MHz |
|                                                                                                                 |                     | 38 MHz HFRCO, CPU running Prime from flash                       | —   | 75   | —   | μA/MHz |
|                                                                                                                 |                     | 38 MHz HFRCO, CPU running while loop from flash                  | —   | 81   | —   | μA/MHz |
|                                                                                                                 |                     | 38 MHz HFRCO, CPU running CoreMark from flash                    | —   | 88   | —   | μA/MHz |
|                                                                                                                 |                     | 26 MHz HFRCO, CPU running while loop from flash                  | —   | 94   | —   | μA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>1</sup> .  | I <sub>EM1</sub>    | 38.4 MHz crystal <sup>2</sup>                                    | —   | 49   | —   | μA/MHz |
|                                                                                                                 |                     | 38 MHz HFRCO                                                     | —   | 32   | —   | μA/MHz |
|                                                                                                                 |                     | 26 MHz HFRCO                                                     | —   | 38   | —   | μA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise CCM mode <sup>3</sup> .  | I <sub>EM1</sub>    | 38.4 MHz crystal <sup>2</sup>                                    | —   | 61   | —   | μA/MHz |
|                                                                                                                 |                     | 38 MHz HFRCO                                                     | —   | 45   | —   | μA/MHz |
|                                                                                                                 |                     | 26 MHz HFRCO                                                     | —   | 58   | —   | μA/MHz |
| Current consumption in EM2 Deep Sleep mode. DCDC in Low Power mode <sup>4</sup> .                               | I <sub>EM2</sub>    | Full RAM retention and RTCC running from LFXO                    | —   | 2.5  | —   | μA     |
|                                                                                                                 |                     | 4 kB RAM retention and RTCC running from LFRCO                   | —   | 2.2  | —   | μA     |
| Current consumption in EM3 Stop mode                                                                            | I <sub>EM3</sub>    | Full RAM retention and CRYO-TIMER running from ULFRCO            | —   | 2.1  | —   | μA     |
| Current consumption in EM4H Hibernate mode                                                                      | I <sub>EM4</sub>    | 128 byte RAM retention, RTCC running from LFXO                   | —   | 0.86 | —   | μA     |
|                                                                                                                 |                     | 128 byte RAM retention, CRYO-TIMER running from ULFRCO           | —   | 0.58 | —   | μA     |
|                                                                                                                 |                     | 128 byte RAM retention, no RTCC                                  | —   | 0.58 | —   | μA     |

| Parameter                                | Symbol     | Test Condition            | Min | Typ  | Max | Unit    |
|------------------------------------------|------------|---------------------------|-----|------|-----|---------|
| Current consumption in EM4S Shutoff mode | $I_{EM4S}$ | no RAM retention, no RTCC | —   | 0.04 | —   | $\mu A$ |

**Note:**

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DCDC voltage.
2. CMU\_HFXOCTRL\_LOWPOWER=0
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DCDC voltage.
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DCDC voltage.

**4.1.4.2 Current Consumption Using Radio**

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T<sub>OP</sub> = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T<sub>OP</sub> = 25 °C.

**Table 4.5. Current Consumption 3.3 V with DC-DC**

| Parameter                                                                                                        | Symbol   | Test Condition                                                    | Min | Typ  | Max | Unit |
|------------------------------------------------------------------------------------------------------------------|----------|-------------------------------------------------------------------|-----|------|-----|------|
| Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled) | $I_{RX}$ | 1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4          | —   | 8.7  | —   | mA   |
|                                                                                                                  |          | 802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3 | —   | 9.8  | —   | mA   |
| Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)                         | $I_{TX}$ | F = 2.4 GHz, CW, 0 dBm, Radio clock prescaled by 3                | —   | 8.2  | —   | mA   |
|                                                                                                                  |          | F = 2.4 GHz, CW, 10.5 dBm                                         | —   | 32.7 | —   | mA   |

**4.1.5 Wake up times****Table 4.6. Wake up times**

| Parameter                                 | Symbol         | Test Condition            | Min | Typ  | Max | Unit       |
|-------------------------------------------|----------------|---------------------------|-----|------|-----|------------|
| Wake up from EM2 Deep Sleep               | $t_{EM2\_WU}$  | Code execution from flash | —   | 10.7 | —   | $\mu s$    |
|                                           |                | Code execution from RAM   | —   | 3    | —   | $\mu s$    |
| Wakeup time from EM1 Sleep                | $t_{EM1\_WU}$  | Executing from flash      | —   | 3    | —   | AHB Clocks |
|                                           |                | Executing from RAM        | —   | 3    | —   | AHB Clocks |
| Wake up from EM3 Stop                     | $t_{EM3\_WU}$  | Executing from flash      | —   | 10.7 | —   | $\mu s$    |
|                                           |                | Executing from RAM        | —   | 3    | —   | $\mu s$    |
| Wake up from EM4H Hiber-nate <sup>1</sup> | $t_{EM4H\_WU}$ | Executing from flash      | —   | 60   | —   | $\mu s$    |
| Wake up from EM4S Shut-off <sup>1</sup>   | $t_{EM4S\_WU}$ |                           | —   | 290  | —   | $\mu s$    |

**Note:**

1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.

#### 4.1.6 Brown Out Detector

For the table below, see [Figure 3.2 ARTIK 030 Power Block on page 5](#) to see the internal connection and relation between DVDD and AVDD. The module itself has only one external power supply input (VDD).

**Table 4.7. Brown Out Detector**

| Parameter           | Symbol               | Test Condition                     | Min  | Typ | Max  | Unit    |
|---------------------|----------------------|------------------------------------|------|-----|------|---------|
| AVDD BOD threshold  | $V_{AVDDBOD}$        | AVDD rising                        | —    | —   | 1.85 | V       |
|                     |                      | AVDD falling                       | 1.62 | —   | —    | V       |
| AVDD BOD hysteresis | $V_{AVDDBOD\_HYST}$  |                                    | —    | 21  | —    | mV      |
| AVDD response time  | $t_{AVDDBOD\_DELAY}$ | Supply drops at 0.1V/ $\mu$ s rate | —    | 2.4 | —    | $\mu$ s |
| EM4 BOD threshold   | $V_{EM4BOD}$         | AVDD rising                        | —    | —   | 1.7  | V       |
|                     |                      | AVDD falling                       | 1.45 | —   | —    | V       |
| EM4 BOD hysteresis  | $V_{EM4BOD\_HYST}$   |                                    | —    | 46  | —    | mV      |
| EM4 response time   | $t_{EM4BOD\_DELAY}$  | Supply drops at 0.1V/ $\mu$ s rate | —    | 300 | —    | $\mu$ s |

#### 4.1.7 Frequency Synthesizer Characteristics

**Table 4.8. Frequency Synthesizer Characteristics**

| Parameter                      | Symbol                 | Test Condition          | Min  | Typ | Max    | Unit |
|--------------------------------|------------------------|-------------------------|------|-----|--------|------|
| RF Synthesizer Frequency range | $F_{RANGE\_2400}$      | 2.4 GHz frequency range | 2400 | —   | 2483.5 | MHz  |
| LO tuning frequency resolution | $F_{RES\_2400}$        | 2400 - 2483.5 MHz       | —    | —   | 73     | Hz   |
| Maximum frequency deviation    | $\Delta F_{MAX\_2400}$ |                         | —    | —   | 1677   | kHz  |

## 4.1.8 2.4 GHz RF Transceiver Characteristics

### 4.1.8.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are:  $T_{OP} = 25^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ . RF center frequency 2.45 GHz. Measurements are conducted from the antenna feed point.

**Table 4.9. RF Transmitter General Characteristics for 2.4 GHz Band**

| Parameter                                              | Symbol          | Test Condition                                   | Min  | Typ | Max    | Unit |
|--------------------------------------------------------|-----------------|--------------------------------------------------|------|-----|--------|------|
| Maximum TX power                                       | $POUT_{MAX}$    |                                                  | —    | 10  | —      | dBm  |
| Minimum active TX Power                                | $POUT_{MIN}$    | CW                                               |      | -30 | —      | dBm  |
| Output power step size                                 | $POUT_{STEP}$   | -5 dBm < Output power < 0 dBm                    | —    | 1   | —      | dB   |
|                                                        |                 | 0 dBm < output power < $POUT_{MAX}$              | —    | 0.5 | —      | dB   |
| Output power variation vs supply at $POUT_{MAX}$       | $POUT_{VAR\_V}$ | 1.85 V < $V_{VDD}$ < 3.3 V using DC-DC converter | —    | 2.2 | —      | dB   |
| Output power variation vs temperature at $POUT_{MAX}$  | $POUT_{VAR\_T}$ | From -40 to +85 °C, DCDC enabled                 | —    | 1.5 | —      | dB   |
| Output power variation vs RF frequency at $POUT_{MAX}$ | $POUT_{VAR\_F}$ | Over RF tuning frequency range                   | —    | 0.4 | —      | dB   |
| RF tuning frequency range                              | $F_{RANGE}$     |                                                  | 2400 | —   | 2483.5 | MHz  |

### 4.1.8.2 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are:  $T_{OP} = 25^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ . RF center frequency 2.440 GHz. Measurements are conducted from the antenna feed point.

**Table 4.10. RF Receiver General Characteristics for 2.4 GHz Band**

| Parameter                                                                 | Symbol           | Test Condition                            | Min  | Typ   | Max    | Unit |
|---------------------------------------------------------------------------|------------------|-------------------------------------------|------|-------|--------|------|
| RF tuning frequency range                                                 | $F_{RANGE}$      |                                           | 2400 | —     | 2483.5 | MHz  |
| Receive mode maximum spurious emission                                    | $SPUR_{RX}$      | 30 MHz to 1 GHz                           | —    | -57   | —      | dBm  |
|                                                                           |                  | 1 GHz to 12 GHz                           | —    | -47   | —      | dBm  |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX\_FCC}$ | 216 MHz to 960 MHz, Conducted Measurement | —    | -55.2 | —      | dBm  |
|                                                                           |                  | Above 960 MHz, Conducted Measurement      | —    | -47.2 | —      | dBm  |

**4.1.8.3 RF Receiver Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band**

Unless otherwise indicated, typical conditions are: T=25 °C, VDD = 3.3 V. RF center frequency 2.445 GHz. Measurements are conducted from the antenna feed point.

**Table 4.11. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band**

| Parameter                                                                                                                                                             | Symbol                  | Test Condition                                                                          | Min | Typ   | Max | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-----------------------------------------------------------------------------------------|-----|-------|-----|------|
| Max usable receiver input level, 1% PER                                                                                                                               | SAT                     | Signal is reference signal <sup>1</sup> . Packet length is 20 octets.                   | —   | 10    | —   | dBm  |
| Sensitivity, 1% PER                                                                                                                                                   | SENS                    | Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.          | —   | -99   | —   | dBm  |
|                                                                                                                                                                       |                         | Signal is reference signal. Packet length is 20 octets. DC-DC converter in bypass mode. | —   | -99   | —   | dBm  |
| Co-channel interferer rejection, 1% PER                                                                                                                               | CCR                     | Desired signal 10 dB above sensitivity limit                                            | —   | -2.6  | —   | dB   |
| High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup>                                       | ACR <sub>+1</sub>       | Interferer is reference signal at +1 channel-spacing.                                   | —   | 33.75 | —   | dB   |
|                                                                                                                                                                       |                         | Interferer is filtered reference signal <sup>3</sup> at +1 channel-spacing.             | —   | 52.2  | —   | dB   |
|                                                                                                                                                                       |                         | Interferer is CW at +1 channel-spacing. <sup>4</sup>                                    | —   | 58.6  | —   | dB   |
| Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup>                                        | ACR <sub>-1</sub>       | Interferer is reference signal at -1 channel-spacing.                                   | —   | 35    | —   | dB   |
|                                                                                                                                                                       |                         | Interferer is filtered reference signal <sup>3</sup> at -1 channel-spacing.             | —   | 54.7  | —   | dB   |
|                                                                                                                                                                       |                         | Interferer is CW at -1 channel-spacing.                                                 | —   | 60.1  | —   | dB   |
| Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup>                                                | ACR <sub>2</sub>        | Interferer is reference signal at ±2 channel-spacing                                    | —   | 45.9  | —   | dB   |
|                                                                                                                                                                       |                         | Interferer is filtered reference signal <sup>3</sup> at ±2 channel-spacing              | —   | 56.8  | —   | dB   |
|                                                                                                                                                                       |                         | Interferer is CW at ±2 channel-spacing                                                  | —   | 65.5  | —   | dB   |
| Image rejection , 1% PER, Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup>                                                           | IR                      | Interferer is CW in image band <sup>4</sup>                                             | —   | 49.3  | —   | dB   |
| Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level <sup>2</sup> . Interferer is reference signal. | BLOCK                   | Interferer frequency < Desired frequency - 3 channel-spacing                            | —   | 57.2  | —   | dB   |
|                                                                                                                                                                       |                         | Interferer frequency > Desired frequency + 3 channel-spacing                            | —   | 57.9  | —   | dB   |
| Blocking rejection of 802.11g signal centered at +12MHz or -13MHz                                                                                                     | BLOCK <sub>80211G</sub> | Desired is reference signal at 6dB above reference sensitivity level <sup>2</sup>       | —   | 51.6  | —   | dB   |

| Parameter                                                                 | Symbol       | Test Condition                    | Min | Typ     | Max | Unit |
|---------------------------------------------------------------------------|--------------|-----------------------------------|-----|---------|-----|------|
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ |                                   | 5   | —       | —   | dBm  |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ |                                   | —   | —       | -98 | dBm  |
| RSSI resolution                                                           | $RSSI_{RES}$ | over $RSSI_{MIN}$ to $RSSI_{MAX}$ | —   | 0.25    | —   | dB   |
| RSSI accuracy in the linear region as defined by 802.15.4-2003            | $RSSI_{LIN}$ |                                   | —   | $\pm 1$ | —   | dB   |

**Note:**

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s
2. Reference sensitivity level is -85 dBm
3. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stop-band rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
4. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency  $\pm 5$  MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

## 4.1.9 Oscillators

### 4.1.9.1 LFXO

**Table 4.12. LFXO**

| Parameter                   | Symbol            | Test Condition | Min  | Typ    | Max  | Unit |
|-----------------------------|-------------------|----------------|------|--------|------|------|
| Crystal Frequency           | $f_{\text{LFXO}}$ |                | —    | 32.768 | —    | kHz  |
| Crystal Frequency Tolerance |                   |                | -100 |        | +100 | ppm  |

### 4.1.9.2 HFXO

**Table 4.13. HFXO**

| Parameter                   | Symbol            | Test Condition | Min | Typ  | Max | Unit |
|-----------------------------|-------------------|----------------|-----|------|-----|------|
| Crystal Frequency           | $f_{\text{HFXO}}$ |                | —   | 38.4 | —   | MHz  |
| Crystal Frequency Tolerance |                   |                | -40 |      | +40 | ppm  |

### 4.1.9.3 LFRCO

**Table 4.14. LFRCO**

| Parameter                        | Symbol             | Test Condition              | Min    | Typ    | Max    | Unit          |
|----------------------------------|--------------------|-----------------------------|--------|--------|--------|---------------|
| Oscillation frequency            | $f_{\text{LFRCO}}$ | ENVREF = 1 in CMU_LFRCOCTRL | 30.474 | 32.768 | 34.243 | kHz           |
|                                  |                    | ENVREF = 0 in CMU_LFRCOCTRL | 30.474 | 32.768 | 33.915 | kHz           |
| Startup time                     | $t_{\text{LFRCO}}$ |                             | —      | 500    | —      | $\mu\text{s}$ |
| Current consumption <sup>1</sup> | $I_{\text{LFRCO}}$ | ENVREF = 1 in CMU_LFRCOCTRL | —      | 342    | —      | nA            |
|                                  |                    | ENVREF = 0 in CMU_LFRCOCTRL | —      | 494    | —      | nA            |

**Note:**

1. Block is supplied by VDD if ANASW = 0, or DCDC if ANASW=1 in EMU\_PWRCTRL register

## 4.1.9.4 HFRCO and AUXHFRCO

Table 4.15. HFRCO and AUXHFRCO

| Parameter                           | Symbol              | Test Condition                                            | Min  | Typ | Max | Unit          |
|-------------------------------------|---------------------|-----------------------------------------------------------|------|-----|-----|---------------|
| Frequency Accuracy                  | $f_{\text{HFRCO}}$  | Any frequency band, across supply voltage and temperature | -2.5 | —   | 2.5 | %             |
| Start-up time                       | $t_{\text{HFRCO}}$  | $f_{\text{HFRCO}} \geq 19 \text{ MHz}$                    | —    | 300 | —   | ns            |
|                                     |                     | $4 < f_{\text{HFRCO}} < 19 \text{ MHz}$                   | —    | 1   | —   | $\mu\text{s}$ |
|                                     |                     | $f_{\text{HFRCO}} \leq 4 \text{ MHz}$                     | —    | 2.5 | —   | $\mu\text{s}$ |
| Current consumption on all supplies | $I_{\text{HFRCO}}$  | $f_{\text{HFRCO}} = 38 \text{ MHz}$                       | —    | 204 | 228 | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 32 \text{ MHz}$                       | —    | 171 | 190 | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 26 \text{ MHz}$                       | —    | 147 | 164 | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 19 \text{ MHz}$                       | —    | 126 | 138 | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 16 \text{ MHz}$                       | —    | 110 | 120 | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 13 \text{ MHz}$                       | —    | 100 | 110 | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 7 \text{ MHz}$                        | —    | 81  | 91  | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 4 \text{ MHz}$                        | —    | 33  | 35  | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 2 \text{ MHz}$                        | —    | 31  | 35  | $\mu\text{A}$ |
|                                     |                     | $f_{\text{HFRCO}} = 1 \text{ MHz}$                        | —    | 30  | 35  | $\mu\text{A}$ |
| Step size                           | $SS_{\text{HFRCO}}$ | Coarse (% of period)                                      | —    | 0.8 | —   | %             |
|                                     |                     | Fine (% of period)                                        | —    | 0.1 | —   | %             |
| Period Jitter                       | $PJ_{\text{HFRCO}}$ |                                                           | —    | 0.2 | —   | % RMS         |

## 4.1.9.5 ULFRCO

Table 4.16. ULFRCO

| Parameter             | Symbol              | Test Condition | Min  | Typ | Max  | Unit |
|-----------------------|---------------------|----------------|------|-----|------|------|
| Oscillation frequency | $f_{\text{ULFRCO}}$ |                | 0.95 | 1   | 1.07 | kHz  |

## 4.1.10 Flash Memory Characteristics

Table 4.17. Flash Memory Characteristics<sup>1</sup>

| Parameter                                                                                                                                                                                                                                                                               | Symbol               | Test Condition | Min   | Typ | Max | Unit   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------|-------|-----|-----|--------|
| Flash erase cycles before failure                                                                                                                                                                                                                                                       | EC <sub>FLASH</sub>  |                | 10000 | —   | —   | cycles |
| Flash data retention                                                                                                                                                                                                                                                                    | RET <sub>FLASH</sub> |                | 10    | —   | —   | years  |
| Word (32-bit) programming time                                                                                                                                                                                                                                                          | t <sub>W_PROG</sub>  |                | 20    | 26  | 40  | μs     |
| Page erase time                                                                                                                                                                                                                                                                         | t <sub>PERASE</sub>  |                | 20    | 27  | 40  | ms     |
| Mass erase time                                                                                                                                                                                                                                                                         | t <sub>MERASE</sub>  |                | 20    | 27  | 40  | ms     |
| Device erase time <sup>2</sup>                                                                                                                                                                                                                                                          | t <sub>DERASE</sub>  |                | —     | 60  | 74  | ms     |
| Page erase current <sup>3</sup>                                                                                                                                                                                                                                                         | I <sub>ERASE</sub>   |                | —     | —   | 3   | mA     |
| Mass or Device erase current <sup>3</sup>                                                                                                                                                                                                                                               |                      |                | —     | —   | 5   | mA     |
| Write current <sup>3</sup>                                                                                                                                                                                                                                                              | I <sub>WRITE</sub>   |                | —     | —   | 3   | mA     |
| <b>Note:</b><br>1. Flash data retention information is published in the Quarterly Quality and Reliability Report.<br>2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW)<br>3. Measured at 25°C |                      |                |       |     |     |        |

## 4.1.11 GPIO

Table 4.18. GPIO

| Parameter                                                      | Symbol          | Test Condition                                                                        | Min             | Typ | Max             | Unit       |
|----------------------------------------------------------------|-----------------|---------------------------------------------------------------------------------------|-----------------|-----|-----------------|------------|
| Input low voltage                                              | $V_{IOIL}$      |                                                                                       | —               | —   | $VDD \cdot 0.3$ | V          |
| Input high voltage                                             | $V_{IOIH}$      |                                                                                       | $VDD \cdot 0.7$ | —   | —               | V          |
| Output high voltage relative to VDD                            | $V_{IOOH}$      | Sourcing 3 mA, $VDD \geq 3$ V,<br>DRIVESTRENGTH <sup>1</sup> = WEAK                   | $VDD \cdot 0.8$ | —   | —               | V          |
|                                                                |                 | Sourcing 1.2 mA, $VDD \geq 1.62$ V<br>DRIVESTRENGTH <sup>1</sup> = WEAK               | $VDD \cdot 0.6$ | —   | —               | V          |
|                                                                |                 | Sourcing 20 mA, $VDD \geq 3$ V,<br>DRIVESTRENGTH <sup>1</sup> = STRONG                | $VDD \cdot 0.8$ | —   | —               | V          |
|                                                                |                 | Sourcing 8 mA, $VDD \geq 1.62$ V<br>DRIVESTRENGTH <sup>1</sup> = STRONG               | $VDD \cdot 0.6$ | —   | —               | V          |
| Output low voltage relative to VDD                             | $V_{IOOL}$      | Sinking 3 mA, $VDD \geq 3$ V,<br>DRIVESTRENGTH <sup>1</sup> = WEAK                    | —               | —   | $VDD \cdot 0.2$ | V          |
|                                                                |                 | Sinking 1.2 mA, $VDD \geq 1.62$ V<br>DRIVESTRENGTH <sup>1</sup> = WEAK                | —               | —   | $VDD \cdot 0.4$ | V          |
|                                                                |                 | Sinking 20 mA, $VDD \geq 3$ V,<br>DRIVESTRENGTH <sup>1</sup> = STRONG                 | —               | —   | $VDD \cdot 0.2$ | V          |
|                                                                |                 | Sinking 8 mA, $VDD \geq 1.62$ V<br>DRIVESTRENGTH <sup>1</sup> = STRONG                | —               | —   | $VDD \cdot 0.4$ | V          |
| Input leakage current                                          | $I_{IOLEAK}$    | All GPIO except LFXO pins, $GPIO \leq VDD$                                            | —               | 0.1 | 30              | nA         |
|                                                                |                 | LFXO Pins, $GPIO \leq VDD$                                                            | —               | 0.1 | 50              | nA         |
| Input leakage current on 5VTOL pads above VDD                  | $I_{5VTOLLEAK}$ | $VDD < GPIO \leq VDD + 2$ V                                                           | —               | 3.3 | 15              | $\mu$ A    |
| I/O pin pull-up resistor                                       | $R_{PU}$        |                                                                                       | 30              | 43  | 65              | k $\Omega$ |
| I/O pin pull-down resistor                                     | $R_{PD}$        |                                                                                       | 30              | 43  | 65              | k $\Omega$ |
| Pulse width of pulses removed by the glitch suppression filter | $t_{IOGLITCH}$  |                                                                                       | 20              | 25  | 35              | ns         |
| Output fall time, From 70% to 30% of $V_{IO}$                  | $t_{IOOF}$      | $C_L = 50$ pF,<br>DRIVESTRENGTH <sup>1</sup> = STRONG,<br>SLEWRATE <sup>1</sup> = 0x6 | —               | 1.8 | —               | ns         |
|                                                                |                 | $C_L = 50$ pF,<br>DRIVESTRENGTH <sup>1</sup> = WEAK,<br>SLEWRATE <sup>1</sup> = 0x6   | —               | 4.5 | —               | ns         |

| Parameter                                            | Symbol            | Test Condition                                                                                         | Min | Typ | Max | Unit |
|------------------------------------------------------|-------------------|--------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| Output rise time, From 30% to 70% of V <sub>IO</sub> | t <sub>IOOR</sub> | C <sub>L</sub> = 50 pF,<br><br>DRIVESTRENGTH <sup>1</sup> = STRONG,<br><br>SLEWRATE = 0x6 <sup>1</sup> | —   | 2.2 | —   | ns   |
|                                                      |                   | C <sub>L</sub> = 50 pF,<br><br>DRIVESTRENGTH <sup>1</sup> = WEAK,<br><br>SLEWRATE <sup>1</sup> = 0x6   | —   | 7.4 | —   | ns   |
| <b>Note:</b><br>1. In GPIO_Pn_CTRL register          |                   |                                                                                                        |     |     |     |      |

#### 4.1.12 VMON

**Table 4.19. VMON**

| Parameter                        | Symbol            | Test Condition                           | Min  | Typ  | Max  | Unit          |
|----------------------------------|-------------------|------------------------------------------|------|------|------|---------------|
| VMON Supply Current              | $I_{VMON}$        | In EM0 or EM1, 1 supply monitored        | —    | 5.8  | 8.26 | $\mu\text{A}$ |
|                                  |                   | In EM0 or EM1, 4 supplies monitored      | —    | 11.8 | 16.8 | $\mu\text{A}$ |
|                                  |                   | In EM2, EM3 or EM4, 1 supply monitored   | —    | 62   | —    | nA            |
|                                  |                   | In EM2, EM3 or EM4, 4 supplies monitored | —    | 99   | —    | nA            |
| VMON Loading of Monitored Supply | $I_{SENSE}$       | In EM0 or EM1                            | —    | 2    | —    | $\mu\text{A}$ |
|                                  |                   | In EM2, EM3 or EM4                       | —    | 2    | —    | nA            |
| Threshold range                  | $V_{VMON\_RANGE}$ |                                          | 1.62 | —    | 3.4  | V             |
| Threshold step size              | $N_{VMON\_STESP}$ | Coarse                                   | —    | 200  | —    | mV            |
|                                  |                   | Fine                                     | —    | 20   | —    | mV            |
| Response time                    | $t_{VMON\_RES}$   | Supply drops at 1V/ $\mu\text{s}$ rate   | —    | 460  | —    | ns            |
| Hysteresis                       | $V_{VMON\_HYST}$  |                                          | —    | 26   | —    | mV            |

## 4.1.13 ADC

Table 4.20. ADC

| Parameter                                                                                                                                    | Symbol                         | Test Condition                                                      | Min               | Typ | Max                | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|---------------------------------------------------------------------|-------------------|-----|--------------------|------|
| Resolution                                                                                                                                   | V <sub>RESOLUTION</sub>        |                                                                     | 6                 | —   | 12                 | Bits |
| Input voltage range                                                                                                                          | V <sub>ADCIN</sub>             | Single ended                                                        | 0                 | —   | 2*V <sub>REF</sub> | V    |
|                                                                                                                                              |                                | Differential                                                        | -V <sub>REF</sub> | —   | V <sub>REF</sub>   | V    |
| Input range of external reference voltage, single ended and differential                                                                     | V <sub>ADCREFIN_P</sub>        |                                                                     | 1                 | —   | V <sub>AVDD</sub>  | V    |
| Power supply rejection <sup>1</sup>                                                                                                          | PSRR <sub>ADC</sub>            | At DC                                                               | —                 | 80  | —                  | dB   |
| Analog input common mode rejection ratio                                                                                                     | CMRR <sub>ADC</sub>            | At DC                                                               | —                 | 80  | —                  | dB   |
| Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE <sup>2</sup> = KEEPADC-WARM                     | I <sub>ADC_CONTINUOUS_LP</sub> | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sub>3</sub>    | —                 | 301 | 350                | μA   |
|                                                                                                                                              |                                | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 <sub>3</sub>   | —                 | 149 | —                  | μA   |
|                                                                                                                                              |                                | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 <sub>3</sub> | —                 | 91  | —                  | μA   |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE <sup>2</sup> = NORMAL                          | I <sub>ADC_NORMAL_LP</sub>     | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sub>3</sub>   | —                 | 51  | —                  | μA   |
|                                                                                                                                              |                                | 5 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sub>3</sub>    | —                 | 9   | —                  | μA   |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE <sup>2</sup> = KEEPINSTANDBY or KEEPINSLOWACC | I <sub>ADC_STANDBY_LP</sub>    | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sub>3</sub>  | —                 | 117 | —                  | μA   |
|                                                                                                                                              |                                | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 <sub>3</sub>   | —                 | 79  | —                  | μA   |
| Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE <sup>2</sup> = KEEPADC-WARM                     | I <sub>ADC_CONTINUOUS_HP</sub> | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 <sub>3</sub>    | —                 | 345 | —                  | μA   |
|                                                                                                                                              |                                | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 <sub>3</sub>   | —                 | 191 | —                  | μA   |
|                                                                                                                                              |                                | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 <sub>3</sub> | —                 | 132 | —                  | μA   |

| Parameter                                                                                                                                    | Symbol                      | Test Condition                                                         | Min | Typ   | Max | Unit   |
|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|------------------------------------------------------------------------|-----|-------|-----|--------|
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE <sup>2</sup> = NORMAL                          | I <sub>ADC_NORMAL_HP</sub>  | 35 ksp/s / 16 MHz ADCCLK,<br>BIASPROG = 0, GPBIASACC = 0 <sub>3</sub>  | —   | 102   | —   | μA     |
|                                                                                                                                              |                             | 5 ksp/s / 16 MHz ADCCLK<br>BIASPROG = 0, GPBIASACC = 0 <sub>3</sub>    | —   | 17    | —   | μA     |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE <sup>2</sup> = KEEPINSTANDBY or KEEPINSLOWACC | I <sub>ADC_STANDBY_HP</sub> | 125 ksp/s / 16 MHz ADCCLK,<br>BIASPROG = 0, GPBIASACC = 0 <sub>3</sub> | —   | 162   | —   | μA     |
|                                                                                                                                              |                             | 35 ksp/s / 16 MHz ADCCLK,<br>BIASPROG = 0, GPBIASACC = 0 <sub>3</sub>  | —   | 123   | —   | μA     |
| Current from HFPERCLK                                                                                                                        | I <sub>ADC_CLK</sub>        | HFPERCLK = 16 MHz                                                      | —   | 140   | —   | μA     |
| ADC Clock Frequency                                                                                                                          | f <sub>ADCCLK</sub>         |                                                                        | —   | —     | 16  | MHz    |
| Throughput rate                                                                                                                              | f <sub>ADCRATE</sub>        |                                                                        | —   | —     | 1   | Msp/s  |
| Conversion time <sup>4</sup>                                                                                                                 | t <sub>ADCCONV</sub>        | 6 bit                                                                  | —   | 7     | —   | cycles |
|                                                                                                                                              |                             | 8 bit                                                                  | —   | 9     | —   | cycles |
|                                                                                                                                              |                             | 12 bit                                                                 | —   | 13    | —   | cycles |
| Startup time of reference generator and ADC core                                                                                             | t <sub>ADCSTART</sub>       | WARMUPMODE <sup>2</sup> = NORMAL                                       | —   | —     | 5   | μs     |
|                                                                                                                                              |                             | WARMUPMODE <sup>2</sup> = KEEPINSTANDBY                                | —   | —     | 2   | μs     |
|                                                                                                                                              |                             | WARMUPMODE <sup>2</sup> = KEEPINSLOWACC                                | —   | —     | 1   | μs     |
| SNDR at 1Msp/s and f <sub>in</sub> = 10kHz                                                                                                   | SNDR <sub>ADC</sub>         | Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)       | 58  | 67    | —   | dB     |
|                                                                                                                                              |                             | vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential      | —   | 68    | —   | dB     |
| Spurious-Free Dynamic Range (SFDR)                                                                                                           | SFDR <sub>ADC</sub>         | 1 MSamples/s, 10 kHz full-scale sine wave                              | —   | 75    | —   | dB     |
| Input referred ADC noise, rms                                                                                                                | V <sub>REF_NOISE</sub>      | Including quantization noise and distortion                            | —   | 380   | —   | μV     |
| Offset Error                                                                                                                                 | V <sub>ADCOFFSETERR</sub>   |                                                                        | -3  | 0.25  | 3   | LSB    |
| Gain error in ADC                                                                                                                            | V <sub>ADC_GAIN</sub>       | Using internal reference                                               | —   | -0.2  | 5   | %      |
|                                                                                                                                              |                             | Using external reference                                               | —   | -1    | —   | %      |
| Differential non-linearity (DNL)                                                                                                             | DNL <sub>ADC</sub>          | 12 bit resolution                                                      | -1  | —     | 2   | LSB    |
| Integral non-linearity (INL), End point method                                                                                               | INL <sub>ADC</sub>          | 12 bit resolution                                                      | -6  | —     | 6   | LSB    |
| Temperature Sensor Slope                                                                                                                     | V <sub>TS_SLOPE</sub>       |                                                                        | —   | -1.84 | —   | mV/°C  |

| Parameter                                                                                                                                                                                                                | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------|-----|-----|-----|------|
| <b>Note:</b> <div>1. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL</div> <div>2. In ADCn_CNTL register</div> <div>3. In ADCn_BIASPROG register</div> <div>4. Derived from ADCCLK</div> |        |                |     |     |     |      |

## 4.1.14 IDAC

Table 4.21. IDAC

| Parameter                                   | Symbol                   | Test Condition                                                                | Min  | Typ  | Max | Unit |
|---------------------------------------------|--------------------------|-------------------------------------------------------------------------------|------|------|-----|------|
| Number of Ranges                            | N <sub>IDAC_RANGES</sub> |                                                                               | —    | 4    | —   | -    |
| Output Current                              | I <sub>IDAC_OUT</sub>    | RANGSEL <sup>1</sup> = RANGE0                                                 | 0.05 | —    | 1.6 | μA   |
|                                             |                          | RANGSEL <sup>1</sup> = RANGE1                                                 | 1.6  | —    | 4.7 | μA   |
|                                             |                          | RANGSEL <sup>1</sup> = RANGE2                                                 | 0.5  | —    | 16  | μA   |
|                                             |                          | RANGSEL <sup>1</sup> = RANGE3                                                 | 2    | —    | 64  | μA   |
| Linear steps within each range              | N <sub>IDAC_STEPS</sub>  |                                                                               | —    | 32   | —   |      |
| Step size                                   | SS <sub>IDAC</sub>       | RANGSEL <sup>1</sup> = RANGE0                                                 | —    | 50   | —   | nA   |
|                                             |                          | RANGSEL <sup>1</sup> = RANGE1                                                 | —    | 100  | —   | nA   |
|                                             |                          | RANGSEL <sup>1</sup> = RANGE2                                                 | —    | 500  | —   | nA   |
|                                             |                          | RANGSEL <sup>1</sup> = RANGE3                                                 | —    | 2    | —   | μA   |
| Total Accuracy, STEPSEL <sup>1</sup> = 0x10 | ACC <sub>IDAC</sub>      | EM0 or EM1, AVDD=3.3 V, T = 25 °C                                             | -2   | —    | 2   | %    |
|                                             |                          | EM0 or EM1                                                                    | -18  | —    | 22  | %    |
|                                             |                          | EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE0, AVDD=3.3 V, T = 25 °C | —    | -2   | —   | %    |
|                                             |                          | EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE1, AVDD=3.3 V, T = 25 °C | —    | -1.7 | —   | %    |
|                                             |                          | EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE2, AVDD=3.3 V, T = 25 °C | —    | -0.8 | —   | %    |
|                                             |                          | EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE3, AVDD=3.3 V, T = 25 °C | —    | -0.5 | —   | %    |
|                                             |                          | EM2 or EM3, Sink mode, RANGSEL <sup>1</sup> = RANGE0, AVDD=3.3 V, T = 25 °C   | —    | -0.7 | —   | %    |
|                                             |                          | EM2 or EM3, Sink mode, RANGSEL <sup>1</sup> = RANGE1, AVDD=3.3 V, T = 25 °C   | —    | -0.6 | —   | %    |
|                                             |                          | EM2 or EM3, Sink mode, RANGSEL <sup>1</sup> = RANGE2, AVDD=3.3 V, T = 25 °C   | —    | -0.5 | —   | %    |
|                                             |                          | EM2 or EM3, Sink mode, RANGSEL <sup>1</sup> = RANGE3, AVDD=3.3 V, T = 25 °C   | —    | -0.5 | —   | %    |
| Start up time                               | t <sub>IDAC_SU</sub>     | Output within 1% of steady state value                                        | —    | 5    | —   | μs   |

| Parameter                                                                                          | Symbol             | Test Condition                                                               | Min | Typ  | Max | Unit    |
|----------------------------------------------------------------------------------------------------|--------------------|------------------------------------------------------------------------------|-----|------|-----|---------|
| Settling time, (output settled within 1% of steady state value)                                    | $t_{IDAC\_SETTLE}$ | Range setting is changed                                                     | —   | 5    | —   | $\mu s$ |
|                                                                                                    |                    | Step value is changed                                                        | —   | 1    | —   | $\mu s$ |
| Current consumption in EM0 or EM1 <sup>2</sup>                                                     | $I_{IDAC}$         | Source mode, excluding output current                                        | —   | 8.9  | 13  | $\mu A$ |
|                                                                                                    |                    | Sink mode, excluding output current                                          | —   | 12   | 16  | $\mu A$ |
| Current consumption in EM2 or EM3 <sup>2</sup>                                                     | $I_{IDAC}$         | Source mode, excluding output current, duty cycle mode, $T = 25^{\circ}C$    | —   | 1.04 | —   | $\mu A$ |
|                                                                                                    |                    | Sink mode, excluding output current, duty cycle mode, $T = 25^{\circ}C$      | —   | 1.08 | —   | $\mu A$ |
|                                                                                                    |                    | Source mode, excluding output current, duty cycle mode, $T \geq 85^{\circ}C$ | —   | 8.9  | —   | $\mu A$ |
|                                                                                                    |                    | Sink mode, excluding output current, duty cycle mode, $T \geq 85^{\circ}C$   | —   | 12   | —   | $\mu A$ |
| Output voltage compliance in source mode, source current change relative to current sourced at 0 V | $I_{COMP\_SRC}$    | RANGESEL1=0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$ | —   | 0.04 | —   | %       |
|                                                                                                    |                    | RANGESEL1=1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$ | —   | 0.02 | —   | %       |
|                                                                                                    |                    | RANGESEL1=2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 150 \text{ mV})$ | —   | 0.02 | —   | %       |
|                                                                                                    |                    | RANGESEL1=3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 250 \text{ mV})$ | —   | 0.02 | —   | %       |
| Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD      | $I_{COMP\_SINK}$   | RANGESEL1=0, output voltage = 100 mV                                         | —   | 0.18 | —   | %       |
|                                                                                                    |                    | RANGESEL1=1, output voltage = 100 mV                                         | —   | 0.12 | —   | %       |
|                                                                                                    |                    | RANGESEL1=2, output voltage = 150 mV                                         | —   | 0.08 | —   | %       |
|                                                                                                    |                    | RANGESEL1=3, output voltage = 250 mV                                         | —   | 0.02 | —   | %       |

**Note:**

1. In IDAC\_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU\_PWRCTRL register and PWRSEL in the IDAC\_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

## 4.1.15 Analog Comparator (ACMP)

Table 4.22. ACMP

| Parameter                                                                                        | Symbol         | Test Condition                                                       | Min   | Typ | Max            | Unit |
|--------------------------------------------------------------------------------------------------|----------------|----------------------------------------------------------------------|-------|-----|----------------|------|
| Input voltage range                                                                              | $V_{ACMPIN}$   | CMPVDD =<br>ACMPn_CTRL_PWRSEL <sup>1</sup>                           | 0     | —   | CMPVDD         | V    |
| Supply Voltage                                                                                   | $V_{ACMPVDD}$  | BIASPROG <sup>2</sup> ≤ 0x10 or FULL-<br>BIAS <sup>2</sup> = 0       | 1.85  | —   | $V_{VDD\_MAX}$ | V    |
|                                                                                                  |                | 0x10 < BIASPROG <sup>2</sup> ≤ 0x20 and<br>FULLBIAS <sup>2</sup> = 1 | 2.1   | —   | $V_{VDD\_MAX}$ | V    |
| Active current not including<br>voltage reference                                                | $I_{ACMP}$     | BIASPROG <sup>2</sup> = 1, FULLBIAS <sup>2</sup> = 0                 | —     | 50  | —              | nA   |
|                                                                                                  |                | BIASPROG <sup>2</sup> = 0x10, FULLBIAS <sup>2</sup><br>= 0           | —     | 306 | —              | nA   |
|                                                                                                  |                | BIASPROG <sup>2</sup> = 0x20, FULLBIAS <sup>2</sup><br>= 1           | —     | 74  | 95             | μA   |
| Current consumption of inter-<br>nal voltage reference                                           | $I_{ACMPREF}$  | VLP selected as input using 2.5 V<br>Reference / 4 (0.625 V)         | —     | 50  | —              | nA   |
|                                                                                                  |                | VLP selected as input using VDD                                      | —     | 20  | —              | nA   |
|                                                                                                  |                | VBDIV selected as input using<br>1.25 V reference / 1                | —     | 4.1 | —              | μA   |
|                                                                                                  |                | VADIV selected as input using<br>VDD/1                               | —     | 2.4 | —              | μA   |
| Hysteresis ( $V_{CM} = 1.25$ V,<br>BIASPROG <sup>2</sup> = 0x10, FULL-<br>BIAS <sup>2</sup> = 1) | $V_{ACMPHYST}$ | HYSTSEL <sup>3</sup> = HYST0                                         | -1.75 | 0   | 1.75           | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST1                                         | 10    | 18  | 26             | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST2                                         | 21    | 32  | 46             | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST3                                         | 27    | 44  | 63             | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST4                                         | 32    | 55  | 80             | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST5                                         | 38    | 65  | 100            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST6                                         | 43    | 77  | 121            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST7                                         | 47    | 86  | 148            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST8                                         | -4    | 0   | 4              | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST9                                         | -27   | -18 | -10            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST10                                        | -47   | -32 | -18            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST11                                        | -64   | -43 | -27            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST12                                        | -78   | -54 | -32            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST13                                        | -93   | -64 | -37            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST14                                        | -113  | -74 | -42            | mV   |
|                                                                                                  |                | HYSTSEL <sup>3</sup> = HYST15                                        | -135  | -85 | -47            | mV   |

| Parameter                            | Symbol           | Test Condition                                          | Min | Typ  | Max  | Unit       |
|--------------------------------------|------------------|---------------------------------------------------------|-----|------|------|------------|
| Comparator delay <sup>4</sup>        | $t_{ACMPDELAY}$  | BIASPROG <sup>2</sup> = 1, FULLBIAS <sup>2</sup> = 0    | —   | 30   | —    | $\mu s$    |
|                                      |                  | BIASPROG <sup>2</sup> = 0x10, FULLBIAS <sup>2</sup> = 0 | —   | 3.7  | —    | $\mu s$    |
|                                      |                  | BIASPROG <sup>2</sup> = 0x20, FULLBIAS <sup>2</sup> = 1 | —   | 35   | —    | ns         |
| Offset voltage                       | $V_{ACMPOFFSET}$ | BIASPROG <sup>2</sup> = 0x10, FULLBIAS <sup>2</sup> = 1 | -35 | —    | 35   | mV         |
| Reference Voltage                    | $V_{ACMPREF}$    | Internal 1.25 V reference                               | 1   | 1.25 | 1.47 | V          |
|                                      |                  | Internal 2.5 V reference                                | 2   | 2.5  | 2.8  | V          |
| Capacitive Sense Internal Resistance | $R_{CSRES}$      | CSRESSEL <sup>5</sup> = 0                               | —   | inf  | —    | k $\Omega$ |
|                                      |                  | CSRESSEL <sup>5</sup> = 1                               | —   | 15   | —    | k $\Omega$ |
|                                      |                  | CSRESSEL <sup>5</sup> = 2                               | —   | 27   | —    | k $\Omega$ |
|                                      |                  | CSRESSEL <sup>5</sup> = 3                               | —   | 39   | —    | k $\Omega$ |
|                                      |                  | CSRESSEL <sup>5</sup> = 4                               | —   | 51   | —    | k $\Omega$ |
|                                      |                  | CSRESSEL <sup>5</sup> = 5                               | —   | 102  | —    | k $\Omega$ |
|                                      |                  | CSRESSEL <sup>5</sup> = 6                               | —   | 164  | —    | k $\Omega$ |
|                                      |                  | CSRESSEL <sup>5</sup> = 7                               | —   | 239  | —    | k $\Omega$ |

**Note:**

1. CMPVDD is a supply chosen by the setting in ACMPn\_CTRL\_PWRSEL and may be VDD or DCDC.
2. In ACMPn\_CTRL register.
3. In ACMPn\_HYSTERESIS register.
4.  $\pm 100$  mV differential drive.
5. In ACMPn\_INPUTSEL register.

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given as:

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

$I_{ACMPREF}$  is zero if an external voltage reference is used.

## 4.1.16 I2C

## I2C Standard-mode (Sm)

Table 4.23. I2C Standard-mode (Sm)<sup>1</sup>

| Parameter                                        | Symbol              | Test Condition | Min | Typ | Max  | Unit |
|--------------------------------------------------|---------------------|----------------|-----|-----|------|------|
| SCL clock frequency <sup>2</sup>                 | f <sub>SCL</sub>    |                | 0   | —   | 100  | kHz  |
| SCL clock low time                               | t <sub>LOW</sub>    |                | 4.7 | —   | —    | μs   |
| SCL clock high time                              | t <sub>HIGH</sub>   |                | 4   | —   | —    | μs   |
| SDA set-up time                                  | t <sub>SU,DAT</sub> |                | 250 | —   | —    | ns   |
| SDA hold time <sup>3</sup>                       | t <sub>HD,DAT</sub> |                | 100 | —   | 3450 | ns   |
| Repeated START condition set-up time             | t <sub>SU,STA</sub> |                | 4.7 | —   | —    | μs   |
| (Repeated) START condition hold time             | t <sub>HD,STA</sub> |                | 4   | —   | —    | μs   |
| STOP condition set-up time                       | t <sub>SU,STO</sub> |                | 4   | —   | —    | μs   |
| Bus free time between a STOP and START condition | t <sub>BUF</sub>    |                | 4.7 | —   | —    | μs   |

**Note:**

1. For CLHR set to 0 in the I2Cn\_CTRL register
2. For the minimum HPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time (t<sub>HD,DAT</sub>) needs to be met only when the device does not stretch the low time of SCL (t<sub>LOW</sub>)

**I2C Fast-mode (Fm)****Table 4.24. I2C Fast-mode (Fm)<sup>1</sup>**

| Parameter                                        | Symbol              | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------------------|---------------------|----------------|-----|-----|-----|------|
| SCL clock frequency <sup>2</sup>                 | f <sub>SCL</sub>    |                | 0   | —   | 400 | kHz  |
| SCL clock low time                               | t <sub>LOW</sub>    |                | 1.3 | —   | —   | μs   |
| SCL clock high time                              | t <sub>HIGH</sub>   |                | 0.6 | —   | —   | μs   |
| SDA set-up time                                  | t <sub>SU,DAT</sub> |                | 100 | —   | —   | ns   |
| SDA hold time <sup>3</sup>                       | t <sub>HD,DAT</sub> |                | 100 | —   | 900 | ns   |
| Repeated START condition set-up time             | t <sub>SU,STA</sub> |                | 0.6 | —   | —   | μs   |
| (Repeated) START condition hold time             | t <sub>HD,STA</sub> |                | 0.6 | —   | —   | μs   |
| STOP condition set-up time                       | t <sub>SU,STO</sub> |                | 0.6 | —   | —   | μs   |
| Bus free time between a STOP and START condition | t <sub>BUF</sub>    |                | 1.3 | —   | —   | μs   |

**Note:**

1. For CLHR set to 1 in the I2Cn\_CTRL register
2. For the minimum HPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time (t<sub>HD,DAT</sub>) needs to be met only when the device does not stretch the low time of SCL (t<sub>LOW</sub>)

**I2C Fast-mode Plus (Fm+)****Table 4.25. I2C Fast-mode Plus (Fm+)<sup>1</sup>**

| Parameter                                        | Symbol              | Test Condition | Min  | Typ | Max  | Unit |
|--------------------------------------------------|---------------------|----------------|------|-----|------|------|
| SCL clock frequency <sup>2</sup>                 | f <sub>SCL</sub>    |                | 0    | —   | 1000 | kHz  |
| SCL clock low time                               | t <sub>LOW</sub>    |                | 0.5  | —   | —    | μs   |
| SCL clock high time                              | t <sub>HIGH</sub>   |                | 0.26 | —   | —    | μs   |
| SDA set-up time                                  | t <sub>SU,DAT</sub> |                | 50   | —   | —    | ns   |
| SDA hold time                                    | t <sub>HD,DAT</sub> |                | 100  | —   | —    | ns   |
| Repeated START condition set-up time             | t <sub>SU,STA</sub> |                | 0.26 | —   | —    | μs   |
| (Repeated) START condition hold time             | t <sub>HD,STA</sub> |                | 0.26 | —   | —    | μs   |
| STOP condition set-up time                       | t <sub>SU,STO</sub> |                | 0.26 | —   | —    | μs   |
| Bus free time between a STOP and START condition | t <sub>BUF</sub>    |                | 0.5  | —   | —    | μs   |

**Note:**

1. For CLHR set to 0 or 1 in the I2Cn\_CTRL register
2. For the minimum HPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual

4.1.17 USART SPI

SPI Master Timing

Table 4.26. SPI Master Timing

| Parameter                      | Symbol               | Test Condition | Min                          | Typ | Max | Unit |
|--------------------------------|----------------------|----------------|------------------------------|-----|-----|------|
| SCLK period <sup>1 2</sup>     | t <sub>SCLK</sub>    |                | 2 *<br>t <sub>HFPERCLK</sub> | —   | —   | ns   |
| CS to MOSI <sup>1 2</sup>      | t <sub>CS_MO</sub>   |                | 0                            | —   | 8   | ns   |
| SCLK to MOSI <sup>1 2</sup>    | t <sub>SCLK_MO</sub> |                | 3                            | —   | 20  | ns   |
| MISO setup time <sup>1 2</sup> | t <sub>SU_MI</sub>   | VDD = 3.0 V    | 37                           | —   | —   | ns   |
| MISO hold time <sup>1 2</sup>  | t <sub>H_MI</sub>    |                | 6                            | —   | —   | ns   |

Note:

- 1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
- 2. Measurement done with 8 pF output loading at 10% and 90% of V<sub>DD</sub> (figure shows 50% of V<sub>DD</sub>)

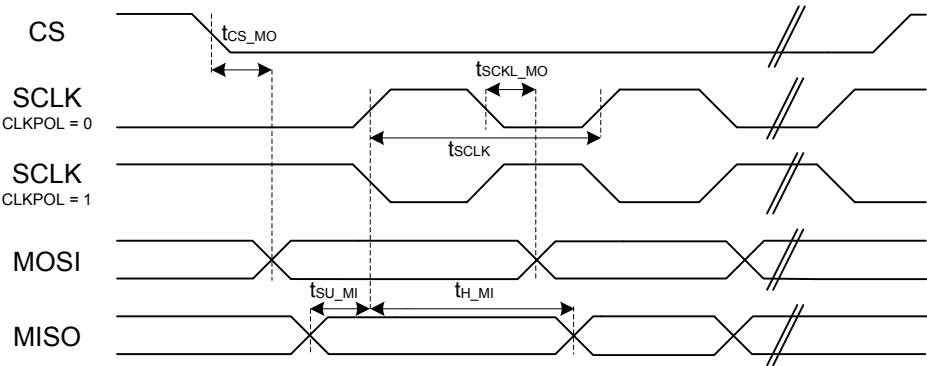


Figure 4.1. SPI Master Timing Diagram

## SPI Slave Timing

Table 4.27. SPI Slave Timing

| Parameter                         | Symbol                   | Test Condition | Min                             | Typ | Max                              | Unit |
|-----------------------------------|--------------------------|----------------|---------------------------------|-----|----------------------------------|------|
| SCKL period <sup>1 2</sup>        | $t_{\text{SCLK\_sl}}$    |                | 2 *<br>$t_{\text{HFERCLK}}$     | —   | —                                | ns   |
| SCLK high period <sup>1 2</sup>   | $t_{\text{SCLK\_hi}}$    |                | 3 *<br>$t_{\text{HFERCLK}}$     | —   | —                                | ns   |
| SCLK low period <sup>1 2</sup>    | $t_{\text{SCLK\_lo}}$    |                | 3 *<br>$t_{\text{HFERCLK}}$     | —   | —                                | ns   |
| CS active to MISO <sup>1 2</sup>  | $t_{\text{CS\_ACT\_MI}}$ |                | 4                               | —   | 50                               | ns   |
| CS disable to MISO <sup>1 2</sup> | $t_{\text{CS\_DIS\_MI}}$ |                | 4                               | —   | 50                               | ns   |
| MOSI setup time <sup>1 2</sup>    | $t_{\text{SU\_MO}}$      |                | 4                               | —   | —                                | ns   |
| MOSI hold time <sup>1 2</sup>     | $t_{\text{H\_MO}}$       |                | 3 + 2 *<br>$t_{\text{HFERCLK}}$ | —   | —                                | ns   |
| SCLK to MISO <sup>1 2</sup>       | $t_{\text{SCLK\_MI}}$    |                | 16 +<br>$t_{\text{HFERCLK}}$    | —   | 66 + 2 *<br>$t_{\text{HFERCLK}}$ | ns   |

**Note:**

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of  $V_{\text{DD}}$  (figure shows 50% of  $V_{\text{DD}}$ )

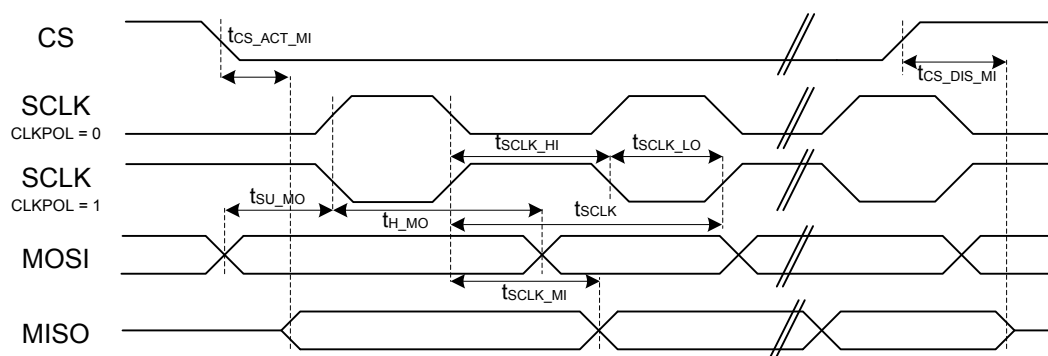


Figure 4.2. SPI Slave Timing Diagram

## 5. Typical Connection Diagrams

### 5.1 Network Co-Processor (NCP) Application with UART Host

The ARTIK 030 can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug, and host interface connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

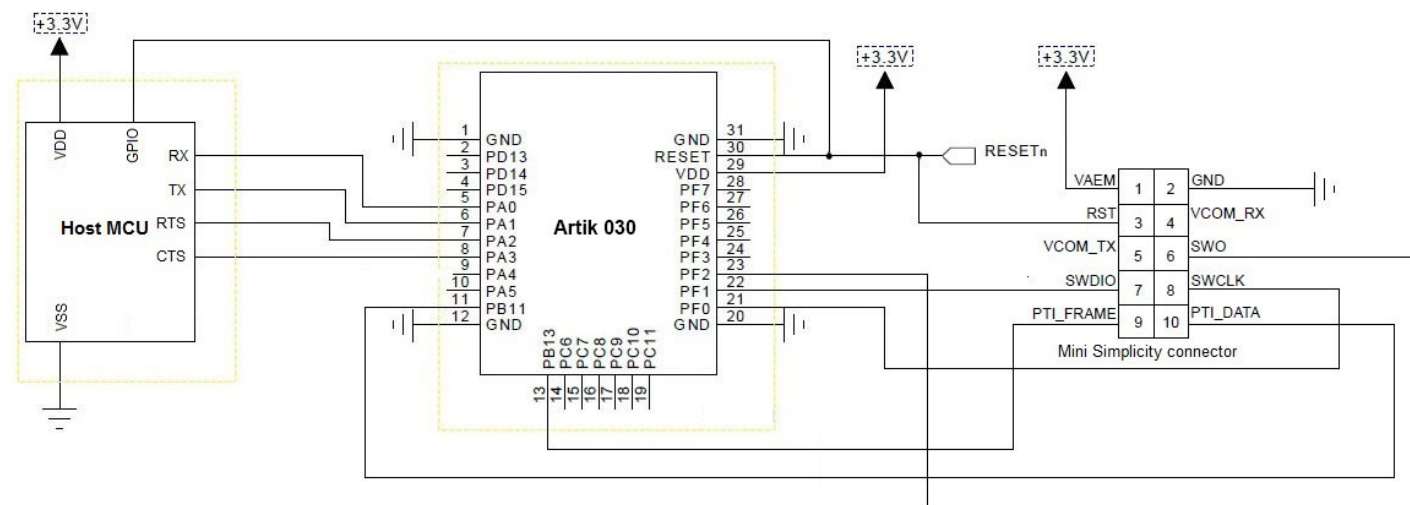


Figure 5.1. Connection Diagram: UART NCP Configuration

### 5.2 Network Co-Processor (NCP) Application with SPI Host

The ARTIK 030 can be controlled over the SPI interface as a peripheral to an external host processor. Typical power supply, programming/debug and host interface connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details.

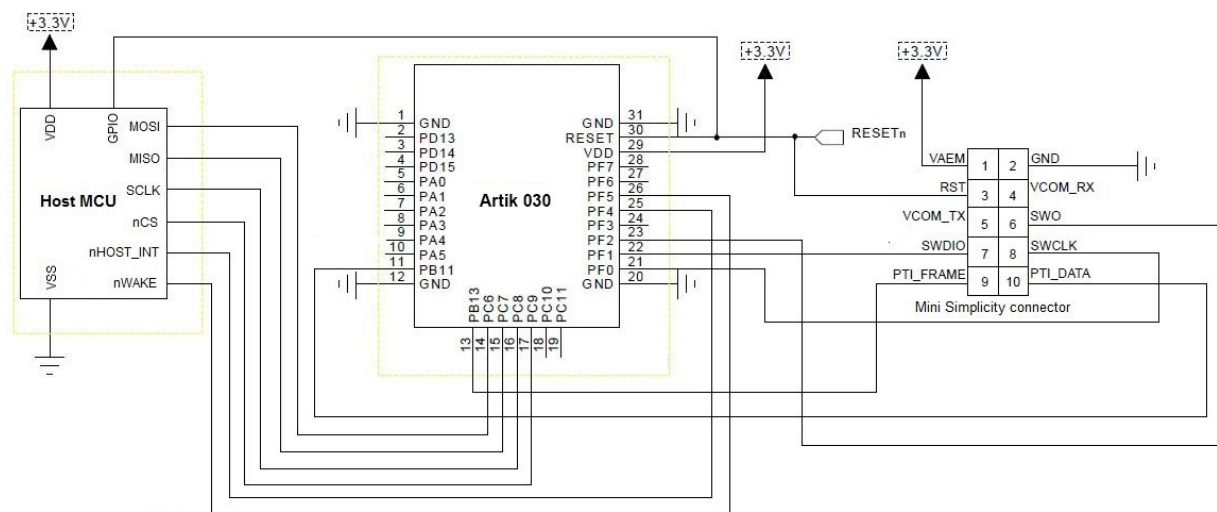


Figure 5.2. Connection Diagram: SPI NCP Configuration

### 5.3 SoC Application

The ARTIK 030 can be used in a standalone SoC configuration with no external host processor. Typical power supply and programming/debug connections are shown in the figure below. Refer to *AN958: Debugging and Programming Interfaces for Custom Designs* for more details. Refer to *AN772: Using the Application Bootloader* for recommendations on supported serial flash ICs (optional).

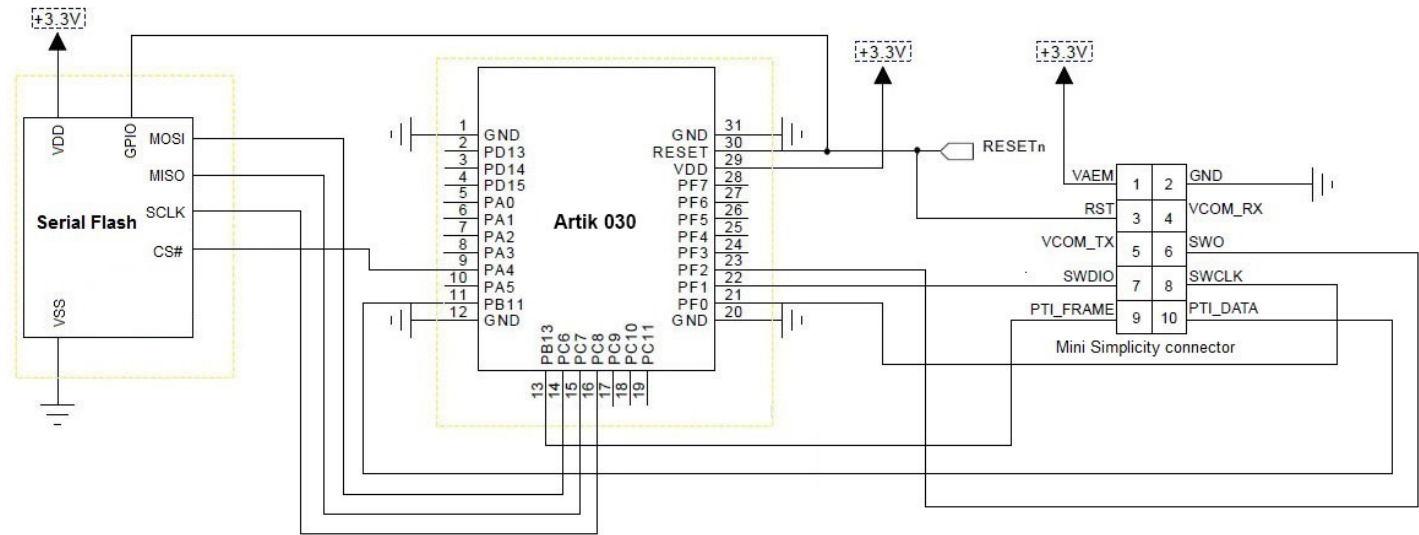


Figure 5.3. Connection Diagram: SoC Configuration

## 6. Layout Guidelines

For optimal performance of the ARTIK 030A (with integrated antenna), please follow the PCB layout guidelines and ground plane recommendations indicated in this section.

### 6.1 Module Placement and Application PCB Layout Guidelines

- Place the module at the edge of the PCB, as shown in the figure below.
- Do not place any metal (traces, components, battery, etc.) within the clearance area of the antenna (shown in the figure below).
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Do not place plastic or any other dielectric material in touch with the antenna.

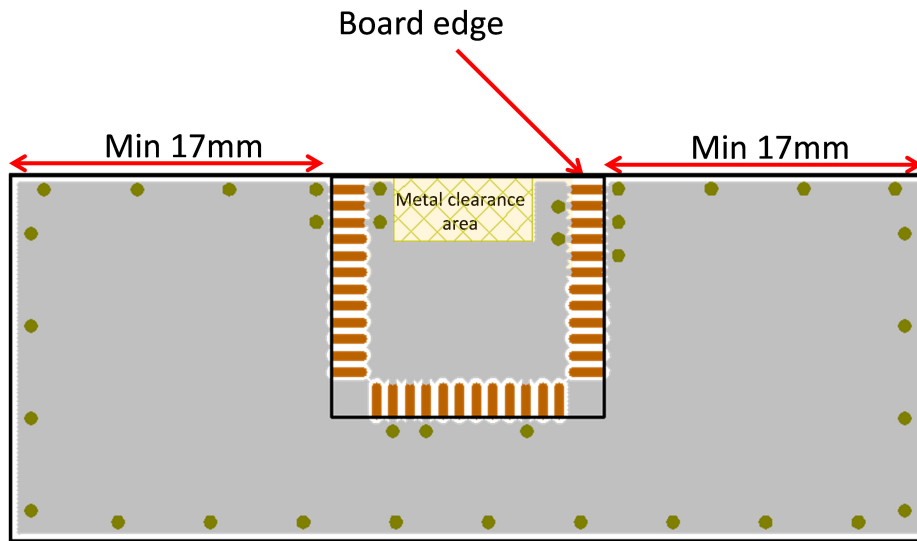


Figure 6.1. Recommended Application PCB Layout for ARTIK 030A

The layouts in the next figure will result in severely degraded RF-performance.

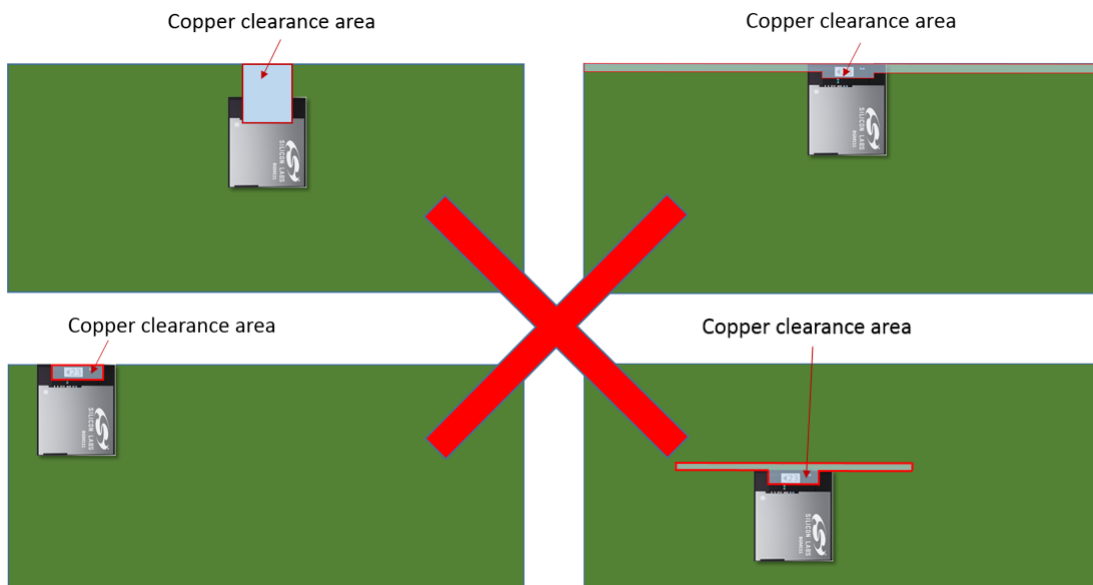
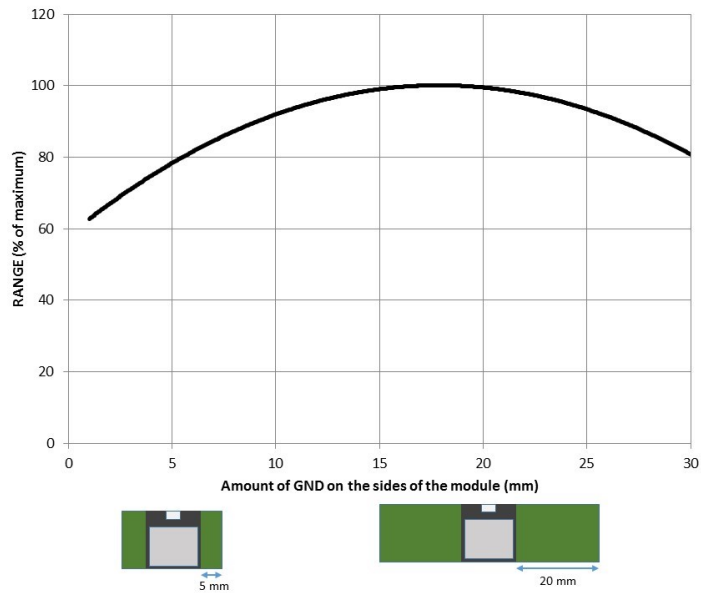


Figure 6.2. Non-optimal Module Placements for ARTIK 030A



**Figure 6.3. Impact of GND Plane Size vs. Range for ARTIK 030A**

## 6.2 Effect of Plastic and Metal Materials

Do not place plastic or any other dielectric material in close proximity to the antenna.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

## 6.3 Locating the Module Close to Human Body

Placing the module in touch or very close to the human body will negatively impact antenna efficiency and reduce range.

## 6.4 2D Radiation Pattern Plots

2D pattern, front view

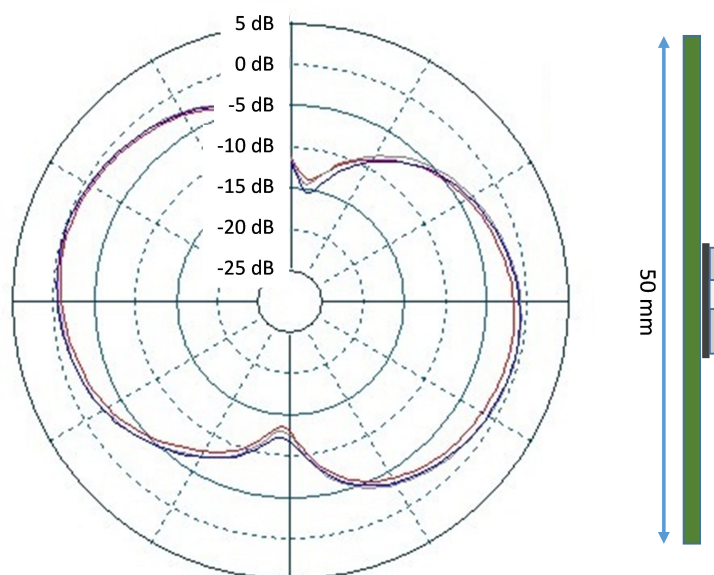


Figure 6.4. Typical 2D Radiation Pattern – Front View

2D pattern, side view

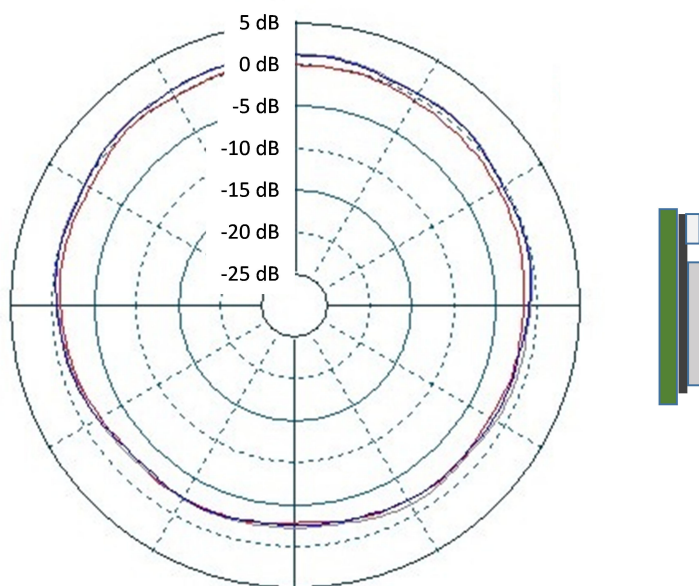
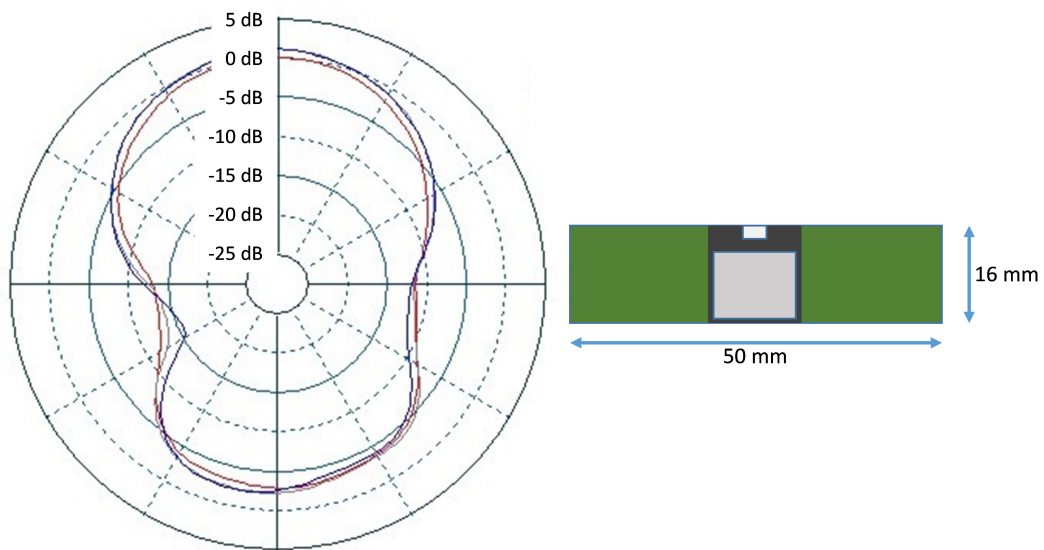


Figure 6.5. Typical 2D Radiation Pattern – Side View

### 2D pattern, top view



**Figure 6.6. Typical 2D Radiation Pattern – Top View**

## 7. Hardware Design Guidelines

The ARTIK 030 is an easy-to-use module with regard to hardware application design but certain design guidelines must be followed to guarantee optimal performance. These guidelines are listed in the next sub-sections.

### 7.1 Power Supply Requirements

Coin cell batteries cannot withstand high peak currents (e.g. higher than 15 mA). If the peak current exceeds 15 mA it's recommended to place 47 - 100  $\mu$ F capacitor in parallel with the coin cell battery to improve the battery life time. Notice that the total current consumption of your application is a combination of the radio, peripherals and MCU current consumption so you must take all of these into account. ARTIK 030 should be powered by a unipolar supply voltage with nominal value of 3.3 V.

### 7.2 Reset Functions

The ARTIK 030 can be reset by three different methods: by pulling the RESET line low, by the internal watchdog timer or software command. The reset state in ARTIK 030 does not provide any power saving functionality and thus is not recommended as a means to conserve power. ARTIK 030 has an internal system power-up reset function. The RESET pin includes an on-chip pull-up resistor and can therefore be left unconnected if no external reset switch or source is needed.

### 7.3 Debug and Firmware Updates

This section contains information on debug and firmware update methods. For additional information, refer to the following application note: *AN958: Debugging and Programming Interfaces for Custom Designs*.

#### 7.3.1 JTAG

It is recommended to expose the JTAG debug pins in your own hardware design for firmware update and debug purposes. The following table lists the required pins for JTAG connection.

The debug pins have pull-down and pull-up enabled by default, so leaving them enabled may increase current consumption if left connected to supply or ground. If enabling the JTAG pins the module must be power cycled to enable a SWD debug session.

**Table 7.1. JTAG Pads**

| PAD NAME | PAD NUMBER | JTAG SIGNAL NAME | COMMENTS                                                                       |
|----------|------------|------------------|--------------------------------------------------------------------------------|
| PF3      | 24         | TDI              | This pin is disabled after reset. Once enabled the pin has a built-in pull-up. |
| PF2      | 23         | TDO              | This pin is disabled after reset                                               |
| PF1      | 22         | TMS              | Pin is enabled after reset and has a built-in pull-up                          |
| PF0      | 21         | TCK              | Pin is enabled after reset and has a built-in pull-down                        |

#### 7.3.2 Packet Trace Interface (PTI)

The ARTIK 030 integrates a true PHY-level PTI with the MAC, allowing complete, non-intrusive capture of all packets to and from the EFR32 Wireless STK development tools.

8. Pin Definitions

8.1 Pin Definitions

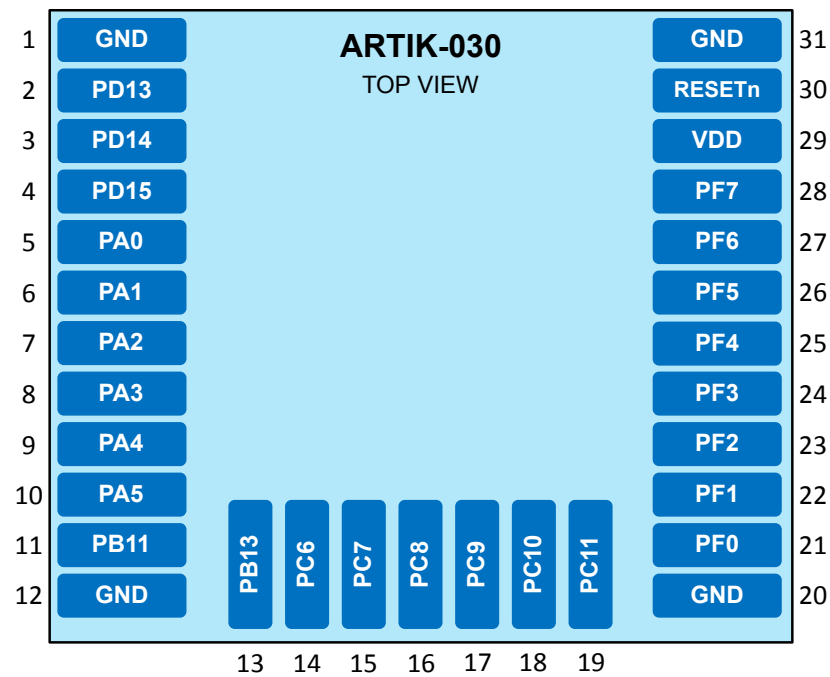


Figure 8.1. ARTIK 030 Pinout

Table 8.1. Device Pinout

| ARTIK 030 |          | Pin Alternate Functionality / Description                                                                                                                                              |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                    |
|-----------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
| Pin #     | Pin Name | Analog                                                                                                                                                                                 | Timers                                                                                                                                                                                                                                         | Communication                                                                                                                                                                                                                            | Radio                                                                                                                                             | Other                                                                                                              |
| 1         | GND      | Ground                                                                                                                                                                                 |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                    |
| 2         | PD13     | BUSCY [ADC0:<br>APORT3YCH5<br>ACMP0:<br>APORT3YCH5<br>ACMP1:<br>APORT3YCH5<br>IDAC0:<br>APORT1YCH5]<br><br>BUSDX [ADC0:<br>APORT4XCH5<br>ACMP0:<br>APORT4XCH5<br>ACMP1:<br>APORT4XCH5] | TIM0_CC0 #21<br>TIM0_CC1 #20<br>TIM0_CC2 #19<br>TIM0_CDTI0 #18<br>TIM0_CDTI1 #17<br>TIM0_CDTI2 #16<br>TIM1_CC0 #21<br>TIM1_CC1 #20<br>TIM1_CC2 #19<br>TIM1_CC3 #18 LE-<br>TIM0_OUT0 #21<br>LETIM0_OUT1 #20<br>PCNT0_S0IN #21<br>PCNT0_S1IN #20 | US0_TX #21<br>US0_RX #20<br>US0_CLK #19<br>US0_CS #18<br>US0_CTS #17<br>US0_RTS #16<br>US1_TX #21<br>US1_RX #20<br>US1_CLK #19<br>US1_CS #18<br>US1_CTS #17<br>US1_RTS #16<br>LEU0_TX #21<br>LEU0_RX #20<br>I2C0_SDA #21<br>I2C0_SCL #20 | FRC_DCLK #21<br>FRC_DOUT #20<br>FRC_DFRAME #19<br>MODEM_DCLK<br>#21 MODEM_DIN<br>#20 MO-<br>DEM_DOUT #19<br>MODEM_ANT0<br>#18 MO-<br>DEM_ANT1 #17 | PRS_CH3 #12<br>PRS_CH4 #4<br>PRS_CH5 #3<br>PRS_CH6 #15<br>ACMP0_O #21<br>ACMP1_O #21                               |
| 3         | PD14     | BUSCX [ADC0:<br>APORT3XCH6<br>ACMP0:<br>APORT3XCH6<br>ACMP1:<br>APORT3XCH6<br>IDAC0:<br>APORT1XCH6]<br><br>BUSDY [ADC0:<br>APORT4YCH6<br>ACMP0:<br>APORT4YCH6<br>ACMP1:<br>APORT4YCH6] | TIM0_CC0 #22<br>TIM0_CC1 #21<br>TIM0_CC2 #20<br>TIM0_CDTI0 #19<br>TIM0_CDTI1 #18<br>TIM0_CDTI2 #17<br>TIM1_CC0 #22<br>TIM1_CC1 #21<br>TIM1_CC2 #20<br>TIM1_CC3 #19 LE-<br>TIM0_OUT0 #22<br>LETIM0_OUT1 #21<br>PCNT0_S0IN #22<br>PCNT0_S1IN #21 | US0_TX #22<br>US0_RX #21<br>US0_CLK #20<br>US0_CS #19<br>US0_CTS #18<br>US0_RTS #17<br>US1_TX #22<br>US1_RX #21<br>US1_CLK #20<br>US1_CS #19<br>US1_CTS #18<br>US1_RTS #17<br>LEU0_TX #22<br>LEU0_RX #21<br>I2C0_SDA #22<br>I2C0_SCL #21 | FRC_DCLK #22<br>FRC_DOUT #21<br>FRC_DFRAME #20<br>MODEM_DCLK<br>#22 MODEM_DIN<br>#21 MO-<br>DEM_DOUT #20<br>MODEM_ANT0<br>#19 MO-<br>DEM_ANT1 #18 | CMU_CLK0 #5<br>PRS_CH3 #13<br>PRS_CH4 #5<br>PRS_CH5 #4<br>PRS_CH6 #16<br>ACMP0_O #22<br>ACMP1_O #22<br>GPIO_EM4WU4 |
| 4         | PD15     | BUSCY [ADC0:<br>APORT3YCH7<br>ACMP0:<br>APORT3YCH7<br>ACMP1:<br>APORT3YCH7<br>IDAC0:<br>APORT1YCH7]<br><br>BUSDX [ADC0:<br>APORT4XCH7<br>ACMP0:<br>APORT4XCH7<br>ACMP1:<br>APORT4XCH7] | TIM0_CC0 #23<br>TIM0_CC1 #22<br>TIM0_CC2 #21<br>TIM0_CDTI0 #20<br>TIM0_CDTI1 #19<br>TIM0_CDTI2 #18<br>TIM1_CC0 #23<br>TIM1_CC1 #22<br>TIM1_CC2 #21<br>TIM1_CC3 #20 LE-<br>TIM0_OUT0 #23<br>LETIM0_OUT1 #22<br>PCNT0_S0IN #23<br>PCNT0_S1IN #22 | US0_TX #23<br>US0_RX #22<br>US0_CLK #21<br>US0_CS #20<br>US0_CTS #19<br>US0_RTS #18<br>US1_TX #23<br>US1_RX #22<br>US1_CLK #21<br>US1_CS #20<br>US1_CTS #19<br>US1_RTS #18<br>LEU0_TX #23<br>LEU0_RX #22<br>I2C0_SDA #23<br>I2C0_SCL #22 | FRC_DCLK #23<br>FRC_DOUT #22<br>FRC_DFRAME #21<br>MODEM_DCLK<br>#23 MODEM_DIN<br>#22 MO-<br>DEM_DOUT #21<br>MODEM_ANT0<br>#20 MO-<br>DEM_ANT1 #19 | CMU_CLK1 #5<br>PRS_CH3 #14<br>PRS_CH4 #6<br>PRS_CH5 #5<br>PRS_CH6 #17<br>ACMP0_O #23<br>ACMP1_O #23<br>DBG_SWO #2  |

| ARTIK 030 |          | Pin Alternate Functionality / Description                                                               |                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                |                                                                                                                                               |                                                                                                  |
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| Pin #     | Pin Name | Analog                                                                                                  | Timers                                                                                                                                                                                                                                       | Communication                                                                                                                                                                                                                  | Radio                                                                                                                                         | Other                                                                                            |
| 5         | PA0      | ADC0_EXTN                                                                                               |                                                                                                                                                                                                                                              | US0_TX #0                                                                                                                                                                                                                      |                                                                                                                                               |                                                                                                  |
|           |          | BUSCX [ADC0:<br>APORT3XCH8<br>ACMP0:<br>APORT3XCH8<br>ACMP1:<br>APORT3XCH8<br>IDAC0:<br>APORT1XCH8]     | TIM0_CC0 #0<br>TIM0_CC1 #31<br>TIM0_CC2 #30<br>TIM0_CDTI0 #29<br>TIM0_CDTI1 #28<br>TIM0_CDTI2 #27<br>TIM1_CC0 #0<br>TIM1_CC1 #31<br>TIM1_CC2 #30<br>TIM1_CC3 #29 LE-<br>TIM0_OUT0 #0 LE-<br>TIM0_OUT1 #31<br>PCNT0_S0IN #0<br>PCNT0_S1IN #31 | US0_RX #31<br>US0_CLK #30<br>US0_CS #29<br>US0_CTS #28<br>US0_RTS #27<br>US1_TX #0<br>US1_RX #31<br>US1_CLK #30<br>US1_CS #29<br>US1_CTS #28<br>US1_RTS #27<br>LEU0_TX #0<br>LEU0_RX #31<br>I2C0_SDA #0<br>I2C0_SCL #31        | FRC_DCLK #0<br>FRC_DOUT #31<br>FRC_DFRAME #30<br>MODEM_DCLK #0<br>MODEM_DIN #31<br>MODEM_DOUT<br>#30 MO-<br>DEM_ANT0 #29<br>MODEM_ANT1<br>#28 | CMU_CLK1 #0<br>PRS_CH6 #0<br>PRS_CH7 #10<br>PRS_CH8 #9<br>PRS_CH9 #8<br>ACMP0_O #0<br>ACMP1_O #0 |
| 6         | PA1      | ADC0_EXTP                                                                                               |                                                                                                                                                                                                                                              | US0_TX #1                                                                                                                                                                                                                      |                                                                                                                                               |                                                                                                  |
|           |          | BUSCY [ADC0:<br>APORT3YCH9<br>ACMP0:<br>APORT3YCH9<br>ACMP1:<br>APORT3YCH9<br>IDAC0:<br>APORT1YCH9]     | TIM0_CC0 #1<br>TIM0_CC1 #0<br>TIM0_CC2 #31<br>TIM0_CDTI0 #30<br>TIM0_CDTI1 #29<br>TIM0_CDTI2 #28<br>TIM1_CC0 #1<br>TIM1_CC1 #0<br>TIM1_CC2 #31<br>TIM1_CC3 #30 LE-<br>TIM0_OUT0 #1 LE-<br>TIM0_OUT1 #0<br>PCNT0_S0IN #1<br>PCNT0_S1IN #0     | US0_RX #0<br>US0_CLK #31<br>US0_CS #30<br>US0_CTS #29<br>US0_RTS #28<br>US1_TX #1<br>US1_RX #0<br>US1_CLK #31<br>US1_CS #30<br>US1_CTS #29<br>US1_RTS #28<br>LEU0_TX #1<br>LEU0_RX #0<br>I2C0_SDA #1<br>I2C0_SCL #0            | FRC_DCLK #1<br>FRC_DOUT #0<br>FRC_DFRAME #31<br>MODEM_DCLK #1<br>MODEM_DIN #0<br>MODEM_DOUT<br>#31 MO-<br>DEM_ANT0 #30<br>MODEM_ANT1<br>#29   | CMU_CLK0 #0<br>PRS_CH6 #1<br>PRS_CH7 #0<br>PRS_CH8 #10<br>PRS_CH9 #9<br>ACMP0_O #1<br>ACMP1_O #1 |
| 7         | PA2      | BUSCX [ADC0:<br>APORT3XCH10<br>ACMP0:<br>APORT3XCH10<br>ACMP1:<br>APORT3XCH10<br>IDAC0:<br>APORT1XCH10] | TIM0_CC0 #2<br>TIM0_CC1 #1<br>TIM0_CC2 #0<br>TIM0_CDTI0 #31<br>TIM0_CDTI1 #30<br>TIM0_CDTI2 #29<br>TIM1_CC0 #2<br>TIM1_CC1 #1<br>TIM1_CC2 #0<br>TIM1_CC3 #31 LE-<br>TIM0_OUT0 #2 LE-<br>TIM0_OUT1 #1<br>PCNT0_S0IN #2<br>PCNT0_S1IN #1       | US0_TX #2<br>US0_RX #1<br>US0_CLK #0<br>US0_CS #31<br>US0_CTS #30<br>US0_RTS #29<br>US1_TX #2<br>US1_RX #1<br>US1_CLK #0<br>US1_CS #31<br>US1_CTS #30<br>US1_RTS #29<br>LEU0_TX #2<br>LEU0_RX #1<br>I2C0_SDA #2<br>I2C0_SCL #1 | FRC_DCLK #2<br>FRC_DOUT #1<br>FRC_DFRAME #0<br>MODEM_DCLK #2<br>MODEM_DIN #1<br>MODEM_DOUT #0<br>MODEM_ANT0<br>#31 MO-<br>DEM_ANT1 #30        | PRS_CH6 #2<br>PRS_CH7 #1<br>PRS_CH8 #0<br>PRS_CH9 #10<br>ACMP0_O #2<br>ACMP1_O #2                |

| ARTIK 030 |          | Pin Alternate Functionality / Description                                                               |                                                                                                                                                                                                                                      |                                                                                                                                                                                                                              |                                                                                                                                     |                                                                                                 |
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| Pin #     | Pin Name | Analog                                                                                                  | Timers                                                                                                                                                                                                                               | Communication                                                                                                                                                                                                                | Radio                                                                                                                               | Other                                                                                           |
| 8         | PA3      | BUSCY [ADC0:<br>APORT3YCH11<br>ACMP0:<br>APORT3YCH11<br>ACMP1:<br>APORT3YCH11<br>IDAC0:<br>APORT1YCH11] | TIM0_CC0 #3<br>TIM0_CC1 #2<br>TIM0_CC2 #1<br>TIM0_CDTI0 #0<br>TIM0_CDTI1 #31<br>TIM0_CDTI2 #30<br>TIM1_CC0 #3<br>TIM1_CC1 #2<br>TIM1_CC2 #1<br>TIM1_CC3 #0 LE-<br>TIM0_OUT0 #3 LE-<br>TIM0_OUT1 #2<br>PCNT0_S0IN #3<br>PCNT0_S1IN #2 | US0_TX #3<br>US0_RX #2<br>US0_CLK #1<br>US0_CS #0<br>US0_CTS #31<br>US0_RTS #30<br>US1_TX #3<br>US1_RX #2<br>US1_CLK #1<br>US1_CS #0<br>US1_CTS #31<br>US1_RTS #30<br>LEU0_TX #3<br>LEU0_RX #2<br>I2C0_SDA #3<br>I2C0_SCL #2 | FRC_DCLK #3<br>FRC_DOUT #2<br>FRC_DFRAME #1<br>MODEM_DCLK #3<br>MODEM_DIN #2<br>MODEM_DOUT #1<br>MODEM_ANT0 #0<br>MODEM_ANT1<br>#31 | PRS_CH6 #3<br>PRS_CH7 #2<br>PRS_CH8 #1<br>PRS_CH9 #0<br>ACMP0_O #3<br>ACMP1_O #3<br>GPIO_EM4WU8 |
|           |          | BUSCX [ADC0:<br>APORT3XCH12<br>ACMP0:<br>APORT3XCH12<br>ACMP1:<br>APORT3XCH12<br>IDAC0:<br>APORT1XCH12] | TIM0_CC0 #4<br>TIM0_CC1 #3<br>TIM0_CC2 #2<br>TIM0_CDTI0 #1<br>TIM0_CDTI1 #0<br>TIM0_CDTI2 #31<br>TIM1_CC0 #4<br>TIM1_CC1 #3<br>TIM1_CC2 #2<br>TIM1_CC3 #1 LE-<br>TIM0_OUT0 #4 LE-<br>TIM0_OUT1 #3<br>PCNT0_S0IN #4<br>PCNT0_S1IN #3  | US0_TX #4<br>US0_RX #3<br>US0_CLK #2<br>US0_CS #1<br>US0_CTS #0<br>US0_RTS #31<br>US1_TX #4<br>US1_RX #3<br>US1_CLK #2<br>US1_CS #1<br>US1_CTS #0<br>US1_RTS #31<br>LEU0_TX #4<br>LEU0_RX #3<br>I2C0_SDA #4<br>I2C0_SCL #3   | FRC_DCLK #4<br>FRC_DOUT #3<br>FRC_DFRAME #2<br>MODEM_DCLK #4<br>MODEM_DIN #3<br>MODEM_DOUT #2<br>MODEM_ANT0 #1<br>MODEM_ANT1 #0     | PRS_CH6 #4<br>PRS_CH7 #3<br>PRS_CH8 #2<br>PRS_CH9 #1<br>ACMP0_O #4<br>ACMP1_O #4                |
| 10        | PA5      | BUSCY [ADC0:<br>APORT3YCH13<br>ACMP0:<br>APORT3YCH13<br>ACMP1:<br>APORT3YCH13<br>IDAC0:<br>APORT1YCH13] | TIM0_CC0 #5<br>TIM0_CC1 #4<br>TIM0_CC2 #3<br>TIM0_CDTI0 #2<br>TIM0_CDTI1 #1<br>TIM0_CDTI2 #0<br>TIM1_CC0 #5<br>TIM1_CC1 #4<br>TIM1_CC2 #3<br>TIM1_CC3 #2 LE-<br>TIM0_OUT0 #5 LE-<br>TIM0_OUT1 #4<br>PCNT0_S0IN #5<br>PCNT0_S1IN #4   | US0_TX #5<br>US0_RX #4<br>US0_CLK #3<br>US0_CS #2<br>US0_CTS #1<br>US0_RTS #0<br>US1_TX #5<br>US1_RX #4<br>US1_CLK #3<br>US1_CS #2<br>US1_CTS #1<br>US1_RTS #0<br>LEU0_TX #5<br>LEU0_RX #4<br>I2C0_SDA #5<br>I2C0_SCL #4     | FRC_DCLK #5<br>FRC_DOUT #4<br>FRC_DFRAME #3<br>MODEM_DCLK #5<br>MODEM_DIN #4<br>MODEM_DOUT #3<br>MODEM_ANT0 #2<br>MODEM_ANT1 #1     | PRS_CH6 #5<br>PRS_CH7 #4<br>PRS_CH8 #3<br>PRS_CH9 #2<br>ACMP0_O #5<br>ACMP1_O #5                |
|           |          | BUSDX [ADC0:<br>APORT4XCH13<br>ACMP0:<br>APORT4XCH13<br>ACMP1:<br>APORT4XCH13]                          |                                                                                                                                                                                                                                      |                                                                                                                                                                                                                              |                                                                                                                                     |                                                                                                 |

| ARTIK 030 |          | Pin Alternate Functionality / Description                                                                                                                                                     |                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                  |                                                                                                                                          |                                                                                                               |
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| Pin #     | Pin Name | Analog                                                                                                                                                                                        | Timers                                                                                                                                                                                                                                   | Communication                                                                                                                                                                                                                    | Radio                                                                                                                                    | Other                                                                                                         |
| 11        | PB11     | BUSCY [ADC0:<br>APORT3YCH27<br>ACMP0:<br>APORT3YCH27<br>ACMP1:<br>APORT3YCH27<br>IDAC0:<br>APORT1YCH27]<br><br>BUSDX [ADC0:<br>APORT4XCH27<br>ACMP0:<br>APORT4XCH27<br>ACMP1:<br>APORT4XCH27] | TIM0_CC0 #6<br>TIM0_CC1 #5<br>TIM0_CC2 #4<br>TIM0_CDTI0 #3<br>TIM0_CDTI1 #2<br>TIM0_CDTI2 #1<br>TIM1_CC0 #6<br>TIM1_CC1 #5<br>TIM1_CC2 #4<br>TIM1_CC3 #3 LE-<br>TIM0_OUT0 #6 LE-<br>TIM0_OUT1 #5<br>PCNT0_S0IN #6<br>PCNT0_S1IN #5       | US0_TX #6<br>US0_RX #5<br>US0_CLK #4<br>US0_CS #3<br>US0_CTS #2<br>US0_RTS #1<br>US1_TX #6<br>US1_RX #5<br>US1_CLK #4<br>US1_CS #3<br>US1_CTS #2<br>US1_RTS #1<br>LEU0_TX #6<br>LEU0_RX #5<br>I2C0_SDA #6<br>I2C0_SCL #5         | FRC_DCLK #6<br>FRC_DOUT #5<br>FRC_DFRAME #4<br>MODEM_DCLK #6<br>MODEM_DIN #5<br>MODEM_DOUT #4<br>MODEM_ANT0 #3<br>MODEM_ANT1 #2          | PRS_CH6 #6<br>PRS_CH7 #5<br>PRS_CH8 #4<br>PRS_CH9 #3<br>ACMP0_O #6<br>ACMP1_O #6                              |
| 12        | GND      | Ground                                                                                                                                                                                        |                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                  |                                                                                                                                          |                                                                                                               |
| 13        | PB13     | BUSCY [ADC0:<br>APORT3YCH29<br>ACMP0:<br>APORT3YCH29<br>ACMP1:<br>APORT3YCH29<br>IDAC0:<br>APORT1YCH29]<br><br>BUSDX [ADC0:<br>APORT4XCH29<br>ACMP0:<br>APORT4XCH29<br>ACMP1:<br>APORT4XCH29] | TIM0_CC0 #8<br>TIM0_CC1 #7<br>TIM0_CC2 #6<br>TIM0_CDTI0 #5<br>TIM0_CDTI1 #4<br>TIM0_CDTI2 #3<br>TIM1_CC0 #8<br>TIM1_CC1 #7<br>TIM1_CC2 #6<br>TIM1_CC3 #5 LE-<br>TIM0_OUT0 #8 LE-<br>TIM0_OUT1 #7<br>PCNT0_S0IN #8<br>PCNT0_S1IN #7       | US0_TX #8<br>US0_RX #7<br>US0_CLK #6<br>US0_CS #5<br>US0_CTS #4<br>US0_RTS #3<br>US1_TX #8<br>US1_RX #7<br>US1_CLK #6<br>US1_CS #5<br>US1_CTS #4<br>US1_RTS #3<br>LEU0_TX #8<br>LEU0_RX #7<br>I2C0_SDA #8<br>I2C0_SCL #7         | FRC_DCLK #8<br>FRC_DOUT #7<br>FRC_DFRAME #6<br>MODEM_DCLK #8<br>MODEM_DIN #7<br>MODEM_DOUT #6<br>MODEM_ANT0 #5<br>MODEM_ANT1 #4          | PRS_CH6 #8<br>PRS_CH7 #7<br>PRS_CH8 #6<br>PRS_CH9 #5<br>ACMP0_O #8<br>ACMP1_O #8<br>DBG_SWO #1<br>GPIO_EM4WU9 |
| 14        | PC6      | BUSAX [ADC0:<br>APORT1XCH6<br>ACMP0:<br>APORT1XCH6<br>ACMP1:<br>APORT1XCH6]<br><br>BUSBY [ADC0:<br>APORT2YCH6<br>ACMP0:<br>APORT2YCH6<br>ACMP1:<br>APORT2YCH6]                                | TIM0_CC0 #11<br>TIM0_CC1 #10<br>TIM0_CC2 #9<br>TIM0_CDTI0 #8<br>TIM0_CDTI1 #7<br>TIM0_CDTI2 #6<br>TIM1_CC0 #11<br>TIM1_CC1 #10<br>TIM1_CC2 #9<br>TIM1_CC3 #8 LE-<br>TIM0_OUT0 #11<br>LETIM0_OUT1 #10<br>PCNT0_S0IN #11<br>PCNT0_S1IN #10 | US0_TX #11<br>US0_RX #10<br>US0_CLK #9<br>US0_CS #8<br>US0_CTS #7<br>US0_RTS #6<br>US1_TX #11<br>US1_RX #10<br>US1_CLK #9<br>US1_CS #8<br>US1_CTS #7<br>US1_RTS #6<br>LEU0_TX #11<br>LEU0_RX #10<br>I2C0_SDA #11<br>I2C0_SCL #10 | FRC_DCLK #11<br>FRC_DOUT #10<br>FRC_DFRAME #9<br>MODEM_DCLK<br>#11 MODEM_DIN<br>#10 MO-<br>DEM_DOUT #9<br>MODEM_ANT0 #8<br>MODEM_ANT1 #7 | CMU_CLK0 #2<br>PRS_CH0 #8<br>PRS_CH9 #11<br>PRS_CH10 #0<br>PRS_CH11 #5<br>ACMP0_O #11<br>ACMP1_O #11          |

| ARTIK 030 |          | Pin Alternate Functionality / Description                                                                                                                      |                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                        |                                                                                                                                                   |                                                                                                      |
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| Pin #     | Pin Name | Analog                                                                                                                                                         | Timers                                                                                                                                                                                                                                        | Communication                                                                                                                                                                                                                          | Radio                                                                                                                                             | Other                                                                                                |
| 15        | PC7      | BUSAY [ADC0:<br>APORT1YCH7<br>ACMP0:<br>APORT1YCH7<br>ACMP1:<br>APORT1YCH7]<br><br>BUSBX [ADC0:<br>APORT2XCH7<br>ACMP0:<br>APORT2XCH7<br>ACMP1:<br>APORT2XCH7] | TIM0_CC0 #12<br>TIM0_CC1 #11<br>TIM0_CC2 #10<br>TIM0_CDTI0 #9<br>TIM0_CDTI1 #8<br>TIM0_CDTI2 #7<br>TIM1_CC0 #12<br>TIM1_CC1 #11<br>TIM1_CC2 #10<br>TIM1_CC3 #9 LE-<br>TIM0_OUT0 #12<br>LETIM0_OUT1 #11<br>PCNT0_S0IN #12<br>PCNT0_S1IN #11    | US0_TX #12<br>US0_RX #11<br>US0_CLK #10<br>US0_CS #9<br>US0_CTS #8<br>US0_RTS #7<br>US1_TX #12<br>US1_RX #11<br>US1_CLK #10<br>US1_CS #9<br>US1_CTS #8<br>US1_RTS #7<br>LEU0_TX #12<br>LEU0_RX #11<br>I2C0_SDA #12<br>I2C0_SCL #11     | FRC_DCLK #12<br>FRC_DOUT #11<br>FRC_DFRAME #10<br>MODEM_DCLK<br>#12 MODEM_DIN<br>#11 MO-<br>DEM_DOUT #10<br>MODEM_ANT0 #9<br>MODEM_ANT1 #8        | CMU_CLK1 #2<br>PRS_CH0 #9<br>PRS_CH9 #12<br>PRS_CH10 #1<br>PRS_CH11 #0<br>ACMP0_O #12<br>ACMP1_O #12 |
| 16        | PC8      | BUSAX [ADC0:<br>APORT1XCH8<br>ACMP0:<br>APORT1XCH8<br>ACMP1:<br>APORT1XCH8]<br><br>BUSBY [ADC0:<br>APORT2YCH8<br>ACMP0:<br>APORT2YCH8<br>ACMP1:<br>APORT2YCH8] | TIM0_CC0 #13<br>TIM0_CC1 #12<br>TIM0_CC2 #11<br>TIM0_CDTI0 #10<br>TIM0_CDTI1 #9<br>TIM0_CDTI2 #8<br>TIM1_CC0 #13<br>TIM1_CC1 #12<br>TIM1_CC2 #11<br>TIM1_CC3 #10 LE-<br>TIM0_OUT0 #13<br>LETIM0_OUT1 #12<br>PCNT0_S0IN #13<br>PCNT0_S1IN #12  | US0_TX #13<br>US0_RX #12<br>US0_CLK #11<br>US0_CS #10<br>US0_CTS #9<br>US0_RTS #8<br>US1_TX #13<br>US1_RX #12<br>US1_CLK #11<br>US1_CS #10<br>US1_CTS #9<br>US1_RTS #8<br>LEU0_TX #13<br>LEU0_RX #12<br>I2C0_SDA #13<br>I2C0_SCL #12   | FRC_DCLK #13<br>FRC_DOUT #12<br>FRC_DFRAME #11<br>MODEM_DCLK<br>#13 MODEM_DIN<br>#12 MO-<br>DEM_DOUT #11<br>MODEM_ANT0<br>#10 MO-<br>DEM_ANT1 #9  | PRS_CH0 #10<br>PRS_CH9 #13<br>PRS_CH10 #2<br>PRS_CH11 #1<br>ACMP0_O #13<br>ACMP1_O #13               |
| 17        | PC9      | BUSAY [ADC0:<br>APORT1YCH9<br>ACMP0:<br>APORT1YCH9<br>ACMP1:<br>APORT1YCH9]<br><br>BUSBX [ADC0:<br>APORT2XCH9<br>ACMP0:<br>APORT2XCH9<br>ACMP1:<br>APORT2XCH9] | TIM0_CC0 #14<br>TIM0_CC1 #13<br>TIM0_CC2 #12<br>TIM0_CDTI0 #11<br>TIM0_CDTI1 #10<br>TIM0_CDTI2 #9<br>TIM1_CC0 #14<br>TIM1_CC1 #13<br>TIM1_CC2 #12<br>TIM1_CC3 #11 LE-<br>TIM0_OUT0 #14<br>LETIM0_OUT1 #13<br>PCNT0_S0IN #14<br>PCNT0_S1IN #13 | US0_TX #14<br>US0_RX #13<br>US0_CLK #12<br>US0_CS #11<br>US0_CTS #10<br>US0_RTS #9<br>US1_TX #14<br>US1_RX #13<br>US1_CLK #12<br>US1_CS #11<br>US1_CTS #10<br>US1_RTS #9<br>LEU0_TX #14<br>LEU0_RX #13<br>I2C0_SDA #14<br>I2C0_SCL #13 | FRC_DCLK #14<br>FRC_DOUT #13<br>FRC_DFRAME #12<br>MODEM_DCLK<br>#14 MODEM_DIN<br>#13 MO-<br>DEM_DOUT #12<br>MODEM_ANT0<br>#11 MO-<br>DEM_ANT1 #10 | PRS_CH0 #11<br>PRS_CH9 #14<br>PRS_CH10 #3<br>PRS_CH11 #2<br>ACMP0_O #14<br>ACMP1_O #14               |

| ARTIK 030 |          | Pin Alternate Functionality / Description                                                                                                                            |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                       |
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| Pin #     | Pin Name | Analog                                                                                                                                                               | Timers                                                                                                                                                                                                                                         | Communication                                                                                                                                                                                                                            | Radio                                                                                                                                             | Other                                                                                                                 |
| 18        | PC10     | BUSAX [ADC0:<br>APORT1XCH10<br>ACMP0:<br>APORT1XCH10<br>ACMP1:<br>APORT1XCH10]<br><br>BUSBY [ADC0:<br>APORT2YCH10<br>ACMP0:<br>APORT2YCH10<br>ACMP1:<br>APORT2YCH10] | TIM0_CC0 #15<br>TIM0_CC1 #14<br>TIM0_CC2 #13<br>TIM0_CDTI0 #12<br>TIM0_CDTI1 #11<br>TIM0_CDTI2 #10<br>TIM1_CC0 #15<br>TIM1_CC1 #14<br>TIM1_CC2 #13<br>TIM1_CC3 #12 LE-<br>TIM0_OUT0 #15<br>LETIM0_OUT1 #14<br>PCNT0_S0IN #15<br>PCNT0_S1IN #14 | US0_TX #15<br>US0_RX #14<br>US0_CLK #13<br>US0_CS #12<br>US0_CTS #11<br>US0_RTS #10<br>US1_TX #15<br>US1_RX #14<br>US1_CLK #13<br>US1_CS #12<br>US1_CTS #11<br>US1_RTS #10<br>LEU0_TX #15<br>LEU0_RX #14<br>I2C0_SDA #15<br>I2C0_SCL #14 | FRC_DCLK #15<br>FRC_DOUT #14<br>FRC_DFRAME #13<br>MODEM_DCLK<br>#15 MODEM_DIN<br>#14 MO-<br>DEM_DOUT #13<br>MODEM_ANT0<br>#12 MO-<br>DEM_ANT1 #11 | CMU_CLK1 #3<br>PRS_CH0 #12<br>PRS_CH9 #15<br>PRS_CH10 #4<br>PRS_CH11 #3<br>ACMP0_O #15<br>ACMP1_O #15<br>GPIO_EM4WU12 |
| 19        | PC11     | BUSAY [ADC0:<br>APORT1YCH11<br>ACMP0:<br>APORT1YCH11<br>ACMP1:<br>APORT1YCH11]<br><br>BUSBX [ADC0:<br>APORT2XCH11<br>ACMP0:<br>APORT2XCH11<br>ACMP1:<br>APORT2XCH11] | TIM0_CC0 #16<br>TIM0_CC1 #15<br>TIM0_CC2 #14<br>TIM0_CDTI0 #13<br>TIM0_CDTI1 #12<br>TIM0_CDTI2 #11<br>TIM1_CC0 #16<br>TIM1_CC1 #15<br>TIM1_CC2 #14<br>TIM1_CC3 #13 LE-<br>TIM0_OUT0 #16<br>LETIM0_OUT1 #15<br>PCNT0_S0IN #16<br>PCNT0_S1IN #15 | US0_TX #16<br>US0_RX #15<br>US0_CLK #14<br>US0_CS #13<br>US0_CTS #12<br>US0_RTS #11<br>US1_TX #16<br>US1_RX #15<br>US1_CLK #14<br>US1_CS #13<br>US1_CTS #12<br>US1_RTS #11<br>LEU0_TX #16<br>LEU0_RX #15<br>I2C0_SDA #16<br>I2C0_SCL #15 | FRC_DCLK #16<br>FRC_DOUT #15<br>FRC_DFRAME #14<br>MODEM_DCLK<br>#16 MODEM_DIN<br>#15 MO-<br>DEM_DOUT #14<br>MODEM_ANT0<br>#13 MO-<br>DEM_ANT1 #12 | CMU_CLK0 #3<br>PRS_CH0 #13<br>PRS_CH9 #16<br>PRS_CH10 #5<br>PRS_CH11 #4<br>ACMP0_O #16<br>ACMP1_O #16<br>DBG_SWO #3   |
| 20        | GND      | Ground                                                                                                                                                               |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                       |
| 21        | PF0      | BUSAX [ADC0:<br>APORT1XCH16<br>ACMP0:<br>APORT1XCH16<br>ACMP1:<br>APORT1XCH16]<br><br>BUSBY [ADC0:<br>APORT2YCH16<br>ACMP0:<br>APORT2YCH16<br>ACMP1:<br>APORT2YCH16] | TIM0_CC0 #24<br>TIM0_CC1 #23<br>TIM0_CC2 #22<br>TIM0_CDTI0 #21<br>TIM0_CDTI1 #20<br>TIM0_CDTI2 #19<br>TIM1_CC0 #24<br>TIM1_CC1 #23<br>TIM1_CC2 #22<br>TIM1_CC3 #21 LE-<br>TIM0_OUT0 #24<br>LETIM0_OUT1 #23<br>PCNT0_S0IN #24<br>PCNT0_S1IN #23 | US0_TX #24<br>US0_RX #23<br>US0_CLK #22<br>US0_CS #21<br>US0_CTS #20<br>US0_RTS #19<br>US1_TX #24<br>US1_RX #23<br>US1_CLK #22<br>US1_CS #21<br>US1_CTS #20<br>US1_RTS #19<br>LEU0_TX #24<br>LEU0_RX #23<br>I2C0_SDA #24<br>I2C0_SCL #23 | FRC_DCLK #24<br>FRC_DOUT #23<br>FRC_DFRAME #22<br>MODEM_DCLK<br>#24 MODEM_DIN<br>#23 MO-<br>DEM_DOUT #22<br>MODEM_ANT0<br>#21 MO-<br>DEM_ANT1 #20 | PRS_CH0 #0<br>PRS_CH1 #7<br>PRS_CH2 #6<br>PRS_CH3 #5<br>ACMP0_O #24<br>ACMP1_O #24<br>DBG_SWCLKTCK<br>#0              |

| ARTIK 030 |          | Pin Alternate Functionality / Description                                                                                                                            |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                                              |
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| Pin #     | Pin Name | Analog                                                                                                                                                               | Timers                                                                                                                                                                                                                                         | Communication                                                                                                                                                                                                                            | Radio                                                                                                                                             | Other                                                                                                                                        |
| 22        | PF1      | BUSAY [ADC0:<br>APORT1YCH17<br>ACMP0:<br>APORT1YCH17<br>ACMP1:<br>APORT1YCH17]<br><br>BUSBX [ADC0:<br>APORT2XCH17<br>ACMP0:<br>APORT2XCH17<br>ACMP1:<br>APORT2XCH17] | TIM0_CC0 #25<br>TIM0_CC1 #24<br>TIM0_CC2 #23<br>TIM0_CDTI0 #22<br>TIM0_CDTI1 #21<br>TIM0_CDTI2 #20<br>TIM1_CC0 #25<br>TIM1_CC1 #24<br>TIM1_CC2 #23<br>TIM1_CC3 #22 LE-<br>TIM0_OUT0 #25<br>LETIM0_OUT1 #24<br>PCNT0_S0IN #25<br>PCNT0_S1IN #24 | US0_TX #25<br>US0_RX #24<br>US0_CLK #23<br>US0_CS #22<br>US0_CTS #21<br>US0_RTS #20<br>US1_TX #25<br>US1_RX #24<br>US1_CLK #23<br>US1_CS #22<br>US1_CTS #21<br>US1_RTS #20<br>LEU0_TX #25<br>LEU0_RX #24<br>I2C0_SDA #25<br>I2C0_SCL #24 | FRC_DCLK #25<br>FRC_DOUT #24<br>FRC_DFRAME #23<br>MODEM_DCLK<br>#25 MODEM_DIN<br>#24 MO-<br>DEM_DOUT #23<br>MODEM_ANT0<br>#22 MO-<br>DEM_ANT1 #21 | PRS_CH0 #1<br>PRS_CH1 #0<br>PRS_CH2 #7<br>PRS_CH3 #6<br>ACMP0_O #25<br>ACMP1_O #25<br>DBG_SWDIOTMS<br>#0                                     |
| 23        | PF2      | BUSAX [ADC0:<br>APORT1XCH18<br>ACMP0:<br>APORT1XCH18<br>ACMP1:<br>APORT1XCH18]<br><br>BUSBY [ADC0:<br>APORT2YCH18<br>ACMP0:<br>APORT2YCH18<br>ACMP1:<br>APORT2YCH18] | TIM0_CC0 #26<br>TIM0_CC1 #25<br>TIM0_CC2 #24<br>TIM0_CDTI0 #23<br>TIM0_CDTI1 #22<br>TIM0_CDTI2 #21<br>TIM1_CC0 #26<br>TIM1_CC1 #25<br>TIM1_CC2 #24<br>TIM1_CC3 #23 LE-<br>TIM0_OUT0 #26<br>LETIM0_OUT1 #25<br>PCNT0_S0IN #26<br>PCNT0_S1IN #25 | US0_TX #26<br>US0_RX #25<br>US0_CLK #24<br>US0_CS #23<br>US0_CTS #22<br>US0_RTS #21<br>US1_TX #26<br>US1_RX #25<br>US1_CLK #24<br>US1_CS #23<br>US1_CTS #22<br>US1_RTS #21<br>LEU0_TX #26<br>LEU0_RX #25<br>I2C0_SDA #26<br>I2C0_SCL #25 | FRC_DCLK #26<br>FRC_DOUT #25<br>FRC_DFRAME #24<br>MODEM_DCLK<br>#26 MODEM_DIN<br>#25 MO-<br>DEM_DOUT #24<br>MODEM_ANT0<br>#23 MO-<br>DEM_ANT1 #22 | CMU_CLK0 #6<br>PRS_CH0 #2<br>PRS_CH1 #1<br>PRS_CH2 #0<br>PRS_CH3 #7<br>ACMP0_O #26<br>ACMP1_O #26<br>DBG_TDO #0<br>DBG_SWO #0<br>GPIO_EM4WU0 |
| 24        | PF3      | BUSAY [ADC0:<br>APORT1YCH19<br>ACMP0:<br>APORT1YCH19<br>ACMP1:<br>APORT1YCH19]<br><br>BUSBX [ADC0:<br>APORT2XCH19<br>ACMP0:<br>APORT2XCH19<br>ACMP1:<br>APORT2XCH19] | TIM0_CC0 #27<br>TIM0_CC1 #26<br>TIM0_CC2 #25<br>TIM0_CDTI0 #24<br>TIM0_CDTI1 #23<br>TIM0_CDTI2 #22<br>TIM1_CC0 #27<br>TIM1_CC1 #26<br>TIM1_CC2 #25<br>TIM1_CC3 #24 LE-<br>TIM0_OUT0 #27<br>LETIM0_OUT1 #26<br>PCNT0_S0IN #27<br>PCNT0_S1IN #26 | US0_TX #27<br>US0_RX #26<br>US0_CLK #25<br>US0_CS #24<br>US0_CTS #23<br>US0_RTS #22<br>US1_TX #27<br>US1_RX #26<br>US1_CLK #25<br>US1_CS #24<br>US1_CTS #23<br>US1_RTS #22<br>LEU0_TX #27<br>LEU0_RX #26<br>I2C0_SDA #27<br>I2C0_SCL #26 | FRC_DCLK #27<br>FRC_DOUT #26<br>FRC_DFRAME #25<br>MODEM_DCLK<br>#27 MODEM_DIN<br>#26 MO-<br>DEM_DOUT #25<br>MODEM_ANT0<br>#24 MO-<br>DEM_ANT1 #23 | CMU_CLK1 #6<br>PRS_CH0 #3<br>PRS_CH1 #2<br>PRS_CH2 #1<br>PRS_CH3 #0<br>ACMP0_O #27<br>ACMP1_O #27<br>DBG_TDI #0                              |

| ARTIK 030 |          | Pin Alternate Functionality / Description                                      |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                   |
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| Pin #     | Pin Name | Analog                                                                         | Timers                                                                                                                                                                                                                                         | Communication                                                                                                                                                                                                                            | Radio                                                                                                                                             | Other                                                                                             |
| 25        | PF4      | BUSAX [ADC0:<br>APORT1XCH20<br>ACMP0:<br>APORT1XCH20<br>ACMP1:<br>APORT1XCH20] | TIM0_CC0 #28<br>TIM0_CC1 #27<br>TIM0_CC2 #26<br>TIM0_CDTI0 #25<br>TIM0_CDTI1 #24<br>TIM0_CDTI2 #23<br>TIM1_CC0 #28<br>TIM1_CC1 #27<br>TIM1_CC2 #26<br>TIM1_CC3 #25 LE-<br>TIM0_OUT0 #28<br>LETIM0_OUT1 #27<br>PCNT0_S0IN #28<br>PCNT0_S1IN #27 | US0_TX #28<br>US0_RX #27<br>US0_CLK #26<br>US0_CS #25<br>US0_CTS #24<br>US0_RTS #23<br>US1_TX #28<br>US1_RX #27<br>US1_CLK #26<br>US1_CS #25<br>US1_CTS #24<br>US1_RTS #23<br>LEU0_TX #28<br>LEU0_RX #27<br>I2C0_SDA #28<br>I2C0_SCL #27 | FRC_DCLK #28<br>FRC_DOUT #27<br>FRC_DFRAME #26<br>MODEM_DCLK<br>#28 MODEM_DIN<br>#27 MO-<br>DEM_DOUT #26<br>MODEM_ANT0<br>#25 MO-<br>DEM_ANT1 #24 | PRS_CH0 #4<br>PRS_CH1 #3<br>PRS_CH2 #2<br>PRS_CH3 #1<br>ACMP0_O #28<br>ACMP1_O #28                |
|           |          | BUSBY [ADC0:<br>APORT2YCH20<br>ACMP0:<br>APORT2YCH20<br>ACMP1:<br>APORT2YCH20] |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                   |
| 26        | PF5      | BUSAY [ADC0:<br>APORT1YCH21<br>ACMP0:<br>APORT1YCH21<br>ACMP1:<br>APORT1YCH21] | TIM0_CC0 #29<br>TIM0_CC1 #28<br>TIM0_CC2 #27<br>TIM0_CDTI0 #26<br>TIM0_CDTI1 #25<br>TIM0_CDTI2 #24<br>TIM1_CC0 #29<br>TIM1_CC1 #28<br>TIM1_CC2 #27<br>TIM1_CC3 #26 LE-<br>TIM0_OUT0 #29<br>LETIM0_OUT1 #28<br>PCNT0_S0IN #29<br>PCNT0_S1IN #28 | US0_TX #29<br>US0_RX #28<br>US0_CLK #27<br>US0_CS #26<br>US0_CTS #25<br>US0_RTS #24<br>US1_TX #29<br>US1_RX #28<br>US1_CLK #27<br>US1_CS #26<br>US1_CTS #25<br>US1_RTS #24<br>LEU0_TX #29<br>LEU0_RX #28<br>I2C0_SDA #29<br>I2C0_SCL #28 | FRC_DCLK #29<br>FRC_DOUT #28<br>FRC_DFRAME #27<br>MODEM_DCLK<br>#29 MODEM_DIN<br>#28 MO-<br>DEM_DOUT #27<br>MODEM_ANT0<br>#26 MO-<br>DEM_ANT1 #25 | PRS_CH0 #5<br>PRS_CH1 #4<br>PRS_CH2 #3<br>PRS_CH3 #2<br>ACMP0_O #29<br>ACMP1_O #29                |
|           |          | BUSBX [ADC0:<br>APORT2XCH21<br>ACMP0:<br>APORT2XCH21<br>ACMP1:<br>APORT2XCH21] |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                   |
| 27        | PF6      | BUSAX [ADC0:<br>APORT1XCH22<br>ACMP0:<br>APORT1XCH22<br>ACMP1:<br>APORT1XCH22] | TIM0_CC0 #30<br>TIM0_CC1 #29<br>TIM0_CC2 #28<br>TIM0_CDTI0 #27<br>TIM0_CDTI1 #26<br>TIM0_CDTI2 #25<br>TIM1_CC0 #30<br>TIM1_CC1 #29<br>TIM1_CC2 #28<br>TIM1_CC3 #27 LE-<br>TIM0_OUT0 #30<br>LETIM0_OUT1 #29<br>PCNT0_S0IN #30<br>PCNT0_S1IN #29 | US0_TX #30<br>US0_RX #29<br>US0_CLK #28<br>US0_CS #27<br>US0_CTS #26<br>US0_RTS #25<br>US1_TX #30<br>US1_RX #29<br>US1_CLK #28<br>US1_CS #27<br>US1_CTS #26<br>US1_RTS #25<br>LEU0_TX #30<br>LEU0_RX #29<br>I2C0_SDA #30<br>I2C0_SCL #29 | FRC_DCLK #30<br>FRC_DOUT #29<br>FRC_DFRAME #28<br>MODEM_DCLK<br>#30 MODEM_DIN<br>#29 MO-<br>DEM_DOUT #28<br>MODEM_ANT0<br>#27 MO-<br>DEM_ANT1 #26 | CMU_CLK1 #7<br>PRS_CH0 #6<br>PRS_CH1 #5<br>PRS_CH2 #4<br>PRS_CH3 #3<br>ACMP0_O #30<br>ACMP1_O #30 |
|           |          | BUSBY [ADC0:<br>APORT2YCH22<br>ACMP0:<br>APORT2YCH22<br>ACMP1:<br>APORT2YCH22] |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                   |

| ARTIK 030 |          | Pin Alternate Functionality / Description                                                                                                                                                   |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                  |
|-----------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| Pin #     | Pin Name | Analog                                                                                                                                                                                      | Timers                                                                                                                                                                                                                                         | Communication                                                                                                                                                                                                                            | Radio                                                                                                                                             | Other                                                                                                            |
| 28        | PF7      | BUSAY [ADC0:<br>APORT1YCH23<br>ACMP0:<br>APORT1YCH23<br>ACMP1:<br>APORT1YCH23]<br><br>BUSBX [ADC0:<br>APORT2XCH23<br>ACMP0:<br>APORT2XCH23<br>ACMP1:<br>APORT2XCH23]                        | TIM0_CC0 #31<br>TIM0_CC1 #30<br>TIM0_CC2 #29<br>TIM0_CDTI0 #28<br>TIM0_CDTI1 #27<br>TIM0_CDTI2 #26<br>TIM1_CC0 #31<br>TIM1_CC1 #30<br>TIM1_CC2 #29<br>TIM1_CC3 #28 LE-<br>TIM0_OUT0 #31<br>LETIM0_OUT1 #30<br>PCNT0_S0IN #31<br>PCNT0_S1IN #30 | US0_TX #31<br>US0_RX #30<br>US0_CLK #29<br>US0_CS #28<br>US0_CTS #27<br>US0_RTS #26<br>US1_TX #31<br>US1_RX #30<br>US1_CLK #29<br>US1_CS #28<br>US1_CTS #27<br>US1_RTS #26<br>LEU0_TX #31<br>LEU0_RX #30<br>I2C0_SDA #31<br>I2C0_SCL #30 | FRC_DCLK #31<br>FRC_DOUT #30<br>FRC_DFRAME #29<br>MODEM_DCLK<br>#31 MODEM_DIN<br>#30 MO-<br>DEM_DOUT #29<br>MODEM_ANT0<br>#28 MO-<br>DEM_ANT1 #27 | CMU_CLK0 #7<br>PRS_CH0 #7<br>PRS_CH1 #6<br>PRS_CH2 #5<br>PRS_CH3 #4<br>ACMP0_O #31<br>ACMP1_O #31<br>GPIO_EM4WU1 |
| 29        | VDD      | Module power supply                                                                                                                                                                         |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                  |
| 30        | RESETn   | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                  |
| 31        | GND      | Ground                                                                                                                                                                                      |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                          |                                                                                                                                                   |                                                                                                                  |

### 8.1.1 GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters A through F, and the individual pins on each port are indicated by a number from 15 down to 0.

**Table 8.2. GPIO Pinout**

| Port   | Pin 15    | Pin 14    | Pin 13    | Pin 12 | Pin 11    | Pin 10    | Pin 9    | Pin 8    | Pin 7    | Pin 6    | Pin 5    | Pin 4    | Pin 3    | Pin 2    | Pin 1    | Pin 0    |
|--------|-----------|-----------|-----------|--------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| Port A | -         | -         | -         | -      | -         | -         | -        | -        | -        | -        | PA5 (5V) | PA4 (5V) | PA3 (5V) | PA2 (5V) | PA1      | PA0      |
| Port B |           |           | PB13 (5V) |        | PB11 (5V) | -         | -        | -        | -        | -        | -        | -        | -        | -        | -        | -        |
| Port C | -         | -         | -         | -      | PC11 (5V) | PC10 (5V) | PC9 (5V) | PC8 (5V) | PC7 (5V) | PC6 (5V) | -        | -        | -        | -        | -        | -        |
| Port D | PD15 (5V) | PD14 (5V) | PD13 (5V) |        |           |           | -        | -        | -        | -        | -        | -        | -        | -        | -        | -        |
| Port E | -         | -         | -         | -      | -         | -         | -        | -        | -        | -        | -        | -        | -        | -        | -        | -        |
| Port F | -         | -         | -         | -      | -         | -         | -        | -        | PF7 (5V) | PF6 (5V) | PF5 (5V) | PF4 (5V) | PF3 (5V) | PF2 (5V) | PF1 (5V) | PF0 (5V) |

**Note:**

- GPIO with 5V tolerance are indicated by (5V).
- The pins PA4, PA3, PA2, PB13, PB11, PD15, PD14, and PD13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins on 5V domains.

## 8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 8.3. Alternate Functionality Overview**

| Alternate     | LOCATION          |                   |         |          |          |                                  |                                          |         |                                                                                                                                                                           |
|---------------|-------------------|-------------------|---------|----------|----------|----------------------------------|------------------------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Functionality | 0 - 3             | 4 - 7             | 8 - 11  | 12 - 15  | 16 - 19  | 20 - 23                          | 24 - 27                                  | 28 - 31 | Description                                                                                                                                                               |
| ACMP0_O       | 0: PA0<br>1: PA1  | 6: PB11           | 8: PB13 | 15: PC10 | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |         | Analog comparator ACMP0, digital output.                                                                                                                                  |
| ACMP1_O       | 0: PA0<br>1: PA1  | 6: PB11           | 8: PB13 | 15: PC10 | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |         | Analog comparator ACMP1, digital output.                                                                                                                                  |
| ADC0_EXTN     | 0: PA0            |                   |         |          |          |                                  |                                          |         | Analog to digital converter ADC0 external reference input negative pin                                                                                                    |
| ADC0_EXTP     | 0: PA1            |                   |         |          |          |                                  |                                          |         | Analog to digital converter ADC0 external reference input positive pin                                                                                                    |
| CMU_CLK0      | 0: PA1<br>3: PC11 | 5: PD14<br>6: PF2 |         |          |          |                                  |                                          |         | Clock Management Unit, clock output number 0.                                                                                                                             |
| CMU_CLK1      | 0: PA0<br>3: PC10 | 5: PD15<br>6: PF3 |         |          |          |                                  |                                          |         | Clock Management Unit, clock output number 1.                                                                                                                             |
| DBG_SWCLKTCK  | 0: PF0            |                   |         |          |          |                                  |                                          |         | Debug-interface Serial Wire clock input and JTAG Test Clock.<br><br>Note that this function is enabled to the pin out of reset, and has a built-in pull down.             |
| DBG_SWDIOTMS  | 0: PF1            |                   |         |          |          |                                  |                                          |         | Debug-interface Serial Wire data input / output and JTAG Test Mode Select.<br><br>Note that this function is enabled to the pin out of reset, and has a built-in pull up. |

| Alternate     | LOCATION                                |                    |         |                      |          |                                             |                                          |                    |                                                                                                                                                         |
|---------------|-----------------------------------------|--------------------|---------|----------------------|----------|---------------------------------------------|------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| Functionality | 0 - 3                                   | 4 - 7              | 8 - 11  | 12 - 15              | 16 - 19  | 20 - 23                                     | 24 - 27                                  | 28 - 31            | Description                                                                                                                                             |
| DBG_SWO       | 0: PF2<br>1: PB13<br>2: PD15<br>3: PC11 |                    |         |                      |          |                                             |                                          |                    | Debug-interface<br>Serial Wire viewer<br>Output.<br><br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| DBG_TDI       | 0: PF3                                  |                    |         |                      |          |                                             |                                          |                    | Debug-interface<br>JTAG Test Data In.<br><br>Note that this function is enabled to pin out of reset, and has a built-in pull up.                        |
| DBG_TDO       | 0: PF2                                  |                    |         |                      |          |                                             |                                          |                    | Debug-interface<br>JTAG Test Data Out.<br><br>Note that this function is enabled to pin out of reset.                                                   |
| FRC_DCLK      | 0: PA0<br>1: PA1                        | 6: PB11            | 8: PB13 | 15: PC10             | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | Frame Controller,<br>Data Sniffer Clock.                                                                                                                |
| FRC_DFRAME    |                                         | 4: PB11<br>6: PB13 |         | 13: PC10<br>14: PC11 | 19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1  | 24: PF2<br>25: PF3                       | 30: PA0<br>31: PA1 | Frame Controller,<br>Data Sniffer Frame active                                                                                                          |
| FRC_DOUT      | 0: PA1                                  | 5: PB11<br>7: PB13 |         | 14: PC10<br>15: PC11 |          | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | Frame Controller,<br>Data Sniffer Output.                                                                                                               |
| GPIO_EM4WU0   | 0: PF2                                  |                    |         |                      |          |                                             |                                          |                    | Pin can be used to wake the system up from EM4                                                                                                          |
| GPIO_EM4WU1   |                                         |                    |         |                      |          |                                             |                                          |                    | Pin can be used to wake the system up from EM4                                                                                                          |
| GPIO_EM4WU4   | 0: PD14                                 |                    |         |                      |          |                                             |                                          |                    | Pin can be used to wake the system up from EM4                                                                                                          |
| GPIO_EM4WU8   |                                         |                    |         |                      |          |                                             |                                          |                    | Pin can be used to wake the system up from EM4                                                                                                          |

| Alternate     | LOCATION         |                    |         |                      |          |                                             |                                          |                    |                                                                                   |
|---------------|------------------|--------------------|---------|----------------------|----------|---------------------------------------------|------------------------------------------|--------------------|-----------------------------------------------------------------------------------|
| Functionality | 0 - 3            | 4 - 7              | 8 - 11  | 12 - 15              | 16 - 19  | 20 - 23                                     | 24 - 27                                  | 28 - 31            | Description                                                                       |
| GPIO_EM4WU9   | 0: PB13          |                    |         |                      |          |                                             |                                          |                    | Pin can be used to wake the system up from EM4                                    |
| GPIO_EM4WU12  | 0: PC10          |                    |         |                      |          |                                             |                                          |                    | Pin can be used to wake the system up from EM4                                    |
| I2C0_SCL      | 0: PA1           | 5: PB11<br>7: PB13 |         | 14: PC10<br>15: PC11 |          | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | I2C0 Serial Clock Line input / output.                                            |
| I2C0_SDA      | 0: PA0<br>1: PA1 | 6: PB11            | 8: PB13 | 15: PC10             | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | I2C0 Serial Data input / output.                                                  |
| LETIM0_OUT0   | 0: PA0<br>1: PA1 | 6: PB11            | 8: PB13 | 15: PC10             | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | Low Energy Timer LETIM0, output channel 0.                                        |
| LETIM0_OUT1   | 0: PA1           | 5: PB11<br>7: PB13 |         | 14: PC10<br>15: PC11 |          | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | Low Energy Timer LETIM0, output channel 1.                                        |
| LEU0_RX       | 0: PA1           | 5: PB11<br>7: PB13 |         | 14: PC10<br>15: PC11 |          | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | LEUART0 Receive input.                                                            |
| LEU0_TX       | 0: PA0<br>1: PA1 | 6: PB11            | 8: PB13 | 15: PC10             | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| MODEM_DCLK    | 0: PA0<br>1: PA1 | 6: PB11            | 8: PB13 | 15: PC10             | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | MODEM data clock out.                                                             |
| MODEM_DIN     | 0: PA1           | 5: PB11<br>7: PB13 |         | 14: PC10<br>15: PC11 |          | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | MODEM data in.                                                                    |
| MODEM_DOUT    |                  | 4: PB11<br>6: PB13 |         | 13: PC10<br>14: PC11 | 19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1  | 24: PF2<br>25: PF3                       | 30: PA0<br>31: PA1 | MODEM data out.                                                                   |
| PCNT0_S0IN    | 0: PA0<br>1: PA1 | 6: PB11            | 8: PB13 | 15: PC10             | 16: PC11 | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | Pulse Counter PCNT0 input number 0.                                               |
| PCNT0_S1IN    | 0: PA1           | 5: PB11<br>7: PB13 |         | 14: PC10<br>15: PC11 |          | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | Pulse Counter PCNT0 input number 1.                                               |

| Alternate     | LOCATION                             |                               |                   |                                  |                      |                                  |                                          |         |                                                   |
|---------------|--------------------------------------|-------------------------------|-------------------|----------------------------------|----------------------|----------------------------------|------------------------------------------|---------|---------------------------------------------------|
| Functionality | 0 - 3                                | 4 - 7                         | 8 - 11            | 12 - 15                          | 16 - 19              | 20 - 23                          | 24 - 27                                  | 28 - 31 | Description                                       |
| PRS_CH0       | 0: PF0<br>1: PF1<br>2: PF2<br>3: PF3 |                               |                   | 12: PC10<br>13: PC11             |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 0.          |
| PRS_CH1       | 0: PF1<br>1: PF2<br>2: PF3           | 7: PF0                        |                   |                                  |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 1.          |
| PRS_CH2       | 0: PF2<br>1: PF3                     | 6: PF0<br>7: PF1              |                   |                                  |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 2.          |
| PRS_CH3       | 0: PF3                               | 5: PF0<br>6: PF1<br>7: PF2    |                   | 12: PD13<br>13: PD14<br>14: PD15 |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 3.          |
| PRS_CH4       |                                      | 4: PD13<br>5: PD14<br>6: PD15 |                   |                                  |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 4.          |
| PRS_CH5       | 3: PD13                              | 4: PD14<br>5: PD15            |                   |                                  |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 5.          |
| PRS_CH6       | 0: PA0<br>1: PA1                     | 6: PB11                       | 8: PB13           | 15: PD13                         | 16: PD14<br>17: PD15 |                                  |                                          |         | Peripheral Reflex System PRS, channel 6.          |
| PRS_CH7       | 0: PA1                               | 5: PB11<br>7: PB13            | 10: PA0           |                                  |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 7.          |
| PRS_CH8       |                                      | 4: PB11<br>6: PB13            | 9: PA0<br>10: PA1 |                                  |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 8.          |
| PRS_CH9       | 3: PB11                              | 5: PB13                       | 8: PA0<br>9: PA1  | 15: PC10                         | 16: PC11             |                                  |                                          |         | Peripheral Reflex System PRS, channel 9.          |
| PRS_CH10      |                                      | 4: PC10<br>5: PC11            |                   |                                  |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 10.         |
| PRS_CH11      | 3: PC10                              | 4: PC11                       |                   |                                  |                      |                                  |                                          |         | Peripheral Reflex System PRS, channel 11.         |
| TIM0_CC0      | 0: PA0<br>1: PA1                     | 6: PB11                       | 8: PB13           | 15: PC10                         | 16: PC11             | 21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |         | Timer 0 Capture Compare input / output channel 0. |

| Alternate     | LOCATION           |                    |                      |                      |                                             |                                             |                                          |                    |                                                      |
|---------------|--------------------|--------------------|----------------------|----------------------|---------------------------------------------|---------------------------------------------|------------------------------------------|--------------------|------------------------------------------------------|
| Functionality | 0 - 3              | 4 - 7              | 8 - 11               | 12 - 15              | 16 - 19                                     | 20 - 23                                     | 24 - 27                                  | 28 - 31            | Description                                          |
| TIM0_CC1      | 0: PA1             | 5: PB11<br>7: PB13 |                      | 14: PC10<br>15: PC11 |                                             | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | Timer 0 Capture Compare input / output channel 1.    |
| TIM0_CC2      |                    | 4: PB11<br>6: PB13 |                      | 13: PC10<br>14: PC11 | 19: PD13                                    | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1  | 24: PF2<br>25: PF3                       | 30: PA0<br>31: PA1 | Timer 0 Capture Compare input / output channel 2.    |
| TIM0_CDTI0    | 3: PB11            | 5: PB13            |                      | 12: PC10<br>13: PC11 | 18: PD13<br>19: PD14                        | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2   | 24: PF3                                  | 29: PA0<br>30: PA1 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDTI1    | 2: PB11            | 4: PB13            | 11: PC10             | 12: PC11             | 17: PD13<br>18: PD14<br>19: PD15            | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3    |                                          | 28: PA0<br>29: PA1 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2    | 1: PB11<br>3: PB13 |                    | 10: PC10<br>11: PC11 |                      | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3               | 27: PA0                                  | 28: PA1            | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0      | 0: PA0<br>1: PA1   | 6: PB11            | 8: PB13              | 15: PC10             | 16: PC11                                    | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | Timer 1 Capture Compare input / output channel 0.    |
| TIM1_CC1      | 0: PA1             | 5: PB11<br>7: PB13 |                      | 14: PC10<br>15: PC11 |                                             | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | Timer 1 Capture Compare input / output channel 1.    |
| TIM1_CC2      |                    | 4: PB11<br>6: PB13 |                      | 13: PC10<br>14: PC11 | 19: PD13                                    | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1  | 24: PF2<br>25: PF3                       | 30: PA0<br>31: PA1 | Timer 1 Capture Compare input / output channel 2.    |
| TIM1_CC3      | 3: PB11            | 5: PB13            |                      | 12: PC10<br>13: PC11 | 18: PD13<br>19: PD14                        | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2   | 24: PF3                                  | 29: PA0<br>30: PA1 | Timer 1 Capture Compare input / output channel 3.    |
| US0_CLK       |                    | 4: PB11<br>6: PB13 |                      | 13: PC10<br>14: PC11 | 19: PD13                                    | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1  | 24: PF2<br>25: PF3                       | 30: PA0<br>31: PA1 | USART0 clock input / output.                         |
| US0_CS        | 3: PB11            | 5: PB13            |                      | 12: PC10<br>13: PC11 | 18: PD13<br>19: PD14                        | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2   | 24: PF3                                  | 29: PA0<br>30: PA1 | USART0 chip select input / output.                   |
| US0_CTS       | 2: PB11            | 4: PB13            | 11: PC10             | 12: PC11             | 17: PD13<br>18: PD14<br>19: PD15            | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3    |                                          | 28: PA0<br>29: PA1 | USART0 Clear To Send hardware flow control input.    |
| US0_RTS       | 1: PB11<br>3: PB13 |                    | 10: PC10<br>11: PC11 |                      | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3               | 27: PA0                                  | 28: PA1            | USART0 Request To Send hardware flow control output. |

| Alternate     | LOCATION           |                    |                      |                      |                                             |                                             |                                          |                    |                                                                                                                                                           |
|---------------|--------------------|--------------------|----------------------|----------------------|---------------------------------------------|---------------------------------------------|------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Functionality | 0 - 3              | 4 - 7              | 8 - 11               | 12 - 15              | 16 - 19                                     | 20 - 23                                     | 24 - 27                                  | 28 - 31            | Description                                                                                                                                               |
| US0_RX        | 0: PA1             | 5: PB11<br>7: PB13 |                      | 14: PC10<br>15: PC11 |                                             | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | USART0 Asynchronous Receive.<br><br>USART0 Synchronous mode Master Input / Slave Output (MISO).                                                           |
| US0_TX        | 0: PA0<br>1: PA1   | 6: PB11            | 8: PB13              | 15: PC10             | 16: PC11                                    | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication.<br><br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK       |                    | 4: PB11<br>6: PB13 |                      | 13: PC10<br>14: PC11 | 19: PD13                                    | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1  | 24: PF2<br>25: PF3                       | 30: PA0<br>31: PA1 | USART1 clock input / output.                                                                                                                              |
| US1_CS        | 3: PB11            | 5: PB13            |                      | 12: PC10<br>13: PC11 | 18: PD13<br>19: PD14                        | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2   | 24: PF3                                  | 29: PA0<br>30: PA1 | USART1 chip select input / output.                                                                                                                        |
| US1_CTS       | 2: PB11            | 4: PB13            | 11: PC10             | 12: PC11             | 17: PD13<br>18: PD14<br>19: PD15            | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3    |                                          | 28: PA0<br>29: PA1 | USART1 Clear To Send hardware flow control input.                                                                                                         |
| US1_RTS       | 1: PB11<br>3: PB13 |                    | 10: PC10<br>11: PC11 |                      | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3               | 27: PA0                                  | 28: PA1            | USART1 Request To Send hardware flow control output.                                                                                                      |
| US1_RX        | 0: PA1             | 5: PB11<br>7: PB13 |                      | 14: PC10<br>15: PC11 |                                             | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3            | 31: PA0            | USART1 Asynchronous Receive.<br><br>USART1 Synchronous mode Master Input / Slave Output (MISO).                                                           |
| US1_TX        | 0: PA0<br>1: PA1   | 6: PB11            | 8: PB13              | 15: PC10             | 16: PC11                                    | 21: PD13<br>22: PD14<br>23: PD15            | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 |                    | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication.<br><br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |

### 8.3 Analog Port (APORT)

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, and DACs. The APORT consists of wires, switches, and control needed to configurably implement the routes. Please see the device Reference Manual for a complete description.

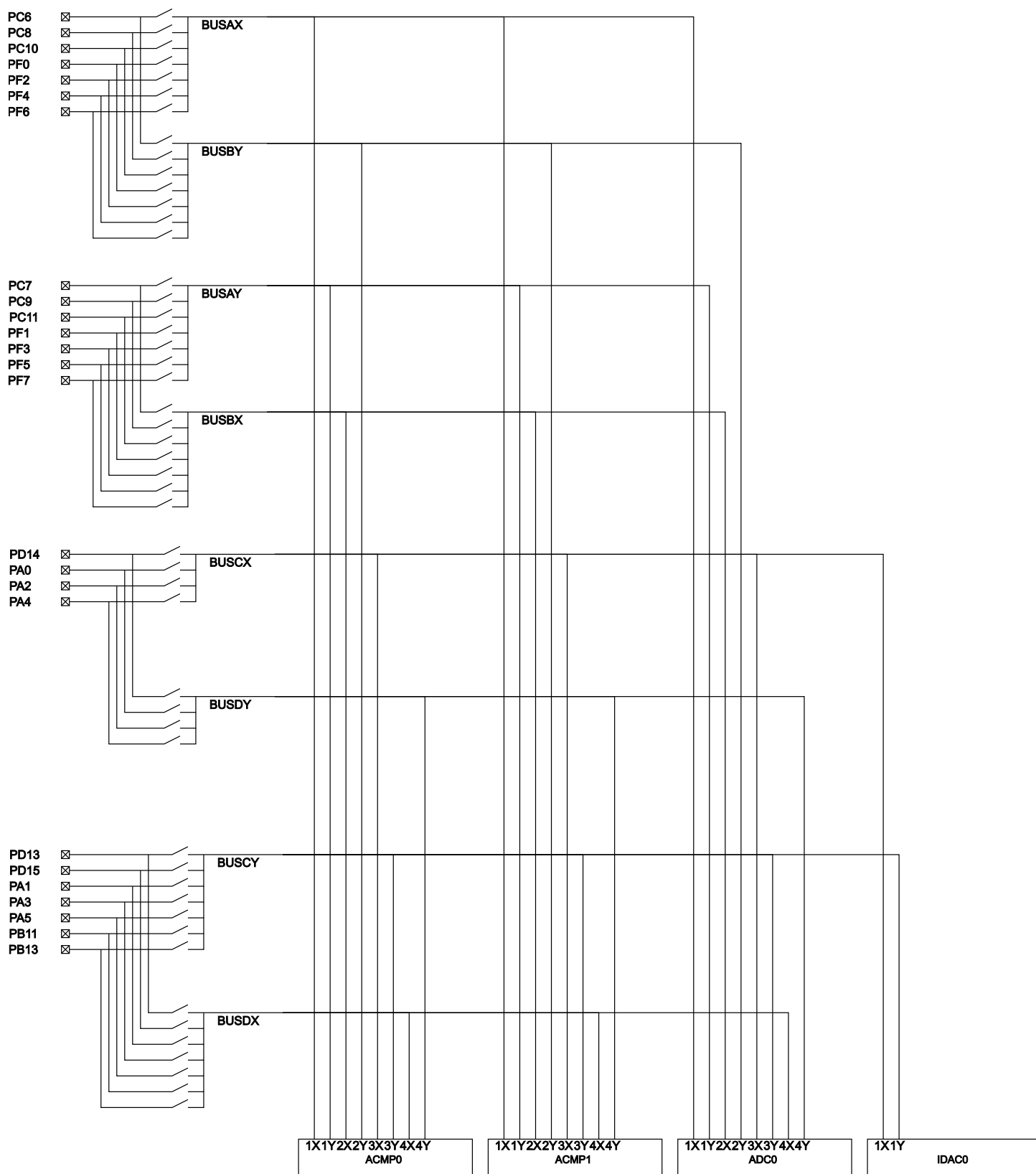


Figure 8.2. ARTIK 030 APORT

Table 8.4. APORT Client Map

| Analog Module | Analog Module Channel | Shared Bus | Pin  |
|---------------|-----------------------|------------|------|
| ACMP0         | APOINT1XCH6           | BUSAX      | PC6  |
|               | APOINT1XCH8           |            | PC8  |
|               | APOINT1XCH10          |            | PC10 |
|               | APOINT1XCH16          |            | PF0  |
|               | APOINT1XCH18          |            | PF2  |
|               | APOINT1XCH20          |            | PF4  |
|               | APOINT1XCH22          |            | PF6  |
| ACMP0         | APOINT1YCH7           | BUSAY      | PC7  |
|               | APOINT1YCH9           |            | PC9  |
|               | APOINT1YCH11          |            | PC11 |
|               | APOINT1YCH17          |            | PF1  |
|               | APOINT1YCH19          |            | PF3  |
|               | APOINT1YCH21          |            | PF5  |
|               | APOINT1YCH23          |            | PF7  |
| ACMP0         | APOINT2XCH7           | BUSBX      | PC7  |
|               | APOINT2XCH9           |            | PC9  |
|               | APOINT2XCH11          |            | PC11 |
|               | APOINT2XCH17          |            | PF1  |
|               | APOINT2XCH19          |            | PF3  |
|               | APOINT2XCH21          |            | PF5  |
|               | APOINT2XCH23          |            | PF7  |
| ACMP0         | APOINT2YCH6           | BUSBY      | PC6  |
|               | APOINT2YCH8           |            | PC8  |
|               | APOINT2YCH10          |            | PC10 |
|               | APOINT2YCH16          |            | PF0  |
|               | APOINT2YCH18          |            | PF2  |
|               | APOINT2YCH20          |            | PF4  |
|               | APOINT2YCH22          |            | PF6  |

| Analog Module | Analog Module Channel | Shared Bus | Pin  |
|---------------|-----------------------|------------|------|
| ACMP0         | APOINT3XCH2           | BUSCX      |      |
|               | APOINT3XCH4           |            |      |
|               | APOINT3XCH6           |            | PD14 |
|               | APOINT3XCH8           |            | PA0  |
|               | APOINT3XCH10          |            | PA2  |
|               | APOINT3XCH12          |            | PA4  |
|               | APOINT3XCH28          |            |      |
|               | APOINT3XCH30          |            |      |
| ACMP0         | APOINT3YCH3           | BUSCY      |      |
|               | APOINT3YCH5           |            | PD13 |
|               | APOINT3YCH7           |            | PD15 |
|               | APOINT3YCH9           |            | PA1  |
|               | APOINT3YCH11          |            | PA3  |
|               | APOINT3YCH13          |            | PA5  |
|               | APOINT3YCH27          |            | PB11 |
|               | APOINT3YCH29          |            | PB13 |
| ACMP0         | APOINT4XCH3           | BUSDX      |      |
|               | APOINT4XCH5           |            | PD13 |
|               | APOINT4XCH7           |            | PD15 |
|               | APOINT4XCH9           |            | PA1  |
|               | APOINT4XCH11          |            | PA3  |
|               | APOINT4XCH13          |            | PA5  |
|               | APOINT4XCH27          |            | PB11 |
|               | APOINT4XCH29          |            | PB13 |
| ACMP0         | APOINT4YCH2           | BUSDY      |      |
|               | APOINT4YCH4           |            |      |
|               | APOINT4YCH6           |            | PD14 |
|               | APOINT4YCH8           |            | PA0  |
|               | APOINT4YCH10          |            | PA2  |
|               | APOINT4YCH12          |            | PA4  |
|               | APOINT4YCH28          |            |      |
|               | APOINT4YCH30          |            |      |

| Analog Module | Analog Module Channel | Shared Bus | Pin  |
|---------------|-----------------------|------------|------|
| ACMP1         | APOINT1XCH6           | BUSAX      | PC6  |
|               | APOINT1XCH8           |            | PC8  |
|               | APOINT1XCH10          |            | PC10 |
|               | APOINT1XCH16          |            | PF0  |
|               | APOINT1XCH18          |            | PF2  |
|               | APOINT1XCH20          |            | PF4  |
|               | APOINT1XCH22          |            | PF6  |
| ACMP1         | APOINT1YCH7           | BUSAY      | PC7  |
|               | APOINT1YCH9           |            | PC9  |
|               | APOINT1YCH11          |            | PC11 |
|               | APOINT1YCH17          |            | PF1  |
|               | APOINT1YCH19          |            | PF3  |
|               | APOINT1YCH21          |            | PF5  |
|               | APOINT1YCH23          |            | PF7  |
| ACMP1         | APOINT2XCH7           | BUSBX      | PC7  |
|               | APOINT2XCH9           |            | PC9  |
|               | APOINT2XCH11          |            | PC11 |
|               | APOINT2XCH17          |            | PF1  |
|               | APOINT2XCH19          |            | PF3  |
|               | APOINT2XCH21          |            | PF5  |
|               | APOINT2XCH23          |            | PF7  |
| ACMP1         | APOINT2YCH6           | BUSBY      | PC6  |
|               | APOINT2YCH8           |            | PC8  |
|               | APOINT2YCH10          |            | PC10 |
|               | APOINT2YCH16          |            | PF0  |
|               | APOINT2YCH18          |            | PF2  |
|               | APOINT2YCH20          |            | PF4  |
|               | APOINT2YCH22          |            | PF6  |
| ACMP1         | APOINT3XCH2           | BUSCX      |      |
|               | APOINT3XCH4           |            |      |
|               | APOINT3XCH6           |            | PD14 |
|               | APOINT3XCH8           |            | PA0  |
|               | APOINT3XCH10          |            | PA2  |
|               | APOINT3XCH12          |            | PA4  |
|               | APOINT3XCH28          |            |      |
|               | APOINT3XCH30          |            |      |

| Analog Module | Analog Module Channel | Shared Bus | Pin  |
|---------------|-----------------------|------------|------|
| ACMP1         | APOINT3YCH3           | BUSCY      |      |
|               | APOINT3YCH5           |            | PD13 |
|               | APOINT3YCH7           |            | PD15 |
|               | APOINT3YCH9           |            | PA1  |
|               | APOINT3YCH11          |            | PA3  |
|               | APOINT3YCH13          |            | PA5  |
|               | APOINT3YCH27          |            | PB11 |
|               | APOINT3YCH29          |            | PB13 |
|               | APOINT3YCH31          |            |      |
| ACMP1         | APOINT4XCH3           | BUSDX      |      |
|               | APOINT4XCH5           |            | PD13 |
|               | APOINT4XCH7           |            | PD15 |
|               | APOINT4XCH9           |            | PA1  |
|               | APOINT4XCH11          |            | PA3  |
|               | APOINT4XCH13          |            | PA5  |
|               | APOINT4XCH27          |            | PB11 |
|               | APOINT4XCH29          |            | PB13 |
|               | APOINT4XCH31          |            |      |
| ACMP1         | APOINT4YCH2           | BUSDY      |      |
|               | APOINT4YCH4           |            |      |
|               | APOINT4YCH6           |            | PD14 |
|               | APOINT4YCH8           |            | PA0  |
|               | APOINT4YCH10          |            | PA2  |
|               | APOINT4YCH12          |            | PA4  |
|               | APOINT4YCH28          |            |      |
|               | APOINT4YCH30          |            |      |
|               |                       |            |      |
| ADC0          | APOINT1XCH6           | BUSAX      | PC6  |
|               | APOINT1XCH8           |            | PC8  |
|               | APOINT1XCH10          |            | PC10 |
|               | APOINT1XCH16          |            | PF0  |
|               | APOINT1XCH18          |            | PF2  |
|               | APOINT1XCH20          |            | PF4  |
|               | APOINT1XCH22          |            | PF6  |

| Analog Module | Analog Module Channel | Shared Bus | Pin  |
|---------------|-----------------------|------------|------|
| ADC0          | APOINT1YCH7           | BUSAY      | PC7  |
|               | APOINT1YCH9           |            | PC9  |
|               | APOINT1YCH11          |            | PC11 |
|               | APOINT1YCH17          |            | PF1  |
|               | APOINT1YCH19          |            | PF3  |
|               | APOINT1YCH21          |            | PF5  |
|               | APOINT1YCH23          |            | PF7  |
| ADC0          | APOINT2XCH7           | BUSBX      | PC7  |
|               | APOINT2XCH9           |            | PC9  |
|               | APOINT2XCH11          |            | PC11 |
|               | APOINT2XCH17          |            | PF1  |
|               | APOINT2XCH19          |            | PF3  |
|               | APOINT2XCH21          |            | PF5  |
|               | APOINT2XCH23          |            | PF7  |
| ADC0          | APOINT2YCH6           | BUSBY      | PC6  |
|               | APOINT2YCH8           |            | PC8  |
|               | APOINT2YCH10          |            | PC10 |
|               | APOINT2YCH16          |            | PF0  |
|               | APOINT2YCH18          |            | PF2  |
|               | APOINT2YCH20          |            | PF4  |
|               | APOINT2YCH22          |            | PF6  |
| ADC0          | APOINT3XCH2           | BUSCX      |      |
|               | APOINT3XCH4           |            |      |
|               | APOINT3XCH6           |            | PD14 |
|               | APOINT3XCH8           |            | PA0  |
|               | APOINT3XCH10          |            | PA2  |
|               | APOINT3XCH12          |            | PA4  |
|               | APOINT3XCH28          |            |      |
|               | APOINT3XCH30          |            |      |

| Analog Module | Analog Module Channel | Shared Bus | Pin  |
|---------------|-----------------------|------------|------|
| ADC0          | APOINT3YCH3           | BUSCY      |      |
|               | APOINT3YCH5           |            | PD13 |
|               | APOINT3YCH7           |            | PD15 |
|               | APOINT3YCH9           |            | PA1  |
|               | APOINT3YCH11          |            | PA3  |
|               | APOINT3YCH13          |            | PA5  |
|               | APOINT3YCH27          |            | PB11 |
|               | APOINT3YCH29          |            | PB13 |
|               | APOINT3YCH31          |            |      |
| ADC0          | APOINT4XCH3           | BUSDX      |      |
|               | APOINT4XCH5           |            | PD13 |
|               | APOINT4XCH7           |            | PD15 |
|               | APOINT4XCH9           |            | PA1  |
|               | APOINT4XCH11          |            | PA3  |
|               | APOINT4XCH13          |            | PA5  |
|               | APOINT4XCH27          |            | PB11 |
|               | APOINT4XCH29          |            | PB13 |
|               | APOINT4XCH31          |            |      |
| ADC0          | APOINT4YCH2           | BUSDY      |      |
|               | APOINT4YCH4           |            |      |
|               | APOINT4YCH6           |            | PD14 |
|               | APOINT4YCH8           |            | PA0  |
|               | APOINT4YCH10          |            | PA2  |
|               | APOINT4YCH12          |            | PA4  |
|               | APOINT4YCH28          |            |      |
|               | APOINT4YCH30          |            |      |
| IDAC0         | APOINT1XCH2           | BUSCX      |      |
|               | APOINT1XCH4           |            |      |
|               | APOINT1XCH6           |            | PD14 |
|               | APOINT1XCH8           |            | PA0  |
|               | APOINT1XCH10          |            | PA2  |
|               | APOINT1XCH12          |            | PA4  |
|               | APOINT1XCH28          |            |      |
|               | APOINT1XCH30          |            |      |

| Analog Module | Analog Module Channel | Shared Bus | Pin  |
|---------------|-----------------------|------------|------|
| IDAC0         | APOINT1YCH3           | BUSCY      |      |
|               | APOINT1YCH5           |            | PD13 |
|               | APOINT1YCH7           |            | PD15 |
|               | APOINT1YCH9           |            | PA1  |
|               | APOINT1YCH11          |            | PA3  |
|               | APOINT1YCH13          |            | PA5  |
|               | APOINT1YCH27          |            | PB11 |
|               | APOINT1YCH29          |            | PB13 |
|               | APOINT1YCH31          |            |      |

## 9. Package Specifications

### 9.1 ARTIK 030 Dimensions

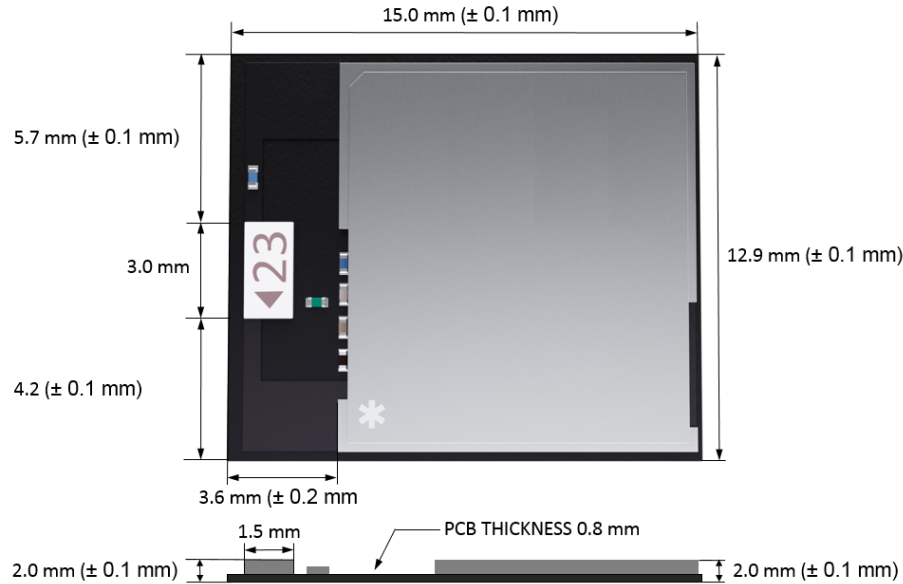


Figure 9.1. ARTIK 030A Package Dimensions

### 9.2 ARTIK 030 Module Footprint

The figure below shows the Module footprint and PCB dimensions.

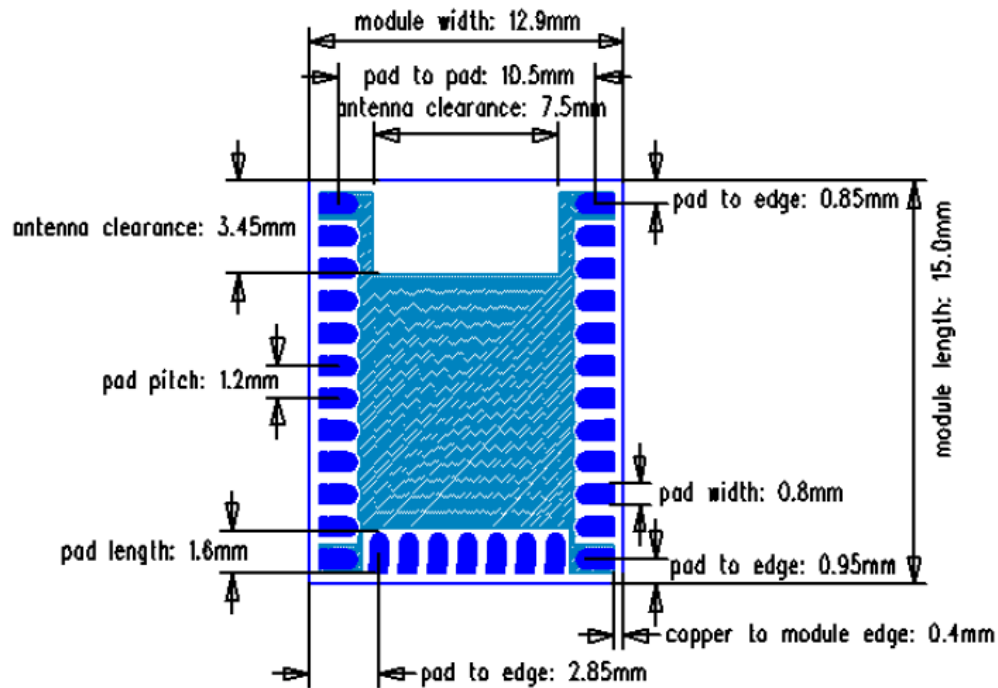


Figure 9.2. ARTIK 030 Footprint

### 9.3 ARTIK 030 Recommended PCB Land Pattern

The figure below shows the recommended land pattern.

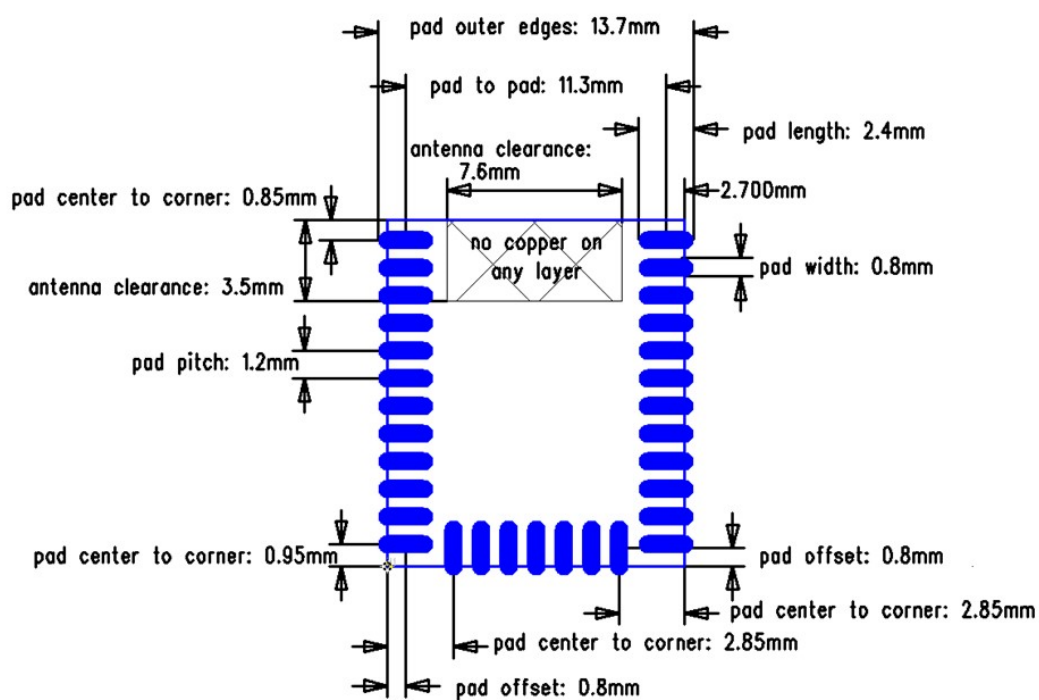


Figure 9.3. ARTIK 030 Recommended PCB Land Pattern

9.4 ARTIK 030 Package Marking

The figure below shows the Module markings printed on the RF-shield.

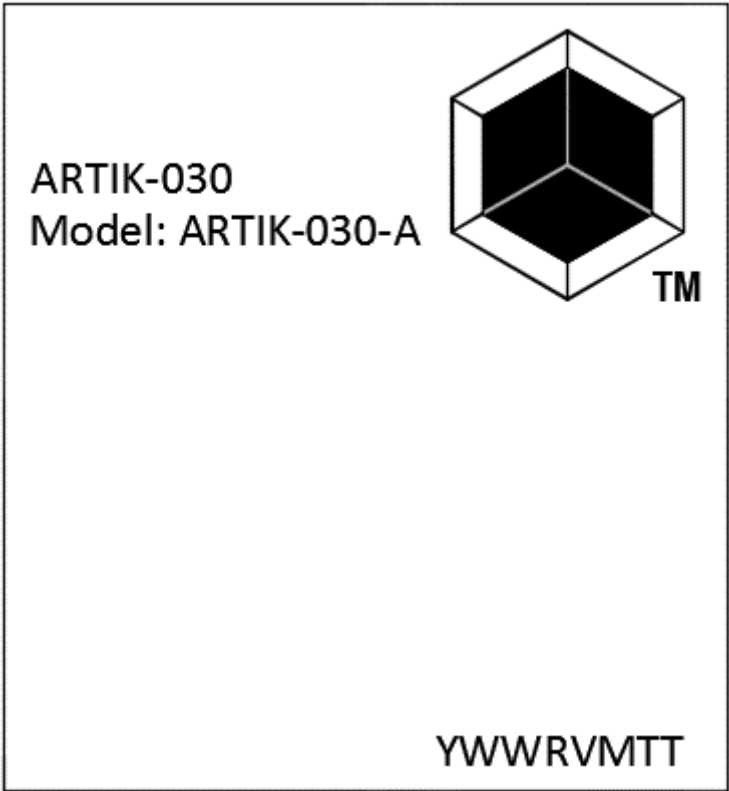


Figure 9.4. ARTIK 030 Package Marking

|                                |                                                |                                                                                      |
|--------------------------------|------------------------------------------------|--------------------------------------------------------------------------------------|
| Mark Method:                   | Laser                                          |                                                                                      |
| Shield Size:<br>X x Y          | 10.75 x 11.70 mm                               |                                                                                      |
| Font Size:                     | 0.70 mm Left-Justified                         |                                                                                      |
| Space between lines :          | 0.40 mm                                        |                                                                                      |
| Distance from edge of package: | 1.00 mm                                        |                                                                                      |
| Line 1                         | Logo(HXW) :<br>4.00 x 3.5mm<br>TM font: 0.45mm |  |
| Line 2 Marking                 | Module Name                                    | ARTIK-030-A-V1                                                                       |
| Line 3 Marking:                | Model Name                                     | Model: ARTIK-030-A                                                                   |

|                        |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Line 4 Marking:</b> | YWWRVMTT | <p>YY -Last digit of Year (e.g.: <b>6</b> for 201<b>6</b>)</p> <p>WW - Work Week (01-53)</p> <p>R - Major Revision (fixed character 1-9, A-Z, assigned by Silicon Labs)</p> <ol style="list-style-type: none"> <li>1. Increment for major changes. Use QS7110-Product Change Action Board as guidance</li> <li>2. Supplier initiated changes reviewed /managed by SLI CAB (W7111F2- Change Matrix for Suppliers)</li> </ol> <p>V - Minor Revision (fixed character 1-9, A-Z, assigned by Silicon Labs)</p> <p>M - Contract Manufacturer Site assigned by Silicon Labs</p> <p>TT - Unique Batch ID assigned by CM (2 characters A-Z)</p> |
|------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

10. Tape and Reel Specifications

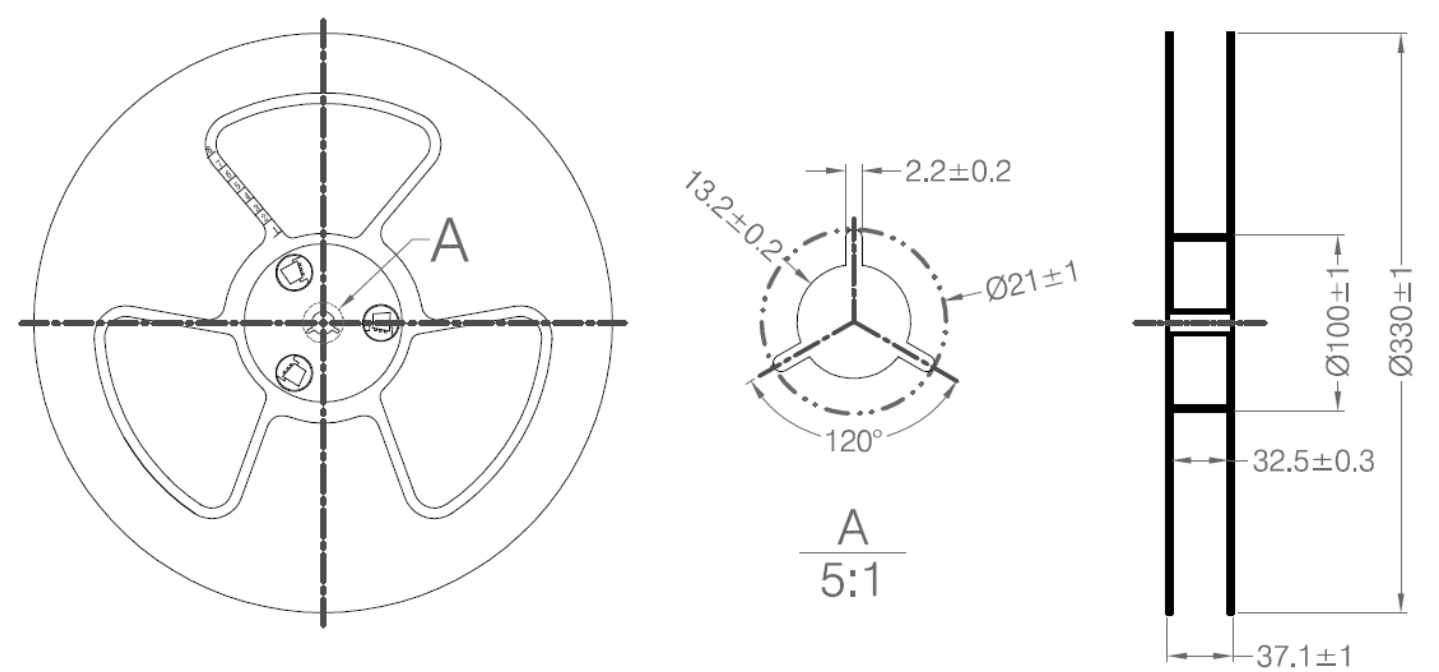
10.1 Tape and Reel Packaging

This section contains information regarding the tape and reel packaging for the ARTIK 030.

10.2 Reel Material and Dimensions

- Reel material: Polystyrene (PS)
- Reel diameter: 13 inches (330 mm)
- Number of modules per reel: 1000 pcs
- Disk deformation, folding whitening and mold imperfections: Not allowed
- Disk set: consists of two 13 inch (330 mm) rotary round disks and one central axis (100 mm)
- Antistatic treatment: Required
- Surface resistivity:  $10^4 - 10^9 \Omega/\text{sq.}$

Figure 10.1. Reel Dimensions - Side View



| Symbol | Dimensions [mm] |
|--------|-----------------|
| W0     | 32.5 ± 0.3      |
| W1     | 37.1 ± 1.0      |

### 10.3 Module Orientation and Tape Feed

The user direction of feed, start and end of tape on reel and orientation of the Modules on the tape are shown in the figures below.

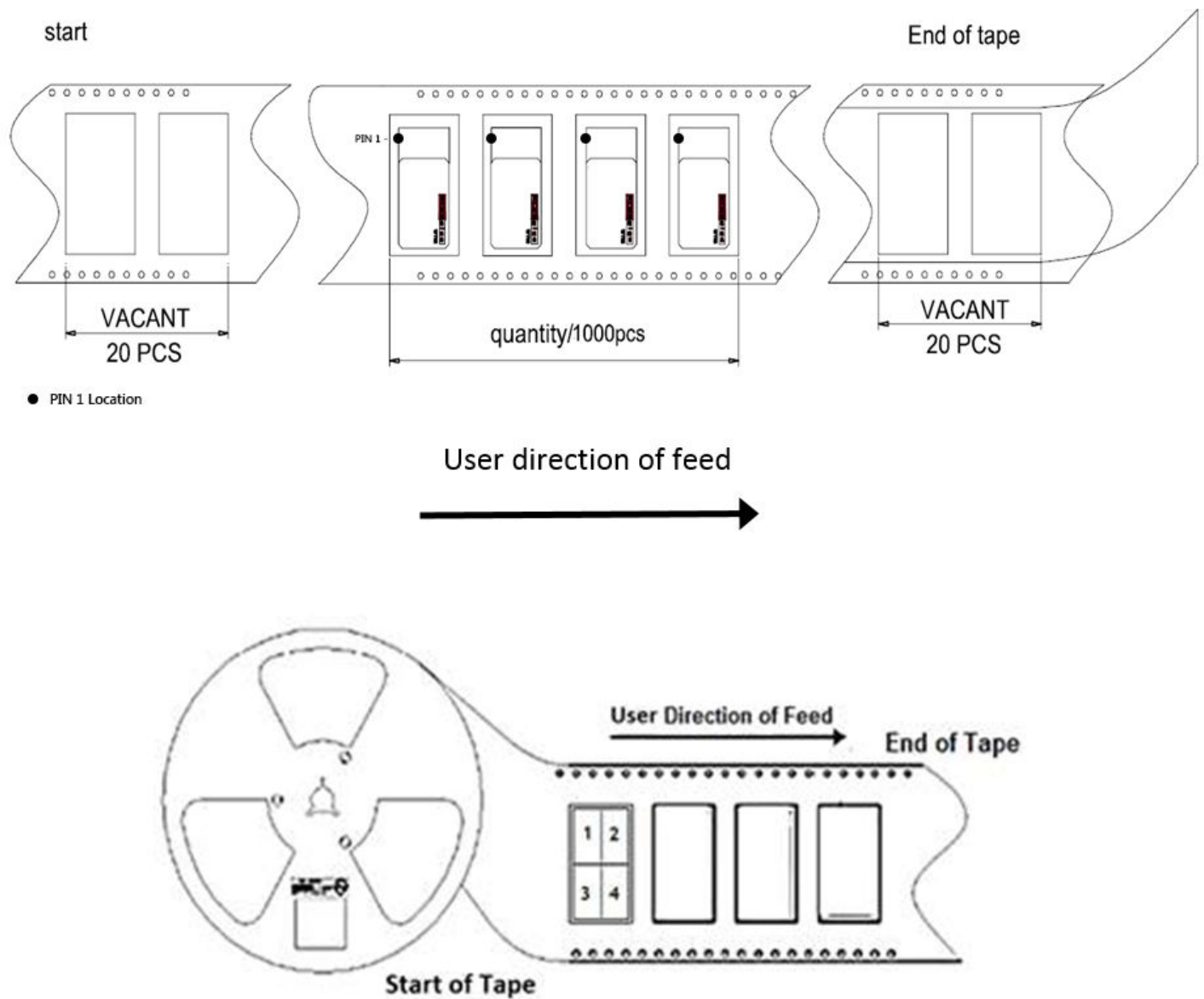
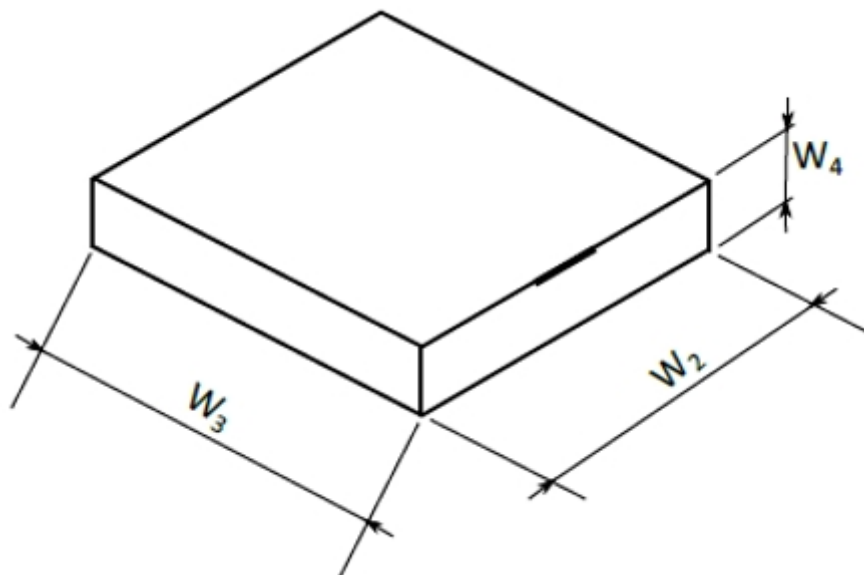


Figure 10.2. Module Orientation and Feed Direction

## 10.4 Tape and Reel Box Dimensions

Figure 10.3. Tape and Reel Box Dimensions



| Symbol | Dimensions [mm] |
|--------|-----------------|
| $W_2$  | 368             |
| $W_3$  | 338             |
| $W_4$  | 72              |

## 10.5 Moisture Sensitivity Level

Reels are delivered in packing which conforms to MSL3 (Moisture Sensitivity Level 3) requirements.

## 11. Certifications

Certifications are ongoing for ARTIK 030. For a complete list of planned certifications and timelines, please contact your sales team.

## 12. Revision History

### 12.1 Revision 0.5

- Initial Publication

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