

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62705CP, TB62705CF, TB62705CFN

8-BIT SHIFT REGISTER, LATCHES & CONSTANT-CURRENT DRIVERS

The TB62705CP / CF / CFN are specifically designed for LED and LED DISPLAY constant-current drivers.

These constant-current output circuits can support the set-up of an external resistor ($I_{OUT} = 5\sim 90\text{mA}$).

This IC is a monolithic integrated circuit designed to be used together with Bi-CMOS process.

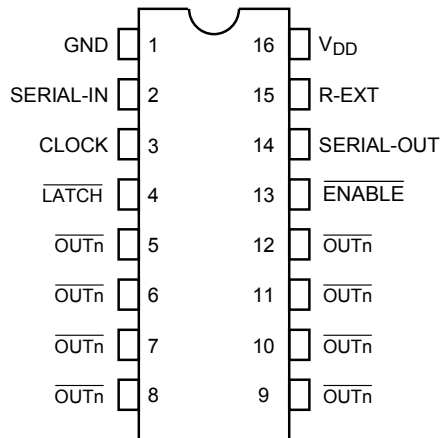
The devices consist of an 8-bit shift register, latch, AND-GATE and constant-current drivers.

FEATURES

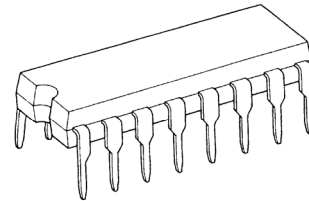
- Constant-current Output : current with one resistor for 5 to 90mA.
- Maximum Clock Frequency : $f_{CLK} = 15 \text{ (MHz)}$
(Cascade Connects Operate, $T_{opr} = 25^\circ\text{C}$)
- 5V C-MOS Compatible Input
- Package : DIP16-P-300-2.54A (TB62705CP)
SSOP16-P-225-1.00A (TB62705CF)
SSOP16-P-225-0.65B (TB62705CFN)
- Constant Output Current Matching:

OUTPUT-GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
$\geq 0.4 \text{ V}$	$\pm 6.0\%$	5~40 mA
$\geq 0.7 \text{ V}$	$\pm 6.0\%$	5~90 mA

PIN CONNECTION (Top view)

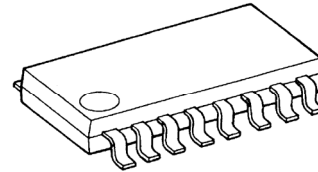


TB62705CP



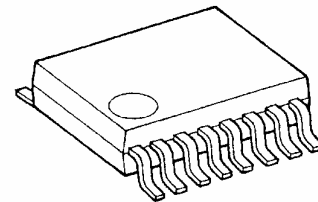
DIP16-P-300-2.54A

TB62705CF



SSOP16-P-225-1.00A

TB62705CFN

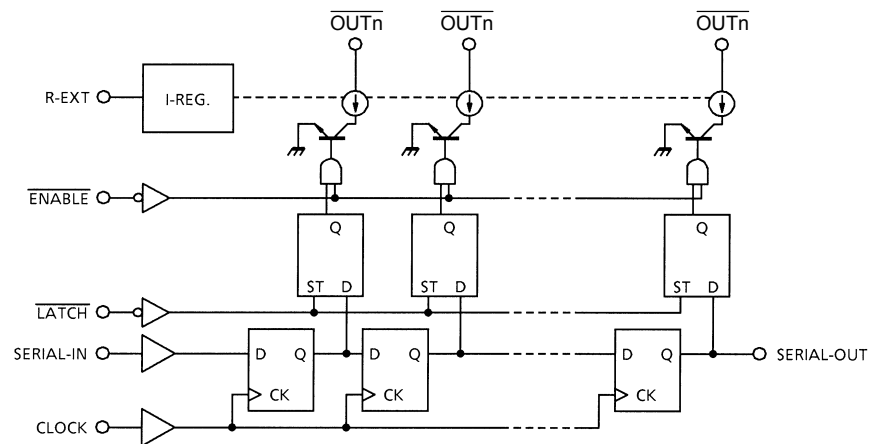


SSOP16-P-225-0.65B

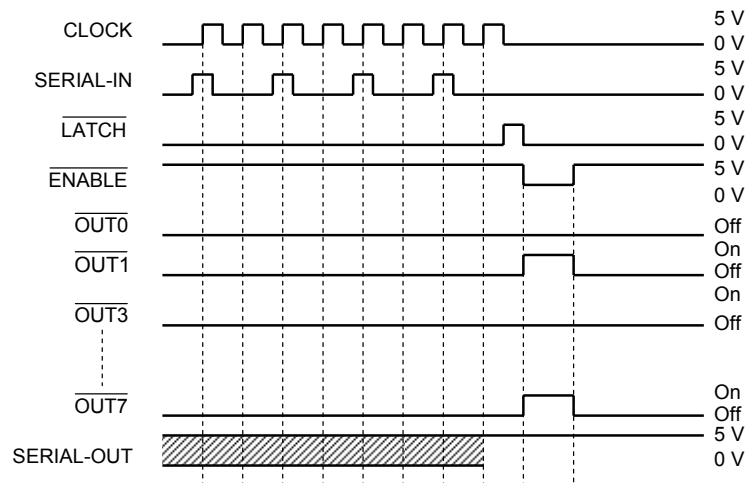
Weight

DIP16-P-300-2.54A: 1.11 g (typ.)
SSOP16-P-225-1.00A: 0.14 g (typ.)
SSOP16-P-225-0.65B: 0.07 g (typ.)

BLOCK DIAGRAM



TIMING DIAGRAM



Note: Latches are level-sensitive, not rising edge-sensitive, and are not synchronized with the CLOCK signal. The data will pass through the latch circuit if the latch input is set at "H" level, and will be retained if the input is set at "L".

PIN DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic
2	SERIAL-IN	Input pin for shift register serial data
3	CLOCK	Clock input terminal for data shift to up-edge.
4	$\overline{\text{LATCH}}$	Data strobe input terminal. Latches pass $\overline{\text{LATCH}}$ data with "H" level input and retain data with "L" level input.
5~12	$\overline{\text{OUTn}}$	Output terminals
13	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ($\overline{\text{OUTn}}$) go off with $\overline{\text{ENABLE}}$ data input at "H" level and go on with data input at "L" level.
14	SERIAL-OUT	Output terminal for serial data for the next SERIAL-IN terminal.
15	R-EXT	Input terminal for connecting a resistor to regulate all output currents.
16	V _{DD}	5-V supply pin of the IC

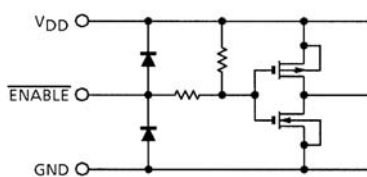
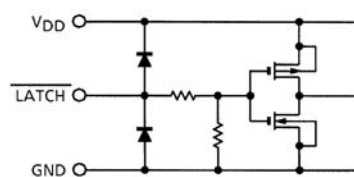
TRUTH TABLE

CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	$\overline{\text{OUTn}}$	SERIAL-OUT
UP	H	L	D _n	D _n ... D _{n-5} ... D _{n-7}	D _{n-7}
UP	L	L	D _{n+1}	No change	D _{n-6}
UP	H	L	D _{n+2}	D _{n+2} ... D _{n-3} ... D _{n-5}	D _{n-5}
DOWN	X	L	D _{n+3}	D _{n+2} ... D _{n-3} ... D _{n-5}	D _{n-5}
DOWN	X	H	D _{n+3}	Off	D _{n-5}

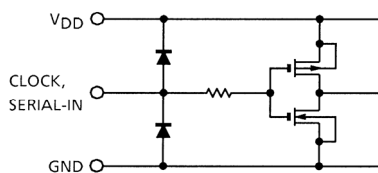
Note: $\overline{\text{OUTn}}$ = on if D_n = H level, and $\overline{\text{OUTn}}$ = off if D_n = L level.

An external resistor is connected with R-EXT and GND. Be sure to administer the correct power supply voltage.

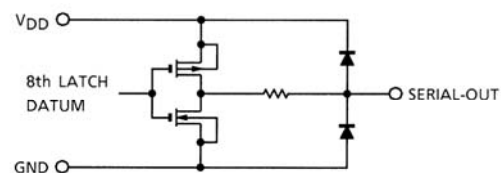
INPUT/OUTPUT EQUIVALENT CIRCUITS

1. $\overline{\text{ENABLE}}$ terminal2. $\overline{\text{LATCH}}$ terminal

3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	0~7.0	V
Input Voltage	V _{IN}	-0.4~V _{DD} + 0.4	V
Output Current	I _{OUT}	90	mA
Output Voltage	V _{CE}	-0.5~17.0	V
Clock Frequency	f _{CK}	15	MHz
GND Terminal Current	I _{GND}	720	mA
Power Dissipation	P _D	1.47 (CP-type : FREE AIR, Ta = 25°C)	W
		0.78 (CF / CFN-type : ON PCB, Ta = 25°C)	
Thermal Resistance	R _{th (j-a)}	85 (CP-type : FREE AIR, Ta = 25°C)	°C / W
		160 (CF / CFN-type : ON PCB, Ta = 25°C)	
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

Note: CP type: For an ambient temperature above 25°C, the derating is 11.8 mW/°C.

CF and CFN type: For an ambient temperature above 25°C, the derating is 6.3 mW/°C.

RECOMMENDED OPERATING CONDITION (Ta = -40~85°C unless otherwise stated)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V _{DD}	—	4.5	5.0	5.5	V
Output Voltage	V _{OUT}	—	—	—	15.0	V
Output Current	I _O	OUTn, DC 1 circuit	5	—	88	mA
	I _{OH}	SERIAL-OUT	—	—	1.0	
	I _{OL}	SERIAL-OUT	—	—	-1.0	
Input Voltage	V _{IH}	—	0.7 V _{DD}	—	V _{DD} +0.3	V
	V _{IL}	—	-0.3	—	0.3 V _{DD}	
LATCH Pulse Width	t _w LAT	V _{DD} = 4.5~5.5 V	100	—	—	ns
CLOCK Pulse Width	t _w CLK		50	—	—	ns
ENABLE Pulse Width	t _w EN		4500	—	—	ns
Set-up Time for DATA	t _{setup} (D)		60	—	—	ns
Hold Time for DATA	t _{hold} (D)		20	—	—	ns
Set-up Time for LATCH	t _{setup} (L)		100	—	—	ns
Hold Time for LATCH	t _{hold} (L)		60	—	—	ns
Clock Frequency	f _{CK}	Cascade operation	10.0	—	—	MHz
Power Dissipation	P _D	Ta = 85°C (CP-type FREE AIR)	—	—	0.82	W
		Ta = 85°C (CF / CFN-type ON PCB)	—	—	0.40	

ELECTRICAL CHARACTERISTICS ($V_{DD} = 5.0 \text{ V}$, $T_a = 25^\circ\text{C}$ unless otherwise stated)

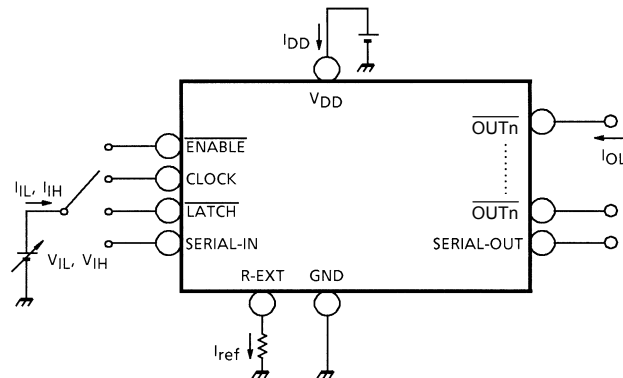
CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	CONDITION		MIN	TYP.	MAX	UNIT
Input Voltage	"H" Level	V _{IH}	—	—		0.7 V _{DD}	—	V _{DD}	V
	"L" Level	V _{IL}	—	—		GND	—	0.3 V _{DD}	
Output Leakage Current		I _{OH}	—	V _{OH} = 15.0 V		—	—	10	μA
Output Voltage	S-OUT	V _{OL}	—	I _{OL} = 1.0 mA		—	—	0.4	V
		V _{OH}	—	I _{OH} = −1.0 mA		4.6	—	—	
Output Current 1		I _{OL1}	—	V _{CE} = 0.7 V	R _{EXT} = 470 Ω (Include skew)	34.1	40.0	45.9	mA
		I _{OL2}	—	V _{CE} = 0.4 V		33.7	39.5	45.3	
	Current Skew	ΔI _{OL1}	—	I _O = 40 mA, V _{CE} = 0.4 V	R _{EXT} = 470 Ω	—	±1.5	±6.0	%
Output Current 2		I _{OL3}	—	V _{CE} = 1.0 V	R _{EXT} = 250 Ω (Include skew)	64.2	75.5	86.8	mA
		I _{OL4}	—	V _{CE} = 0.7 V		63.8	75.0	86.2	
	Current Skew	ΔI _{OL2}	—	I _O = 75 mA, V _{CE} = 0.7 V	R _{EXT} = 250 Ω	—	±1.5	±6.0	%
Supply Voltage Regulation		% / V _{DD}	—	R _{EXT} = 470 Ω, Ta = −40~85°C		—	1.5	5.0	% / V
Pull-Up Resistor		R _{IN} (up)	—	—		150	300	600	Ω
Pull-Down Resistor		R _{IN} (down)	—	—		100	200	400	Ω
Supply Current	"OFF"	I _{DD} (off) 1	—	R _{EXT} = OPEN, $\overline{\text{OUT0}} \sim \overline{7}$ = off		—	0.6	1.2	mA
		I _{DD} (off) 2	—	R _{EXT} = 470 Ω, $\overline{\text{OUT0}} \sim \overline{7}$ = off		3.5	5.8	8.0	
		I _{DD} (off) 3	—	R _{EXT} = 250 Ω, $\overline{\text{OUT0}} \sim \overline{7}$ = off		6.5	10.7	15.0	
	"ON"	I _{DD} (on) 1	—	R _{EXT} = 470 Ω, $\overline{\text{OUT0}} \sim \overline{7}$ = on		7.0	12.0	18.0	
		I _{DD} (on) 2	—	R _{EXT} = 250 Ω, $\overline{\text{OUT0}} \sim \overline{7}$ = on		10.0	22.0	32.0	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise stated)

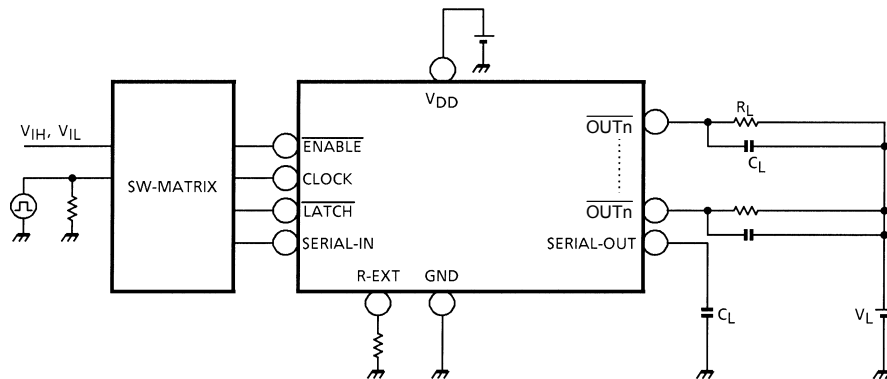
CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time ("L" to "H")	SIN - $\overline{\text{OUTn}}$	t_{pLH}	—	$V_{\text{DD}} = 5.0 \text{ V}$ $V_{\text{CE}} = 0.4 \text{ V}$ $V_{\text{IH}} = V_{\text{DD}}$ $V_{\text{IL}} = \text{GND}$ $R_{\text{EXT}} = 470 \text{ }\Omega$ $I_{\text{OUT}} = 40 \text{ mA}$ $V_{\text{L}} = 3.0 \text{ V}$ $R_{\text{L}} = 65 \text{ }\Omega$ $C_{\text{L}} = 10.5 \text{ pF}$	—	1200	1500	ns
	$\overline{\text{LATCH}} - \overline{\text{OUTn}}$				—	1200	1500	
	$\overline{\text{ENABLE}} - \overline{\text{OUTn}}$				—	1200	1500	
	CLK-SOUT				—	30	70	
Propagation Delay Time ("H" to "L")	SIN - $\overline{\text{OUTn}}$	t_{pHL}	—		—	700	1000	ns
	$\overline{\text{LATCH}} - \overline{\text{OUTn}}$				—	700	1000	
	$\overline{\text{ENABLE}} - \overline{\text{OUTn}}$				—	700	1000	
	CLK-SOUT				—	30	70	
Pulse Width	CK	$t_{\text{w CLK}}$	—		—	20	30	ns
	LATCH	$t_{\text{w LAT}}$	—		—	10	25	
Set-up Time for LATCH	L-H	t_{setup}	—		—	25	50	ns
	H-L				—	25	50	
Hold Time for LATCH	L-H	t_{hold}	—		—	0	30	ns
	H-L				—	0	30	
Maximum CLOCK Rise Time		t_{r}	—		—	—	10	μs
Maximum CLOCK Fall Time		t_{f}	—		—	—	10	μs
Output Rise Time		t_{or}	—	300	600	1000	ns	
Output Fall Time		t_{of}	—	150	300	600	ns	

TEST CIRCUIT

DC characteristics



AC characteristics

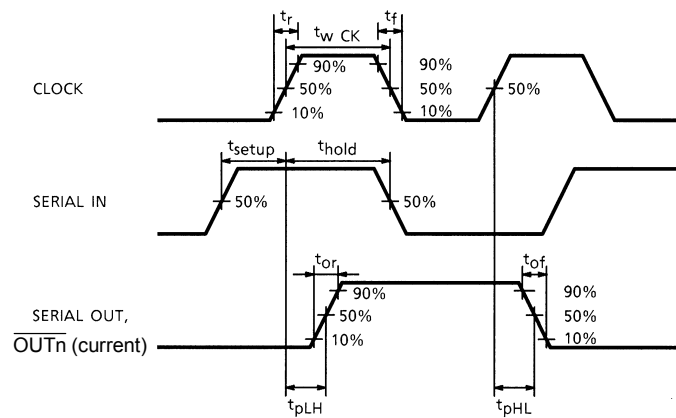


Precaution on Use

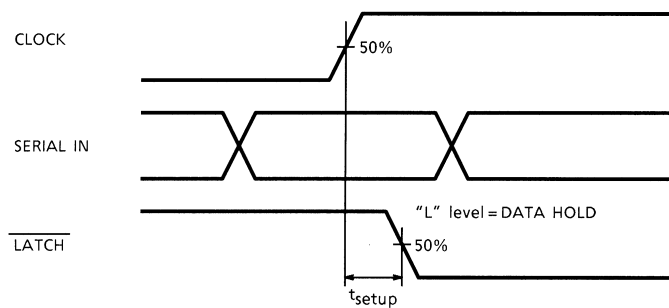
Utmost care is necessary in the design of the output line, VCC (VDD) and GND line since the IC may be damaged due to short-circuits between outputs, air contamination faults, or faults caused by improper grounding.

TIMING WAVEFORM

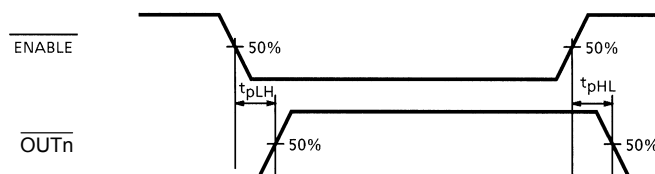
1. CLOCK-SERIAL OUT, $\overline{\text{OUTn}}$

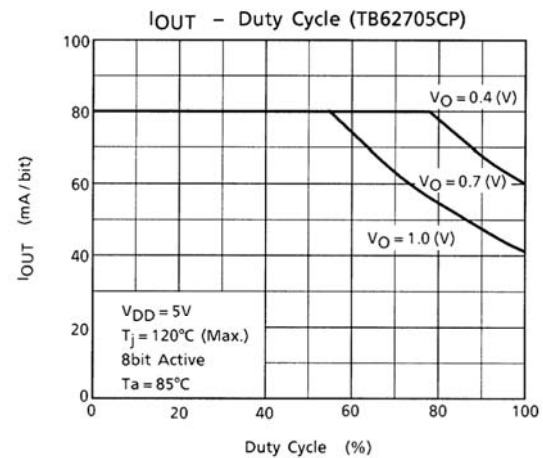
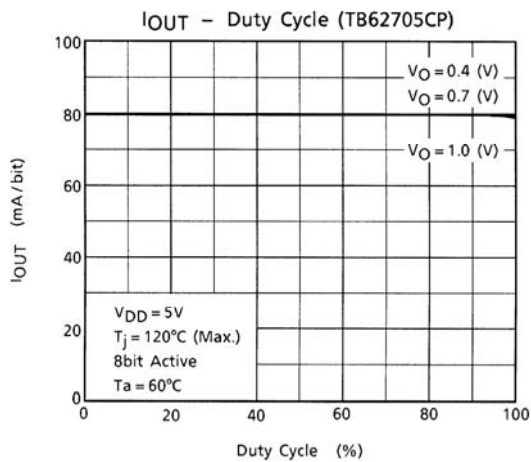
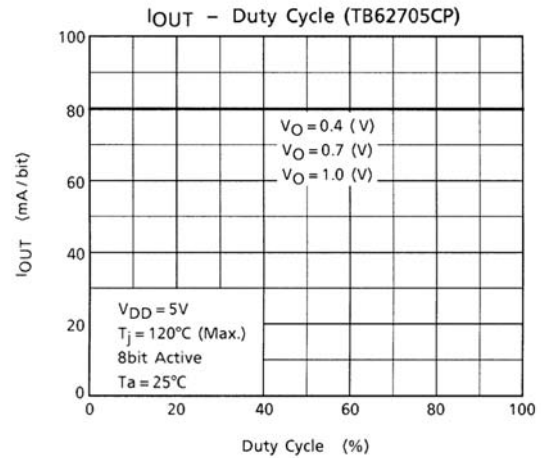
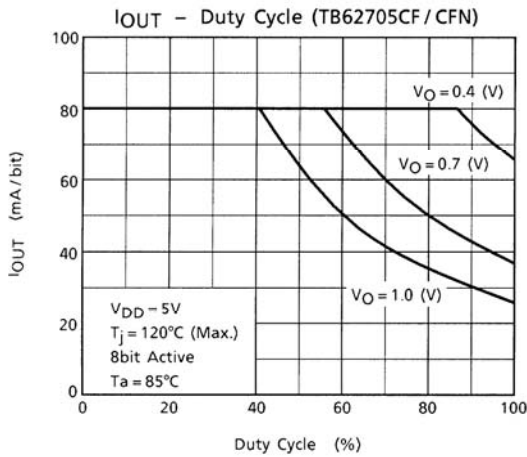
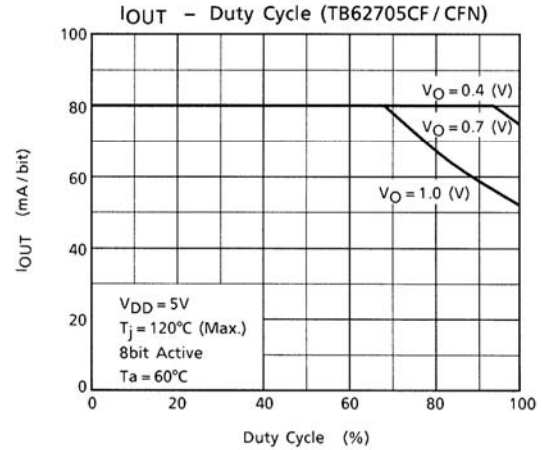
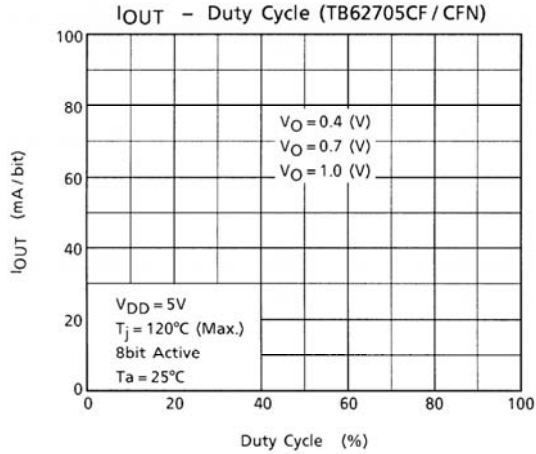


2. CLOCK-LATCH

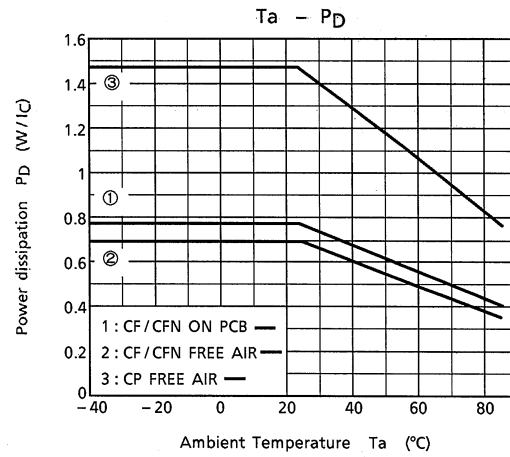
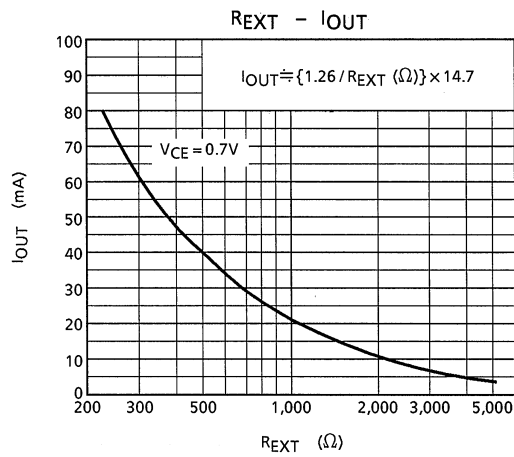


3. ENABLE - $\overline{\text{OUTn}}$





LED DRIVER TB6270X SERIES APPLICATION NOTE



- IO_{UT} is set by the external resistor (R-EXT), as shown in Fig. 1.

- When a higher voltage is input to the device, the excess voltage is consumed inside the device, which leads to power dissipation. To minimize power dissipation and loss, we recommend that the total supply voltage be set as follows:

When the total supply is too high in the light of the power dissipation of this device, an additional resistor (R) can be used to decrease the supply voltage (VO).

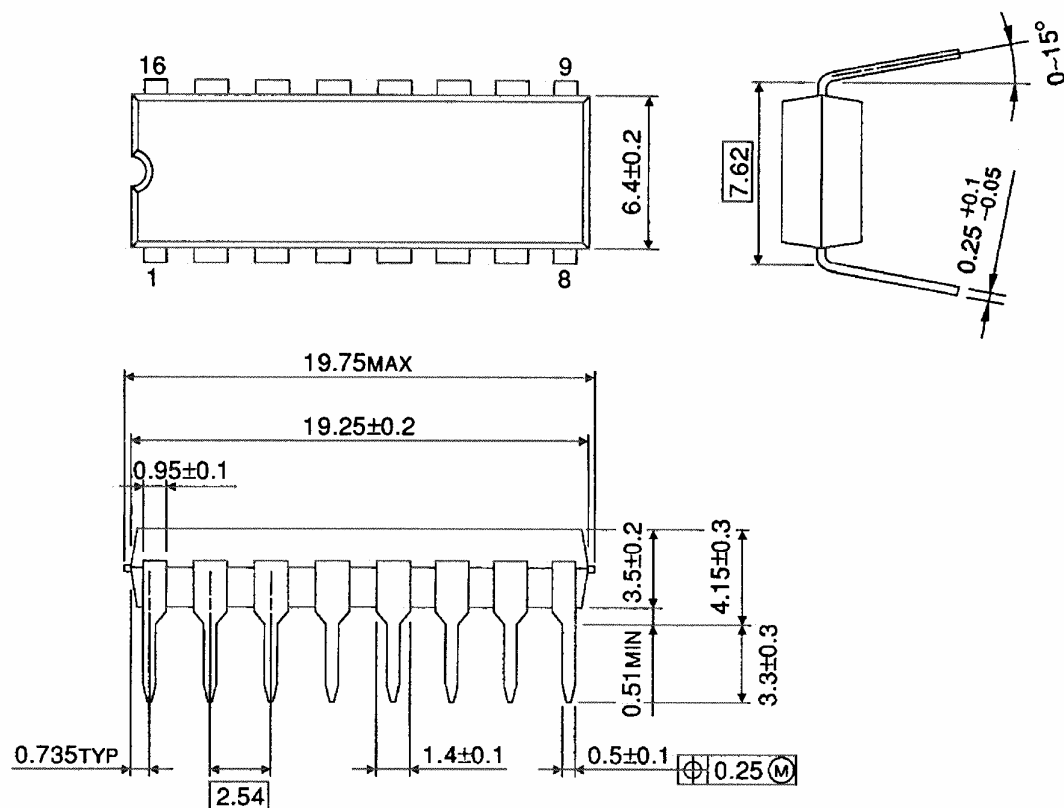
The diagram illustrates a 16-bit parallel LED driver circuit. A CPU is connected to two 8-bit shift registers (labeled '8-BIT SHIFT REGISTER'). The CPU provides a common VDD supply and a SCAN signal. The SCAN signal is connected to the SERIAL-IN of both shift registers. The CPU also provides individual control signals (ENABLE, CLOCK, LATCH) to each shift register. The shift registers are configured with their R-EXT pins to ground and their GND pins to a common ground. The SERIAL-OUT of each shift register is connected to the SERIAL-IN of the other, forming a daisy-chain configuration. The output of each shift register (OUTn) is connected to an LED through a current-limiting resistor R. The LEDs are connected to a common VLED supply, which is specified as 3~4 (V).

- If the ground pattern layout contains a large amount of inductance and impedance, and the voltage between the ground and LATCH or CLOCK terminals exceeds 2.5 V due to switching noise, the device may not operate correctly. Be sure to pay attention to pattern layout to minimize inductance.

PACKAGE DIMENSIONS

DIP16-P-300-2.54A

Unit : mm

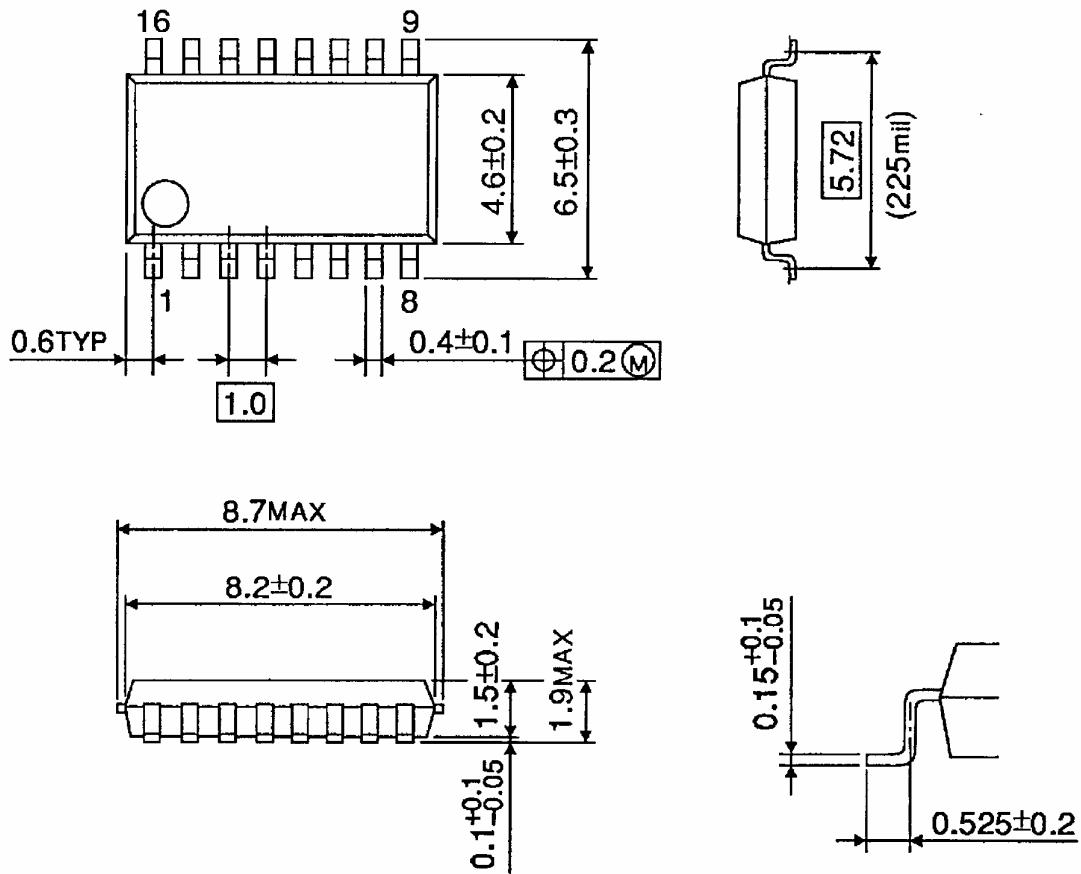


Weight: 1.11 g (Typ.)

PACKAGE DIMENSIONS

SSOP16-P-225-1.00A

Unit : mm

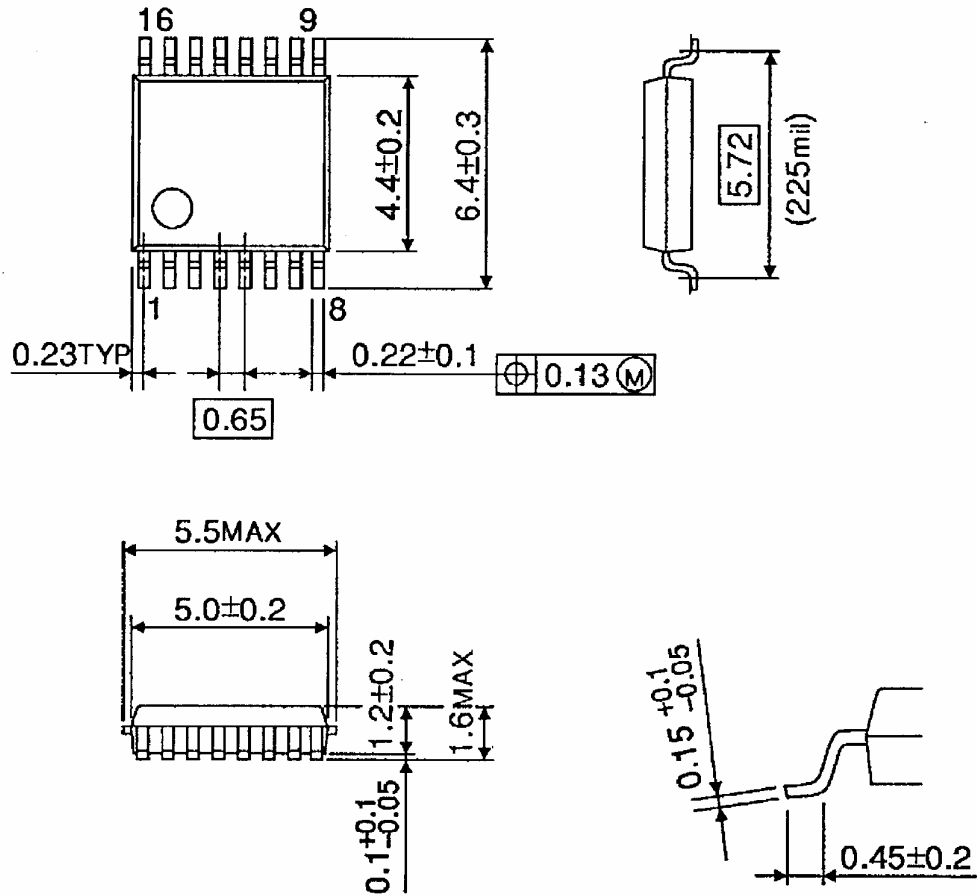


Weight: 0.14 g (Typ.)

PACKAGE DIMENSIONS

SSOP16-P-225-0.65B

Unit : mm



Weight: 0.07 g (Typ.)

Notes on Contents**1. Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.

Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.
- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

- (1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.
- (2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

RESTRICTIONS ON PRODUCT USE

060116EBA

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In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc. 021023_A
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