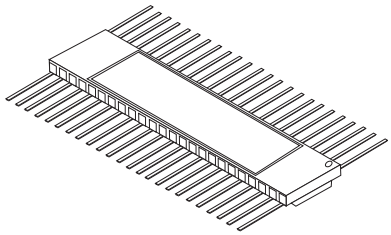
54VCXHR162245

Rad hard low voltage CMOS 16-bit bus buffer transceiver (3-state) with 3.6 V tolerant inputs and outputs

Datasheet - production data



Flat-48

Features

- 1.65 to 3.6 V inputs and outputs
- High speed in both A, B outputs:
  - t_{PD} = 3.4 ns at V_{CC} = 3.0 to 3.6 V
  - t_{PD} = 4.3 ns at V_{CC} = 2.3 to 2.7 V
- Symmetrical impedance outputs:
  - $|I_{OH}| = I_{OL}$ = 12 mA (min.) at V_{CC} = 3.0 V
  - $|I_{OH}| = I_{OL}$ = 8 mA (min.) at V_{CC} = 2.3 V
- Power down protection on inputs and outputs
- 26 Ω series resistors in both A and B port outputs
- Operating voltage range:
  - V_{CC}(opr) = 1.65 V to 3.6 V
- Pin and function compatible with 54 series HR162245
- Bus hold provided on both sides
- Cold spare function
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance:
  - HBM > 2000 V (MIL STD 883 method 3015); MM > 200 V
- 300 krad Mil1019.6 condition A, (RHA QML qualification extension undergone)
- SEL-free and SET-free up to 110 MeV.cm^2/mg
- QML qualified product
- SMD 5962-05213
- 100 mV typical input hysteresis
- Mass:1.50 g

Description

The 54VCXHR162245 is a low voltage CMOS 16-bit bus transceiver (3-state) developed with sub-micron silicon gate and five-layer metal wiring C²MOS technology. It is ideal for low power and very high speed 1.65 to 3.6 V applications; it can be interfaced to 3.6 V signal environment for both inputs and outputs. This IC is intended for two-way asynchronous communication between data buses; the direction of data transmission is determined by DIR input. The two enable inputs $n\overline{G}$ can be used to disable the device so that the buses are effectively isolated. The device circuits include 26 Ω series resistance in the A and B port outputs. These resistors reduce the line noise in high speed applications. Bus hold on data inputs is provided in order to eliminate the need for the external pull-up or pull-down resistor. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2 kV ESD immunity and transient excess voltage. All floating bus terminals during high Z state must be held HIGH or LOW.

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1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

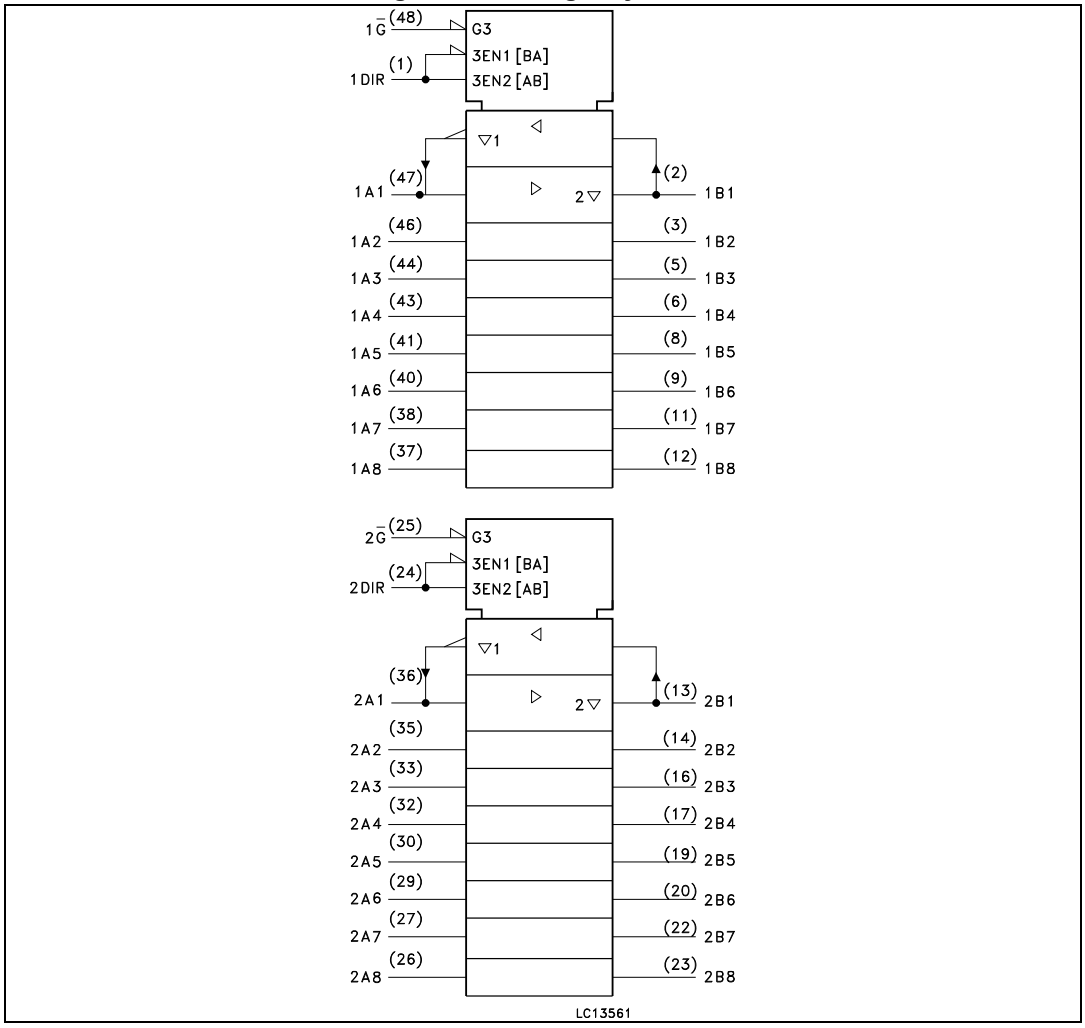
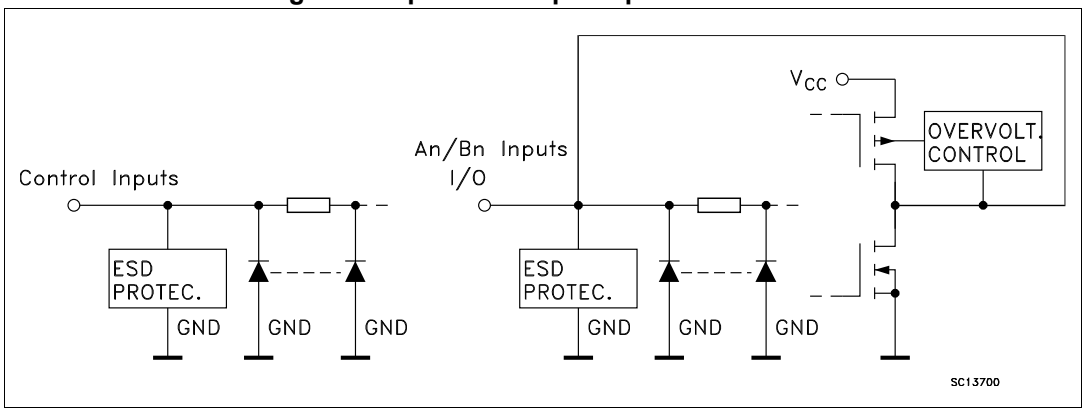


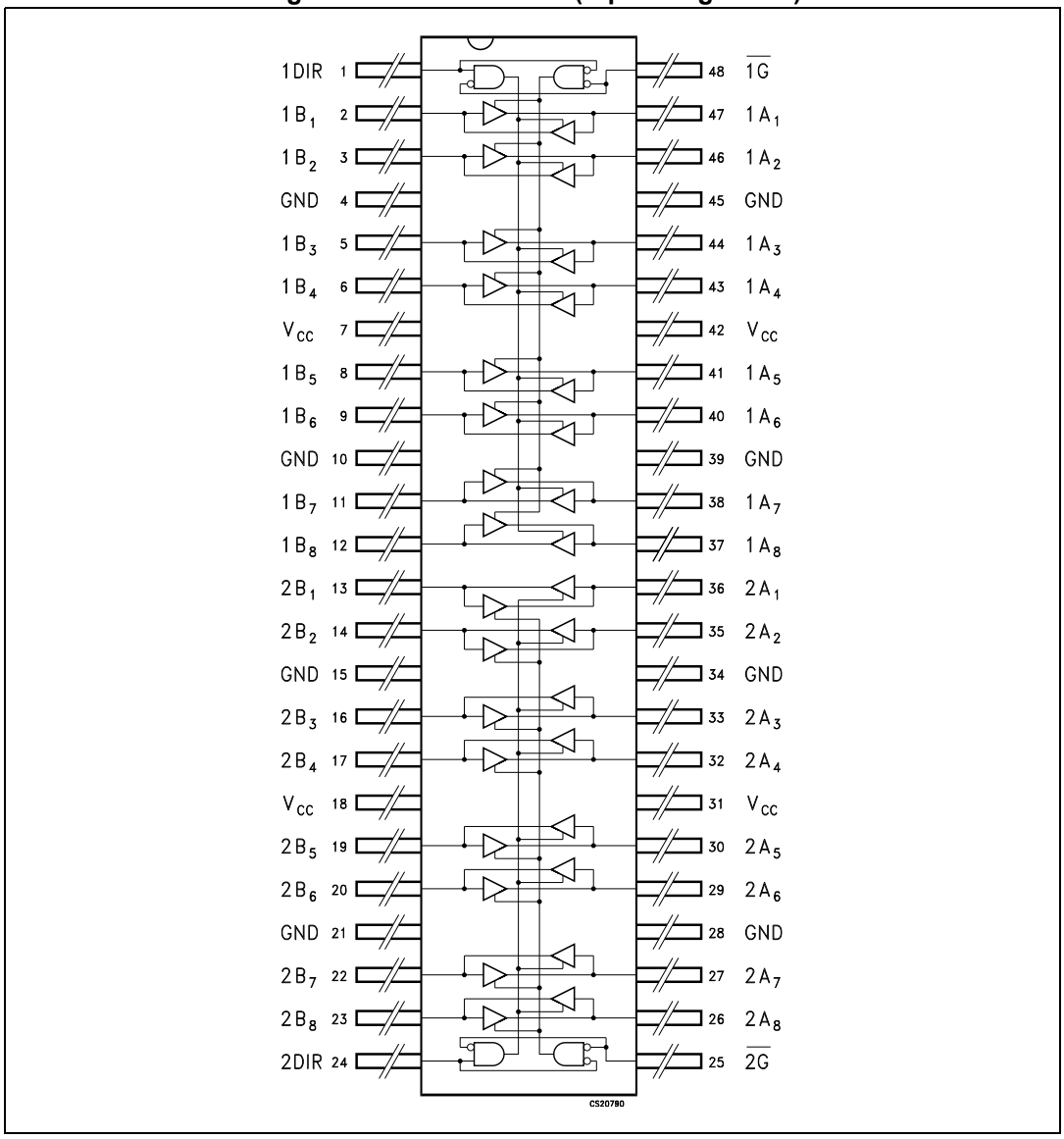
Figure 2. Input and output equivalent circuit



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top through view)



2.2 Pin description

Table 1. Pin description

Pin n°	Symbol	Name and function
1	1DIR	Directional control
2, 3, 5, 6, 8, 9, 11, 12	1B1 to 1B8	Data inputs/outputs
13, 14, 16, 17, 19, 20, 22, 23	2B1 to 2B8	Data inputs/outputs
24	2DIR	Directional control
25	$2\overline{G}$	Output enable input
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 38	1A1 to 1A8	Data inputs/outputs
48	$1\overline{G}$	Output enable input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

2.3 Truth table

Table 2. Truth table

Inputs		Function		Output
$\overline{G}$	DIR	A bus	B bus	Yn
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

Note: X = do not care; Z = high impedance

3 Maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +4.6	V
V_I	DC input voltage	-0.5 to +4.6	V
V_O	DC output voltage (OFF-state)	-0.5 to +4.6	V
V_O	DC output voltage (high or low-state) (1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC input diode current	- 50	mA
I_{OK}	DC output diode current (2)	- 50	mA
I_O	DC output current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current per supply pin	± 100	mA
P_D	Power dissipation	400	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 s)	260	°C

1. I_O absolute maximum ratings must be observed
2. V_O < GND, V_O > V_{CC}

3.1 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.8 to 3.6	V
V_I	Input voltage	-0.3 to 3.6	V
V_O	Output voltage (OFF-state)	0 to 3.6	V
V_O	Output voltage (high or low-state)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or low level output current (V_{CC} = 3.0 to 3.6 V)	± 12	mA
I_{OH}, I_{OL}	High or low level output current (V_{CC} = 2.3 to 2.7 V)	± 8	mA
T_{op}	Operating temperature	-55 to 125	°C
dt/dv	Input rise and fall time (1)	0 to 10	ns/V

1. V_{IN} from 0.8 V to 2 V at V_{CC} = 3.0 V

4 Electrical characteristics

2.7 V < V_{CC} < 3.6 V unless otherwise specified.

Table 5. DC specifications

Symbol	Parameter	Test conditions		Value		Unit
		V_{CC} (V)		-55 to 125 °C		
				Min.	Max.	
V_{IH}	High level input voltage	2.7 to 3.6		2.0		V
V_{IL}	Low level input voltage				0.8	
V_{OH}	High level output voltage	2.7 to 3.6	I_O=-100 µA	V_{CC}-0.2		V
		2.7	I_O=-6 mA	2.2		
		3.0	I_O=-8 mA	2.4		
			I_O=-12 mA	2.2		
V_{OL}	Low level output voltage	2.7 to 3.6	I_O=100 µA		0.2	V
		2.7	I_O=6 mA		0.4	
		3.0	I_O=8 mA		0.55	
			I_O=12 mA		0.8	
I_I	Input leakage current	2.7 to 3.6	V_I = 0 to 3.6 V		± 5	µA
$I_{I(HOLD)}$	Input hold current	3.0	V_I = 0.8 V	75		µA
			V_I = 2 V	-75		
		3.6	V_I = 0 to 3.6 V		± 500	
I_{off}	Power off leakage current	0	V_I or V_O = 0 to 3.6 V		10	µA
I_{OZ}	High impedance output leakage current	2.7 to 3.6	V_I = V_{IH} or V_{IL} V_O = 0 to 3.6 V		± 10	µA
I_{CC}	Quiescent supply current	2.7 to 3.6	V_I = V_{CC} or GND		20	µA
			V_I or V_O = V_{CC} to 3.6 V		± 20	
ΔI_{CC}	I_{CC} incr. per input	2.7 to 3.6	V_{IH} = V_{CC} - 0.6 V		750	µA

2.3 V < V_{CC} < 2.7 V unless otherwise specified.

Table 6. DC specifications

Symbol	Parameter	Test conditions		Value		Unit
		V_{CC} (V)		-55 to 125 °C		
				Min.	Max.	
V_{IH}	High level input voltage	2.3 to 2.7		1.6		V
V_{IL}	Low level input voltage				0.7	
V_{OH}	High level output voltage	2.3 to 2.7	I_O=-100 µA	V_{CC}-0.2		V
		2.3	I_O=-4 mA	2.0		
			I_O=-6 mA	1.8		
			I_O=-8 mA	1.7		
V_{OL}	Low level output voltage	2.3 to 2.7	I_O=100 µA		0.2	V
		2.3	I_O=6 mA		0.4	
			I_O=8 mA		0.6	
I_I	Input leakage current	2.3 to 2.7	V_I = V_{CC} or GND		± 5	µA
$I_{I(HOLD)}$	Input hold current	2.3	V_I = 0.7 V	45		µA
			V_I = 1.7 V	-45		
I_{off}	Power off leakage current	0	V_I or V_O = 0 to 3.6 V		10	µA
I_{OZ}	High impedance output leakage current	2.3 to 2.7	V_I = V_{IH} or V_{IL} V_O = 0 to 3.6 V		± 10	µA
I_{CC}	Quiescent supply current	2.3 to 2.7	V_I = V_{CC} or GND		20	µA
			V_I or V_O = V_{CC} to 3.6 V		± 20	

T_A = 25 °C, Input $t_r = t_f$ = 2.0 ns, C_L = 30 pF, R_L = 500 Ω

Table 7. Dynamic switching characteristics

Symbol	Parameter	Test conditions		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLV}	Dynamic valley low voltage quiet output (1) (2)	2.5	V_{IL} = 0V V_{IH} = V_{CC}	-	0.25	-	V
		3.3		-	0.35	-	
V_{OHV}	Dynamic valley high voltage quiet output (2) (3)	2.5	V_{IL} = 0V V_{IH} = V_{CC}	-	-0.25	-	V
		3.3		-	-0.35	-	
V_{OHV}	Dynamic valley high voltage quiet output (2) (3)	2.5	V_{IL} = 0V V_{IH} = V_{CC}	-	2.05	-	V
		3.3		-	2.65	-	

1. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.
2. Parameters guaranteed by design.
3. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the HIGH state.

C_L = 30 pF, R_L = 500 Ω, Input $t_r = t_f$ = 2.0 ns

Table 8. AC electrical characteristics

Symbol	Parameter	Test conditions	Value		Unit
		V_{CC} (V)	-55 to 125 °C		
			Min.	Max.	
t_{PLH} t_{PHL}	Propagation delay time	2.3 to 2.7	1.0	4.0	ns
		3.0 to 3.6	0.8	3.6	
t_{PLH} t_{PHL}	Propagation delay time	2.3 to 2.7	1.0	4.9	ns
		3.0 to 3.6	0.8	4.0	
t_{PZL} t_{PZH}	Output enable time	2.3 to 2.7	1.0	5.8	ns
		3.0 to 3.6	0.8	4.3	
t_{PZL} t_{PZH}	Output enable time	2.3 to 2.7	1.0	6.8	ns
		3.0 to 3.6	0.8	4.8	
t_{PLZ} t_{PHZ}	Output disable time	2.3 to 2.7	1.0	4.8	ns
		3.0 to 3.6	0.8	5.6	
t_{PLZ} t_{PHZ}	Output disable time	2.3 to 2.7	1.0	5.7	ns
		3.0 to 3.6	0.8	7.0	
t_{OSLH} t_{OSHL}	Output to output skew time (1) (2)	2.3 to 2.7		0.5	ns
		3.0 to 3.6		0.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} - t_{PLHn}|, t_{OSHL} = | t_{PHLm} - t_{PHLn}|)
2. Parameter guaranteed by design

Table 9. Capacitive characteristics

Symbol	Parameter	Test conditions		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input capacitance	2.5 or 3.3	V_{IN} = 0 or V_{CC}	-	4	-	pF
C_{OUT}	Output capacitance	2.5 or 3.3	V_{IN} = 0 or V_{CC}	-	8	-	pF
C_{PD}	Power dissipation capacitance (1)	2.5 or 3.3	f_{IN} = 10 MHz V_{IN} = 0 or V_{CC}	-	28	-	pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)}$ = C_{PD} x V_{CC} x f_{IN} + I_{CC}/16 (per circuit)

5 Test circuit

Figure 4. Test circuit

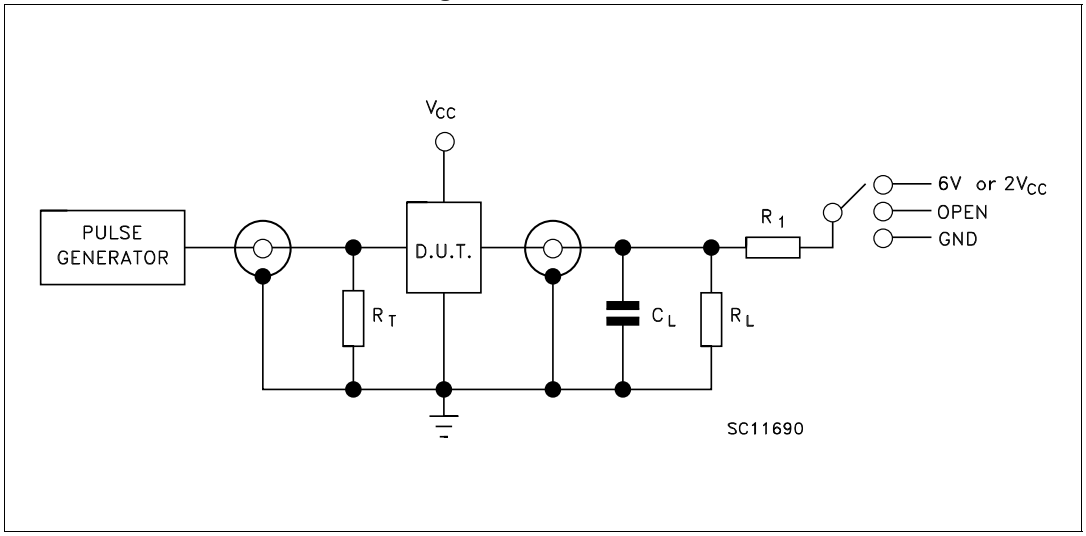


Table 10. Test circuit

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ} (V_{CC} = 3.0 to 3.6 V)	6 V
t_{PZL}, t_{PLZ} (V_{CC} = 2.3 to 2.7 V)	2 V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 30 pF or equivalent (includes jig and probe capacitance)

R_L = R_1 = 500 Ω or equivalent

R_T = Z_{OUT} of pulse generator (typically 50 Ω)

6 Waveforms

Table 11. Waveform symbol value

Symbol	V_{CC}	
	3.0 to 3.6 V	2.3 to 2.7 V
V_{IH}	2.7 V	V_{CC}
V_M	1.5 V	$V_{CC}/2$
V_X	V_{OL} +0.3 V	V_{OL} +0.15 V
V_Y	V_{OH} -0.3 V	V_{OH} -0.15 V

Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)

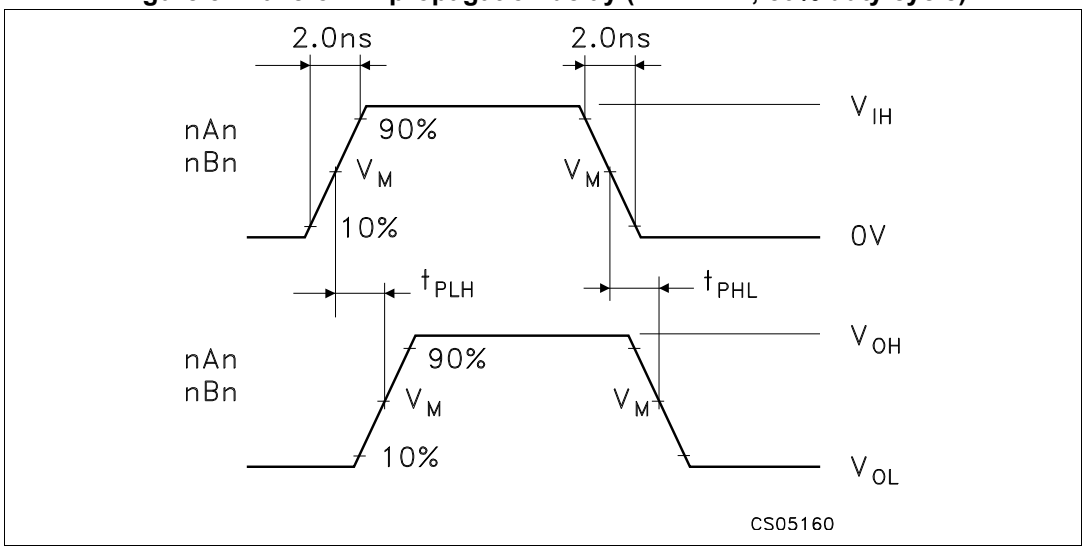
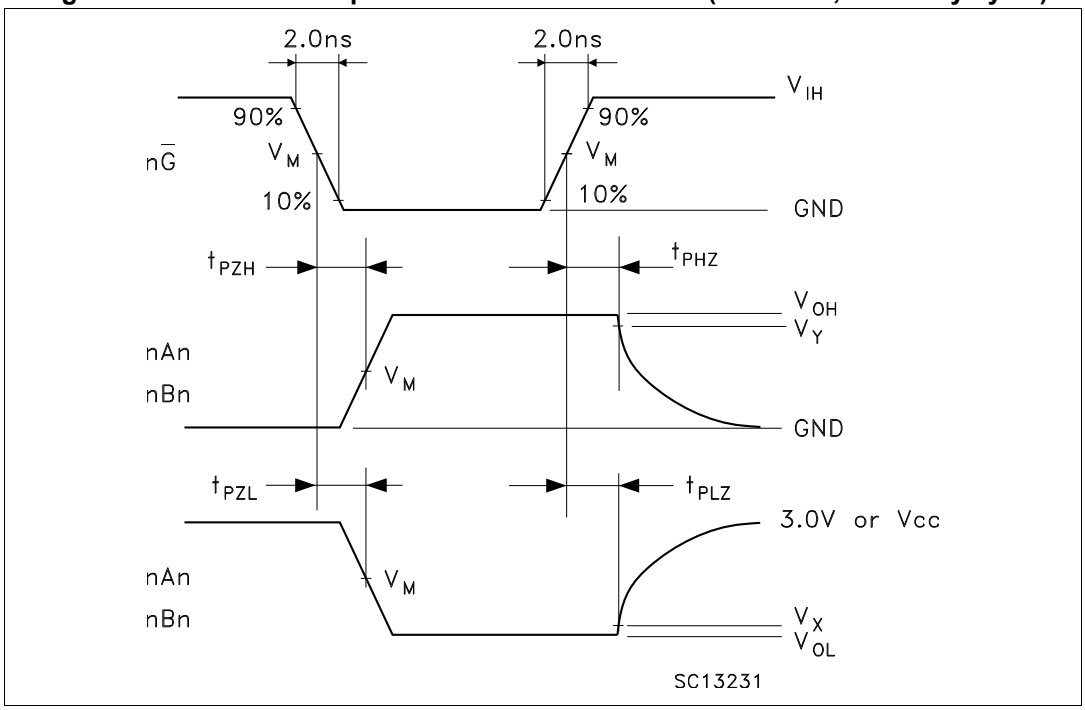


Figure 6. Waveform - output enable and disable time (f = 1 MHz; 50% duty cycle)



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 7. Flat-48 (MIL-STD-1835) package outline

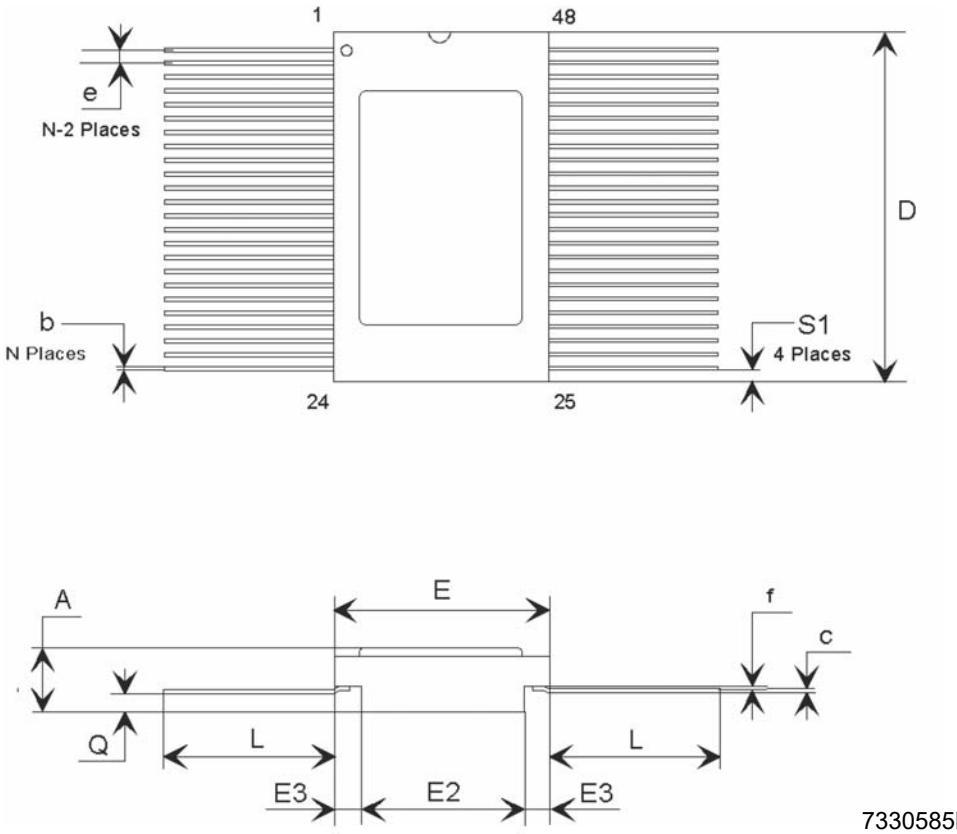


Table 12. Flat-48 (MIL-STD-1835) mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	6.85	8.38	9.40	0.270	0.330	0.370
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

8 Order codes

Table 13. Ordering information

Order code	SMD[1]	Quality level	Package	Marking[2]	Finish.	Pack.
RHRXHR162245K1		Eng. model	Flat-48	RHRXHR162245K1	Gold	Strip pack
RHFXHR162245K03V	5962F0521302VXC	QML-V flight		5962F0521302VXC		
RHFXHR162245K05V	5962F0521302VYC		Flat-48 with grounded lid	5962F0521302VYC		

1. Standard microcircuit drawing
2. Specific marking only. Complete marking includes the following:

-ST logo

-Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)

-Country of origin (FR=France)

Other information

Date code:

The date code is structured as engineering model: EM xyywwz

where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 14. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID
QML-V flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

9 Revision history

Table 15. Document revision history

Date	Revision	Changes
09-Jul-2004	1	First release
17-May-2005	2	SMD qualified
19-Jun-2006	3	300 Krad bullet updated, new template, mechanical data updated
11-Apr-2007	4	Updated cover page features
30-Jul-2007	5	Typo in *Table 12 on page 16*
17-Sep-2008	6	Updated cover page
08-Sep-2009	7	Updated *Table 13 on page 17*
02-Aug-2011	8	Added *Note: on page 16* and in the "Pin connections" diagram on the cover page
18-Nov-2019	9	Updated cover page and *Table 13: Ordering information*. Added *Table 14*.