

# VR13/13.HC Digital Multiphase Controller with PMBus®

## FD3501

### Description

The FD3501 is a high performance 8 phase digital buck controller which can be configured for single or dual rail output rails. It is fully compatible with Intel® SVID protocol. It is designed to power Intel's VR13 and VR13.HC processor rails, DDR memory DIMM banks and high current low voltage digital loads. All of the required parameters are programmable through the PMBus interface.

The FD3501 device uses onsemi's proprietary Advanced COT architecture to implement control and power management functions with maximum flexibility, performance and minimal controller and overall solution size. The Advanced COT control features extremely low latency against severe load transients and easily permits a high switching frequency design with ceramic only output capacitors. Non-Volatile OTP Memory is included to store multiple custom configurations. It also achieves the best platform efficiency by implementing fast-to-change dynamic phase management and a variable frequency light load control.

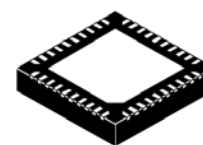
The FD3501 device is designed to be used with onsemi's smart power stage 3 and 4 (SPS3 and SPS4) generations of parts which accurately integrate inductor current sensing and temperature monitoring.

### Features

- VR13 and VR13.HC Compliant with 25 MHz SVID Bus
- Phase and Rail Configurability is  $M + N \leq 8$ .  $M \geq 1$  and  $N \leq 4$ 
  - ♦ M: Number of Phases for Rail 1
  - ♦ N: Number of Phases for Rail 2
- PMBus 1.2 Configuration and Monitoring
- Programmable Switching Frequency 400 kHz to 1.5 MHz
- User Programmable Droop, and Internal Compensation
- Auto Phase Shedding
- Pulse Skipping
- Fault Management
- Extensive and Accurate Telemetry
- Pre-Bias Soft Startup with Soft-Stop Support

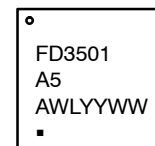
### Applications

- High-Current Voltage Regulator for VR13 and VR13.HC Based Intel's Microprocessors
- DDR Memory Voltage Regulator in Intel's VR13 and VR13.HC Based Systems
- Multiphase Voltage Regulators in Servers, Data Networking and Telecommunications Equipment



QFN40 5x5, 0.4P  
CASE 485FW

### MARKING DIAGRAM



|        |                        |
|--------|------------------------|
| FD3501 | = Specific Device Code |
| A5     | = Revision             |
| A      | = Assembly Location    |
| WL     | = Wafer Lot            |
| YY     | = Year                 |
| WW     | = Work Week            |
| ■      | = Pb-Free Package      |

### ORDERING INFORMATION

| Device      | Package             | Shipping†             |
|-------------|---------------------|-----------------------|
| FD3501MNTXG | QFN40L<br>(Pb-Free) | 2500 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# FD3501

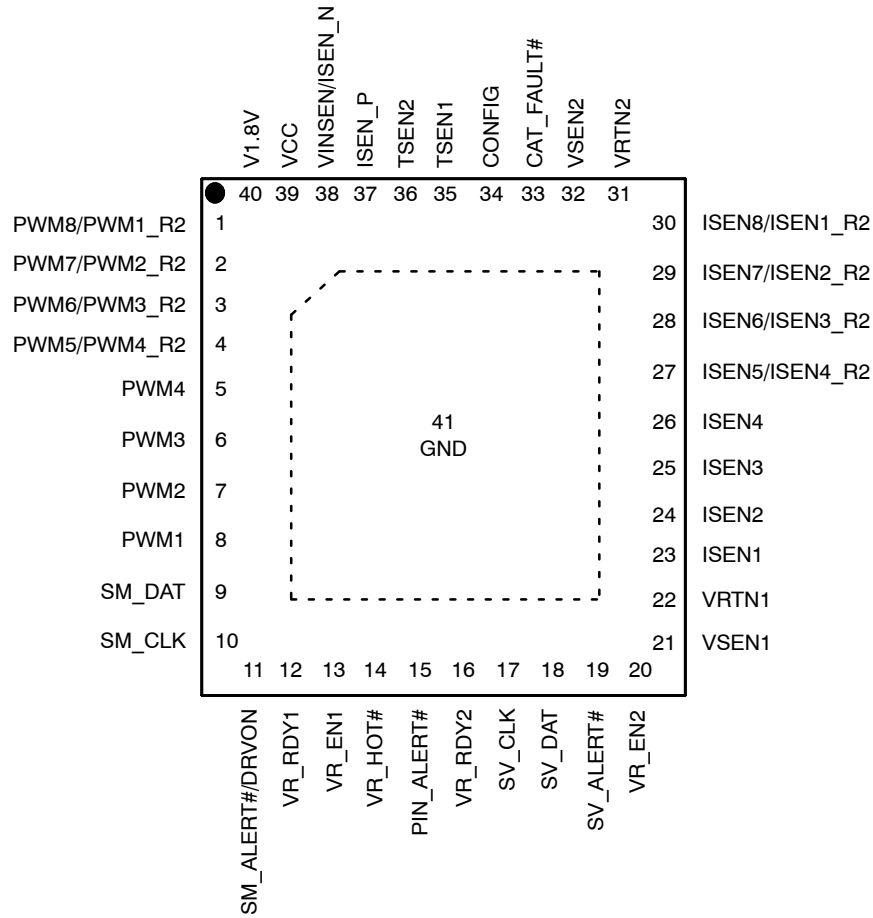


**Figure 1. Pin Configuration**

**Table 1. PIN LIST**

| Pin No. | Symbol              | Description                                                                                                                                                                                                                     |
|---------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | PWM8/PWM1_R2        | PWM output signal for Rail 1 Phase 8 or Rail 2 Phase 1. Tri-state output signal                                                                                                                                                 |
| 2       | PWM7/PWM2_R2        | PWM output signal for Rail 1 Phase 7 or Rail 2 Phase 2. Tri-state output signal                                                                                                                                                 |
| 3       | PWM6/PWM3_R2        | PWM output signal for Rail 1 Phase 6 or Rail 2 Phase 3. Tri-state output signal                                                                                                                                                 |
| 4       | PWM5/PWM4_R2        | PWM output signal for Rail 1 Phase 5 or Rail 2 Phase 4. Tri-state output signal                                                                                                                                                 |
| 5       | PWM4                | PWM output signal for Rail 1 Phase 4. Tri-state output signal                                                                                                                                                                   |
| 6       | PWM3                | PWM output signal for Rail 1 Phase 3. Tri-state output signal                                                                                                                                                                   |
| 7       | PWM2                | PWM output signal for Rail 1 Phase 2. Tri-state output signal                                                                                                                                                                   |
| 8       | PWM1                | PWM output signal for Rail 1 Phase 1. Tri-state output signal                                                                                                                                                                   |
| 9       | SM_DAT              | PMBus data pin. Open drain connection and a pull up resistor is required                                                                                                                                                        |
| 10      | SM_CLK              | PMBus clock pin. Open drain connection and a pull up resistor is required                                                                                                                                                       |
| 11      | SM_ALERT#/<br>DRVON | SM_ALERT# output is used to signal PMBus host that the chipset needs attention. Open drain connection and a pull up resistor is required. DRVON pin output can also be used to enable gate drivers for DrMOS. (User selectable) |
| 12      | VR_RDY1             | Rail 1 output "Ready" indicator. Open drain connection and a pull up resistor is required. VR_RDY1 will be pulled low if a shutdown fault occurs                                                                                |
| 13      | VR_EN1              | Enable pin for Rail 1 output. Polarity is user programmable.                                                                                                                                                                    |

Table 1. PIN LIST (continued)

| Pin No. | Symbol         | Description                                                                                                                                                                                                                                                                                                                                                                                    |
|---------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14      | VR_HOT#        | Active Low indicates that TSEN1 or TSEN2 is over set threshold. Open drain connection and a pull up resistor is required                                                                                                                                                                                                                                                                       |
| 15      | PIN_ALERT#     | Active Low indicates that input power over limit is triggered. Open drain connection and a pull up resistor is required                                                                                                                                                                                                                                                                        |
| 16      | VR_RDY2        | Rail 2 output "Ready" indicator. Open drain connection and a pull up resistor is required. VR_RDY2 will be pulled low if a shutdown fault occurs                                                                                                                                                                                                                                               |
| 17      | SV_CLK         | SV Bus clock pin. Open drain connection and a pull up resistor is required                                                                                                                                                                                                                                                                                                                     |
| 18      | SV_DAT         | SV Bus data pin. Open drain connection and a pull up resistor is required                                                                                                                                                                                                                                                                                                                      |
| 19      | SV_ALERT#      | Output used to signal SVID Bus host that the chipset needs attention. Open drain connection and a pull up resistor is required                                                                                                                                                                                                                                                                 |
| 20      | VR_EN2         | This pin serves as the enable signal for Rail 2 output. Polarity is user programmable. If unused, it is recommended to be set to GND                                                                                                                                                                                                                                                           |
| 21      | VSEN1          | Positive input of the remote voltage sense of Rail 1                                                                                                                                                                                                                                                                                                                                           |
| 22      | VRTN1          | Negative input of the remote voltage sense of Rail 1                                                                                                                                                                                                                                                                                                                                           |
| 23      | ISEN1          | Current sense input for Rail 1 phase 1                                                                                                                                                                                                                                                                                                                                                         |
| 24      | ISEN2          | Current sense input for Rail 1 phase 2                                                                                                                                                                                                                                                                                                                                                         |
| 25      | ISEN3          | Current sense input for Rail 1 phase 3                                                                                                                                                                                                                                                                                                                                                         |
| 26      | ISEN4          | Current sense input for Rail 1 phase 4                                                                                                                                                                                                                                                                                                                                                         |
| 27      | ISEN5/ISEN4_R2 | Current sense input for Rail 1 phase 5 or Rail 2 phase 4                                                                                                                                                                                                                                                                                                                                       |
| 28      | ISEN6/ISEN3_R2 | Current sense input for Rail 1 phase 6 or Rail 2 phase 3                                                                                                                                                                                                                                                                                                                                       |
| 29      | ISEN7/ISEN2_R2 | Current sense input for Rail 1 phase 7 or Rail 2 phase 2                                                                                                                                                                                                                                                                                                                                       |
| 30      | ISEN8/ISEN1_R2 | Current sense input for Rail 1 phase 8 or Rail 2 phase 1                                                                                                                                                                                                                                                                                                                                       |
| 31      | VRTN2          | Negative remote sense pin for Rail 2. If unused, leave it as N/C                                                                                                                                                                                                                                                                                                                               |
| 32      | VSEN2          | Positive remote sense pin for Rail 2. If unused, leave it as N/C                                                                                                                                                                                                                                                                                                                               |
| 33      | CAT_FAULT#     | Catastrophe Fault indicator pin. This pin is de-asserted LOW to indicate a catastrophic fault is detected, such as component's failure in the regulator power train (reported on TSEN1/2 asserted HIGH), or an OVP condition                                                                                                                                                                   |
| 34      | CONFIG         | Resistor-to-Code configuration pin. Connect this pin to GND through a resistor, according to Table 8. Resistor's value selects the OTP stored user configuration table. If no user configuration is present in OTP, then the resistor's value only selects the IC PMBus address                                                                                                                |
| 35      | TSEN1          | Temperature monitoring pin for Rail 1. TMON pins of all phases operating in Rail 1 are to be OR-wired to TSEN1 pin. TSEN1 also monitors the phases' reported faults (TSEN1 forced HIGH)                                                                                                                                                                                                        |
| 36      | TSEN2          | It is the temperature and fault monitor pin for Rail 2. This operates the same as the TSEN1 pin (refer to TSEN1 pin description and connection requirements)                                                                                                                                                                                                                                   |
| 37      | ISEN_P         | It operates as an input current sensing pin (together with pin#38 ISEN_N) connected to the positive node of the sensing device (e.g. shunt resistor)                                                                                                                                                                                                                                           |
| 38      | VINSEN/ISEN_N  | Multi-function pin. Functionality is OTP configured by user.<br>In VINSEN configuration, it allows the FD3501 for input voltage sensing for input voltage feed-forward control and for input voltage monitoring.<br>In ISEN_N configuration, it operates as input current sensing pin (together with pin#37 ISEN_P) connected to the negative node of the sensing device (e.g. shunt resistor) |
| 39      | VCC            | 3.3 V input power supply pin. Bypass to GND with 1 $\mu$ F capacitor                                                                                                                                                                                                                                                                                                                           |
| 40      | V1.8V          | Internal 1.8 V LDO output pin for bypassing to GND. Connect to GND through 1 $\mu$ F capacitor                                                                                                                                                                                                                                                                                                 |
| 41      | GND            | Package exposed pad for analog ground. Connect to Ground planes with multi-vias                                                                                                                                                                                                                                                                                                                |

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Description                                             | PIN Names                                                                            | Min  | Max | Unit |
|---------------------------------------------------------|--------------------------------------------------------------------------------------|------|-----|------|
| Input Voltage Range<br>(referenced to PGND)             | VINSEN/ISEN_N, ISEN_P                                                                | –0.3 | 25  | V    |
|                                                         | ISEN1~ISEN8, SM_DAT, SM_CLK, CONFIG, VCC, VR_EN1, VR_EN2, VSEN1, VSEN2, TSEN1, TSEN2 | –0.3 | 3.7 | V    |
|                                                         | SV_CLK, SV_DAT                                                                       | –0.3 | 3.7 | V    |
|                                                         | AGND, VRTN1, VRTN2                                                                   | –0.3 | 0.3 | V    |
| Output Voltage Range<br>(referenced to PGND<br>or AGND) | PWM1~PWM8, VR_HOT#, PIN_ALERT#, SM_ALERT#, VR_RDY1, VR_RDY2, CAT_FAULT#, SV_ALERT#   | –0.3 | 3.7 | V    |
|                                                         | V1.8V                                                                                | –0.3 | 2.0 | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. RECOMMENDED OPERATING CONDITIONS**

| Symbol         | Parameter                | Min   | Typ | Max   | Unit |
|----------------|--------------------------|-------|-----|-------|------|
| VCC            | Supply Voltage           | 3.135 | 3.3 | 3.465 | V    |
| VINSEN, ISEN_P | Input Power Sensor, 12 V | 10    | 12  | 15    | V    |
| VID (Max.)     | Programmed               | –     | –   | 3.04  | V    |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. THERMAL DATA**

| Symbol            | Parameter                                                                 | Min | Max | Unit |
|-------------------|---------------------------------------------------------------------------|-----|-----|------|
| R <sub>THJA</sub> | Thermal Resistance Junction-to-Ambient (Device Soldered on 2s2p PC Board) | –   | 30  | °C/W |
| T <sub>STG</sub>  | Storage Temperature Range                                                 | –40 | 150 | °C   |
| T <sub>A</sub>    | Operating Ambient Temperature Range                                       | –40 | 125 | °C   |
| T <sub>J</sub>    | Operating Junction Temperature Range                                      | –40 | 125 | °C   |

**Table 5. ENVIRONMENTAL QUALIFICATIONS**

|                                       |                                                |      |      |   |
|---------------------------------------|------------------------------------------------|------|------|---|
| Electrostatic<br>Discharge Protection | Machine Model: Class A (JESD22–A115A)          | –    | 200  | V |
|                                       | Human Body Model: Class 1C (JESD22–A114F)      | 1000 | 2000 | V |
|                                       | Charged Device Model: Class III (JESD22–C101D) | 500  | 1000 | V |
| Moisture Sensitivity                  | JEDEC Level 1 at 260°C                         | –    | –    |   |
| RoHS Compliant                        | YES                                            | –    | –    |   |

# FD3501

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ ,  $3.135\text{ V} < V_{CC} < 3.465\text{ V}$ ,  $T_{amb} = 0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ )

| Symbol                     | Parameter                                        | Condition                                                                       | Min  | Typ  | Max  | Unit          |
|----------------------------|--------------------------------------------------|---------------------------------------------------------------------------------|------|------|------|---------------|
| <b>VCC UVLO</b>            |                                                  |                                                                                 |      |      |      |               |
| $I_{VCC\_SW}$              | Supply Current at Normal Operation               | ENABLE = High, $f_s = 600\text{ kHz}$ , No PMBus or SVID activity               | –    | 55   | –    | mA            |
| $V_{CCON}$                 | UVLO Turn-On                                     | VCC Voltage Rising                                                              | 2.55 | 2.75 | 2.95 | V             |
| $V_{CCOFF\_HYS}$           | UVLO Turn-Off-Hys                                | VCC Voltage Hyst                                                                | –    | 115  | –    | mV            |
| <b>V1.8V REGULATOR</b>     |                                                  |                                                                                 |      |      |      |               |
| $V_{1.8V}$                 | Internal LDO Output Voltage                      | $I_{load} = 0\text{ mA}$                                                        | –    | 1.8  | –    | V             |
| $I_{V1.8V}$                | Internal LDO Sourcing Current Capability         | $V_{OL} = V_{1.8V} - 50\text{ mV}$                                              | –    | 50   | –    | mA            |
| $V1P8\_DUVLOH$             | V1P8 UVLO threshold                              |                                                                                 | 1.3  | 1.4  | 1.5  | V             |
| $V1P8\_Hyst$               | UVLO Hysteresis                                  |                                                                                 | –    | 100  | –    | mV            |
| <b>VR_EN1</b>              |                                                  |                                                                                 |      |      |      |               |
| $EN_H$                     | Input High Voltage                               | Voltage Rising                                                                  | –    | –    | 0.7  | V             |
| $EN_L$                     | Input Low Voltage                                | Voltage Falling                                                                 | 0.6  | –    | –    | V             |
| $I_{EN}$                   | Leakage Current                                  | $VR\_EN1 = 0\text{ V}$                                                          | –1   | –    | 1    | $\mu\text{A}$ |
| <b>VR_EN2</b>              |                                                  |                                                                                 |      |      |      |               |
| $EN_H$                     | Input High Voltage                               | Voltage Rising                                                                  | –    | –    | 0.7  | V             |
| $EN_L$                     | Input Low Voltage                                | Voltage Falling                                                                 | 0.6  | –    | –    | V             |
| $I_{EN}$                   | Leakage Current                                  | $VR\_EN2 = 0\text{ V}$                                                          | –1   | –    | 1    | $\mu\text{A}$ |
| <b>CAT_FAULT#</b>          |                                                  |                                                                                 |      |      |      |               |
| $R_{CAT\_FAULT\#}$         | Low Output Impedance                             | Sink current is 4 mA                                                            | –    | –    | 13   | $\Omega$      |
| $I_{CAT\_FAULT\#}$         | Leakage Current                                  | 3.3 V pull up                                                                   | –1   | –    | 1    | $\mu\text{A}$ |
| $C_{PAD}$                  | Pad Capacitance                                  | CPAD includes die capacitance only. No package parasitics are included.         | –    | –    | 4    | pF            |
| <b>VR_RDY1 AND VR_RDY2</b> |                                                  |                                                                                 |      |      |      |               |
| $V_{OL}$                   | Output Low Voltage                               | Sinking 4 mA<br>Starts pulling down as VCC is rising above $V_{th}$ of the NMOS | 0    | –    | 0.3  | V             |
| $V_{OH}$                   | Output High Leakage                              | Pull up to 3.3 V                                                                | 0    | –    | 1    | $\mu\text{A}$ |
| $T_{EN-OFF-DLY}$           | From $VR\_ENx$ low to $VR\_RDY$ low              |                                                                                 | –    | –    | 0.5  | $\mu\text{s}$ |
| <b>ISENSx</b>              |                                                  |                                                                                 |      |      |      |               |
| $ISENS_{V\_BIAS}$          |                                                  |                                                                                 | –    | 1.8  | –    | V             |
| <b>OSCILLATOR</b>          |                                                  |                                                                                 |      |      |      |               |
| $F_{SW}$                   | Switching Frequency                              | 16 options (< 800 kHz, 50 kHz per step, > 800 kHz, 100 kHz per step)            | 400  | –    | 1500 | kHz           |
| $F_{SW\_ACC\_ALL}$         | $F_{SW}$ Accuracy at Entire Operation Conditions |                                                                                 | –10  | –    | 10   | %             |

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ ,  $3.135\text{ V} < V_{CC} < 3.465\text{ V}$ ,  $T_{amb} = 0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ) (continued)

| Symbol                                                                          | Parameter                      | Condition                                             | Min | Typ | Max | Unit          |
|---------------------------------------------------------------------------------|--------------------------------|-------------------------------------------------------|-----|-----|-----|---------------|
| <b>VOUT REMOTE SENSE DIFFERENTIAL SUMMING AMPLIFIER (FOR BOTH RAIL 1 AND 2)</b> |                                |                                                       |     |     |     |               |
| $I_{SEN1,2}$                                                                    | VSEN1,2 Pin Bias Current       | $V_{SEN1,2} = 3\text{ V}$ , $V_{RTN1,2} = 0\text{ V}$ | –   | –   | 500 | $\mu\text{A}$ |
| $I_{RTN1,2}$                                                                    | VRTN1,2 Pin Bias Current       |                                                       | –   | –   | 500 | $\mu\text{A}$ |
| $\text{Gain}_{DIFF}$                                                            | Gain of Differential Amplifier | 15 options programmable                               | 2   | –   | 16  |               |

**OUTPUT VOLTAGE SETTING, TRIMMING AND CALIBRATION**

|                |                                                     |                         |                                               |      |      |       |
|----------------|-----------------------------------------------------|-------------------------|-----------------------------------------------|------|------|-------|
| $V_{VID-STEP}$ | VID Step Size                                       | ID register (05h) = 07h | –                                             | 5    | –    | mV    |
|                |                                                     | ID register (05h) = 04h | –                                             | 10   | –    | mV    |
| $V_{VID}$      | VID Programming Range                               | ID register (05h) = 07h | 0                                             | –    | 1.52 | V     |
|                |                                                     | ID register (05h) = 04h | 0                                             | –    | 3.04 | V     |
| $V_{VID\_ERR}$ | VID DC Set Point Tolerance ( $25^{\circ}\text{C}$ ) | ID register (05h) = 07h | $V_{VID} \geq 1\text{ V}$                     | –0.5 | –    | 0.5 % |
|                |                                                     |                         | $V_{VID} = 0.8\text{ V} \sim 0.995\text{ V}$  | –5   | –    | 5 mV  |
|                |                                                     |                         | $V_{VID} = 0.25\text{ V} \sim 0.795\text{ V}$ | –8   | –    | 8 mV  |
|                |                                                     | ID register (05h) = 04h | $V_{VID} \geq 1.5\text{ V}$                   | –0.5 | –    | 0.5 % |
|                |                                                     |                         | $V_{VID} = 1.0\text{ V} \sim 1.49\text{ V}$   | –8   | –    | 8 mV  |
|                |                                                     |                         | $V_{VID} = 0.5\text{ V} \sim 0.99\text{ V}$   | –10  | –    | 10 mV |

**OUTPUT VOLTAGE SLEW RATE SELECTION (DAC CHANGING RATE)**

|              |                                                            |                                                                                    |      |                  |     |                   |
|--------------|------------------------------------------------------------|------------------------------------------------------------------------------------|------|------------------|-----|-------------------|
| $SR_{SET}$   | PMBus Command Set Vout Changing Slew Rate                  | $V_{OUT\_TRANSITION\_RATE}$ set 8 options, 5 mV/ $\mu\text{s}$ resolution          | 10   | 25               | 45  | mV/ $\mu\text{s}$ |
| $SR1_{FAST}$ | Rail 1 VID Slew Rate Fast                                  |                                                                                    | –    | $SR_{SET}$       | –   | mV/ $\mu\text{s}$ |
| $SR1_{SLOW}$ | Rail 1 VID Slew Rate Slow                                  | 4 options: 1/2, 1/4, 1/8, 1/16                                                     | 1/16 | –                | 1/2 | $SR1_{FAST}$      |
| $SR2_{FAST}$ | Rail 2 VID Slew Rate Fast (PMBus Manufacturer Command Set) | Option 1                                                                           | –    | $SR_{SET}$       | –   | mV/ $\mu\text{s}$ |
|              |                                                            | Option 2 (default)                                                                 | –    | $SR_{SET} / 2$   | –   | mV/ $\mu\text{s}$ |
| $SR2_{SLOW}$ | Rail 2 VID Slew Rate Slow                                  | 4 options: 1/2, 1/4, 1/8, 1/16                                                     | 1/16 | –                | 1/2 | $SR2_{FAST}$      |
| $SR1_{SS}$   | Rail 1 VID Slew Rate for Soft Start up                     | It can use $SR1_{SLOW}$ for it. This is an option if we need slower soft start up. | –    | $SR1_{SLOW}$     | –   | mV/ $\mu\text{s}$ |
|              |                                                            |                                                                                    | –    | $SR1_{SLOW} / 4$ | –   | mV/ $\mu\text{s}$ |
| $SR2_{SS}$   | Rail 2 VID Slew Rate for Soft Start up                     | It can use $SR2_{SLOW}$ for it. This is an option if we need slower soft start up. | –    | $SR2_{SLOW}$     | –   | mV/ $\mu\text{s}$ |
|              |                                                            |                                                                                    | –    | $SR2_{SLOW} / 4$ | –   | mV/ $\mu\text{s}$ |

**IIN HIGH SIDE CURRENT SENSE**

|                         |                                    |                         |      |      |      |               |
|-------------------------|------------------------------------|-------------------------|------|------|------|---------------|
| $V_{COM}$               | Common Input Voltage               |                         | 10   | 12   | 15   | V             |
| $V_{DIF}$               | Maximum Differential Input Voltage |                         | 0    | –    | 25   | mV            |
| Analog Gain Settings    |                                    |                         | 23.5 | 24.3 | 25.2 | V/V           |
| $I_{IN\_SEN\_ERR}$      | Digital IIN Error                  | at $25^{\circ}\text{C}$ | –2   | –    | 2    | LSB           |
| $I_{SEN\_SAMPLE\_RATE}$ |                                    |                         | –    | 10   | –    | kHz           |
| $I_{VINSEN}$            | VINSEN pin bias current            | $V_{IN} = 12\text{ V}$  | –    | –    | 20   | $\mu\text{A}$ |
| $I_{IINSEN}$            | IINSENS pin bias current           | $V_{IN} = 12\text{ V}$  | –    | –    | 200  | $\mu\text{A}$ |

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ ,  $3.135\text{ V} < V_{CC} < 3.465\text{ V}$ ,  $T_{amb} = 0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ) (continued)

| Symbol                                      | Parameter                                                  | Condition                                                       | Min                             | Typ                               | Max                             | Unit          |
|---------------------------------------------|------------------------------------------------------------|-----------------------------------------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------|
| <b>TOTAL OUTPUT CURRENT SENSE (IOUT)</b>    |                                                            |                                                                 |                                 |                                   |                                 |               |
| $I_{SEN\_SAMPLE\_RATE}$                     |                                                            |                                                                 | –                               | 20                                |                                 | kHz           |
| $I_{SEN\_ANTIALISING\_FILTER}$              | Filter Pole Frequency                                      |                                                                 | –                               | 4                                 | –                               | kHz           |
| $I_{SEN\_GAIN\_A}$                          | Total IOUT Gain                                            | 8 phase, IMON total current = $800\text{ }\mu\text{A}$          | –                               | 1.625                             | –                               | mV/A          |
| $I_{SEN\_GAIN\_A\_ERR}$                     | Total IMON Gain Error                                      | 8 phase, IMON total current = $800\text{ }\mu\text{A}$          | –2                              | –                                 | 2                               | %             |
| $I_{SEN\_GAIN\_A\_OFF}$                     | Total IMON Offset                                          | 8 phase, IMON total current = $0\text{ }\mu\text{A}$ , Gain = 1 | –1                              | –                                 | 1                               | LSB           |
| $I_{SEN\_ANALOG\_GAIN\_SETTINGS}$           | Analog Gain Settings                                       |                                                                 | –<br>–<br>–<br>–<br>–<br>–<br>– | 1<br>2<br>4<br>6<br>8<br>16<br>32 | –<br>–<br>–<br>–<br>–<br>–<br>– |               |
| <b>RDROOP</b>                               |                                                            |                                                                 |                                 |                                   |                                 |               |
| $R_{DROOP\_STEP\_SIZE}$                     | Load Line Programmability Resolution                       | 5 mV VID DAC step<br>10 mV VID DAC step                         | –<br>–                          | 20.313<br>40.625                  | –<br>–                          | $\mu\Omega$   |
| $R_{DROOP\_RANGE}$                          | Load Line Impedance                                        | 5 mV VID DAC step<br>10 mV VID DAC step                         | 0<br>0                          | –<br>–                            | 2.011<br>4.022                  | m $\Omega$    |
| $R_{DROOP\_GAIN\_ERROR}$                    | Rdroop Error                                               | Rdroop > $0.5\text{ m}\Omega$                                   | –2                              | –                                 | 2                               | %             |
| <b>PWM [1:8] OUTPUTS</b>                    |                                                            |                                                                 |                                 |                                   |                                 |               |
| $V_{OL-PWM}$                                | Output Low Voltage                                         | $I_{PWM-SINK} = 1\text{ mA}$                                    | –                               | 0.05                              | 0.2                             | V             |
| $V_{OH-PWM}$                                | Output High Voltage                                        | $I_{PWM-SOURCE} = -1\text{ mA}$                                 | $V_{CC}-0.2$                    | $V_{CC}-0.05$                     | –                               | V             |
| $V_{OM-PWM}$                                | Output Middle Voltage                                      | $I_{PWM-SOURCE} = -1\text{ mA}$                                 | 1.5                             | 1.6                               | 1.7                             | V             |
| $T_{RISE}$                                  | PWM Rising Time from Low to High                           | $C = 10\text{ pF}$                                              | –                               | –                                 | 10                              | ns            |
| $T_{FALL}$                                  | PWM Falling Time from High to Low                          | $C = 10\text{ pF}$                                              | –                               | –                                 | 10                              | ns            |
| $I_{LK-PWM}$                                | PWM Leakage Current                                        | $V_{CC} < UVLO$ , or PHASE not used                             | –1                              | –                                 | 1                               | $\mu\text{A}$ |
| <b>ZCD DETECTOR</b>                         |                                                            |                                                                 |                                 |                                   |                                 |               |
| $ZCD_{SETTINGS}$                            | Threshold Range                                            | Sense feedback $5\text{ }\mu\text{A/A}$<br>4 steps              | 0.5                             | –                                 | 2                               | A             |
| $ZCD_{TOL}$                                 | Threshold Tolerance                                        | $5\text{ }\mu\text{A/A}$ on the sense inputs                    | –1.3                            | –                                 | 1.3                             | A             |
| <b>INPUT UNDER VOLTAGE PROTECTION (UVP)</b> |                                                            |                                                                 |                                 |                                   |                                 |               |
| $V_{INSENS_{ON}}$                           | Minimum Input Voltage ( $V_{INSEN}$ ) to Make IC Switching | 3 options                                                       | –                               | 4.5<br>6.5<br>8.5                 | –                               | V             |
| $V_{INUVP_{DELAY}}$                         |                                                            |                                                                 | –                               | 500                               | –                               | ns            |
| <b>OUTPUT OVER VOLTAGE PROTECTION (OVP)</b> |                                                            |                                                                 |                                 |                                   |                                 |               |
| $OVP_{SETTINGS}$                            | OVP Settings                                               | 8 steps, $50\text{ mV/step}$                                    | 50                              | –                                 | 400                             | mV            |
| $OVP_{OFFSET}$                              | OVP Offset Accuracy                                        |                                                                 | –25                             | –                                 | 25                              | mV            |
| $OVP_{DELAY}$                               | OVP Response Time                                          | OVP threshold to PWM Low or CAT_FAULT#                          | –                               | 25                                | –                               | ns            |

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ ,  $3.135\text{ V} < V_{CC} < 3.465\text{ V}$ ,  $T_{amb} = 0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ) (continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
|--------|-----------|-----------|-----|-----|-----|------|

**OUTPUT UNDER VOLTAGE PROTECTION (UVP)**

|                  |                     |                     |     |    |      |    |
|------------------|---------------------|---------------------|-----|----|------|----|
| $UVP_{SETTINGS}$ | UVP Settings        | 8 steps, 50 mV/step | -50 | -  | -400 | mV |
| $UVP_{OFFSET}$   | UVP Offset Accuracy |                     | -25 | -  | 25   | mV |
| $UVP_{DELAY}$    | UVP Response Time   |                     | -   | 75 | -    | ns |

**OUTPUT OVER CURRENT PROTECTION (OCP)**

|                  |                     |                                                           |     |     |     |    |
|------------------|---------------------|-----------------------------------------------------------|-----|-----|-----|----|
| $OCP_{RANGE}$    | OCP Threshold Range | 256 steps, 3 A per step based on $5\text{ }\mu\text{A/A}$ | 3   | -   | 750 | A  |
| $OCP_{ACCURACY}$ | OCP Accuracy        |                                                           | -15 | -   | 15  | A  |
| $OCP_{DELAY}$    | Over Current Delay  |                                                           | -   | 700 | -   | ns |

**OVER TEMPERATURE PROTECTION (OTP)**

|               |                                |                                                                                                        |    |   |   |                    |
|---------------|--------------------------------|--------------------------------------------------------------------------------------------------------|----|---|---|--------------------|
| $T_{TH\_ACC}$ | Temperature Threshold Accuracy | Applies for Fault and Warn limit.<br>TMON = 0.8 V at $25^{\circ}\text{C}$ , 0.8 mV/ $^{\circ}\text{C}$ | -1 | - | 1 | $^{\circ}\text{C}$ |
|---------------|--------------------------------|--------------------------------------------------------------------------------------------------------|----|---|---|--------------------|

**TSENSE CATASTROPHIC FAULT DETECT**

|               |                                     |                  |       |     |       |    |
|---------------|-------------------------------------|------------------|-------|-----|-------|----|
| $CFT_{VTH}$   | Catastrophic Fault Threshold        | Rising Threshold | 1.985 | 2.0 | 2.015 | V  |
| $CFT_{HYST}$  | Threshold Hysteresis                |                  | -     | 100 | -     | mV |
| $CFT_{DELAY}$ | Catastrophic Fault Comparator Delay |                  | -     | 400 | -     | ns |

**DRVON / SM\_ALERT#**

|                                   |                                              |                           |     |    |     |            |
|-----------------------------------|----------------------------------------------|---------------------------|-----|----|-----|------------|
| $DRVON_{RL}$                      | DRVON Mode Internal Pull Down Resistance     |                           | -   | 25 | -   | k $\Omega$ |
| $DRVON_{RON\_PU}$                 | DRVON Pull Up ON Resistance                  | Sinking 500 $\mu\text{A}$ | -   | -  | 600 | $\Omega$   |
| $DRVON_{VOL} / SM\_ALERT\#_{VOL}$ | Output Low Voltage                           | Sinking 5 mA              | 0   | -  | 65  | mV         |
| $SM\_ALERT\#_{RL}$                | SM_ALERT# Mode Internal Pull Down Resistance |                           | 100 | -  | -   | k $\Omega$ |

**TSENSE UVLO DETECT**

|                        |                               |                  |     |     |     |    |
|------------------------|-------------------------------|------------------|-----|-----|-----|----|
| $Tsense_{UVLO\_VTH}$   | Tsense UVLO Rising Threshold  | Rising Threshold | 185 | 200 | 215 | mV |
| $Tsense_{UVLO\_HYST}$  | Tsense UVLO detect Hysteresis |                  | -   | 50  | -   | mV |
| $Tsense_{UVLO\_DELAY}$ | Tsense UVLO Delay             |                  | -   | 400 | -   | ns |

**TELEMETRY ADC**

|                 |                         |  |    |   |     |      |
|-----------------|-------------------------|--|----|---|-----|------|
| $ADC_{IN\_RNG}$ | ADC Input Voltage Range |  | 0  | - | 2.0 | V    |
| $ADC_{RE}$      | System ADC Resolution   |  | -  | 8 | -   | bits |
| $ADC_{ACC}$     | ADC Conversion Accuracy |  | -1 | 0 | 1   | LSB  |

**PIN\_ALERT#**

|                           |                      |                                                                           |    |   |    |               |
|---------------------------|----------------------|---------------------------------------------------------------------------|----|---|----|---------------|
| $R_{RL-PWR\_IN\_ALERT\#}$ | Low Output Impedance | Sink current is 4 mA                                                      | -  | - | 13 | $\Omega$      |
| $I_{LK-PWR\_IN\_ALERT\#}$ | Leakage Current      | 3.3 V pull up                                                             | -1 | - | 1  | $\mu\text{A}$ |
| $C_{PAD}$                 | Pad Capacitance      | CPAD includes die capacitance only.<br>No package parasitics are included | -  | - | 4  | pF            |

**VR\_HOT#**

|           |                      |                                                                           |    |   |    |               |
|-----------|----------------------|---------------------------------------------------------------------------|----|---|----|---------------|
| $R_{RL}$  | Low Output Impedance | Sink current is 4 mA                                                      | -  | - | 13 | $\Omega$      |
| $I_{LK}$  | Leakage Current      | 3.3 V pull up                                                             | -1 | - | 1  | $\mu\text{A}$ |
| $C_{PAD}$ | Pad Capacitance      | CPAD includes die capacitance only.<br>No package parasitics are included | -  | - | 4  | pF            |

**Table 6. ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 12\text{ V}$ ,  $3.135\text{ V} < V_{CC} < 3.465\text{ V}$ ,  $T_{amb} = 0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ) (continued)

| Symbol                 | Parameter                                                                | Condition                   | Min  | Typ | Max   | Unit          |
|------------------------|--------------------------------------------------------------------------|-----------------------------|------|-----|-------|---------------|
| <b>SVID SERIAL BUS</b> |                                                                          |                             |      |     |       |               |
| $V_{IH-SVID}$          | Input High Voltage, SV_CLK, SV_DATA                                      |                             | 0.65 | –   | –     | V             |
| $V_{IL-SVID}$          | Input Low Voltage, SV_CLK, SV_DATA                                       |                             | –    | –   | 0.45  | V             |
| $V_{OL-SVID}$          | Output Low Level Voltage, SV_DATA, SV_ALERT#                             | $I_{OL} = 5\text{ mA}$      | –    | –   | 65    | mV            |
| $I_{OH-SVID}$          | Output High Level Open Drain Leakage Current, SV_CLK, SV_DATA, SV_ALERT# | Pull up voltage is $V_{TT}$ | –10  | –   | 10    | $\mu\text{A}$ |
| $C_{OUT-SVID}$         | Pin Capacitance, SV_CLK, SV_DATA                                         |                             | –    | –   | 4     | pF            |
| $F_{SVID}$             | SVID Operating Frequency Range                                           | Slave Mode                  | 10   | 25  | 26.25 | MHz           |

**PMBUS INTERFACE**

|                 |                                                                          |                          |      |   |     |               |
|-----------------|--------------------------------------------------------------------------|--------------------------|------|---|-----|---------------|
| $V_{IH-PMBus}$  | Input High Voltage, SM_CLK, SM_DATA                                      |                          | 1.35 | – | –   | V             |
| $V_{IL-PMBus}$  | Input Low Voltage, SM_CLK, SM_DATA                                       |                          | –    | – | 0.8 | V             |
| $V_{OL-PMBus}$  | Output Low Level Voltage, SM_DATA, SM_ALERT#                             | $I_{OL} = 5\text{ mA}$   | –    | – | 65  | mV            |
| $I_{OH-PMBus}$  | Output High Level Open Drain Leakage Current, SM_CLK, SM_DATA, SM_ALERT# | Pull up voltage is 3.3 V | –10  | – | 10  | $\mu\text{A}$ |
| $C_{OUT-PMBus}$ | Pin Capacitance, SM_CLK, SM_DATA                                         |                          | –    | – | 10  | pF            |
| $F_{PMB}$       | PMBus Operating Frequency Range                                          | Slave Mode               | 10   | – | 400 | kHz           |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

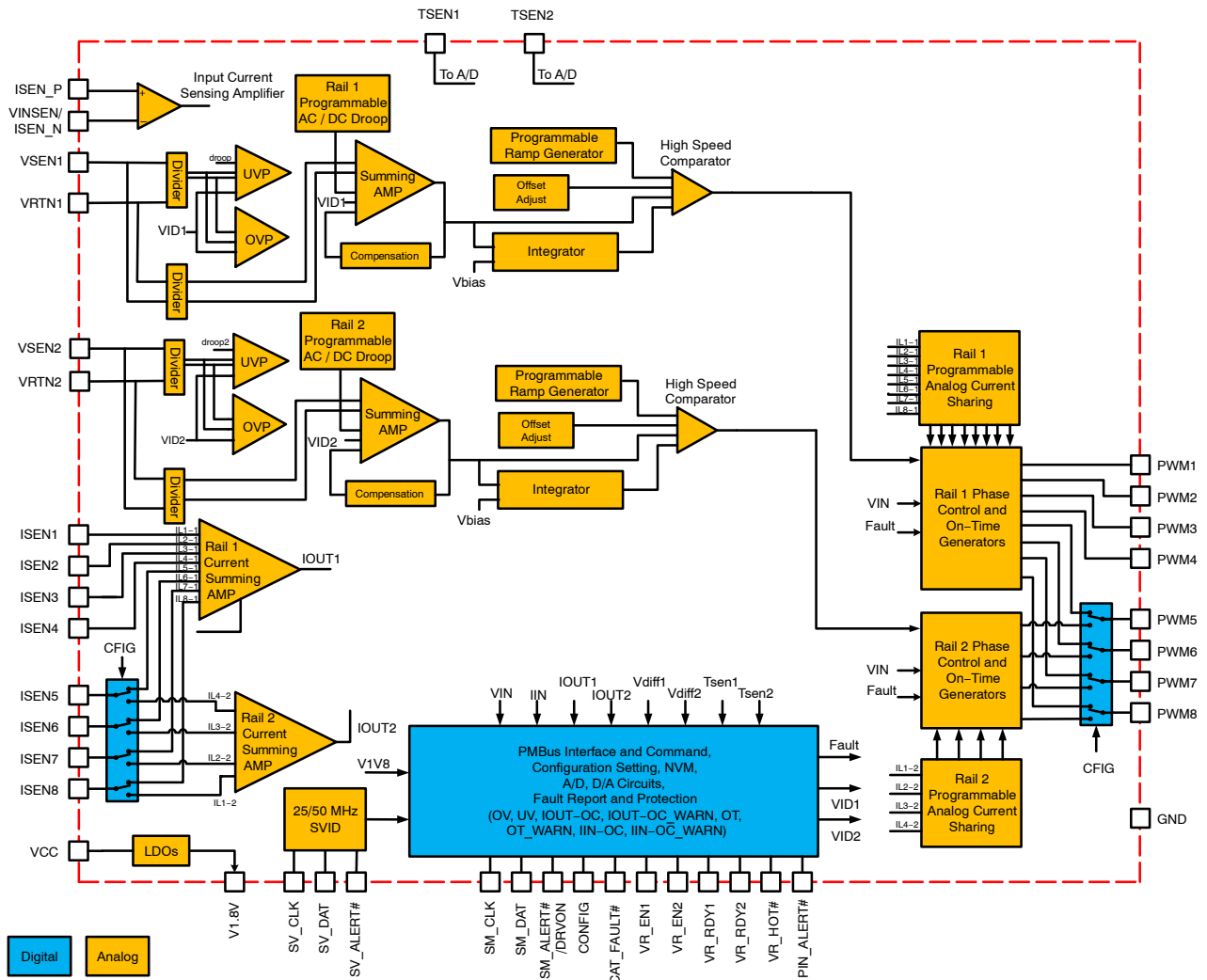


Figure 2. System Block Diagram

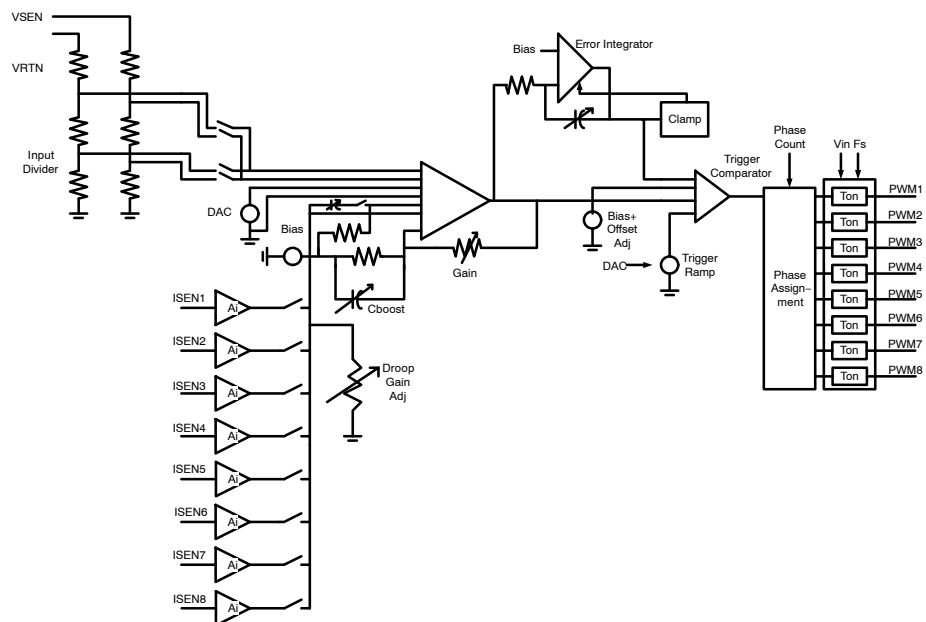


Figure 3. Feedback Control Diagram

Table 7. SUPPORTED PMBUS COMMANDS AND DEFAULT VALUES (Note 1)

| CMD Code | PMBus 1.2 Command Name | PMBus Command Description                                                                                                                                                                                                                                                | PMBus Access |
|----------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|
| 0x00     | PAGE                   | Provides ability to configure, control and monitor multiple outputs through a single physical address.                                                                                                                                                                   | R/W Byte     |
| 0x01     | OPERATION              | Configures the operational state of the converter, in conjunction with input from the ENABLE pin.<br>Turn ON and OFF the unit in conjunction with its ENABLE input signal and also initiates VOUT margining with the values set in VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW. | R/W Byte     |
| 0x02     | ON_OFF_CONFIG          | Configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.<br>Unit powers up ONLY when commanded by the ENABLE pin and OPERATION command is valid            | R/W Byte     |
| 0x03     | CLEAR_FAULTS           | Clears all fault status registers to 0x00 and releases SM_ALERT#.                                                                                                                                                                                                        | Send Byte    |
| 0x10     | WRITE_PROTECT          | Used to control writing to the PMBus device. Provide protection against accidental changes.                                                                                                                                                                              | R/W Byte     |
| 0x19     | CAPABILITY             | Provides a way for a host system to determine some key capabilities of a PMBus device.                                                                                                                                                                                   | Read Byte    |
| 0x1B     | SMBALERT_MASK          | May be used to prevent a warning or fault condition from asserting the SM_ALERT# signal                                                                                                                                                                                  | R/W Word     |
| 0x20     | VOUT_MODE              | Indicates data mode for all related Vout commands                                                                                                                                                                                                                        | Read Byte    |
| 0x21     | VOUT_COMMAND           | Sets default regulation point                                                                                                                                                                                                                                            | R/W Word     |
| 0x24     | VOUT_MAX               | Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations                                                                                                                                                          | R/W Word     |
| 0x25     | VOUT_MARGIN_HIGH       | Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High".                                                                                                                                                 | R/W Word     |
| 0x26     | VOUT_MARGIN_LOW        | Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin Low".                                                                                                                                                  | R/W Word     |
| 0x27     | VOUT_TRANSITION_RATE   | Sets the rate in mV/s at which the output should change voltage.                                                                                                                                                                                                         | R/W Word     |
| 0x47     | IOUT_OC_FAULT_RESPONSE | Indicate the output on what action to take in response to an output over current fault                                                                                                                                                                                   | R/W Byte     |
| 0x4A     | IOUT_OC_WARN_LIMIT     | Sets the value of the output current, in Amperes, that causes an output overcurrent warning condition. VR_EN must be asserted for this command to function properly.                                                                                                     | R/W Word     |
| 0x4F     | OT_FAULT_LIMIT         | Sets the temperature of the unit, in degrees Celsius, at which it should indicate an Over temperature Fault                                                                                                                                                              | R/W Word     |
| 0x50     | OT_FAULT_RESPONSE      | Indicate the output on what action to take in response to an over temperature fault                                                                                                                                                                                      | R/W Byte     |
| 0x51     | OT_WARN_LIMIT          | Sets the temperature of the unit, in degrees Celsius, at which it should indicate an Over temperature Warning alarm.                                                                                                                                                     | R/W Word     |
| 0x5D     | IIN_OC_WARN_LIMIT      | Sets the value of the input current, in Amperes, that causes an input overcurrent warning condition.                                                                                                                                                                     | R/W Word     |
| 0x60     | TON_DELAY              | The TON_DELAY command sets the time, in msec (Literal Format), from when a start condition is received until the Vout starts to rise.                                                                                                                                    | R/W Word     |
| 0x78     | STATUS_BYTE            | Returns one byte of information with a summary of the most critical faults.                                                                                                                                                                                              | R/W Byte     |
| 0x79     | STATUS_WORD            | Returns two bytes of information with a summary of the unit's fault condition.                                                                                                                                                                                           | R/W Word     |
| 0x7A     | STATUS_VOUT            | Returns one byte detailing if an output voltage fault or warning has occurred                                                                                                                                                                                            | R/W Byte     |

**Table 7. SUPPORTED PMBUS COMMANDS AND DEFAULT VALUES** (Note 1) (continued)

| <b>CMD Code</b> | <b>PMBus 1.2 Command Name</b>      | <b>PMBus Command Description</b>                                                                     | <b>PMBus Access</b> |
|-----------------|------------------------------------|------------------------------------------------------------------------------------------------------|---------------------|
| 0x7B            | STATUS_IOUT                        | Returns one byte detailing if an output current fault or warning has occurred                        | R/W Byte            |
| 0x7C            | STATUS_INPUT                       | Returns one byte detailing if an input fault or warning has occurred                                 | R/W Byte            |
| 0x7D            | STATUS_TEMPERATURE                 | Returns one byte detailing if a temperature fault or warning has occurred                            | R/W Byte            |
| 0x7E            | STATUS_CML                         | Returns one byte detailing if a PMBus serial communication fault has occurred                        | R/W Byte            |
| 0x7F            | STATUS_OTHER                       | Returns one byte detailing if an Other fault has occurred                                            | R/W Byte            |
| 0x80            | STATUS_MFR_SPECIFIC                | Returns one byte detailing if a MFR specific fault has occurred                                      | R/W Byte            |
| 0x88            | READ_VIN                           | Returns the input voltage in Volts                                                                   | Read Word           |
| 0x89            | READ_IIN                           | Returns the input current in Amperes                                                                 | Read Word           |
| 0x8B            | READ_VOUT                          | Returns the output voltage in Volts                                                                  | Read Word           |
| 0x8C            | READ_IOUT                          | Returns the output current in Amperes                                                                | Read Word           |
| 0x8D            | READ_TEMPERATURE_1                 | Returns the Power Stage temperature in degrees Celsius                                               | Read Word           |
| 0x96            | READ_POUT                          | Returns the output power, in watts                                                                   | Read Word           |
| 0x97            | READ_PIN                           | Returns the input power, in watts                                                                    | Read Word           |
| 0x98            | PMBUS_REVISION                     | Returns PMBus revision to which the device is compliant                                              | Read Byte           |
| 0x99            | MFR_ID                             | Returns the manufacturer's ID (name, abbreviation or symbol that identifies the unit's manufacturer) | Read Block          |
| 0x9A            | MFR_MODEL                          | Returns the manufacturer's model number                                                              | Read Block          |
| 0x9B            | MFR_REVISION                       | Returns the manufacturer's revision number                                                           | Read Block          |
| 0x9D            | MFR_DATE                           | Returns the date the device was manufactured.                                                        | Read Block          |
| 0xCF            | MFR_OTP_REMAIN                     | Returns the remaining of time for OTP upload                                                         | Read Byte           |
| 0xD0            | MFR_FW_REV                         | Returns the revision of FW inside device.                                                            | Read Byte           |
| 0xD1            | MFR_SVID_IOUT_SCALE_FACTOR_CONTROL | Used to set the SVID Iout reporting scaling factor                                                   | R/W Byte            |
| 0xD2            | MFR_DEV_REVISION                   | Return the revision of device.                                                                       | Read Byte           |
| 0xD3            | MFR_I2C_ADDR                       | Indicate current I2C/PMBus slave address                                                             | R/W Byte            |
| 0xD6            | MFR_STORE_USER_CONFIG              | Used to upload config from RAM to OTP Memory                                                         | R/W Byte            |
| 0xD7            | MFR_USER_INDEX                     | Return the 4-bit code to indicate the resistor value place at CONFIG (pin34) pin.                    | Read Byte           |
| 0xDB            | MFR_RAIL_NAME                      | Indicate the name of the output rail.                                                                | R/W Word            |

**Table 7. SUPPORTED PMBUS COMMANDS AND DEFAULT VALUES** (Note 1) (continued)

| CMD Code | PMBus 1.2 Command Name  | PMBus Command Description                              | PMBus Access |
|----------|-------------------------|--------------------------------------------------------|--------------|
| 0xDC     | MFR_DIGITAL_IO_STTS     | Returns the status of digital I/O                      | Read Byte    |
| 0xDD     | MFR_RESTORE_USER_CONFIG | Used to download config from OTP Memory to RAM         | R/W Byte     |
| 0xED     | MFR_VID_OFFSET          | Used to set the output voltage offset.                 | R/W Byte     |
| 0xEE     | MFR_GET_USER_CRC        | Return the CRC value for USER config table burn in OTP | Read Word    |
| 0xEF     | MFR_HC_ACTIVE           | Used to set HC_ACTIVE behavior                         | R/W Byte     |

1. Reference UM70016/D – FD3501 PMBus Command Information document for detailed information.

## CONFIGURATION

FD3501 operation is controlled by application specific configuration settings loaded into control registers. For typical applications, the control registers are pre-programmed at the factory and stored in nonvolatile memory (NVM). However the user control registers can be reprogrammed in the field via the serial communication PMBus and stored into the NVM if necessary. The number of updates are limited. The NVM memory is implemented with an OTP technology and once the OTP is full no further updates are possible. Reprogramming the FD3501 can easily be accomplished with the GUI interface. It is recommended to use the FD3501 working registers for configuration verification testing as much as possible before saving the final configuration to the NVM.

The internal NVM storage elements are one-time programmable, but the memory structure imitates a multi-time programmable memory and can hold up to 8 updates.

### Device Configuration

The FD3501 provides all the control functions necessary to support a total phase count of two rails up to 8 phases of high performance DC–DC buck converter regulators. Rail 1 supports a multi-phase buck converter with up to 8 phases, and Rail 2 supports a multi-phase buck converter with up to 4 phases. If only Rail 2 is used, Rail 1 must still be enabled to ensure proper functionality.

Each rail supports independent differential voltage sensing, current sensing on individual DR MOS phases, temperature sensing, enable control, power ready report, while sharing the SVID and PMBus, and input voltage sense.

The switching frequencies for Rail 1 and Rail 2 can be independently selected. Rail 1 and 2 multi-phase PWM output signals are set in an interleaving effect under all different phase conditions to take advantage of input and output ripple cancellations.

The devices are compliant with the PMBus specification part I and part II, revision 1.2 ([www.pmbus.org](http://www.pmbus.org)) for read/write access in byte, word, block mode.

The FD3501 is fully compliant with Intel SVID protocol. To guarantee proper device and CPU operations, refer to this document for bus design and layout guidelines. Different platforms may require different pull-up impedance on the SVID bus. Impedance matching and spacing between SV\_DAT, SV\_CLK, and SV\_ALERT# must be followed.

### Device Address Definition

The PMBus and the VR13/13.HC slave addresses of un-configured multiphase and single phase outputs are initially determined by reading the voltage on the CONFIG pin passed on Table 8. The 1% resistor to ground on the config pin determines the values based on Table 8.

**Table 8. DEVICE ADDRESS SETTING**

| R <sub>ext</sub><br>[Ω] | 4-bit<br>CODE | SMBus Address<br>(8-bit) |
|-------------------------|---------------|--------------------------|
| ≤1300                   | 0             | 0xB0                     |
| 4120                    | 1             | 0xB4                     |
| 7320                    | 2             | 0xB8                     |
| 11300                   | 3             | 0xBC                     |
| 15800                   | 4             | 0xC0                     |
| 21000                   | 5             | 0xC4                     |
| 27400                   | 6             | 0xC8                     |
| 35700                   | 7             | 0xCC                     |
| 45200                   | 8             | 0xD0                     |
| 59000                   | 9             | 0xD4                     |
| 76800                   | A             | 0xD8                     |
| 102000                  | B             | 0xDC                     |
| 143000                  | C             | 0xE0                     |
| 215000                  | D             | 0xE4                     |
| 383000                  | E             | 0xE8                     |
| 1240000 (Open)          | F             | 0xEC                     |

## HC (High Current) Support

On the VR13.HC platform, most CPU SKUs have Iccmax over 255 A and require the controller VR to support the higher current capability. FD3501 supports the Intel HC requirement by default and automatically optimizes DAC scaling to ensure accurate current and power telemetry reporting.

For CPU SKUs with Iccmax less than 255 A, either one of the following can be performed to disable the HC support.

1. Use the controller GUI to disable HC\_SUPPORT.
2. Through PMBus, issue the MFR\_HC\_ACTIVE command to set HC\_ACTIVE to 0.

## THEORY OF OPERATION

### Device Initializing and Startup

Operating from a single +3.3 V supply (VCC), an on-chip low drop-out (LDO) regulator generates an internal +1.8 V supply for both analog and digital circuits. The system will be reset by the internal power-on reset (POR) signal, which is determined by VCC ready and 1.8 V ready. After the controller comes out of POR, the contents of the NVM are downloaded into the control registers to configure the VR operation. For typical applications, the control registers are pre-programmed at the factory and stored in the on-chip nonvolatile memory (NVM). Control registers can also be reprogrammed in the field via the PMBus interface and stored into the NVM. FD3501 supports adjusting working registers before the final OTP write to evaluate changes in settings on the fly during development testing and debug.

After the UVLO has been checked and has entered a power good state, the state machine will check the config pin voltage and then determine which User configuration to use or if the part is blank. If the part is not configured, the config pin will be used to set the initial PMBus address and then the part will wait to be configured by PMBus. If the part was pre-programmed, then the part will use the config pin to select the user configuration page which includes all the user settings including the PMBus address, the SVID addresses, and the phase configuration. The OTP information is then loaded into the working registers.

After the user trims are loaded, the OVP/CAT\_FAULT# function will become active to help protect the system.

During the controller configuration and initialization, the PWM outputs are held in high impedance state, allowing Smart Power Stage (SPS) resistors to set the correct default levels. The SPS PWM pins cannot be loaded if the FD3501 is off or in initial power up, in other cases the PWM pin can be held at MID state during operation as needed such as DCM mode operation and phase shedding operation.

The FD3501 provides a configuration and initialization done signal (can be a fixed delay from POR) to make sure correct working for any sequence of VR\_EN and VCC. Both VR\_EN high, and configuration and initialization done signal can enable the chip to go to the next stage.

### Soft Start

After the IC has been properly initialized, the IC is set to enable the output rails. Startup sequence is independently programmable for both rails, but it depends essentially by the VBOOT, SLEW RATE and delay settings.

In case the VBOOT register contains non-zero value, upon VR\_ENx assertion, the corresponding output voltage will ramp to the programmed VBOOT. The DAC ramp up is controlled and monotonic without any previous bias voltage. The controller will not sink negative current from a pre-biased output. The PWM signals will stay in the MID state or high Z state until the PWMs start triggering as the DAC ramps up. The start-up ramp rate and final target voltage are programmable for the two loops by the SVID slew rate register. The ALERT# is held low until the STATUS1 register is read. If a valid SetVID command is received, the controller will ramp to the new voltage target at a rate determined by the SVID\_FAST or SVID\_SLOW transition rates. If a valid SetVID command is not received, FD3501 will continue to regulate at the Vboot target voltage. After the regulator completes the initial voltage ramp, it enters the Active Regulation state, and the VR\_READY signal is asserted indicating that the output voltage for that loop is within its target value.

For the case where Vboot is initially set to 0, the response of the controller is to keep the power stage in a MID state until such time as a valid SVID voltage is received. VR\_Ready will assert with a delay from VR\_EN to make sure the controller is ready for the SVID commands. When the first SetVID command is received the controller will then digitally ramp the voltage from the pre-biased voltage to the SVID target value and assert the ALERT# pin (active low). The start-up transition rate to the SVID target under this scenario is governed by SVID\_FAST or SVID\_SLOW.

### Active Regulation

Both loops of the FD3501 controller are implemented as constant-on time voltage mode control architectures. The system uses both input voltage and VID feedforward as well as a digital frequency control loop to achieve an almost constant switching frequency in steady state operation. Very fast response is achieved by constant on time control rapidly increasing the frequency of operation during transient loads. During operation each loop's output voltage is sensed differentially. Voltage droop is programmable with either 20  $\mu\Omega$  or 40  $\mu\Omega$  steps depending on the DAC step size. The 10 mV VID DAC stepping provides 40  $\mu\Omega$  droop step settings from 0 to 4.02 m $\Omega$ . Phase shedding can be set as automatic according to the output load current or be set to manual according to the SVID power state. The current thresholds are programmable for auto phase shedding mode.

### Dynamic Phase Management (DPM)

Dynamic Phase Management allows the number of working phases to be adjusted according to the output load current automatically so that the efficiency can be optimized in the entire load range. The current thresholds and hysteresis can be programmed through PMBus configuration commands for the DPM.

DPM will be disabled and all the populated phases will be forced on when changing dynamically the regulated voltage (DVID) or sudden load transient is detected.

DPM function can also be disabled through PMBus configuration.

### Current Sharing

Each phase power stage current sensing signal is fed to ISENx pin as a current source. The current source is treated as a gain of 5  $\mu\text{A}/\text{A}$  gain. For Rail 1 with a multiphase configuration, phase 1's current is used as a reference. For Rail 2 with a multiphase configuration, phase 8's current is used as a reference. Other phase currents are compared with the reference with an integrated compensator to adjust the PWM on time so that the current can follow the reference accurately. For shedded phase, the current sharing loop is disabled.

### Shut Down

The FD3501 enters the shutdown state as per direct command (VR\_EN de-asserted), or as a response to a detected fault condition such as Over Temperature (OT), Over Current (OC), Over Voltage Protection (OVP), or the Power Stage's reported fault.

Vout shut down behavior can be programmed through a configuration bit. If Decay shut down is selected, both high side and low side FETs are turned off and the PWM goes to forced MID-state, and then High-Z if the controller is being disabled for some reason. If Controlled Shut down is selected, the Vout is actively regulated down until Vout is 0.

The de-assertion of the VR\_EN pin is deglitched with a 1  $\mu\text{s}$  filter to provide immunity to errant shutdowns due to noise on the VR\_EN pin.

### OCP Fault Shutdown Response

The total current COP threshold is user programmable with a setting from 3 A to 750 A using a 3 A step. Once the FD3501 enters the OCP shutdown state, it will transition to an Inactive state. Once the OCP condition is removed, the Vout can only occur if VCC or VR\_EN is toggled.

### OVP/UVF Fault Shutdown Response

The over-voltage protection acts differently based on the operating state of the system, and on the system requirements. During the power up sequence, the maximum allowed voltage level is set by the MAX\_VID register.

During normal operation, the OVP threshold tracks the VID settings. The OV protection is selectively blanked during specific operating mode, to allow the VR to move to a new operating state without triggering false fault conditions.

Figure 4 below summarizes blanking periods versus specific operating conditions. In particular, Dynamic VID Transitions: OVP is blanked for the entire duration of a VID downward transition, plus a time TDR. Conversely, the UVP is blanked for the entire duration of DVID upward transition, plus a time TDR. Time TDR is approximately 15  $\mu\text{s}$ .

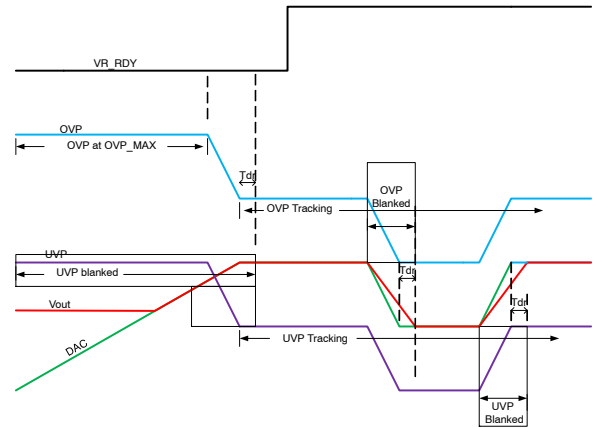


Figure 4. OVP UVP Blanking Timing Diagram

If an OVP event occurs, the SPS power stage PWM signals associated with the rail experiencing the OVP event are set to low. If a UVP occurs the PWM signals will be set to the MID state. OVP and UVP are latched fault events. To reset the fault the rail's enable pin can be cycled or the controller's VCC UVLO can be cycled.

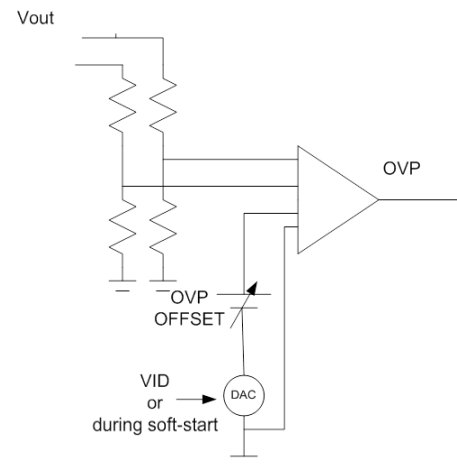


Figure 5. OVP Detector Block Diagram

## APPLICATION INFORMATION

### Power Up Sequence Control

Following is the recommended power up sequence.

1. Controller 3.3 V VCC applied
2. Power Stage 5 V VCC applied
3. Power Stage enabled
4. 12 V Power applied
5. VR\_EN signals asserted

To be noted that the IC must have the TSEN1/2 pin rising up from 0 V to at least 0.2 V based on temperature after all power stages are ready. If this signal is low the controller output will be held in a disabled state. The VR\_EN pins have a 10  $\mu$ s deglitching filter on rising edge and a 50 mV hysteresis to prevent noise.

### Input Voltage, Current and Power Sensing

Input voltage VIN and current IIN are sensed through the VINSEN/ISEN\_N and ISEN\_P pins. A series shunt resistor should be connected to the input supply rail. The VIN voltage is sensed at pin VINSEN. The IIN current is sensed differentially between pins ISEN\_P and ISEN\_N. Input power PIN is calculated digitally based on the sensed VIN and IIN ADC values.

The sensed input voltage is compared with the Vin UVLO threshold to make sure that the input voltage is in the desired range for normal operation. This threshold is OTP adjustable in the user settings. VIN is also used to set the constant-on time, which is inversely-proportional to VIN.

The sensed input current is compared with the set threshold of IIN<sub>OC-WARN-LIMIT</sub> for the input over current warn protection.

The sensed input power is compared with the set threshold of PIN<sub>LIM</sub>. PIN\_ALERT# pin will be pulled low when input power exceeds PIN<sub>LIM</sub> as defined by the Intel SVID protocol specification. PIN\_ALERT# is used for fault reporting only and cannot initiate a shutdown.

### Temperature Sensing and Power Stage Fault Sensing

The FD3501 can sense the highest temperature of the power stages in the related rails independently by connecting TSENx pin to all the power stage TMON pins in the related rail.

If the sensed temperature in one of the converters exceeds the programmed TMAX, FD3501 asserts VR\_HOT# as long as the over-temperature event lasts.

In the same time, if any power stage has a fault, its TMON pin will be pulled high. FD3501 can detect it through TSENx pin and trigger catastrophic fault. CAT\_FAULT# pin is pulled low.

### PMBus and SVID Telemetry

The FD3501 provide real time telemetry for multiple parameters over the PMBus and SVID interfaces. The available telemetry options are:

- Input Voltage
- Input Current
- Input Power
- Output Voltages of two rails
- Total output current of two rails
- Output power of two rails
- Temperatures of two rails

### Phase Current Sensing

FD3501 can monitor up to 8 phase currents, based on the  $M + N \leq 8$  selections made in the Rail 1 and Rail 2. M (number of phases for Rail 1) should be greater than or equal to 1 and N (number of phases for Rail 2) should be less than or equal to 4. These current signals are monitored using the 8 ISENx pins on FD3501. The 'current' signals from the power stages, proportional to each phase inductor current with a gain of 5  $\mu$ A/A can be directly connected to the ISENx pins on FD3501. Since FD3501 can monitor directly these current signals, there is no requirement to convert these current signals into voltage signals on the application board. Therefore, the typical current sensing resistor as well as the noise filtering decoupling capacitors can be avoided between the power stage IMON pins and FD3501 ISENx pins.

### PMBus Support

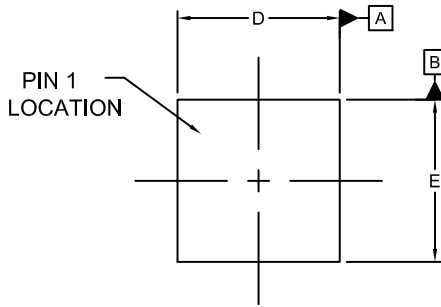
The FD3501 are compatible with PMBus standard revision 1.2 refer to PMBus standard documentation for further information ([www.pmbus.org](http://www.pmbus.org)).

The FD3501 PMBus engine is based on the embedded 8051 micro controller with a powerful and flexibility design.

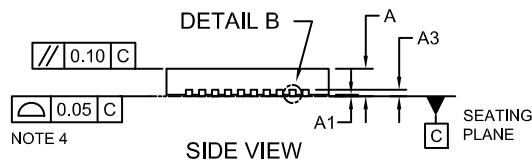
The device supports memory paging so that the same command can be applied to either the controller #1 (page 0, multiphase) or the controller #2 (page 1, single-phase) to access the required information.

The list of the PMBus commands supported are reported into Table 7.

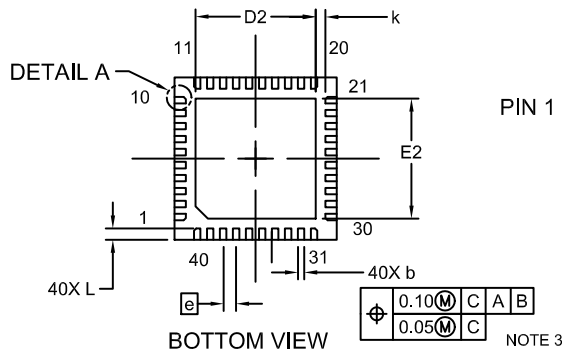
## PACKAGE DIMENSIONS

QFN40 5x5, 0.4P  
CASE 485FW  
ISSUE O

TOP VIEW



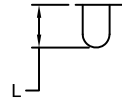
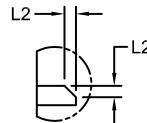
SIDE VIEW



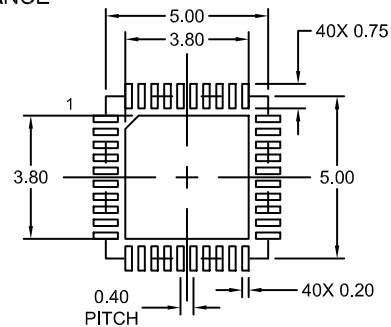
BOTTOM VIEW

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DETAIL A  
ALTERNATE  
CONSTRUCTIONDETAIL B  
PIN 1 TERMINAL APPEARANCE

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NOM. | MAX. |
| A   | 0.80        | 0.85 | 1.00 |
| A1  | —           | —    | 0.05 |
| A3  | 0.20 REF    |      |      |
| b   | 0.15        | 0.20 | 0.25 |
| D   | 4.90        | 5.00 | 5.10 |
| D2  | 3.60        | 3.70 | 3.80 |
| E   | 4.90        | 5.00 | 5.10 |
| E2  | 3.60        | 3.70 | 3.80 |
| e   | 0.40 BSC    |      |      |
| K   | 0.25        | —    | ---  |
| L   | 0.30        | 0.35 | 0.40 |
| L2  | 0.118 REF   |      |      |



## RECOMMENDED LANDPATTERN\*

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marketing.pdf](http://www.onsemi.com/site/pdf/Patent-Marketing.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:  
Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi** Website: [www.onsemi.com](http://www.onsemi.com)

TECHNICAL SUPPORT  
North American Technical Support:  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:  
Phone: 00421 33 790 2910  
For additional information, please contact your local Sales Representative