# F0111

Dual Path Ultra-Low Noise Amplifier 2200MHz to 4200MHz

The F0111 is a dual-path 2200MHz to 4200MHz High Gain / Ultra-Low Noise Amplifier (LNA) that is used in receiver applications.

The F0111 LNA is operated as a *balanced amplifier* where the inputs and outputs are combined using external 90° couplers and provides 18.5dB of gain with 0.55dB noise figure and 38.5dBm OIP3 performance at 2600MHz. The device uses a single 5V supply and 90mA typical of total $I_{CC}$.

The F0111 is packaged in a 4 × 4 mm, 16-VFQFPN with 50Ω single-ended RF input and output impedances for ease of integration into the signal path.

## Competitive Advantage

- Ultra-low noise performance of 0.55dB over wide bandwidths improves receiver sensitivity
- High gain and linearity

## Features

- RF range: 2200MHz to 4200MHz
  - F0109: 650MHz to 1000MHz
  - F0110: 1500MHz to 2300MHz
- 18.5dB typical gain at 2600MHz
- 0.55dB typical NF at 2600MHz
- +38.5dBm typical OIP3 at 2600MHz
- 50Ω Single-ended input/output impedances
- +5V power supply
- $I_{CC}$ = 45mA per channel
- Independent channel standby modes for power savings
- 1.8V logic standby control
- Operating temperature (TEP) range: -40°C to +105°C
- 4 × 4 mm, 16-VFQFPN package

## Applications

- 3G, 4G, 5G wireless infrastructure
- Public safety infrastructure
- General-purpose RF

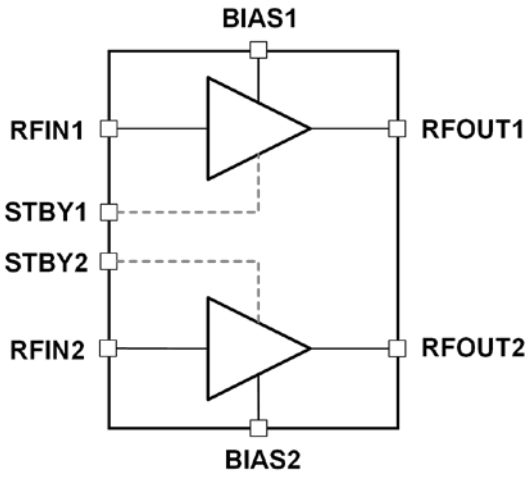



**Figure 1. Block Diagram**


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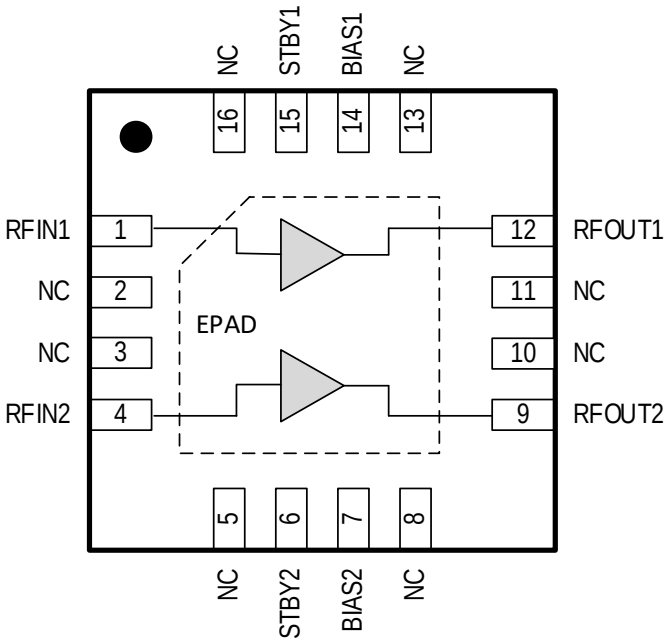
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# 1. Pin Information

## 1.1 Pin Assignments




**4 × 4 × 0.75 mm 16-VFQFPN Package**
**Top View**

## 1.2 Pin Descriptions

| Number | Name | Description |
|---|---|---|
| 1 | RFIN1 | Path 1 RF input. Must use external DC block. DC block is also a tuning element and must be close to the pin for best RF performance. |
| 4 | RFIN2 | Path 2 RF input. Must use external DC block. DC block is also a tuning element and must be close to the pin for best RF performance. |
| 2, 3, 5, 8, 10, 11, 13, 16 | NC | No internal connection. These pins can be left unconnected or be connected to ground (highly recommended). Use a via as close to the pin as possible if grounded. |
| 6 | STBY2 | Standby pin for path 2. With Logic LOW applied to this pin (or if the pin is left unconnected), the amplifier on path 2 is powered ON. With Logic HIGH applied to this pin, the path 2 amplifier is powered OFF and the path is in Standby mode. Pin is 1.8V logic compatible. |
| 7 | BIAS2 | Path 2 voltage control. |
| 9 | RFOUT2 | Path 2 RF output internally matched to 50Ω. An external pull-up inductor to a common $V_{CC}$ is required to bias the amplifier. Must use an external DC block after the pull-up inductor. DC block is also a tuning element and must be close to the pin for best RF performance. |
| 12 | RFOUT1 | Path 1 RF output internally matched to 50Ω. An external pull-up inductor to a common $V_{CC}$ is required to bias the amplifier. Must use an external DC block after the pull-up inductor. DC block is also a tuning element and must be close to the pin for best RF performance. |
| 14 | BIAS1 | Path 1 voltage control. |
| 15 | STBY1 | Standby pin for path 1. With Logic LOW applied to this pin (or if the pin is left unconnected), the amplifier on path 1 is powered ON. With Logic HIGH applied to this pin, the path 1 amplifier is powered OFF and the path is in Standby mode. Pin is 1.8V logic compatible. |
| - | EPAD | Exposed paddle. Internally connected to ground. Solder this exposed paddle to a Printed Circuit Board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance. |



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# 2. Specifications

## 2.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed can cause permanent damage to the device. Functional operation of the F0111 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CC}$ to GND | $V_{CC}$ | -0.3 | + 6.0 | V |
| STBY1, STBY2 | $V_{CTL}$ | -0.3 | +5.25 | V |
| RFIN1, RFIN2 externally applied DC voltage | $V_{RFIN}$ | - 0.3 | + 0.3 | V |
| RFOUT1, RFOUT2 externally applied DC voltage | $V_{RFOUT}$ | - 0.3 | + 6.0 | V |
| **ON STATE:** RF CW Input Power (RFIN1, RFIN2) applied for 2 hours max. $V_{CC}$ = 5V, $T_{EP}$ = 105˚C, input / output VSWR < 2:1 based on a 50Ω system. [a] | $P_{MAX_IN_ON}$ | | 22 | dBm |
| **OFF STATE:** RF CW Input Power (RFIN1, RFIN2) applied for 2 hours max. $V_{CC}$ = 5V, $T_{EP}$ = 105˚C, input / output VSWR < 2:1 based on a 50Ω system. [a] | $P_{MAX_IN_OFF}$ | | 22 | dBm |
| Storage Temperature Range | $T_{STOR}$ | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | $T_{LEAD}$ | | +260 | °C |
| Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012) | $V_{ESDHBM}$ | | 500 | V |
| Electrostatic Discharge – CDM (JEDEC 22-C101F) | $V_{ESDCDM}$ | | 500 | V |

[a] Exposure to these maximum RF levels can result in significantly higher $I_{CC}$ current draw due to overdriving the amplifier stages.

## 2.2 Recommended Operating Conditions

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Power Supply Voltage [a] | $V_{CC}$ | | 4.75 | | 5.25 | V |
| Operating Temperature Range | $T_{EP}$ | Exposed paddle | -40 | | +105 | °C |
| Junction Temperature | $T_J$ | | | | +160 | °C |
| RF Frequency Range | $F_{RF}$ | | 2200 | | 4200 | MHz |
| Maximum Operating RF Input Power to RFIN1, RFIN2 [b] | $P_{MAX}$ | | | | +5 | dBm |
| RF Source Impedances | $Z_{RFI}$ | Single-ended | | 50 | | Ω |
| RF Load Impedances | $Z_{RFO}$ | Single-ended | | 50 | | Ω |

[a] Functional voltage operating range. Device is designed to function with any supply voltage ≥ 4.75V, although performance may be degraded when operated outside the recommended voltage range.

[b] CW power over operating temperature, operating voltage and operating frequency range. Input / output VSWR < 2:1



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## 2.3 Electrical Specifications

### 2.3.1. General

See the F0111 Typical Application Circuit. Specifications apply when operated as a dual RX LNA with $V_{CC}$ = +5.0V, $f_{RF}$ = 2600MHz, $T_{EP}$ = +25°C, STBY1 = STBY2 = Logic LOW, $Z_S$ = $Z_L$ = 50Ω, $P_{OUT}$ = +5dBm/tone for two-tone parameters, two-tone spacing = 1MHz, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Logic Input High Threshold | $V_{IH}$ | | ***1.17*** [a] | | Lower of ($V_{CC}$, 5.25) | V |
| Logic Input Low Threshold | $V_{IL}$ | | -0.3 | | ***0.63*** | V |
| Logic Current High Threshold | $I_{IH}$ | | ***5*** | | ***250*** | µA |
| Logic Current Low Threshold | $I_{IL}$ | | ***-20*** | | ***50*** | µA |
| Quiescent Current | $I_{CC_Q}$ | Single path | | 45 | ***70*** | mA |
| | | Both paths | | 90 | ***140*** | mA |
| Standby Current | $I_{CC_STBY}$ | STBY1 = STBY2 = HIGH | | 5 | ***15*** | mA |
| Standby Switching Time | $T_{ON}$ | 50% STBY control to within 0.1dB of the on-state final gain value and 1 degree of final phase value | | 430 | | ns |
| | $T_{OFF}$ | 50% STBY control to $I_{CC}$ < 10mA | | 80 | | ns |

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

### 2.3.2. RF (Balanced Configuration, 2.5GHz to 2.7GHz) Performance

See the F0111 Typical Application Circuit. Specifications apply when operated as a ***dual RX LNA*** with $V_{CC}$ = +5.0V, $f_{RF}$ = 2600MHz, $T_{EP}$ = +25°C, STBY1 = STBY2 = Logic LOW, $Z_S$ = $Z_L$ = 50Ω, $P_{OUT}$ = +5dBm/tone for two-tone parameters, two-tone spacing = 1MHz, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| RF Input Return Loss | $RL_{IN}$ | | | 27 | | dB |
| RF Output Return Loss | $RL_{OUT}$ | | | 23 | | dB |
| Gain | G | | ***16.5*** | 18.5 | ***20.5*** | dB |
| Gain Flatness | G | Freq = 2500MHz – 2700MHz. Flatness referenced to Gain at band center | | ±0.3 | | dB |
| Gain Variation over Temperature | G | $T_{EPAD}$ = -40°C to 105°C | | -0.5/+0.7 | | dB |
| Reverse Isolation | ISO | | | 28 | | dB |
| STBY Mode Gain | G | | | -21 | | dB |
| Noise Figure | NF | Freq = 2600MHz, De-embedded to the input pin of the Hybrid Coupler | | 0.55 | 0.75 | dB |
| Output IP3 | OIP3 | $P_{OUT}$ = 5dBm/tone, Δf = 1MHz | 35 | 38.5 | | dBm |
| Output P1dB | OP1dB | | 19 | 23 | | dBm |
| Stability | K | K-Factor<br>$V_{CC}$ = 4.75V – 5.25V<br>$T_{EP}$ = -40°C – 105°C<br>$f_{RF}$ = 10MHz – 20GHz | 1 | | | |

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization using external matching BOM optimizing for 2.5GHz to 2.7GHz.



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### 2.3.3. RF (Balanced Configuration, 3.3GHz to 4.2GHz) Performance

See the F0111 Typical Application Circuit. Specifications apply when operated as a ***dual RX LNA*** with $V_{CC}$ = +5.0V, $f_{RF}$ = 3500MHz, $T_{EP}$ = +25°C, STBY1 = STBY2 = Logic LOW, $Z_S = Z_L$ = 50Ω, $P_{OUT}$ = +0dBm/tone for two-tone parameters, two-tone spacing = 1MHz, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| RF Input Return Loss | $RL_{IN}$ | | | 19 | | dB |
| RF Output Return Loss | $RL_{OUT}$ | | | 20 | | dB |
| Gain | G | | | 16 | | dB |
| Gain Flatness | G | Freq = 3300MHz – 3600MHz. Worst case over any 200MHz bandwidth. | | 0.65 | | dB |
| | | Freq = 3600MHz – 4200MHz. Worst case over any 200MHz bandwidth. | | 3 | | |
| Gain Variation over Temperature | G | $T_{EPAD}$ = -40°C to 105°C | | -0.6/+0.7 | | dB |
| Reverse Isolation | ISO | | | 26 | | dB |
| STBY Mode Gain | G | | | -20 | | dB |
| Noise Figure | NF | Freq = 3500MHz, De-embedded to the input pin of the Hybrid Coupler | | 1.05 | | dB |
| Output IP3 | OIP3 | $P_{OUT}$ = 0dBm/tone, Δf = 1MHz | | 40 | | dBm |
| Output P1dB | OP1dB | | | 21 | | dBm |
| Stability | K | K-Factor<br>$V_{CC}$ = 4.75V – 5.25V<br>$T_{EP}$ = -40°C – 105°C<br>$f_{RF}$ = 10MHz – 20GHz | 1 | | | |

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization using external matching BOM optimizing for 3.4GHz to 3.6GHz.

## 2.4 Thermal Characteristics

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction to Ambient Thermal Resistance. | $\theta_{JA}$ | 95.6 | °C/W |
| Junction to Case Thermal Resistance.<br>(Case is defined as the exposed paddle) | $\theta_{JC\text{-}BOT}$ | 23.6 | °C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | | MSL 1 | |



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# 3. Typical Operating Conditions (TOC) for Balanced Configuration

## 3.1 Typical Operating Conditions (2.5GHz to 2.7GHz)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- $V_{CC}$ = 5.0V
- STBY = Low
- $f_{RF}$ = 2600MHz
- $Z_L = Z_S$ = 50Ω Single-ended
- $P_{OUT}$ = +5dBm/Tone (Two-tone parameters)
- 1MHz Tone Spacing
- All temperatures are referenced to the exposed paddle
- Evaluation kit traces and connector losses are de-embedded

### 3.1.1. Typical Performance Characteristics

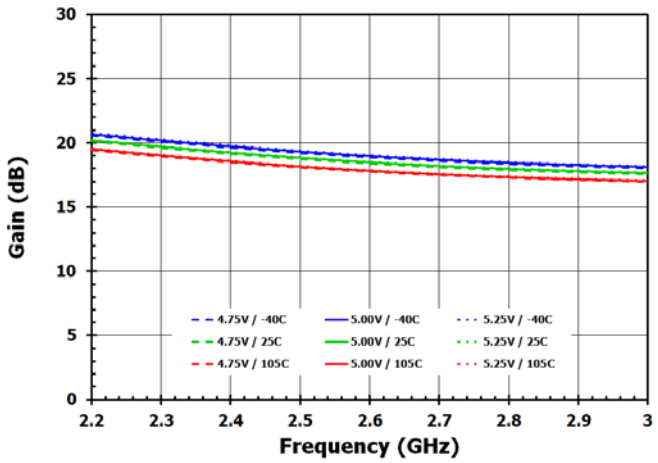



Figure 2. Gain

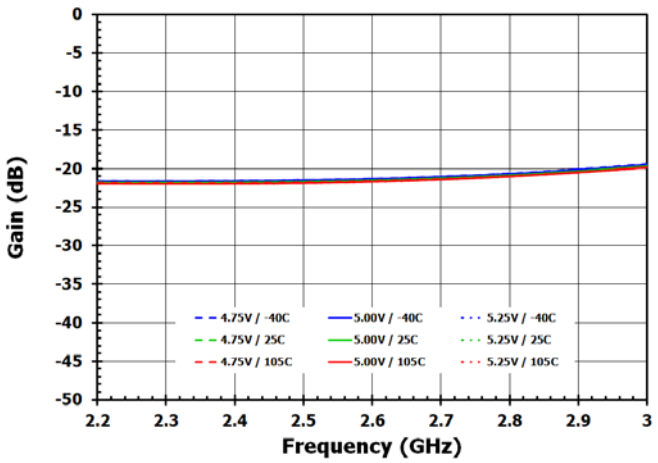



Figure 3. STBY Mode Gain

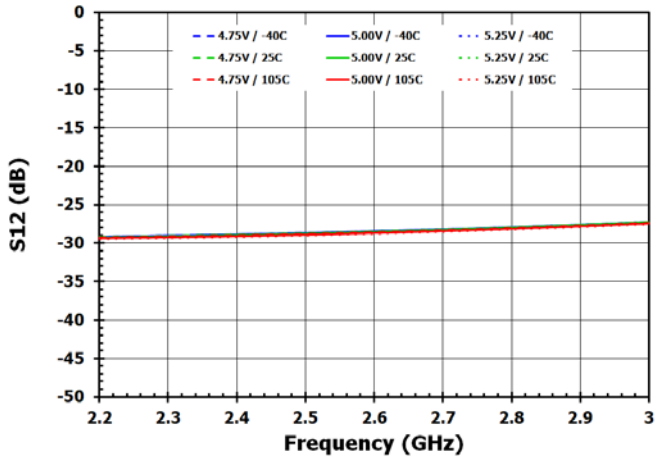



Figure 4. Reverse Isolation

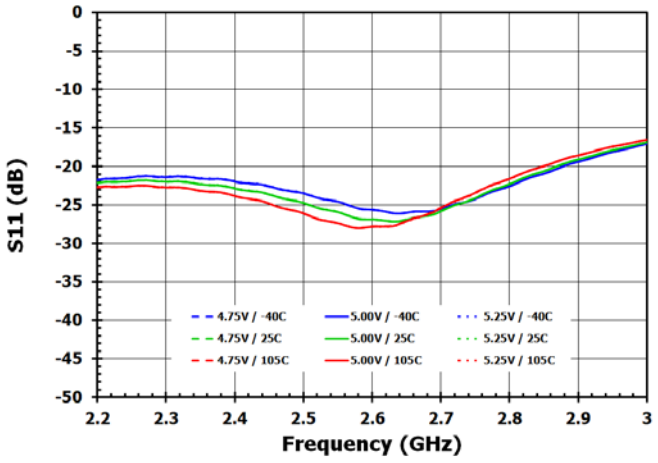



Figure 5. Input Return Loss



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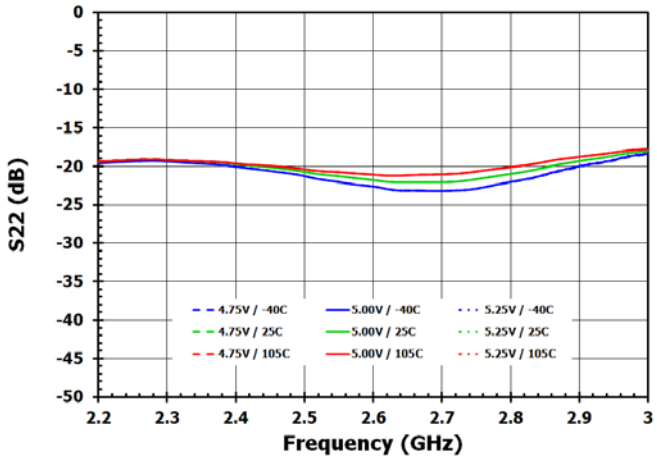



Figure 6. Output Return Loss

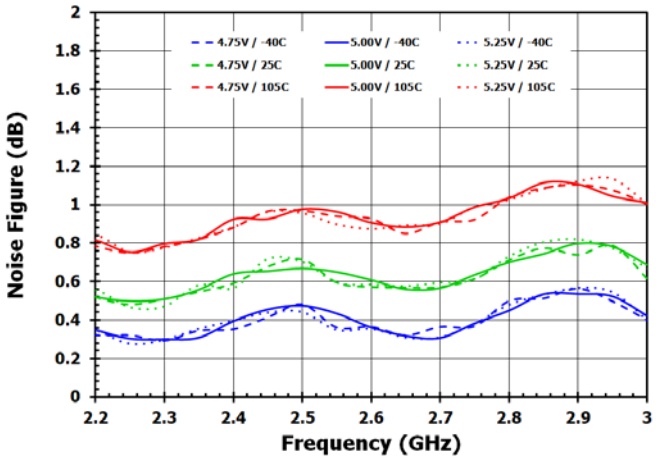



Figure 7. Noise Figure

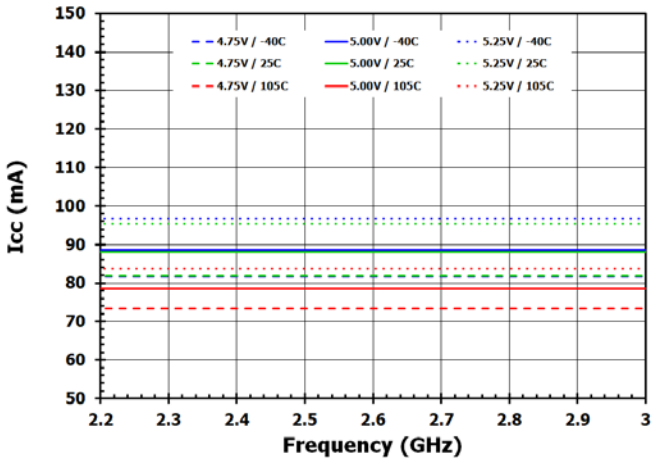



Figure 8. DC Current (Icc) Vs Frequency

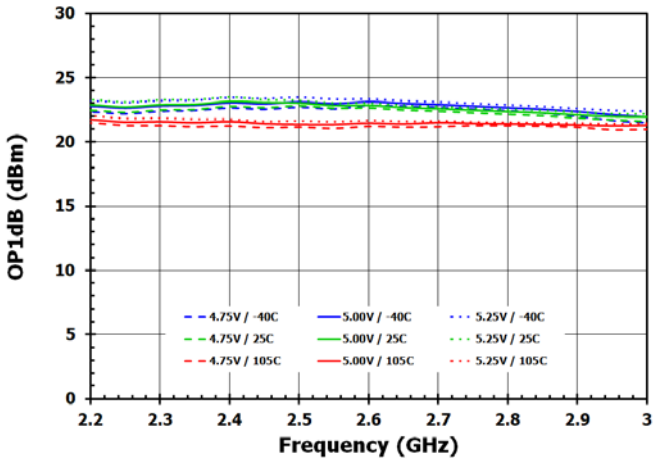



Figure 9. OP1dB

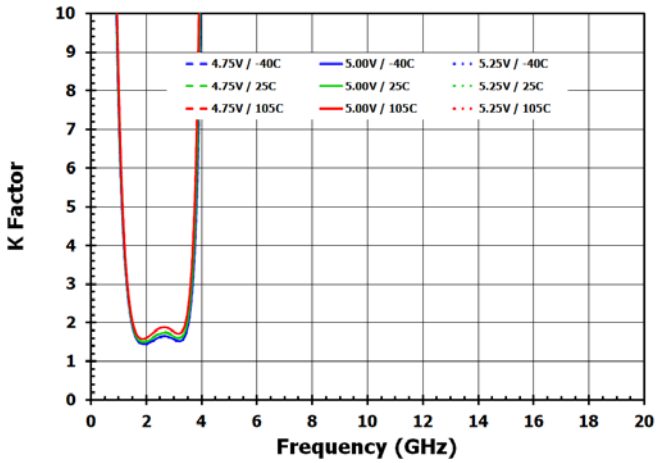



Figure 10. K Factor

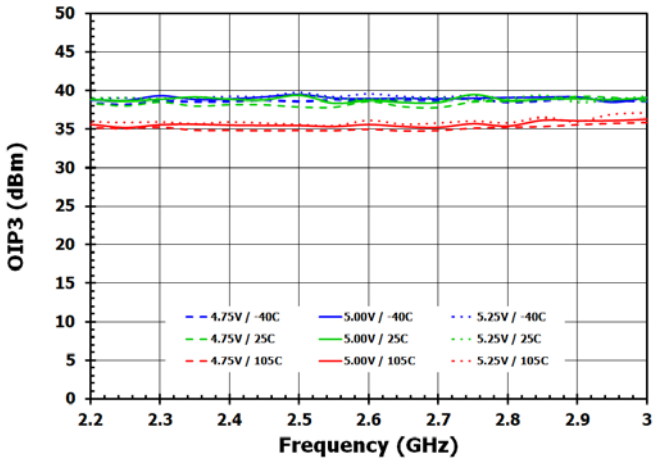



Figure 11: OIP3



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## 3.2 Typical Operating Conditions (3.3GHz to 4.2GHz)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- $V_{CC}$ = 5.0V
- STBY = LOW
- $f_{RF}$ = 3500MHz
- $Z_L = Z_S$ = 50Ω Single-ended
- $P_{OUT}$ = +0dBm/Tone (Two-tone parameters)
- 1MHz Tone Spacing
- All temperatures are referenced to the exposed paddle
- Evaluation kit traces and connector losses are de-embedded

### 3.2.1. Typical Performance Characteristics

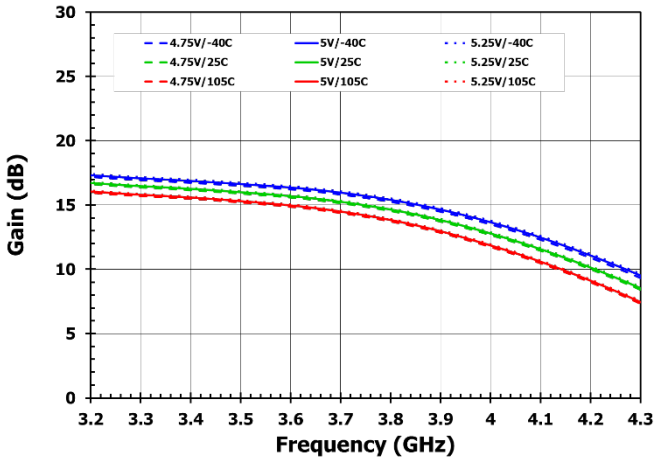



Figure 12. Gain

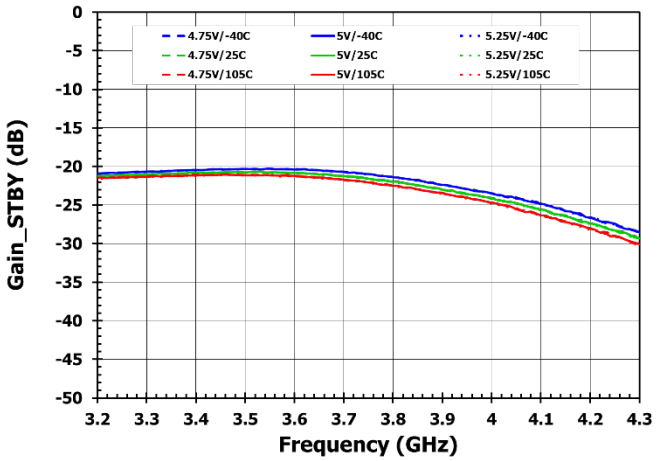



Figure 13. STBY Gain Mode

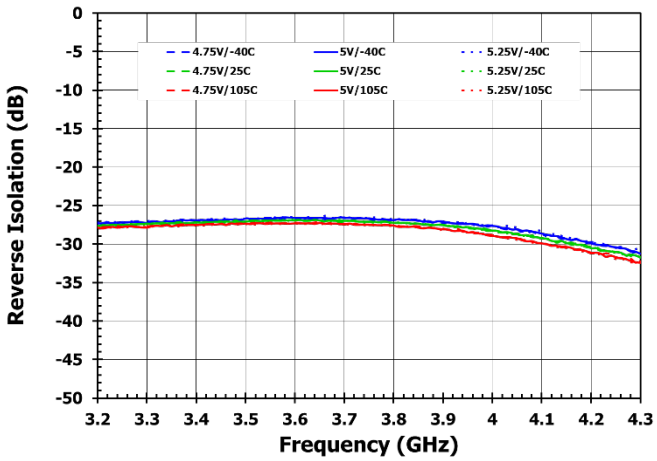



Figure 14. Reverse Isolation

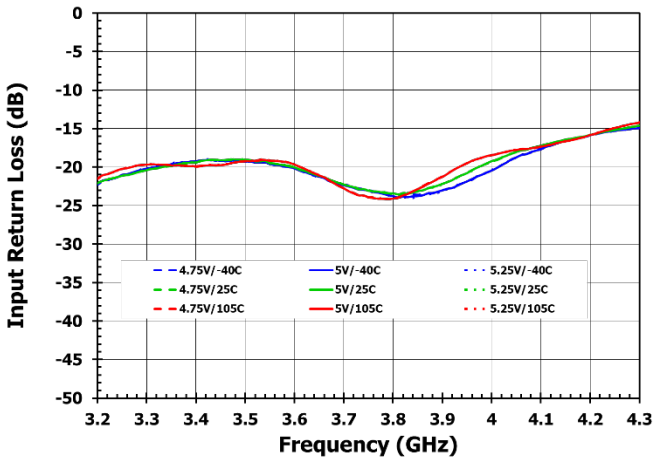



Figure 15. Input Return Loss



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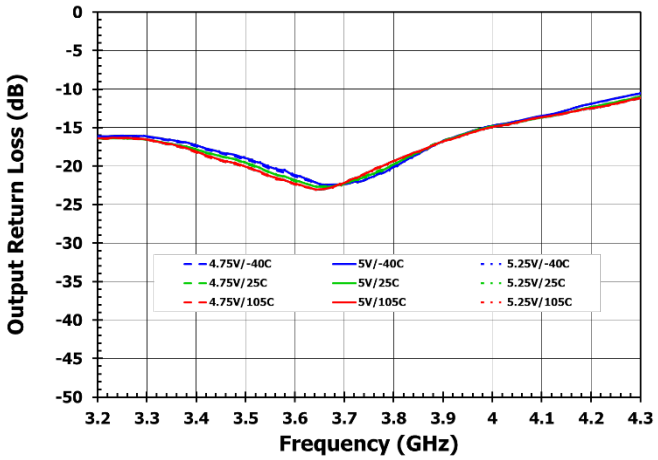



Figure 16. Output Return Loss

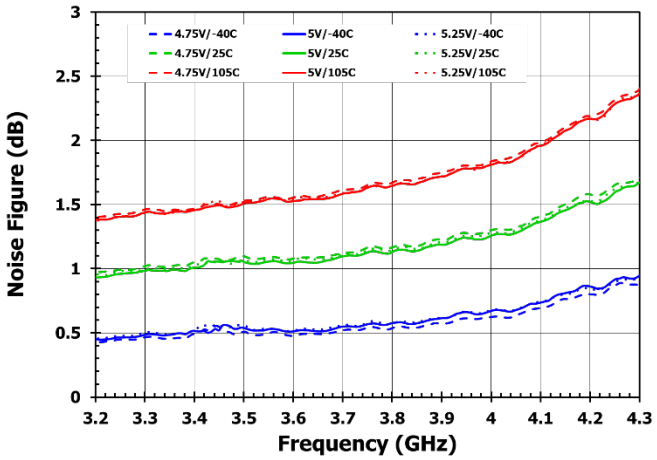



Figure 17. Noise Figure

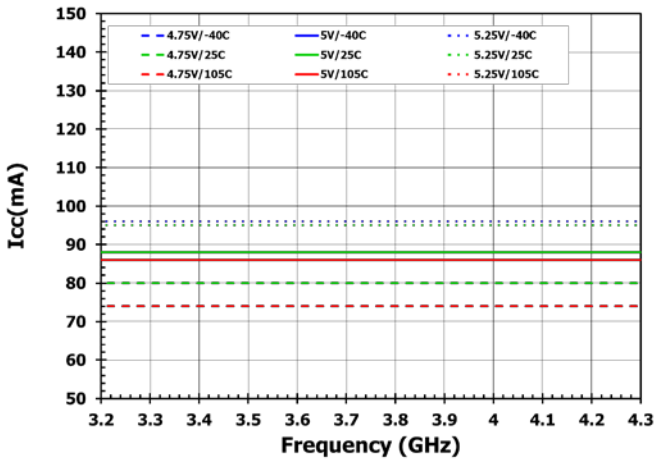



Figure 18. DC Current (Icc) Vs Frequency

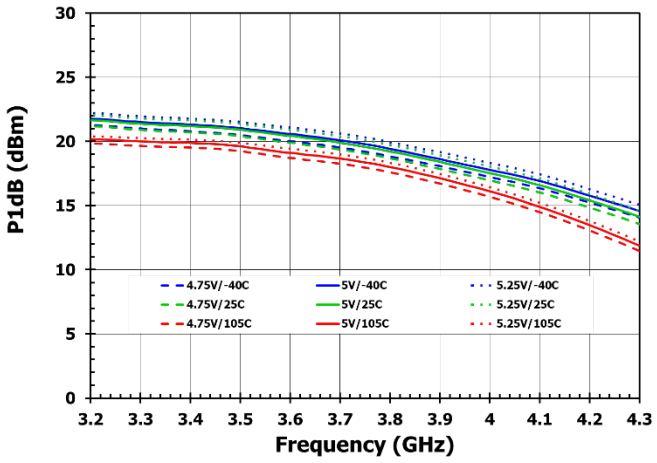



Figure 19. OP1dB

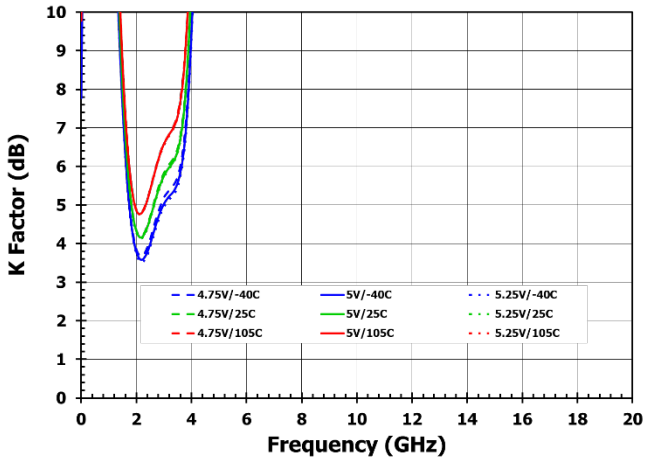



Figure 20. K Factor

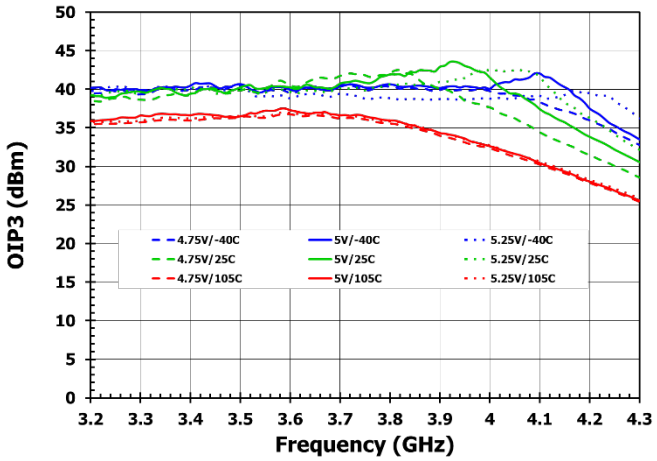



Figure 21. OIP3



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# 4. Functional Description

## 4.1 Programming

The F0111 uses two dedicated control pins (STBY1 and STBY2) to place each respective signal path into its standby mode. The following section provide specific details on the functionality of each pin.

## 4.2 STBY Mode Programming

The F0111 allows for the independent shutdown of each signal path. Simply apply the logic shown in Table 1 below to control paths 1 and 2, respectively.

**Table 1. STBY Mode Truth Table**

| Path | Pin | Logic | Path Power State |
|---|---|---|---|
| 1 | 15 / STBY1 | Low | Path 1 Power On |
| | | High | Path 1 Standby |
| 2 | 6 / STBY2 | Low | Path 2 Power On |
| | | High | Path 2 Standby |



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# 5. Evaluation Kit Information

## 5.1 Evaluation Kit Picture

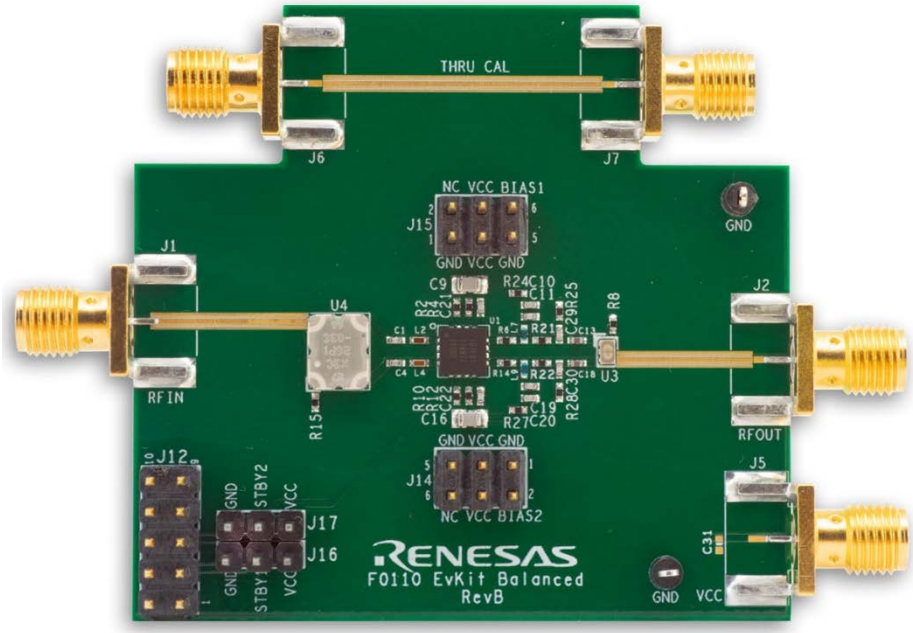



**Figure 22. Evaluation Kit Top View**

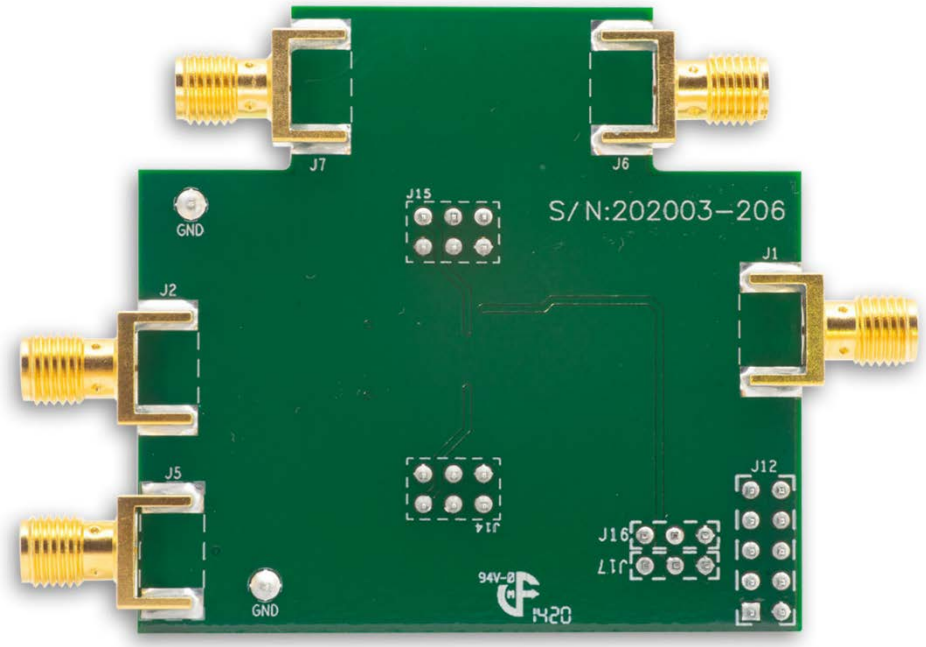



**Figure 23. Evaluation Kit Bottom View**



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## 5.2 Evaluation Kit Schematic

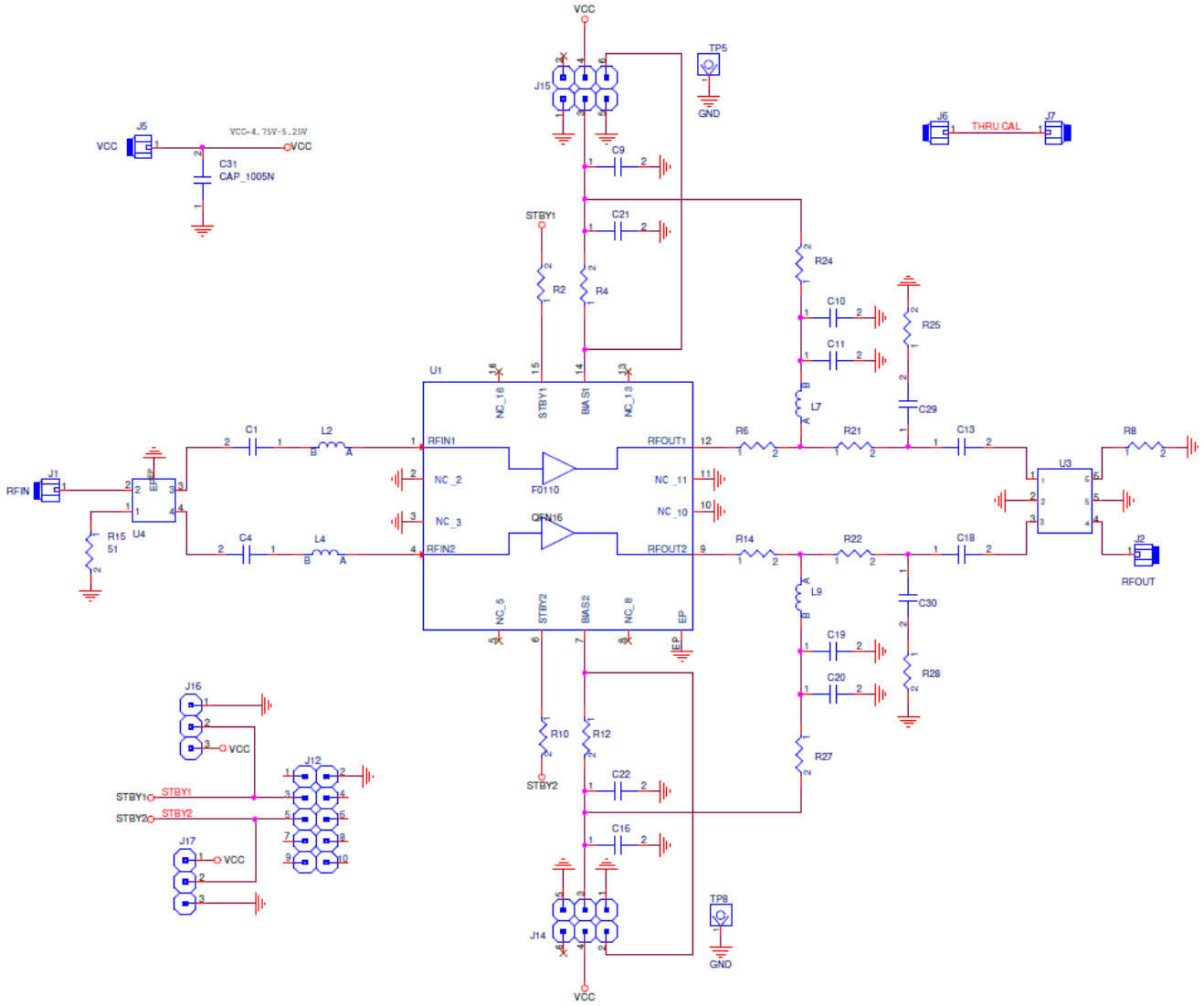



**Figure 24. Electrical Schematic**



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**Table 2. Bill of Materials (BOM) (2.5GHz to 2.7GHz)**

| Part Reference | QTY | Description | Manufacturer Part # | Manufacturer |
|---|---|---|---|---|
| C1, C4 | 2 | 10pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H100J | Murata |
| C13, C18 | 2 | 39pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H390J | Murata |
| C21, C22, C11, C19 | 4 | 100pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H101J | Murata |
| C9, C16 | 2 | 10,000pF ±10% 50V Ceramic Capacitor X7R (0805) | GRM216R71H103KA | Murata |
| C10, C20 | 2 | 1000pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H102J | Murata |
| C29, C30 | 2 | 0.8pF ±0.05pF, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1HR80W | Murata |
| L2, L4 | 2 | 1.2nH ±5%, Inductor (0402) | LQP15MN1N2B02 | Murata |
| L7, L9 | 2 | 2nH ±5%, Inductor 0402 | 0402CT-2N0XJR | Coilcraft |
| R4, R12 | 2 | 1.47kΩ ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1471X | Panasonic |
| R8, R15 | 2 | 51Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF51R0X | Panasonic |
| R2, R6, R10, R14, R21, R22 | 6 | 0Ω Resistors (0402) | ERJ-2GE0R00X | Panasonic |
| R24, R25, R27, R28 | 4 | 0Ω Resistors (0402) | ERJ-2GE0R00X | Panasonic |
| U4 | 1 | Hybrid Coupler | X3C26P1-03S | Anaren |
| U3 | 1 | Hybrid Coupler | C2327J5003AHF | Anaren |
| U1 | 1 | F0111 | Renesas | Renesas |
| J14, J15 | 2 | CONN HEADER VERT DBL 3x2 POS GOLD | | 3M |
| J12 | 1 | CONN HEADER VERT DBL 5x2 POS GOLD | 961210-6404-AR | 3M |
| J17, J18 | 2 | CONN HEADER VERT DBL 3x1 POS GOLD | | 3M |
| J1, J2, J5, J6, J7 | 5 | Edge Launch SMA (0.375inch pitch ground, tab) (50Ω) | 142-0701-851 | Emerson Johnson |
| | 1 | Printed Circuit Board (Rev B) | Renesas | Renesas |
| C31 | 1 | DNP | | |



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**Table 3. Bill of Materials (BOM) (3.3GHz to 4.2GHz)**

| Part Reference | QTY | Description | Manufacturer Part # | Manufacturer |
|---|---|---|---|---|
| C1, C4 | 2 | 10pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H100J | Murata |
| C13, C18 | 2 | 39pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H390J | Murata |
| C21, C22, C11, C19 | 4 | 100pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H101J | Murata |
| C9, C16 | 2 | 10,000pF ±10% 50V Ceramic Capacitor X7R (0805) | GRM216R71H103KA | Murata |
| C10, C20 | 2 | 1000pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H102J | Murata |
| C29, C30 | 2 | 0.6pF ±0.05pF, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1HR60W | Murata |
| L2, L4 | 2 | 1.2nH ±5%, Inductor (0402) | LQP15MN1N2B02 | Murata |
| L7, L9 | 2 | 2nH ±5%, Inductor 0402 | 0402CT-2N0XJR | Coilcraft |
| R4, R12 | 2 | 1.47kΩ ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1471X | Panasonic |
| R8, R15 | 2 | 51Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF51R0X | Panasonic |
| R2, R6, R10, R14, R21, R22 | 6 | 0Ω Resistors (0402) | ERJ-2GE0R00X | Panasonic |
| R24, R25, R27, R28 | 4 | 0Ω Resistors (0402) | ERJ-2GE0R00X | Panasonic |
| U4 | 1 | Hybrid Coupler | XC3500P-03S | Anaren |
| U3 | 1 | Hybrid Coupler | C3337J5003AHF | Anaren |
| U1 | 1 | F0111 | Renesas | Renesas |
| J14, J15 | 2 | CONN HEADER VERT DBL 3x2 POS GOLD | | 3M |
| J12 | 1 | CONN HEADER VERT DBL 5x2 POS GOLD | 961210-6404-AR | 3M |
| J17, J18 | 2 | CONN HEADER VERT DBL 3x1 POS GOLD | | 3M |
| J1, J2, J5, J6, J7 | 5 | Edge Launch SMA (0.375inch pitch ground, tab) (50Ω) | 142-0701-851 | Emerson Johnson |
| | 1 | Printed Circuit Board (Rev B) | Renesas | Renesas |
| C31 | 1 | DNP | | |

## 5.3 Evaluation Kit Operation

### 5.3.1. Power Supply Setup

Set up a power supply in the voltage range of 4.75V to 5.25V with the power supply output disabled. The voltage can be applied using one of the following connections:

- Directly to the J5 SMA and connecting Pins 3 and 4 together on both J14 and J15.
- Directly to Pin 3 on both J14 and J15.

### 5.3.2. Power-On Procedure

Set up the voltage supplies, and Evaluation Board as described in the Power Supply Setup section and Enable the $V_{CC}$ supply. Make sure the correct logic voltage is applied to the STBY pins on each path as defined in Table 1.

### 5.3.3. Power-Off Procedure

Disable the $V_{CC}$ supply.



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# 6. Application Information

The F0111 has been optimized for use in high performance RF applications ranging from 2.5GHz to 2.7GHz and from 3.3GHz and 4.2GHz. For specific Bill of Material (BOM), see Table 2 and Table 3.

## 6.1 Power Supplies

Use a common $V_{CC}$ power supply for all pins requiring DC power. Bypass all supply pins with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change, or transients should have a slew rate smaller than 1V/20µs. In addition, keep all control pins at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

## 6.2 Start-up Condition

At device power-up, both channels default to the power state as determined by the logic present on the STBY1 and STBY2 pins.

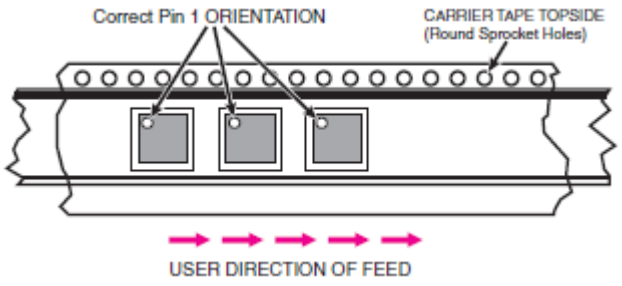
# 7. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

# 8. Ordering Information

| Part Number | Package | MSL Rating | Carrier Type | Temp. Range |
|---|---|---|---|---|
| F0111NBTI | 4 × 4 × 0.75 mm 16-VFQFPN | 1 | Tray | -40° to +105°C |
| F0111NBTI8 | 4 × 4 × 0.75 mm 16-VFQFPN | 1 | Tape and Reel | -40° to +105°C |
| F0111EVB-2P6 | Evaluation Board (2.5GHz to 2.7GHz) | | | |
| F0111EVB-3P5 | Evaluation Board (3.3GHz to 4.2GHz) | | | |

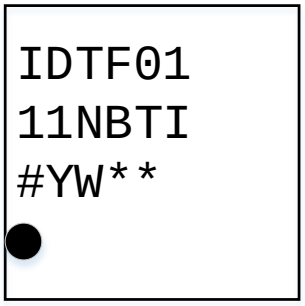
**Table 4. Pin1 Orientation in Tape and Reel Packaging**

| Part Number Suffix | Pin 1 Orientation | Illustration |
|---|---|---|
| BTI8 | Quadrant 1 (EIA-481-C) |   |



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# 9. Marking Diagram




- Line 1 and 2 are the part number.
- Line 2:
  - "NBT" is for package code.
  - "I" is for Industrial Grade.
- Line 3:
  - "#" is for die version.
  - "YW" are for year and week that the part was assembled.
  - "**" is for assembly lot number.

# 10. Revision History

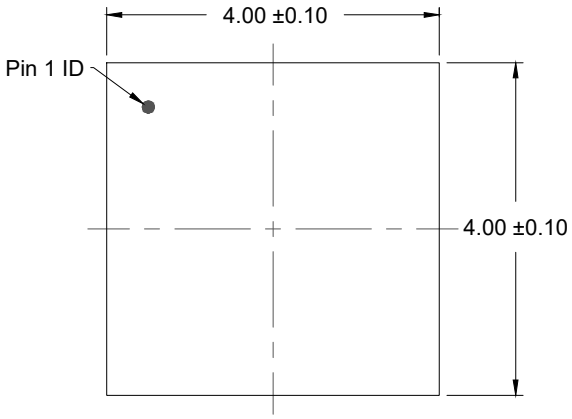
| Revision | Date | Description |
|---|---|---|
| 1.07 | Jan 13, 2022 | • Added Tape and Reel Information (Table 4). |
| 1.06 | Aug 02, 2021 | • Modified the pin descriptions of 2, 3, 10, 11 to NC, and updated the relevant pin map and symbol in schematic to NC.<br>• Changed HBM back to 500V in Absolute Maximum Ratings. |
| 1.05 | May 10, 2021 | • Added 3.3GHz – 4.2GHz frequency range information.<br>• Updated minimum frequency range from 2500MHz to 2200MHz.<br>• Updated EVK ordering information. |
| 1.04 | Apr 13, 2021 | Update Ordering Information. |
| 1.03 | Mar 19, 2021 | Updated HBM rating data from 500V to 1kV. |
| 1.02 | Feb 09, 2021 | Added RF performance table, Typical Performance Characteristics and Bill of Materials for 3.3GHz – 4.2GHz frequency range. |
| 1.01 | Oct 14, 2020 | Updated RF Performance table and Typical Performance Characteristics. |
| 1.00 | Aug 28, 2020 | Initial release. |



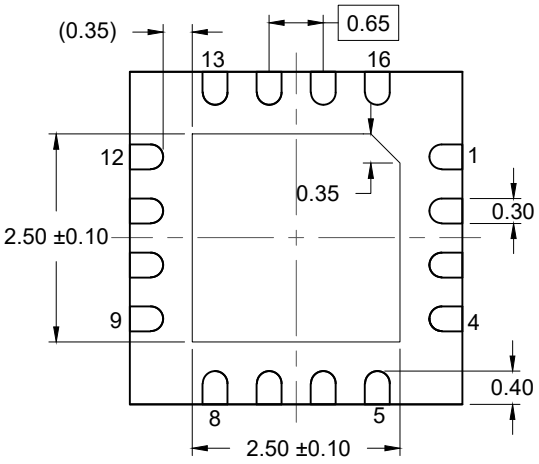
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# Package Outline Drawing

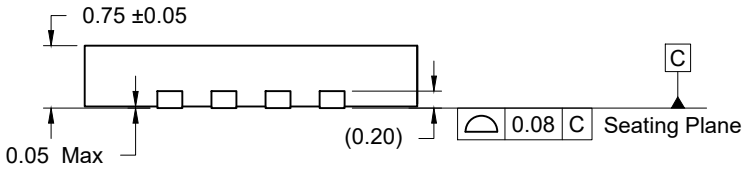
Package Code: NBT16P1
16-VFQFPN 4.0 x 4.0 x 0.75 mm Body, 0.65mm Pitch
PSC-4809-01, Revision: 02, Date Created: Jul 9, 2024



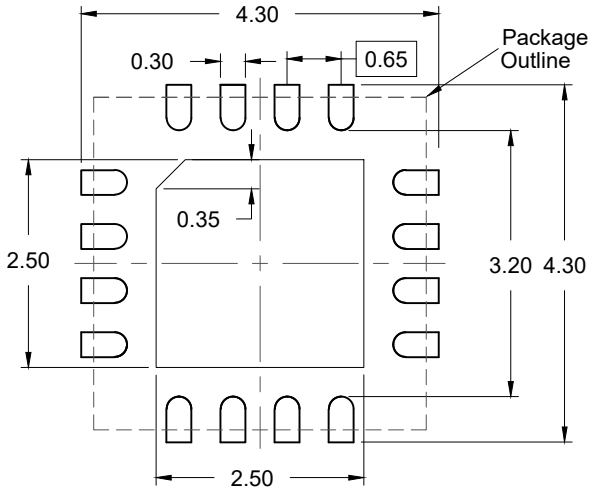

TOP VIEW




BOTTOM VIEW




SIDE VIEW




RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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