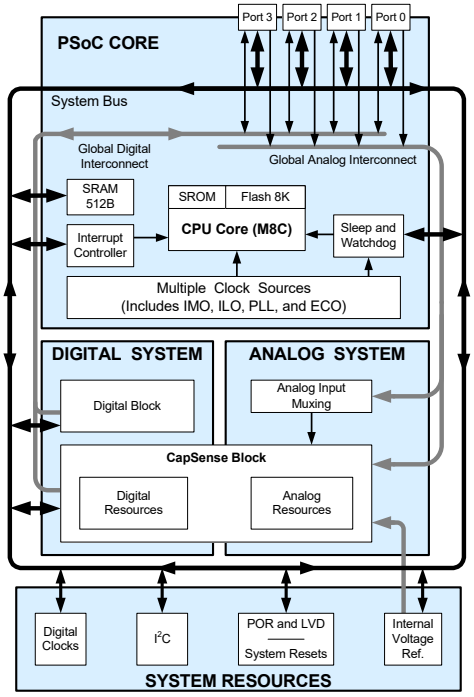
CY8C21312
CY8C21512

# Automotive PSoC® Programmable System-on-Chip™

## Features

- Automotive Electronics Council (AEC) Q100 qualified
- Powerful Harvard-architecture processor
  - M8C processor speeds up to 24 MHz
  - Low power at high speed
  - Operating voltage: 3.0 V to 5.25 V
  - Automotive temperature range: –40 °C to +85 °C
- Advanced peripherals
  - One CapSense® block:
    - Provides configurable capacitive sensing elements
    - Supports combination of CapSense buttons, sliders, touchpads, and proximity sensors
  - One limited digital PSoC® block provides:
    - 8-bit timer, counter, or pulse-width modulator (PWM)
    - Half-duplex UART
    - SPI slave
    - Connectable to all general purpose I/O (GPIO) pins
- Flexible on-chip memory
  - 8 KB flash program storage
  - 512 bytes SRAM data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Complete development tools
  - Free development software (PSoC Designer™)
  - Full-featured in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Precision, programmable clocking
  - Internal ±5% 24 MHz oscillator
  - Internal low-speed, low-power oscillator for Watchdog and Sleep functionality
  - Optional external oscillator, up to 24 MHz
- Programmable pin configurations
  - 25 mA sink, 10 mA drive on all GPIOs
  - Pull-up, pull-down, high Z, strong, or open drain drive modes on all GPIOs
  - Analog input on all GPIOs
  - Configurable interrupt on all GPIOs
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
- Additional system resources
  - Inter-Integrated Circuit ($I^2C$™) master, slave, or multi-master operation up to 400 kHz
  - Watchdog and sleep timers
  - User-configurable low-voltage detection (LVD)
  - Integrated supervisory circuit
  - On-chip precision voltage reference

## Logic Block Diagram






Downloaded from Arrow.com.

## Contents

**PSoC Functional Overview ..... 3**
The PSoC Core ..... 3
The Digital System ..... 3
The Analog System ..... 4
Additional System Resources ..... 4
PSoC Device Characteristics ..... 5
**Getting Started ..... 5**
Application Notes ..... 5
Development Kits ..... 5
Training ..... 5
CYPros Consultants ..... 5
Solutions Library ..... 5
Technical Support ..... 5
**Development Tools ..... 6**
PSoC Designer Software Subsystems ..... 6
**Designing with PSoC Designer ..... 7**
Select Components ..... 7
Configure Components ..... 7
Organize and Connect ..... 7
Generate, Verify, and Debug ..... 7
**Pinouts ..... 8**
20-Pin Part Pinout ..... 8
28-Pin Part Pinout ..... 9
**Registers ..... 10**
Register Conventions ..... 10
Register Mapping Tables ..... 10
**Electrical Specifications ..... 13**
Absolute Maximum Ratings ..... 14
Operating Temperature ..... 14
DC Electrical Characteristics ..... 15
AC Electrical Characteristics ..... 18
**Packaging Information ..... 23**
Packaging Diagram ..... 23
Thermal Impedances ..... 24
Solder Reflow Specifications ..... 24
Tape and Reel Information ..... 25
**Development Tool Selection ..... 27**
Software ..... 27
Development Kits ..... 27
Evaluation Tools ..... 27
Device Programmers ..... 28
Accessories (Emulation and Programming) ..... 28
**Ordering Information ..... 29**
Ordering Code Definitions ..... 29
**Acronyms ..... 30**
**Reference Documents ..... 30**
**Document Conventions ..... 31**
Units of Measure ..... 31
**Numeric Conventions ..... 31**
**Glossary ..... 31**
**Document History Page ..... 36**
**Sales, Solutions, and Legal Information ..... 38**
Worldwide Sales and Design Support ..... 38
Products ..... 38
PSoC® Solutions ..... 38
Cypress Developer Community ..... 38
Technical Support ..... 38



Downloaded from Arrow.com.

## PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, as illustrated in the Logic Block Diagram on page 1, comprises of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow all the device resources to be combined into a complete custom system. Each CY8C21x12 device includes one limited digital block and one CapSense block. Depending on the PSoC package, up to 24 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

### The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep, and watchdog timers, and an internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability, such as digital clocks for increased flexibility, $I^2C$ functionality for implementing an $I^2C$ master, slave, or multi-master, an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems, and various system resets supported by the M8C.

The Digital System is composed of a programmable limited digital block and fixed-function digital resources inside the CapSense block. The limited digital block can be configured into a number of digital peripherals. The fixed-function digital resources in the CapSense block provide external modulation signals, measurement timing, and measurement conversion. The digital resources can be connected to the GPIO through a series of global buses that provide very flexible routing options.

The Analog System is composed of a comparator and a filter that are used in the CapSense block to implement capacitive sensing measurement.

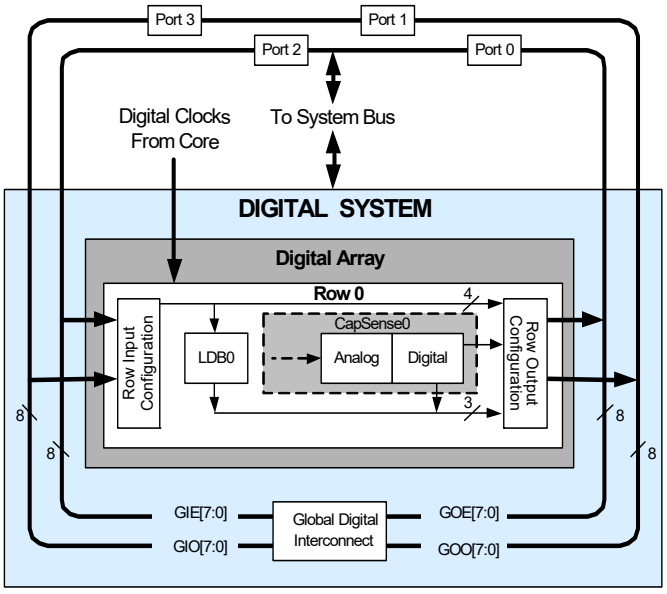
### The Digital System

The Digital System is composed of one digital block. This block is an 8-bit resource that can implement various 8-bit digital peripherals. Digital peripheral configurations include those listed.

- PWM (8-bit)
- Counter (8-bit)
- Timer (8-bit)
- Half-duplex 8-bit UART with selectable parity
- SPI slave
- $I^2C$ master, slave, or multi-master (implemented in a dedicated $I^2C$ block)

The digital block can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

**Figure 1. Digital System Block Diagram**





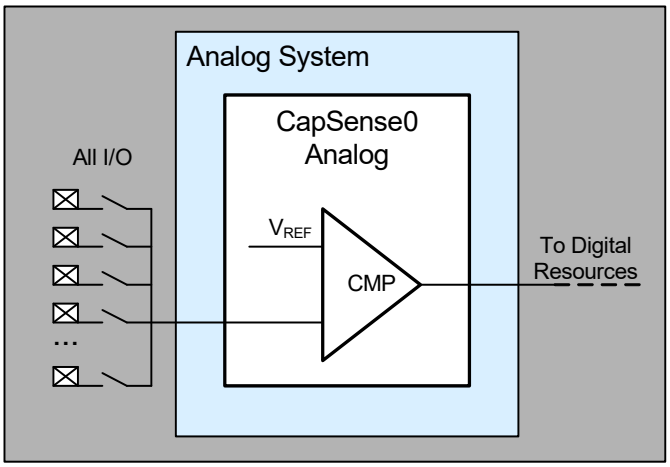

Downloaded from Arrow.com.

## The Analog System

The Analog System is composed of analog resources inside of the CapSense block. These resources are used to implement a flexible capacitive sensing and measurement module. The analog resources in the CapSense block are listed.

- Comparator used in capacitance-to-digital conversion
- Fixed, absolute reference or adjustable, ratiometric reference can be used with the comparator
- Low-pass filter converts a digital bit stream into the adjustable, ratiometric analog reference

**Figure 2. Analog System Block Diagram**




*The Analog Multiplexer System*

The Analog Mux Bus can connect to every GPIO pin. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system. Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combination.

## Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful for complete systems. Brief statements describing the merits of each system resource are presented.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems.
- The $I^2C$ module provides communication up to 400 kHz over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system.
- Versatile analog multiplexer system.



Downloaded from Arrow.com.

### PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in Table 1

**Table 1. PSoC Device Characteristics**

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---|---|---|---|---|---|---|---|---|---|
| CY8C29x66[1] | up to 64 | 4 | 16 | up to 12 | 4 | 4 | 12 | 2K | 32K |
| CY8C28xxx | up to 44 | up to 3 | up to 12 | up to 44 | up to 4 | up to 6 | up to 12 + 4[2] | 1K | 16K |
| CY8C27x43 | up to 44 | 2 | 8 | up to 12 | 4 | 4 | 12 | 256 | 16K |
| CY8C24x94[1] | up to 56 | 1 | 4 | up to 48 | 2 | 2 | 6 | 1K | 16K |
| CY8C24x23A[1] | up to 24 | 1 | 4 | up to 12 | 2 | 2 | 6 | 256 | 4K |
| CY8C23x33 | up to 26 | 1 | 4 | up to 12 | 2 | 2 | 4 | 256 | 8K |
| CY8C22x45[1] | up to 38 | 2 | 8 | up to 38 | 0 | 4 | 6[2] | 1K | 16K |
| CY8C21x45[1] | up to 24 | 1 | 4 | up to 24 | 0 | 4 | 6[2] | 512 | 8K |
| CY8C21x34[1] | up to 28 | 1 | 4 | 28 | 0 | 2 | 4[2] | 512 | 8K |
| CY8C21x23 | up to 16 | 1 | 4 | up to 8 | 0 | 2 | 4[2] | 256 | 4K |
| CY8C21x12[1] | up to 24 | 1 | 1[2] | 24 | 0 | 0 | 1[2] | 512 | 8K |
| CY8C20x34[1] | up to 28 | 0 | 0 | up to 28 | 0 | 0 | 3[2,3] | 512 | 8K |
| CY8C20xx6 | up to 36 | 0 | 0 | up to 36 | 0 | 0 | 3[2,3] | up to 2K | up to 32K |

## Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

### Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

### Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

### Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

### Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

### Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

**Notes**
1. Automotive qualified devices available in this group.
2. Limited analog functionality.
3. Two analog blocks and one CapSense® block.



Downloaded from Arrow.com.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software $I^2C$ slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

### PSoC Designer Software Subsystems

*Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

*Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers**. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

**C Language Compilers**. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

*Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

*In-Circuit Emulator*

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.



Downloaded from Arrow.com.

## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

### Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.



Downloaded from Arrow.com.

## Pinouts

TheCY8C21x12 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, $V_{SS}$, $V_{DD}$, and XRES are not capable of digital I/O.

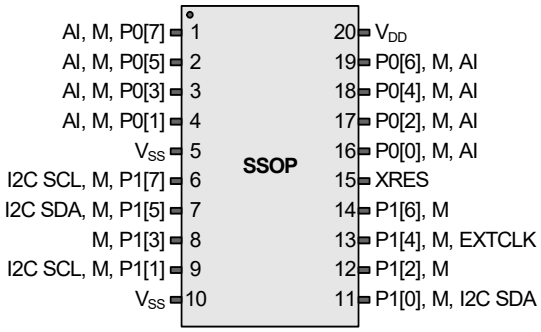
### 20-Pin Part Pinout

**Table 2. 20-Pin Part Pinout (shrink small-outline package (SSOP))**

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I, M | P0[7] | Analog column mux input |
| 2 | I/O | I, M | P0[5] | Analog column mux input |
| 3 | I/O | I, M | P0[3] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 4 | I/O | I, M | P0[1] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 5 | Power | | $V_{SS}$ | Ground connection |
| 6 | I/O | M | P1[7] | $I^2C$ serial clock (SCL) |
| 7 | I/O | M | P1[5] | $I^2C$ serial data (SDA) |
| 8 | I/O | M | P1[3] | |
| 9 | I/O | M | P1[1] | $I^2C$ SCL, ISSP-SCLK[4] |
| 10 | Power | | $V_{SS}$ | Ground connection |
| 11 | I/O | M | P1[0] | $I^2C$ SDA, ISSP-SDATA[4] |
| 12 | I/O | M | P1[2] | |
| 13 | I/O | M | P1[4] | Optional external clock input (EXTCLK) |
| 14 | I/O | M | P1[6] | |
| 15 | Input | | XRES | Active high external reset with internal pull-down |
| 16 | I/O | I, M | P0[0] | Analog column mux input |
| 17 | I/O | I, M | P0[2] | Analog column mux input |
| 18 | I/O | I, M | P0[4] | Analog column mux input |
| 19 | I/O | I, M | P0[6] | Analog column mux input |
| 20 | Power | | $V_{DD}$ | Supply voltage |

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

**Figure 3. CY8C21312 20-Pin PSoC Device**




**Note**
4. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoC Technical Reference Manual* for details.



Downloaded from Arrow.com.

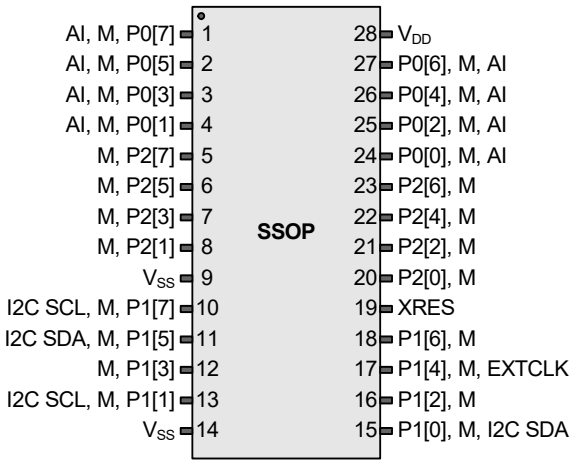
## 28-Pin Part Pinout

### Table 3. 28-Pin Part Pinout (SSOP)

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I, M | P0[7] | Analog column mux input |
| 2 | I/O | I, M | P0[5] | Analog column mux input |
| 3 | I/O | I, M | P0[3] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 4 | I/O | I, M | P0[1] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 5 | I/O | M | P2[7] | |
| 6 | I/O | M | P2[5] | |
| 7 | I/O | M | P2[3] | |
| 8 | I/O | M | P2[1] | |
| 9 | Power | | $V_{SS}$ | Ground connection |
| 10 | I/O | M | P1[7] | $I^2C$ SCL |
| 11 | I/O | M | P1[5] | $I^2C$ SDA |
| 12 | I/O | M | P1[3] | |
| 13 | I/O | M | P1[1] | $I^2C$ SCL, ISSP-SCLK[5] |
| 14 | Power | | $V_{SS}$ | Ground connection |
| 15 | I/O | M | P1[0] | $I^2C$ SDA, ISSP-SDATA[5] |
| 16 | I/O | M | P1[2] | |
| 17 | I/O | M | P1[4] | Optional EXTCLK |
| 18 | I/O | M | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull-down |
| 20 | I/O | M | P2[0] | |
| 21 | I/O | M | P2[2] | |
| 22 | I/O | M | P2[4] | |
| 23 | I/O | M | P2[6] | |
| 24 | I/O | I, M | P0[0] | Analog column mux input |
| 25 | I/O | I, M | P0[2] | Analog column mux input |
| 26 | I/O | I, M | P0[4] | Analog column mux input |
| 27 | I/O | I, M | P0[6] | Analog column mux input |
| 28 | Power | | $V_{DD}$ | Supply voltage |

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

### Figure 4. CY8C21512 28-Pin PSoC Device




**Note**
5. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoC Technical Reference Manual* for details.



Downloaded from Arrow.com.

# Registers

## Register Conventions

This section lists the registers of the CY8C21x12 PSoC device. For detailed register information, refer to the *PSoC Technical Reference Manual*.

The register conventions specific to this section are listed in the following table.

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

## Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, bank 0 and bank 1. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set to ‘1’, the user is in bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and must not be accessed.



Downloaded from Arrow.com.

**Table 4. Register Map 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | | 80 | | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | CSREF_CR1 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2IE | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2GS | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | CUR_PP | D0 | RW |
| | 11 | | | 51 | | | 91 | | STK_PP | D1 | RW |
| | 12 | | | 52 | | | 92 | | | D2 | |
| | 13 | | | 53 | | | 93 | | IDX_PP | D3 | RW |
| | 14 | | | 54 | | | 94 | | MVR_PP | D4 | RW |
| | 15 | | | 55 | | | 95 | | MVW_PP | D5 | RW |
| | 16 | | | 56 | | | 96 | | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | | 97 | | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| CSCNT_DR0 | 20 | # | | 60 | | | A0 | | INT_MSK0 | E0 | RW |
| CSCNT_DR1 | 21 | W | AMUX_CFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| CSCNT_DR2 | 22 | RW | CSCMP_CR0 | 62 | RW | | A2 | | INT_VC | E2 | RC |
| CSCNT_CR0 | 23 | # | | 63 | | | A3 | | RES_WDT | E3 | W |
| CSMOD0_DR0 | 24 | # | CSCMP_CR1 | 64 | # | | A4 | | | E4 | |
| CSMOD0_DR1 | 25 | W | | 65 | | | A5 | | | E5 | |
| CSMOD0_DR2 | 26 | RW | CSCMP_CR2 | 66 | RW | | A6 | | CSCMP_CR5 | E6 | RW |
| CSMOD0_CR0 | 27 | # | | 67 | | | A7 | | CSCMP_CR6 | E7 | RW |
| CSMOD1_DR0 | 28 | # | | 68 | | | A8 | | | E8 | |
| CSMOD1_DR1 | 29 | W | CSREF_CR0 | 69 | # | | A9 | | | E9 | |
| CSMOD1_DR2 | 2A | RW | | 6A | | | AA | | | EA | |
| CSMOD1_CR0 | 2B | # | | 6B | | | AB | | | EB | |
| LDB0_DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | | EC | |
| LDB0_DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | | ED | |
| LDB0_DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| LDB0_CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | | 72 | | RDI0IS | B2 | RW | | F2 | |
| | 33 | | | 73 | | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | CSCMP_CR3 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | CSCMP_CR4 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed. # Access is bit specific.



Downloaded from Arrow.com.

**Table 5. Register Map 1 Table: Configuration Space**

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | | 80 | | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | | 84 | | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | | 91 | | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | | 92 | | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | | 93 | | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | | 94 | | | D4 | |
| | 15 | | | 55 | | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | | D6 | |
| | 17 | | | 57 | | | 97 | | | D7 | |
| | 18 | | | 58 | | | 98 | | MUX_CR0 | D8 | RW |
| | 19 | | | 59 | | | 99 | | MUX_CR1 | D9 | RW |
| | 1A | | | 5A | | | 9A | | MUX_CR2 | DA | RW |
| | 1B | | | 5B | | | 9B | | MUX_CR3 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | | DD | |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| CSCNT_CR1 | 20 | RW | CSCLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| CSCNT_CR2 | 21 | RW | CSCLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| CSCNT_CR3 | 22 | RW | | 62 | | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | CSREF_CR2 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| CSMOD0_CR1 | 24 | RW | CSCMP_CR7 | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| CSMOD0_CR2 | 25 | RW | | 65 | | | A5 | | | E5 | |
| CSMOD0_CR3 | 26 | RW | CSREF_CR3 | 66 | RW | | A6 | | CSREF_CR4 | E6 | RW |
| | 27 | | CSCMP_CR8 | 67 | RW | | A7 | | | E7 | |
| CSMOD1_CR1 | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| CSMOD1_CR2 | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| CSMOD1_CR3 | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | CSCLK_CR2 | 6B | RW | | AB | | ECO_TR | EB | W |
| LDB0_FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| LDB0_IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| LDB0_OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | | 72 | | RDI0IS | B2 | RW | | F2 | |
| | 33 | | | 73 | | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | | 76 | | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | | 77 | | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed. # Access is bit specific.



Downloaded from Arrow.com.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x12 PSoC device. For the most up-to-date electrical specifications, visit the Cypress website at http://www.cypress.com.

Specifications are valid for –40 °C ≤ $T_A$ ≤ 85 °C and $T_J$ ≤ 100 °C as specified, except where noted. Refer to Table 12 on page 18 for the electrical specifications for the IMO using slow IMO (SLIMO) mode.

**Figure 5. Voltage versus CPU Frequency**

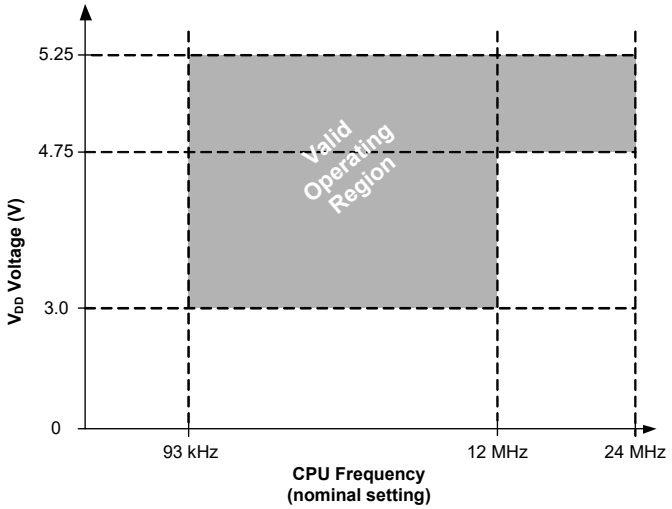
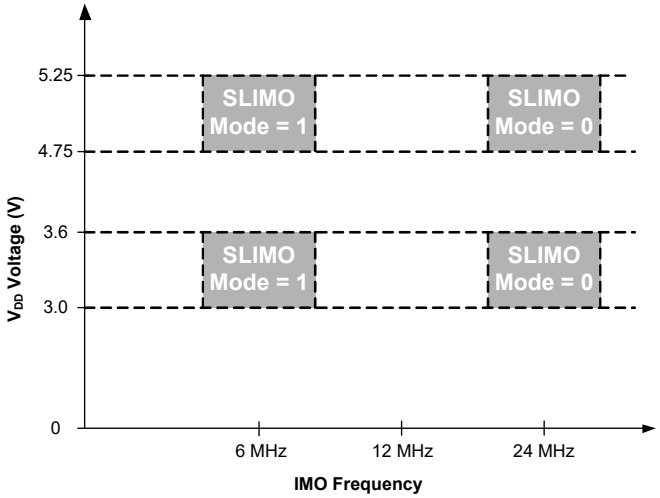



**Figure 6. IMO Frequency Trim Options**






Downloaded from Arrow.com.

### Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 25 | +100 | °C | Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the $Flash_{DR}$ electrical specification in Table 11 on page 17. |
| $T_{BAKETEMP}$ | Bake temperature | – | 125 | See package label | °C | |
| $t_{BAKETIME}$ | Bake time | See package label | – | 72 | Hours | |
| $T_A$ | Ambient temperature with power applied | –40 | – | +85 | °C | |
| $V_{DD}$ | Supply voltage on $V_{DD}$ relative to $V_{SS}$ | –0.5 | – | +6.0 | V | |
| $V_{IO}$ | DC input voltage | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V | |
| $V_{IOZ}$ | DC voltage applied to tri-state | $V_{SS}$ – 0.5 | – | $V_{DD}$ + 0.5 | V | |
| $I_{MIO}$ | Maximum current into any port pin | –25 | – | +50 | mA | |
| ESD | Electrostatic discharge voltage | 2000 | – | – | V | Human Body Model ESD |
| LU | Latch up current | – | – | 200 | mA | |

### Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | –40 | – | +85 | °C | |
| $T_J$ | Junction temperature | –40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 24. The user must limit the power consumption to comply with this requirement. |



Downloaded from Arrow.com.

## DC Electrical Characteristics

*DC Chip Level Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 6. DC Chip Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3.0 | – | 5.25 | V | See table titled DC POR and LVD Specifications on page 16 |
| $I_{DD}$ | Supply current, IMO = 24 MHz | – | 4 | 6 | mA | Conditions are $V_{DD}$ = 5.25 V, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz |
| $I_{DD3}$ | Supply current, IMO = 6 MHz using SLIMO mode | – | 2 | 4 | mA | Conditions are $V_{DD}$ = 3.3 V, CPU = 3 MHz, 48 MHz disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz |
| $I_{SB1}$ | Sleep (mode) current with POR, LVD, sleep timer, WDT, and ILO active | – | 2.8 | 7 | µA | $V_{DD}$ = 3.3 V, –40 °C ≤ $T_A$ ≤ 85 °C |
| $I_{SB2}$ | Sleep (mode) current with POR, LVD, sleep timer, WDT, and ILO active | – | 5 | 15 | µA | $V_{DD}$ = 5.25 V, –40 °C ≤ $T_A$ ≤ 85 °C |
| $V_{REF}$ | Reference voltage (Bandgap) | 1.28 | 1.30 | 1.32 | V | Trimmed for appropriate $V_{DD}$ range |

*DC GPIO Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 7. DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull-down resistor | 4 | 5.6 | 8 | kΩ | Also applies to the internal pull-down resistor on the XRES pin |
| $V_{OH}$ | High output level | $V_{DD}$ – 1.0 | – | – | V | $I_{OH}$ = 10 mA, $V_{DD}$ = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])) |
| $V_{OL}$ | Low output level | – | – | 0.75 | V | $I_{OL}$ = 25 mA, $V_{DD}$ = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])) |
| $I_{OH}$ | High level source current | 10 | – | – | mA | $V_{OH}$ ≥ $V_{DD}$ – 1.0 V, see the limitations of the total current in the note for $V_{OH}$ |
| $I_{OL}$ | Low level sink current | 25 | – | – | mA | $V_{OL}$ ≤ 0.75 V, see the limitations of the total current in the note for $V_{OL}$ |
| $V_{IL}$ | Input low level | – | – | 0.8 | V | |
| $V_{IH}$ | Input high level | 2.1 | – | | V | |
| $V_H$ | Input hysteresis | – | 60 | – | mV | |
| $I_{IL}$ | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 µA. |
| $C_{IN}$ | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent Temp = 25 °C |
| $C_{OUT}$ | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent Temp = 25 °C |



Downloaded from Arrow.com.

*DC Comparator Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.
These comparator electrical specifications apply to the comparator in the CapSense block.

**Table 8. DC Comparator Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSCMP}$ | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| $TCV_{OSCMP}$ | Average input offset voltage drift | – | 10 | – | µV/°C | |
| $I_{EBCMP}$[6] | Input leakage current (Port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 µA |
| $C_{INCMP}$ | Input capacitance (Port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent Temp = 25 °C |
| $V_{CMCMP}$ | Common mode voltage range | 0.0 | – | $V_{DD}$ – 1 | V | |
| $G_{OLCMP}$ | Open loop gain | – | 80 | – | dB | |
| $I_{SCMP}$ | Supply current | | | | | |
| | 3.0 V ≤ $V_{DD}$ ≤ 3.6 V | – | 30 | – | µA | |
| | 4.75 V ≤ $V_{DD}$ ≤ 5.25 V | – | 35 | – | µA | |

*DC Analog Mux Bus Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 9. DC Analog Mux Bus Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{SW}$ | Switch resistance to common analog bus | – | – | 400 | Ω | |
| $R_{VDD}$ | Resistance of initialization switch to $V_{DD}$ | – | – | 800 | Ω | |

*DC POR and LVD Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 10. DC POR and LVD Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| | $V_{DD}$ value for precision POR (PPOR) trip | | | | | $V_{DD}$ must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog. |
| $V_{PPOR0}$ | PORLEV[1:0] = 00b | – | 2.36 | 2.40 | V | |
| $V_{PPOR1}$ | PORLEV[1:0] = 01b | – | 2.82 | 2.95 | V | |
| $V_{PPOR2}$ | PORLEV[1:0] = 10b | – | 4.55 | 4.70 | V | |
| | $V_{DD}$ value for LVD trip | | | | | |
| $V_{LVD1}$ | VM[2:0] = 001b | 2.85 | 2.92 | 2.99[7] | V | |
| $V_{LVD2}$ | VM[2:0] = 010b | 2.95 | 3.02 | 3.09 | V | |
| $V_{LVD3}$ | VM[2:0] = 011b | 3.06 | 3.13 | 3.20 | V | |
| $V_{LVD4}$ | VM[2:0] = 100b | 4.37 | 4.48 | 4.55 | V | |
| $V_{LVD5}$ | VM[2:0] = 101b | 4.50 | 4.64 | 4.75 | V | |
| $V_{LVD6}$ | VM[2:0] = 110b | 4.62 | 4.73 | 4.83 | V | |
| $V_{LVD7}$ | VM[2:0] = 111b | 4.71 | 4.81 | 4.95 | V | |

**Notes**
6. Atypical behavior: $I_{EBOA}$ of Port 0 Pin 0 is below 1 nA at 25 °C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 pA.
7. Always greater than 50 mV above $V_{PPOR1}$ (PORLEV[1:0] = 01b) for falling supply.



Downloaded from Arrow.com.

*DC Programming Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 11. DC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DDP}$ | $V_{DD}$ for programming and erase | 4.5 | 5 | 5.5 | V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDLV}$ | Low $V_{DD}$ for verify | 3.0 | 3.1 | 3.2 | V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDHV}$ | High $V_{DD}$ for verify | 5.1 | 5.2 | 5.3 | V | This specification applies to the functional requirements of external programmer tools |
| $V_{DDIWRITE}$ | Supply voltage for flash write operation | 3.0 | – | 5.25 | V | This specification applies to this device when it is executing internal flash writes |
| $I_{DDP}$ | Supply current during programming or verify | – | 5 | 25 | mA | |
| $V_{ILP}$ | Input low voltage during programming or verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input high voltage during programming or verify | 2.2 | – | – | V | |
| $I_{ILP}$ | Input current when applying $V_{ILP}$ to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull-down resistor |
| $I_{IHP}$ | Input current when applying $V_{IHP}$ to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull-down resistor |
| $V_{OLV}$ | Output low voltage during programming or verify | – | – | 0.75 | V | |
| $V_{OHV}$ | Output high voltage during programming or verify | $V_{DD}$ – 1.0 | – | $V_{DD}$ | V | |
| $Flash_{ENPB}$ | Flash endurance (per block)[8, 9] | 1,000 | – | – | – | Erase/write cycles per block |
| $Flash_{ENT}$ | Flash endurance (total)[9, 10] | 128,000 | – | – | – | Erase/write cycles |
| $Flash_{DR}$ | Flash data retention | 15 | – | – | Years | |

**Notes**

8. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.



Downloaded from Arrow.com.

## AC Electrical Characteristics

*AC Chip Level Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 12. AC Chip Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO24}$ | IMO frequency for 24 MHz | 22.8[11] | 24 | 25.2[11] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 0. |
| $F_{IMO6}$ | IMO frequency for 6 MHz | 5.5[11] | 6 | 6.5[11] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1. |
| $F_{CPU1}$ | CPU frequency (5 V $V_{DD}$ nominal) | 0.089[11] | 24 | 25.2[11] | MHz | 24 MHz only for SLIMO mode = 0 |
| $F_{CPU2}$ | CPU frequency (3.3 V $V_{DD}$ nominal) | 0.089[11] | 12 | 12.6[11] | MHz | |
| $F_{BLK5}$ | Digital PSoC block frequency (5 V $V_{DD}$ nominal) | 0 | 48 | 50.4[11,12] | MHz | Refer to the AC Digital Block Specifications below |
| $F_{BLK33.}$ | Digital PSoC block frequency (3.3 V $V_{DD}$ nominal) | 0 | 24 | 25.2[11, 12] | MHz | Refer to the AC Digital Block Specifications below |
| $F_{32K1}$ | ILO frequency | 15 | 32 | 64 | kHz | This specification applies when the ILO has been trimmed |
| $F_{32KU}$ | ILO untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C processor starts to execute, the ILO is not trimmed. |
| $t_{XRST}$ | External reset pulse width | 10 | – | – | µs | |
| DC24M | 24 MHz duty cycle | 40 | 50 | 60 | % | |
| $DC_{ILO}$ | ILO duty cycle | 20 | 50 | 80 | % | |
| Step24M | 24 MHz trim step size | – | 50 | – | kHz | |
| Fout48M | 48 MHz output frequency | 45.6[11] | 48.0 | 50.4[11] | MHz | |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output | – | – | 12.6 | MHz | |
| $SR_{POWERUP}$ | Power supply slew rate | – | – | 250 | V/ms | $V_{DD}$ slew rate during power-up |
| $t_{POWERUP}$ | Time between end of POR state and CPU code execution | – | 16 | 100 | ms | Power-up from 0 V. |
| $t_{JIT_IMO}$[13] | 24 MHz IMO cycle-to-cycle jitter (RMS) | – | 200 | 700 | ps | |
| | 24 MHz IMO long term N cycle-to-cycle jitter (RMS) | – | 300 | 900 | ps | N = 32 |
| | 24 MHz IMO period jitter (RMS) | – | 100 | 400 | ps | |

**Notes**
11. Accuracy derived from IMO with appropriate trim for $V_{DD}$ range.
12. See the individual user module datasheets for information on maximum frequencies for user modules.
13. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.



Downloaded from Arrow.com.

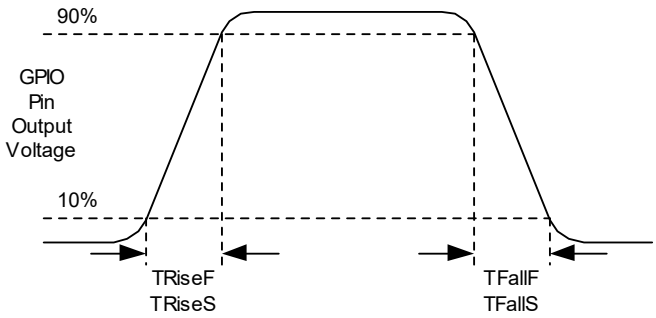
*AC GPIO Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 13. AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | 0 | – | 12.6 | MHz | Normal Strong Mode |
| TRiseF | Rise time, normal strong mode, Cload = 50 pF | 2 | 6 | 18 | ns | $V_{DD}$ = 4.75 to 5.25 V, 10% to 90% |
| TFallF | Fall time, normal strong mode, Cload = 50 pF | 2 | 6 | 18 | ns | $V_{DD}$ = 4.75 to 5.25 V, 10% to 90% |
| TRiseS | Rise time, slow strong mode, Cload = 50 pF | 7 | 27 | – | ns | $V_{DD}$ = 3 to 5.25 V, 10% to 90% |
| TFallS | Fall time, slow strong mode, Cload = 50 pF | 7 | 22 | – | ns | $V_{DD}$ = 3 to 5.25 V, 10% to 90% |

**Figure 7. GPIO Timing Diagram**






Downloaded from Arrow.com.

*AC Comparator Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

These comparator electrical specifications apply to the comparator in the CapSense block.

**Table 14. AC Comparator Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{COMP}$ | Response time, 50 mV overdrive | – | 75 | 100 | ns | |

*AC Digital Block Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 15. AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Timer | Input clock frequency | | | | | |
| | No capture, $V_{DD} \geq 4.75$ V | – | – | 50.4[15] | MHz | |
| | No capture, $V_{DD} < 4.75$ V | – | – | 25.2[15] | MHz | |
| | With capture | – | – | 25.2[15] | MHz | |
| | Capture pulse width | 50[14] | – | – | ns | |
| Counter | Input clock frequency | | | | | |
| | No enable input, $V_{DD} \geq 4.75$ V | – | – | 50.4[15] | MHz | |
| | No enable input, $V_{DD} < 4.75$ V | – | – | 25.2[15] | MHz | |
| | With enable input | – | – | 25.2[15] | MHz | |
| | Enable input pulse width | 50[14] | – | – | ns | |
| SPIS | Input clock (SCLK) frequency | – | – | 4.2[15] | MHz | The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_Negated between transmissions | 50[14] | – | – | ns | |
| Transmitter | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75$ V, 2 stop bits | – | – | 50.4[15] | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 stop bit | – | – | 25.2[15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2[15] | MHz | |
| Receiver | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75$ V, 2 stop bits | – | – | 50.4[15] | MHz | |
| | $V_{DD} \geq 4.75$ V, 1 stop bit | – | – | 25.2[15] | MHz | |
| | $V_{DD} < 4.75$ V | – | – | 25.2[15] | MHz | |

**Notes**
14. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).
15. Accuracy derived from IMO with appropriate trim for $V_{DD}$ range.



Downloaded from Arrow.com.

*AC External Clock Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 16. 5-V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency | 0.093 | – | 24.6 | MHz | |
| – | High period | 20.6 | – | 5300 | ns | |
| – | Low period | 20.6 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | µs | |

**Table 17. 3.3-V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 1 | 0.093 | – | 12.3 | MHz | Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements. |
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 2 or greater | 0.186 | – | 24.6 | MHz | If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met. |
| – | High period with CPU clock divide by 1 | 41.7 | – | 5300 | ns | |
| – | Low period with CPU clock divide by 1 | 41.7 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | µs | |

*AC Programming Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 18. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | 1 | – | 20 | ns | |
| $t_{FSCLK}$ | Fall time of SCLK | 1 | – | 20 | ns | |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | 40 | – | – | ns | |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| $t_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $t_{ERASEB}$ | Flash block erase time | – | 10 | 40[16] | ms | |
| $t_{WRITE}$ | Flash block write time | – | 40 | 160[16] | ms | |
| $t_{DSCLK}$ | Data out delay from falling edge of SCLK | – | 38 | 45 | ns | $3.6 < V_{DD}$ |
| $t_{DSCLK3}$ | Data out delay from falling edge of SCLK | – | 44 | 50 | ns | $3.0 \le V_{DD} \le 3.6$ |
| $t_{PRGH}$ | Total flash block program time ($t_{ERASEB}$ + $t_{WRITE}$), hot | – | – | 100[16] | ms | $T_J \ge 0$ °C |
| $t_{PRGC}$ | Total flash block program time ($t_{ERASEB}$ + $t_{WRITE}$), cold | – | – | 200[16] | ms | $T_J < 0$ °C |

**Note**
16. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.



Downloaded from Arrow.com.

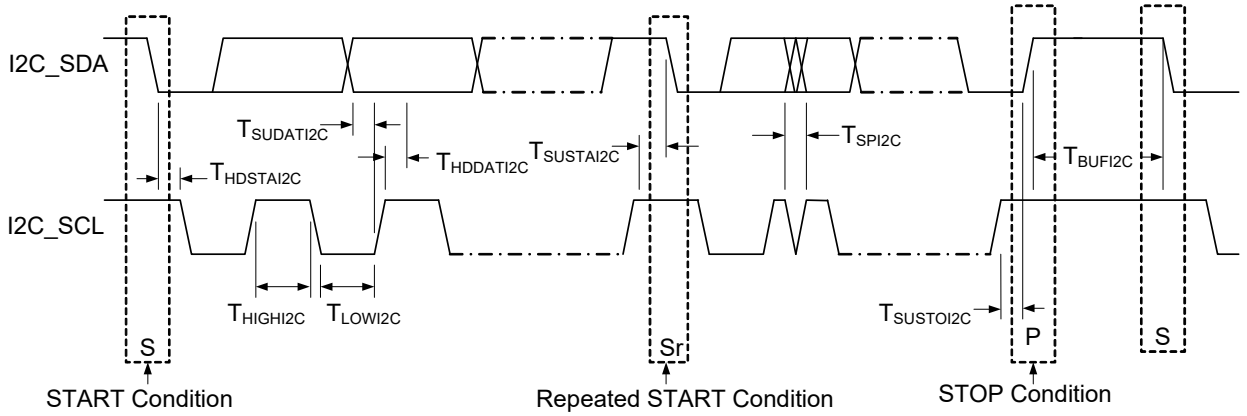
*AC I²C Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

**Table 19. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $F_{SCLI2C}$ | SCL clock frequency | 0 | 100[17] | 0 | 400[17] | kHz | |
| $t_{HDSTAI2C}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs | |
| $t_{LOWI2C}$ | LOW period of the SCL clock | 4.7 | – | 1.3 | – | µs | |
| $t_{HIGHI2C}$ | HIGH period of the SCL clock | 4.0 | – | 0.6 | – | µs | |
| $t_{SUSTAI2C}$ | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | µs | |
| $t_{HDDATI2C}$ | Data hold time | 0 | – | 0 | – | µs | |
| $t_{SUDATI2C}$ | Data setup time | 250 | – | 100[18] | – | ns | |
| $t_{SUSTOI2C}$ | Setup time for STOP condition | 4.0 | – | 0.6 | – | µs | |
| $t_{BUFI2C}$ | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | µs | |
| $t_{SPI2C}$ | Pulse width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns | |

**Figure 8. Definition for Timing for Fast/Standard Mode on the I²C Bus**




**Notes**

17. $F_{SCLI2C}$ is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the $F_{SCLI2C}$ specification adjusts accordingly
18. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.



Downloaded from Arrow.com.

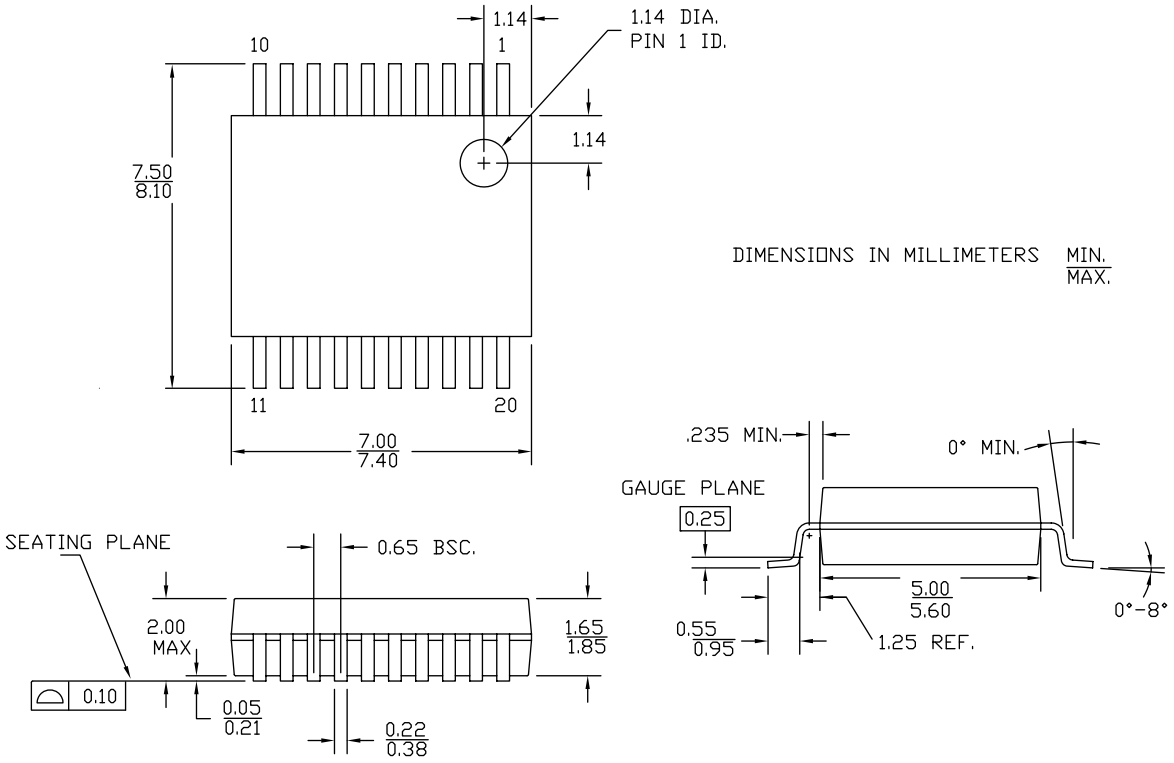
## Packaging Information

This section illustrates the packaging specifications for the CY8C21x12 PSoC device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

### Package Diagrams

**Figure 9. 20-pin SSOP (210 Mils) Package Outline, 51-85077**

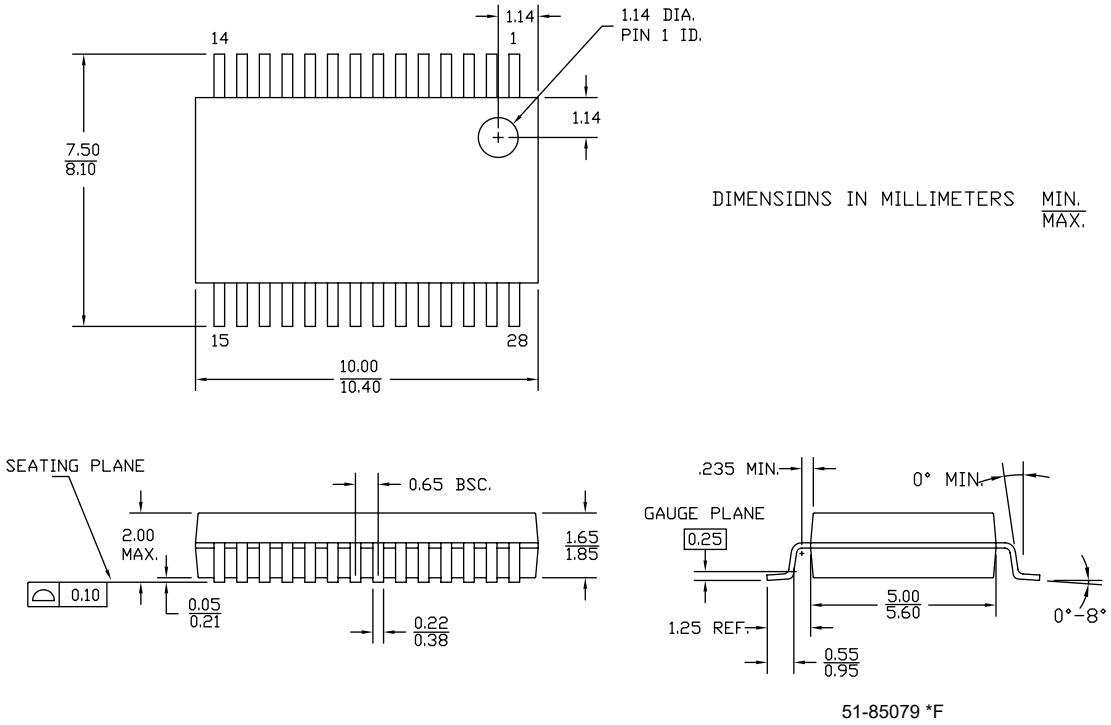



51-85077 *F



Downloaded from Arrow.com.

**Figure 10. 28-pin SSOP (210 Mils) Package Outline, 51-85079**




## Thermal Impedances

**Table 20. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ [19] | Typical $\theta_{JC}$ |
|---|---|---|
| 20-Pin SSOP | 117 °C/W | 41 °C/W |
| 28-Pin SSOP | 96 °C/W | 39 °C/W |

## Solder Reflow Specifications

Table 21 shows the solder reflow temperature limits that must not be exceeded.

**Table 21. Solder Reflow Specifications**

| Package | Maximum Peak Temperature ($T_C$) | Maximum Time above $T_C$ – 5 °C |
|---|---|---|
| 20-Pin SSOP | 260 °C | 30 seconds |
| 28-Pin SSOP | 260 °C | 30 seconds |

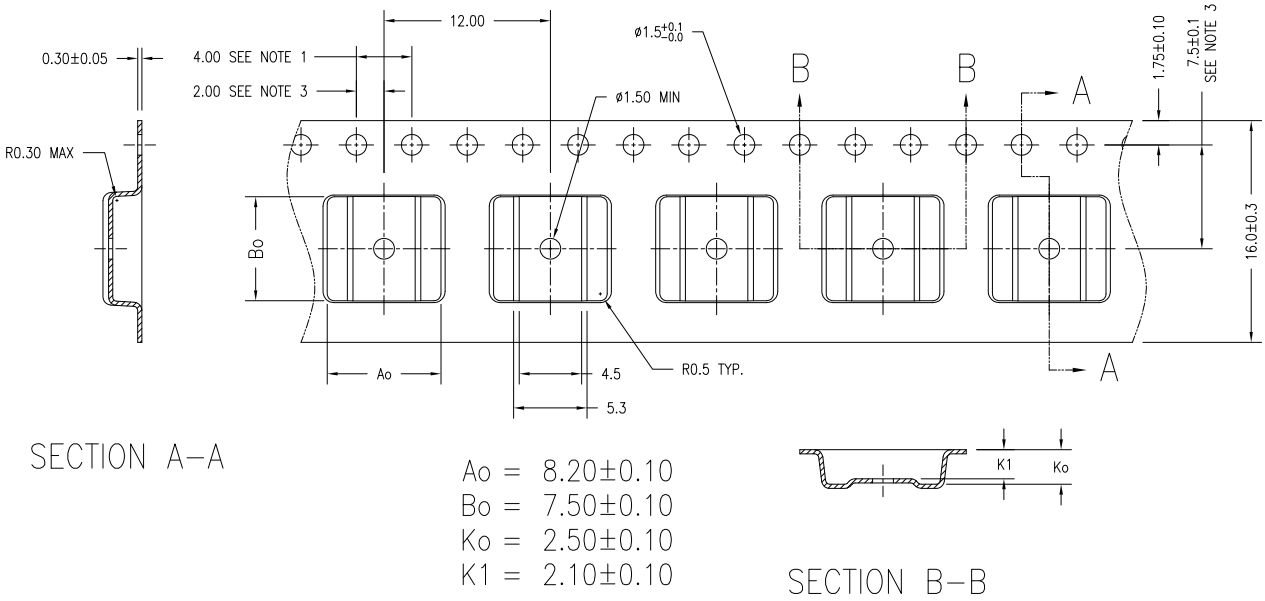
**Note**
19. $T_J = T_A + \text{Power} \times \theta_{JA}$



Downloaded from Arrow.com.

## Tape and Reel Information

**Figure 11. 20-Pin SSOP Carrier Tape Drawing**



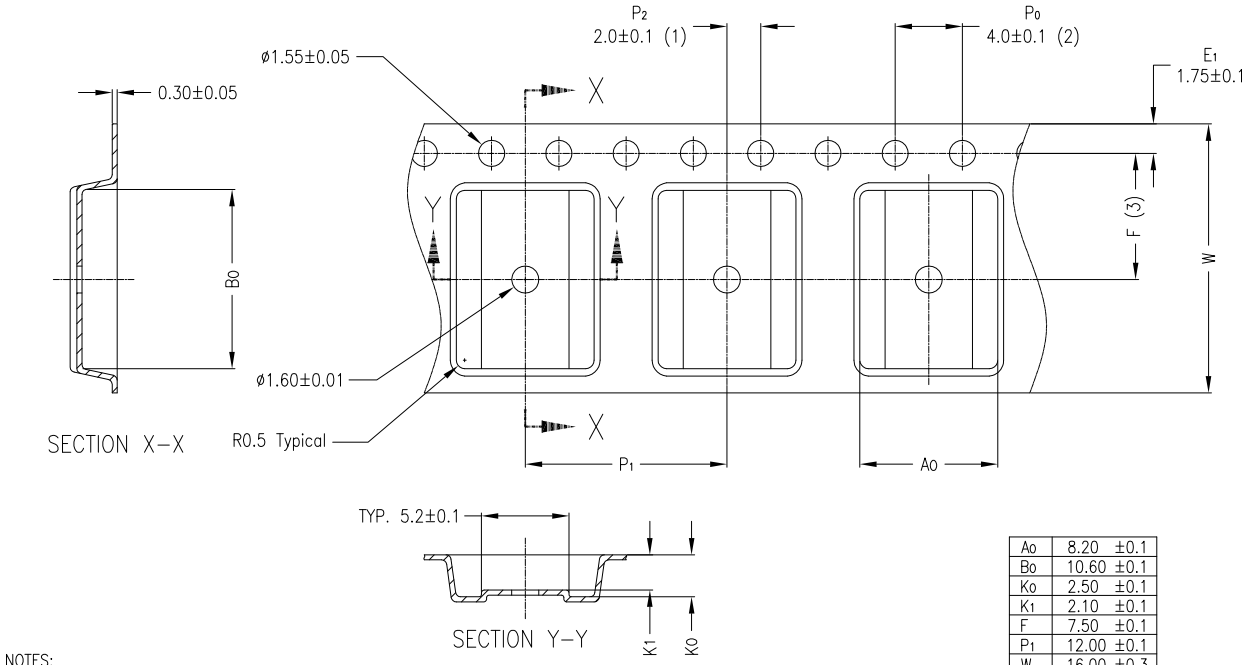

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

51-51101 *C



Downloaded from Arrow.com.

**Figure 12. 28-Pin SSOP Carrier Tape Drawing**




| | |
|---|---|
| Ao | 8.20 ±0.1 |
| Bo | 10.60 ±0.1 |
| Ko | 2.50 ±0.1 |
| K1 | 2.10 ±0.1 |
| F | 7.50 ±0.1 |
| P1 | 12.00 ±0.1 |
| W | 16.00 ±0.3 |

NOTES:
( 1 ) Measured from centerline of sprocket hole to centerline of pocket.
( 2 ) Cumulative tolerance of 10 sprocket holes is ± 0.10.
( 3 ) Measured from centerline of sprocket hole to centerline of pocket
4 Material: Conductive Polystyrene
5 Camber not to exceed 1mm in 100mm
6 Supplier P/N: SSOP28–3 CL3 22B3 Lxx W16

51-51100 *D

**Table 22. Tape and Reel Specifications**

| Package | Cover Tape Width (mm) | Hub Size (inches) | Minimum Leading Empty Pockets | Minimum Trailing Empty Pockets | Standard Full Reel Quantity |
|---|---|---|---|---|---|
| 20-Pin SSOP | 13.3 | 4 | 42 | 25 | 2000 |
| 28-Pin SSOP | 13.3 | 7 | 42 | 25 | 1000 |



Downloaded from Arrow.com.

## Development Tool Selection

This section presents the development tools available for the CY8C21x12 family.

### Software

*PSoC Designer*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

*PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

### Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up-to-date information on kit contents, descriptions, and availability.

*CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface allows you to run, halt, and single step the processor, and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube unit
- 28-Pin PDIP emulation pod for CY8C29466-24PXI
- Two 28-Pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC designer software CD
- ISSP cable
- MiniEval socket programming and evaluation board
- Backward compatibility cable (for connecting to legacy pods)
- Universal 110/220 power supply (12 V)
- European plug adapter
- USB 2.0 cable
- Getting Started guide
- Development kit registration form

*CY3280-BK1*

The CY3280-BK1 Universal CapSense Control Kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The kit comes with a control boards for CY8C20x34 and CY8C21x34 devices as well as a breadboard module and a button(5)/slider module.

The CY8C21x34 on-chip debugger device that is part of this kit is capable of emulating CY8C21x12 devices as well. Therefore, this kit can be used to evaluate and develop projects for CY8C21x12 devices.

### Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-Pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

*CY3210-21X34 Evaluation Pod (EvalPod)*

The CY3210-21X34 PSoC EvalPods are pods that connect to the ICE in-circuit emulator (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-21X34 provides evaluation of the CY8C21x34 PSoC device family.

The CY8C21x34 on-chip debugger device that is part of this kit is capable of emulating CY8C21x12 devices as well. Therefore, this kit can be used to evaluate CY8C21x12 devices.



Downloaded from Arrow.com.

## Device Programmers

All device programmers can be purchased from the Cypress Online Store.

*CY3217-MiniProg1*

The CY3217-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg1 programmer
- USB A to Mini B cable
- CY3217-MiniProg1 kit CD, which has kit documents, PSoC Designer and PSoC Programmer installation files
- Getting Started Guide

## Accessories (Emulation and Programming)

**Table 23. Emulation and Programming Accessories**

| Part Number | Pin Package | Pod Kit[20] | Foot Kit[21] | Adapter[22] |
|---|---|---|---|---|
| CY8C21312-24PVXA | 20-Pin SSOP | CY3250-21X34 | CY3250-20SSOP-FK | Adapters are available at http://www.emulation.com. |
| CY8C21512-24PVXA | 28-Pin SSOP | CY3250-21X34 | CY3250-28SSOP-FK | |

**Notes**
20. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
21. Foot kit includes surface mount feet that can be soldered to the target PCB.
22. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are available at http://www.emulation.com.



Downloaded from Arrow.com.

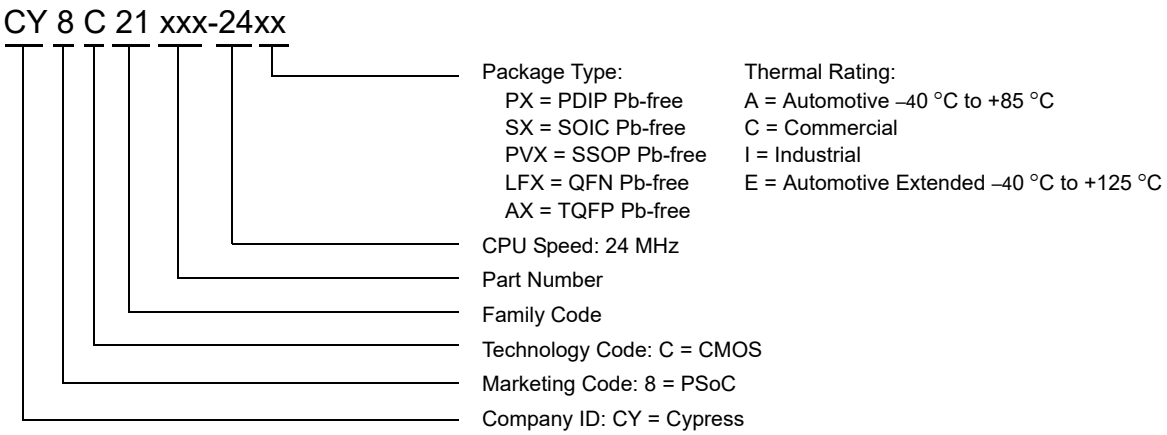
## Ordering Information

The following table lists theCY8C21x12 PSoC device's key package features and ordering codes.

**Table 24. PSoC Device Key Features and Ordering Information**

| Package | Ordering Code | Flash (Bytes) | SRAM (Bytes) | Temperature Range | Limited Digital Blocks | CapSense Blocks | Digital I/O Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---|---|---|---|---|---|---|---|---|---|---|
| 20-Pin (210-Mil) SSOP | CY8C21312-24PVXA | 8K | 512 | –40 °C to +85 °C | 1 | 1 | 16 | 16 | 0 | Yes |
| 20-Pin (210-Mil) SSOP (Tape and Reel) | CY8C21312-24PVXAT | 8K | 512 | –40 °C to +85 °C | 1 | 1 | 16 | 16 | 0 | Yes |
| 28-Pin (210-Mil) SSOP | CY8C21512-24PVXA | 8K | 512 | –40 °C to +85 °C | 1 | 1 | 24 | 24 | 0 | Yes |
| 28-Pin (210-Mil) SSOP (Tape and Reel) | CY8C21512-24PVXAT | 8K | 512 | –40 °C to +85 °C | 1 | 1 | 24 | 24 | 0 | Yes |

### Ordering Code Definitions






Downloaded from Arrow.com.

## Acronyms

Table 25 lists the acronyms that are used in this document.

**Table 25. Acronyms Used in this Datasheet**

| Acronym | Description | Acronym | Description |
|---|---|---|---|
| AC | alternating current | MIPS | million instructions per second |
| AEC | Automotive Electronics Council | PCB | printed circuit board |
| ADC | analog-to-digital converter | PDIP | plastic dual in-line package |
| API | application programming interface | PLL | phase-locked loop |
| CPU | central processing unit | POR | power-on reset |
| CRC | cyclic redundancy check | PPOR | precision power-on reset |
| CSD | capsense sigma delta | PRS | pseudo-random sequence |
| CT | continuous time | PSoC® | Programmable System-on-Chip |
| DAC | digital-to-analog converter | PWM | pulse width modulator |
| DC | direct current or duty cycle | SC | switched capacitor |
| EEPROM | electrically erasable programmable read-only memory | SCL / SCLK | serial clock |
| EXTCLK | external clock | SDA | serial data |
| GPIO | general-purpose I/O | SLIMO | slow internal main oscillator |
| $I^2C$ | Inter-Integrated Circuit | SMP | switch mode pump |
| ICE | in-circuit emulator | SOIC | small-outline integrated circuit |
| IDE | integrated development environment | SPI | serial peripheral interface |
| ILO | internal low-speed oscillator | SRAM | static random access memory |
| IMO | internal main oscillator | SROM | supervisory read-only memory |
| I/O | input/output | SSOP | shrink small-outline package |
| IrDA | Infrared Data Association | TQFP | thin quad flat pack |
| ISSP | in-system serial programming | UART | universal asynchronous reciever / transmitter |
| LCD | liquid crystal display | USB | universal serial bus |
| LED | light-emitting diode | WDT | watchdog timer |
| LVD | low voltage detect | XRES | external reset |
| MCU | microcontroller unit | | |

## Reference Documents

*CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM)* (001-14463)

*Design Aids – Reading and Writing PSoC® Flash – AN2015* (001-40459)

*Understanding Data Sheet Jitter Specifications for Cypress Timing Products – AN5054* (001-14503)



Downloaded from Arrow.com.

## Document Conventions

### Units of Measure

The following table lists the units of measure that are used in this document.

**Table 26. Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| °C | degree Celsius | µV | microvolts |
| dB | decibels | mA | milliampere |
| KB | 1024 bytes | ms | millisecond |
| Kbit | 1024 bits | mV | millivolts |
| kHz | kilohertz | nA | nanoampere |
| kΩ | kilohm | ns | nanosecond |
| Mbaud | megabaud | Ω | ohm |
| Mbps | megabits per second | pA | picoampere |
| MHz | megahertz | pF | picofarad |
| µA | microampere | ps | picosecond |
| µs | microsecond | V | volts |

## Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are in decimal format.

## Glossary

| | |
|---|---|
| active high | 1. A logic signal having its asserted state as the logic 1 state.<br>2. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital converter (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog converter (DAC) performs the reverse operation. |
| Application programming interface (API) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | 1. The frequency range of a message or information processing system measured in hertz.<br>2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |



Downloaded from Arrow.com.

## Glossary *(continued)*

| | |
|---|---|
| bias | 1. A systematic deviation of a value from a reference value.<br>2. The amount by which the average of a set of values departs from a reference value.<br>3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |
| block | 1. A functional unit that performs a single function, such as an oscillator.<br>2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | 1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written.<br>2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.<br>3. An amplifier used to lower the output impedance of a system. |
| bus | 1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.<br>2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].<br>3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |
| digital-to-analog converter (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital converter (ADC) performs the reverse operation. |



Downloaded from Arrow.com.

## Glossary *(continued)*

| | |
|---|---|
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |
| external reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| flash | An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off. |
| flash block | The smallest amount of flash ROM space that may be programmed at one time and the smallest amount of flash space that may be protected. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| $I^2C$ | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at the $V_{DD}$ supply voltage and pulled high with resistors. The bus operates up to100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the CPU receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.<br>2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses $V_{DD}$ and provides an interrupt to the system when $V_{DD}$ falls below a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the flash, SRAM, and register space. |
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*. |



Downloaded from Arrow.com.

## Glossary *(continued)*

| | |
|---|---|
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |
| modulator | A device that imposes a signal on a carrier. |
| noise | 1. A disturbance that affects a signal and that may distort the information carried by the signal.<br>2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitted data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| phase-locked loop (PLL) | An electronic circuit that controls an *oscillator* so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| power-on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset. |
| PSoC® | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress. |
| PSoC Designer™ | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied value. |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a known state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | 1. Pertaining to a process in which all events occur one after the other.<br>2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |



Downloaded from Arrow.com.

## Glossary *(continued)*

| | |
|---|---|
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |
| SRAM | An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform flash operations. The functions of the SROM may be accessed in normal user code, operating from flash. |
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | 1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.<br>2. A system whose operation is synchronized by a clock signal. |
| tri-state | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-built, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level analog and digital PSoC blocks. User modules also provide high level *API (Application Programming Interface)* for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| $V_{DD}$ | A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V. |
| $V_{SS}$ | A name for a power net meaning “voltage source.” The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |



Downloaded from Arrow.com.

## Document History Page

| Document Title: CY8C21312/CY8C21512, Automotive PSoC® Programmable System-on-Chip™<br>Document Number: 001-63745 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 3023789 | BTK / AESA | 09/06/2010 | New data sheet. |
| *A | 3094401 | BTK | 11/23/2010 | With reference to CDT#88767.<br>Updated Packaging Information:<br>Added Tape and Reel Information. |
| *B | 3157903 | BTK / NJF | 01/31/2011 | With reference to CDT#92832.<br>Updated PSoC Functional Overview:<br>Updated PSoC Device Characteristics:<br>Updated Table 1.<br>Updated Electrical Specifications:<br>With reference to CDT#82750.<br>Updated Absolute Maximum Ratings:<br>Updated details in “Notes” column corresponding to $T_{STG}$ parameter (to add more clarity).<br>Updated DC Electrical Characteristics:<br>With reference to CDT#90944.<br>Updated DC GPIO Specifications:<br>Updated Table 7 (Added details in “Notes” column corresponding to $R_{PD}$ parameter).<br>With reference to CDT#86716.<br>Updated DC POR and LVD Specifications:<br>Updated Table 10 (Added $V_{PPOR0}$ parameter and its details).<br>With reference to CDT#92822.<br>Updated DC Programming Specifications:<br>Updated Table 11 (Added $V_{DDP}$, $V_{DDLV}$, and $V_{DDHV}$ parameters and their details).<br>Updated AC Electrical Characteristics:<br>With reference to CDT#92994 and CDT#92831.<br>Updated AC Chip Level Specifications:<br>Updated Table 12 (Added details in “Max” column corresponding to $F_{32KU}$ parameter; removed Jitter32k, Jitter32k, Jitter24M1 parameters and their details; added $t_{JIT_IMO}$ parameter and its details; added Note 13 and referred the same note in $t_{JIT_IMO}$ parameter).<br>With reference to CDT#92819.<br>Updated AC Digital Block Specifications:<br>Updated Table 15 (Updated wording, formatting, and notes to improve clarity).<br>With reference to CDT#92817.<br>Updated AC I2C Specifications:<br>Updated Figure 8 (to improve clarity).<br>Updated Packaging Information:<br>With reference to CDT#92828.<br>Updated Solder Reflow Specifications:<br>Updated Table 21.<br>Updated Tape and Reel Information:<br>spec 51-51100 – Changed revision from *A to *B.<br>Updated Reference Documents:<br>Added spec 001-14503. |



Downloaded from Arrow.com.

## Document History Page *(continued)*

| Document Title: CY8C21312/CY8C21512, Automotive PSoC® Programmable System-on-Chip™<br>Document Number: 001-63745 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *C | 4111812 | JICG | 09/02/2013 | Updated Packaging Information:<br>Updated Package Diagrams:<br>spec 51-85077 – Changed revision from *D to *E.<br>spec 51-85079 – Changed revision from *D to *E.<br>Updated Tape and Reel Information:<br>spec 51-51101 – Changed revision from *A to *C.<br>spec 51-51100 – Changed revision from *B to *C.<br>Updated Development Tool Selection:<br>Updated Device Programmers:<br>Removed “CY3207ISSP In-System Serial Programmer (ISSP)”.<br>Updated to new template.<br>Completing Sunset Review. |
| *D | 4560572 | SNPR | 11/04/2014 | Updated Development Tool Selection:<br>Updated Device Programmers:<br>Replaced CY3210-MiniProg1 with CY3217-MiniProg1.<br>Updated Packaging Information:<br>Updated Tape and Reel Information:<br>spec 51-51100 – Changed revision from *C to *D.<br>Completing Sunset Review. |
| *E | 5999185 | SNPR | 12/19/2017 | Updated Packaging Information:<br>Updated Package Diagrams:<br>spec 51-85077 – Changed revision from *E to *F.<br>spec 51-85079 – Changed revision from *E to *F.<br>Updated to new template.<br>Completing Sunset Review. |
| *F | 6113262 | SNPR | 03/28/2018 | Updated to new template. |



Downloaded from Arrow.com.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| Arm® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Memory | cypress.com/memory |
| Microcontrollers | cypress.com/mcu |
| PSoC | cypress.com/psoc |
| Power Management ICs | cypress.com/pmic |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless Connectivity | cypress.com/wireless |

### PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

### Cypress Developer Community

Community | Projects | Video | Blogs | Training | Components

### Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2010-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.



PSoC Designer™ and Programmable System-on-Chip™ are trademarks and PSoC® and CapSense® are registered trademarks of Cypress Semiconductor Corporation.

Purchase of $I^2C$ components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips $I^2C$ Patent Rights to use these components in an $I^2C$ system, provided that the system conforms to the $I^2C$ Standard Specification as defined by Philips. As from October 1st, 2006 Philips Semiconductors has a new trade name - NXP Semiconductors.

Downloaded from Arrow.com.