

Triple Buffer/Driver With Open-drain Outputs

Check for Samples: [SN74LVC3G07](#)

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Input and Open-Drain Output Accepts Voltages up to 5.5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Live Insertion, Partial-Power-Down Mode and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

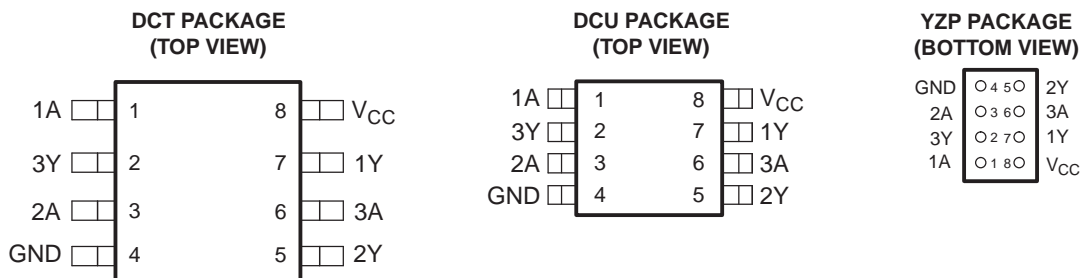
DESCRIPTION

This triple buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC3G07 is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



See mechanical drawings for dimensions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

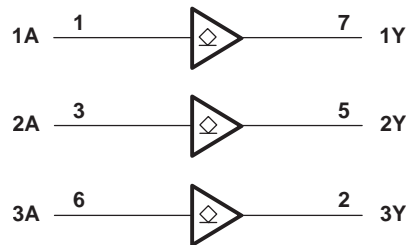
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**Function Table
(Each Buffer/Driver)**

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-------------|-----|---------|
| V_{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ^{(2) (3)} | -0.5 | 6.5 | V |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 mA |
| I_O | Continuous output current | | | ±50 mA |
| | Continuous current through V_{CC} or GND | | | ±100 mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DCT package | | 220 |
| | | DCU package | | 227 |
| | | YZP package | | 102 |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|---|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 |
| | | Data retention only | 1.5 | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | |
| | | V _{CC} = 3 V to 3.6 V | 2 | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | 0.8 | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.3 × V _{CC} | |
| V _I | Input voltage | 0 | 5.5 | V |
| V _O | Output voltage | 0 | 5.5 | V |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | 4 | mA |
| | | V _{CC} = 2.3 V | 8 | |
| | | V _{CC} = 3 V | 16 | |
| | | | 24 | |
| | | V _{CC} = 4.5 V | 32 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | 20 | ns/V |
| | | V _{CC} = 3.3 V ± 0.3 V | 10 | |
| | | V _{CC} = 5 V ± 0.5 V | 5 | |
| T _A | Operating free-air temperature | –40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | –40°C to 85°C | | | –40°C to 125°C | | | UNIT |
|------------------|----------|--|-----------------|---------------|--------------------|------|----------------|--------------------|------|------|
| | | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V _{OL} | | I _{OL} = 100 μA | 1.65 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | | I _{OL} = 4 mA | 1.65 V | | | 0.45 | | | 0.45 | |
| | | I _{OL} = 8 mA | 2.3 V | | | 0.3 | | | 0.3 | |
| | | I _{OL} = 16 mA | 3 V | | | 0.4 | | | 0.4 | |
| | | I _{OL} = 24 mA | | | | 0.55 | | | 0.75 | |
| | | I _{OL} = 32 mA | 4.5 V | | | 0.55 | | | 0.75 | |
| I _I | A inputs | V _I = 5.5 V or GND | 0 to 5.5 V | | | ±5 | | | ±5 | μA |
| I _{off} | | V _I or V _O = 5.5 V | 0 | | | ±10 | | | ±10 | μA |
| I _{CC} | | V _I = 5.5 V or GND, I _O = 0 | 1.65 V to 5.5 V | | | 10 | | | 10 | μA |
| ΔI _{CC} | | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | | | 500 | | | 500 | μA |
| C _I | | V _I = V _{CC} or GND | 3.3 V | | | 3.5 | | | 3.5 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC3G07 –40°C to 85°C | | | | | | | | UNIT |
|-----------------|-----------------|----------------|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
| | | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 1.5 | 7.8 | 1 | 4.3 | 1.1 | 3.7 | 1 | 2.9 | ns |

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

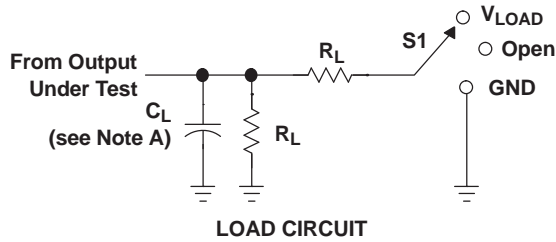
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC3G07 –40°C to 125°C | | | | | | | | UNIT |
|-----------------|-----------------|----------------|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
| | | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 1.5 | 8.3 | 1 | 4.8 | 1.1 | 4.2 | 1 | 3.4 | ns |

Operating Characteristics

$T_A = 25^\circ\text{C}$

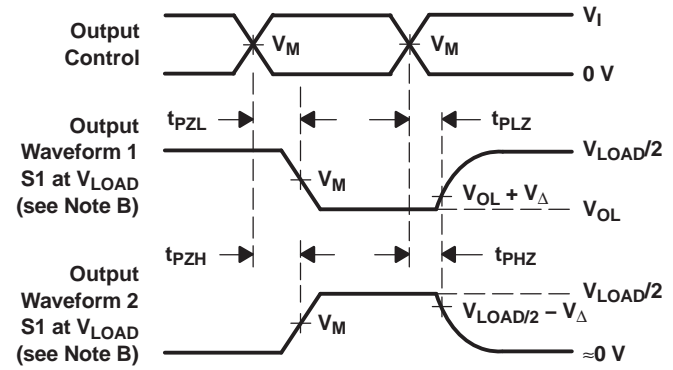
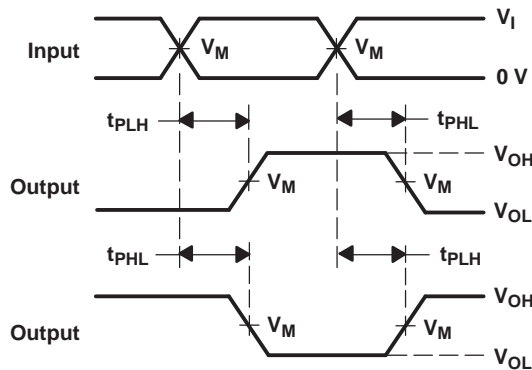
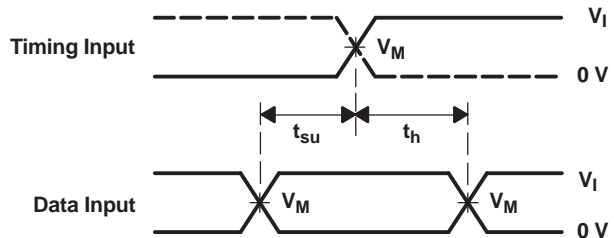
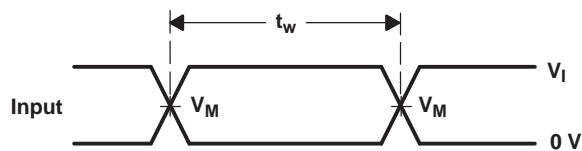
| PARAMETER | | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|-----------|-------------------------------|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | | TYP | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance | $f = 10\text{ MHz}$ | 3 | 3 | 4 | 5 | pF |

Parameter Measurement Information (Open Drain)



| TEST | S1 |
|-------------------------------|------------|
| t_{PZL} (see Notes E and F) | V_{LOAD} |
| t_{PLZ} (see Notes E and G) | V_{LOAD} |
| t_{PHZ}/t_{PZH} | V_{LOAD} |

| V_{CC} | INPUT | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 - t_{PZL} is measured at V_M .
 - t_{PLZ} is measured at $V_{OL} + V_{\Delta}$.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

| Changes from Revision J (Feburary 2007) to Revision K | Page |
|---|-------------------|
| • Updated document formatting. | 1 |
| • Updated operating temperature range. | 3 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------|
| SN74LVC3G07DCT3 | Active | Production | SSOP (DCT) 8 | 3000 LARGE T&R | Yes | SNBI | Level-1-260C-UNLIM | -40 to 85 | C07 Z |
| SN74LVC3G07DCTR | Active | Production | SSOP (DCT) 8 | 3000 LARGE T&R | Yes | NIPDAU SN NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (2WZ5, C07) (R, Z) |
| SN74LVC3G07DCUR | Active | Production | VSSOP (DCU) 8 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C07J, C07Q, C07R) |
| SN74LVC3G07DCURG4 | Active | Production | VSSOP (DCU) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C07R |
| SN74LVC3G07DCUT | Active | Production | VSSOP (DCU) 8 | 250 SMALL T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C07J, C07Q, C07R) |
| SN74LVC3G07DCUTG4 | Active | Production | VSSOP (DCU) 8 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C07R |
| SN74LVC3G07YZPR | Active | Production | DSBGA (YZP) 8 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CVN |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC3G07 :

- Automotive : [SN74LVC3G07-Q1](#)
- Enhanced Product : [SN74LVC3G07-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC3G07DCT3 | SSOP | DCT | 8 | 3000 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74LVC3G07DCTR | SSOP | DCT | 8 | 3000 | 180.0 | 12.4 | 3.15 | 4.35 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74LVC3G07DCUR | VSSOP | DCU | 8 | 3000 | 178.0 | 9.0 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC3G07DCURG4 | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC3G07DCUT | VSSOP | DCU | 8 | 250 | 178.0 | 9.0 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC3G07DCUT | VSSOP | DCU | 8 | 250 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC3G07DCUTG4 | VSSOP | DCU | 8 | 250 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC3G07YZPR | DSBGA | YZP | 8 | 3000 | 178.0 | 9.2 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

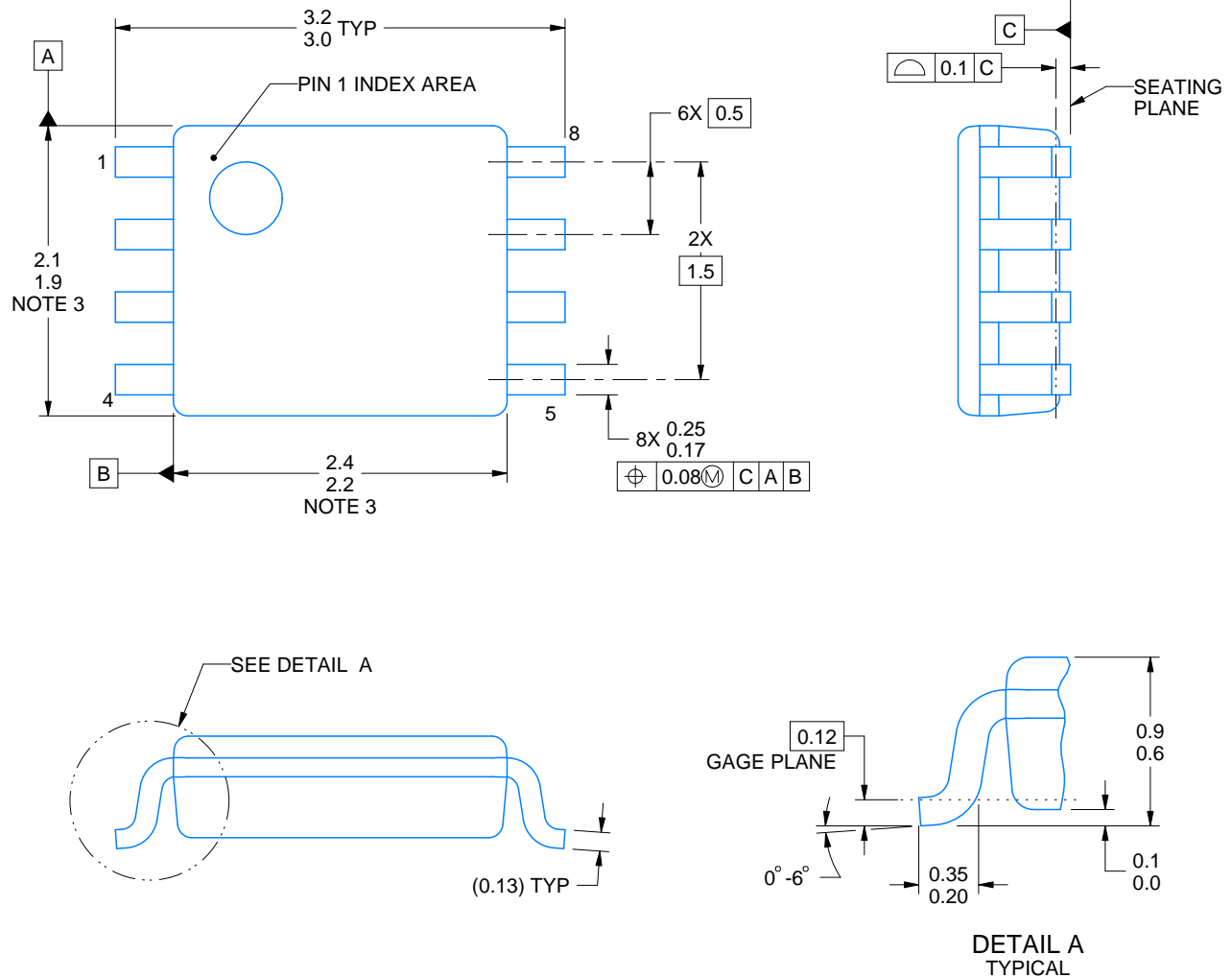


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC3G07DCT3 | SSOP | DCT | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74LVC3G07DCTR | SSOP | DCT | 8 | 3000 | 190.0 | 190.0 | 30.0 |
| SN74LVC3G07DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC3G07DCURG4 | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC3G07DCUT | VSSOP | DCU | 8 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC3G07DCUT | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC3G07DCUTG4 | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC3G07YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 35.0 |

DCU0008A**PACKAGE OUTLINE****VSSOP - 0.9 mm max height**

SMALL OUTLINE PACKAGE



4225266/A 09/2014

NOTES:

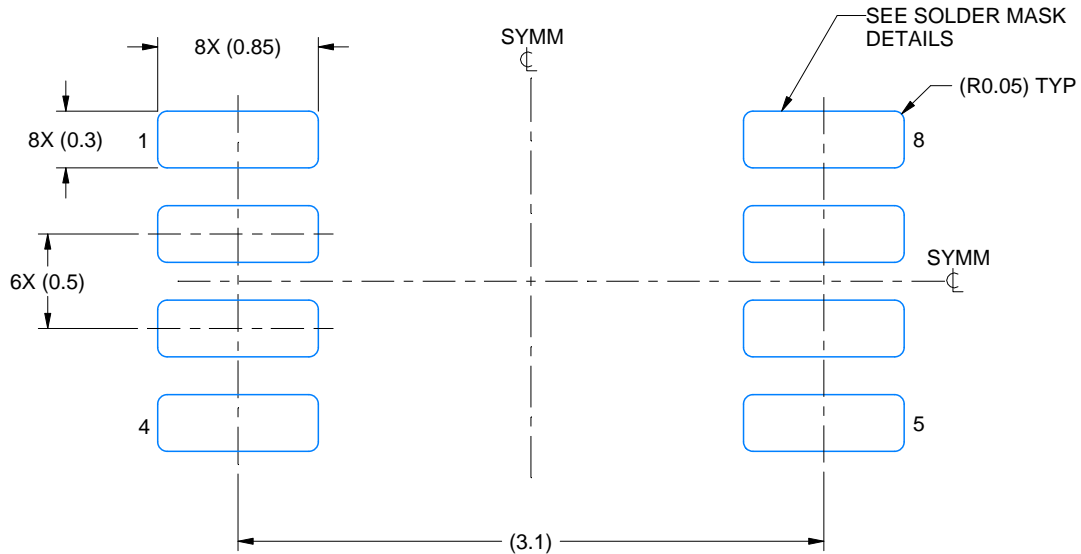
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

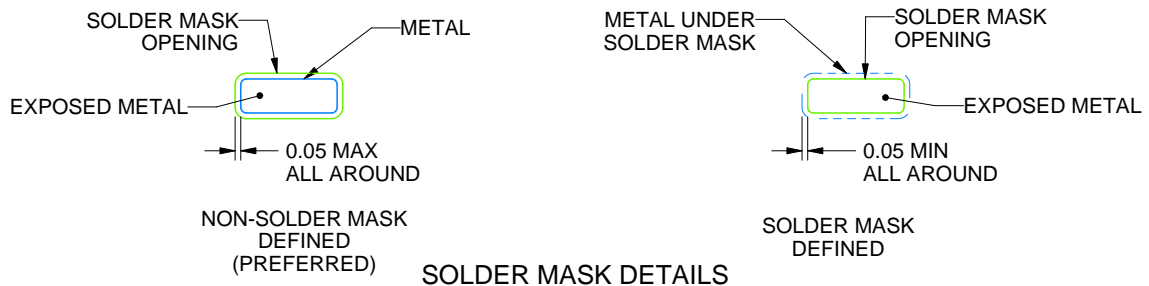
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

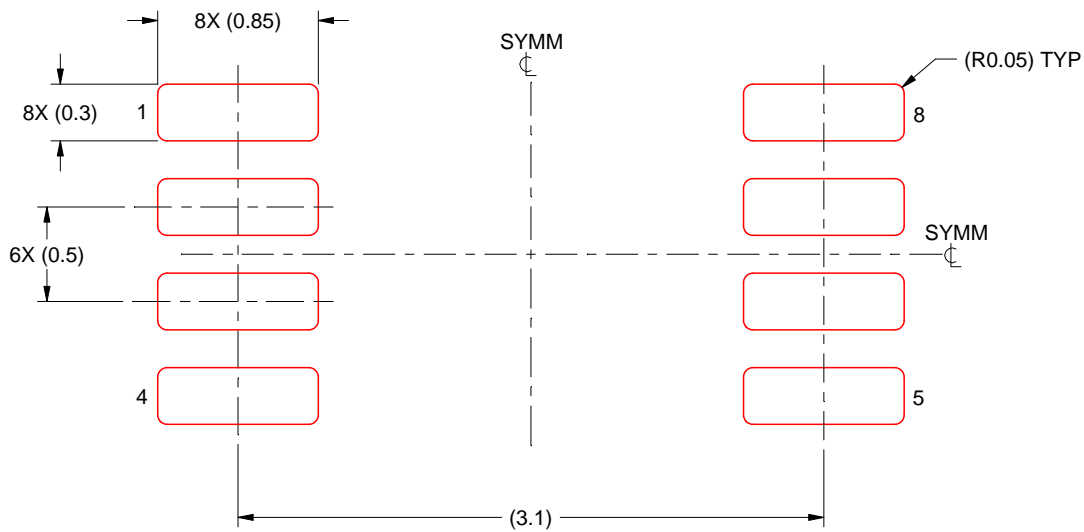
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

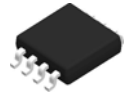


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

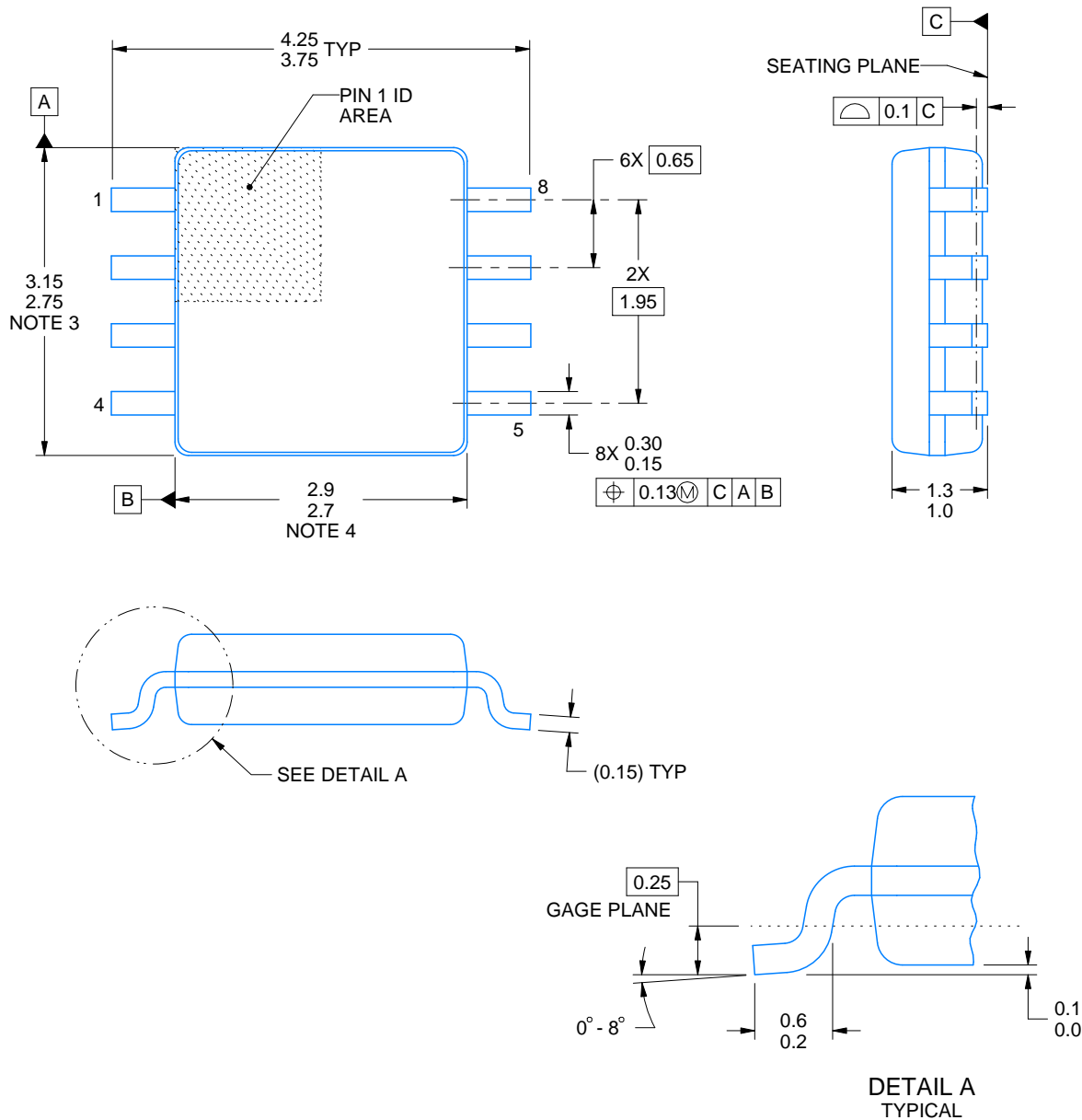
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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCT0008A**PACKAGE OUTLINE****SSOP - 1.3 mm max height**

SMALL OUTLINE PACKAGE



4220784/C 06/2021

NOTES:

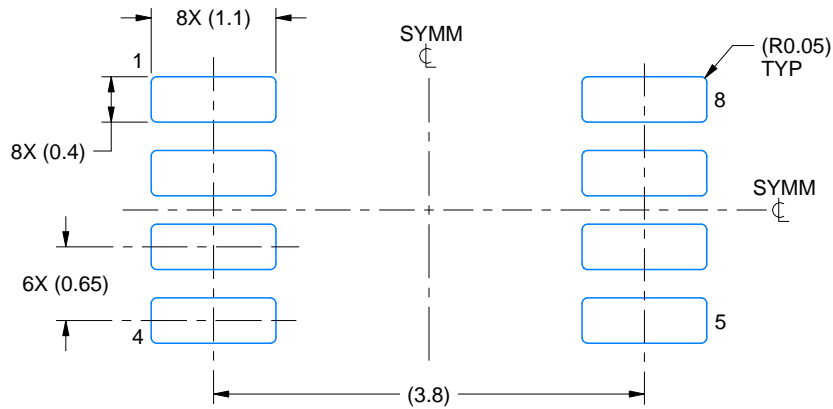
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

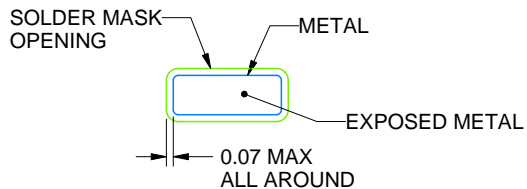
DCT0008A

SSOP - 1.3 mm max height

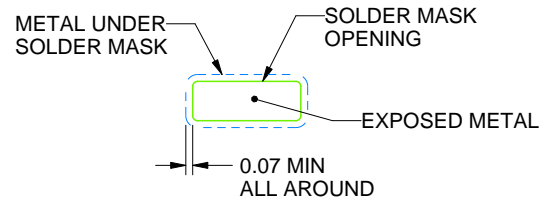
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

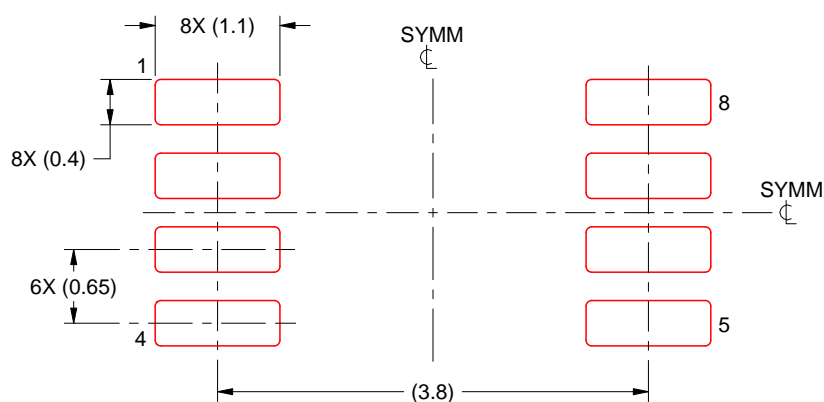
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



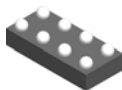
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

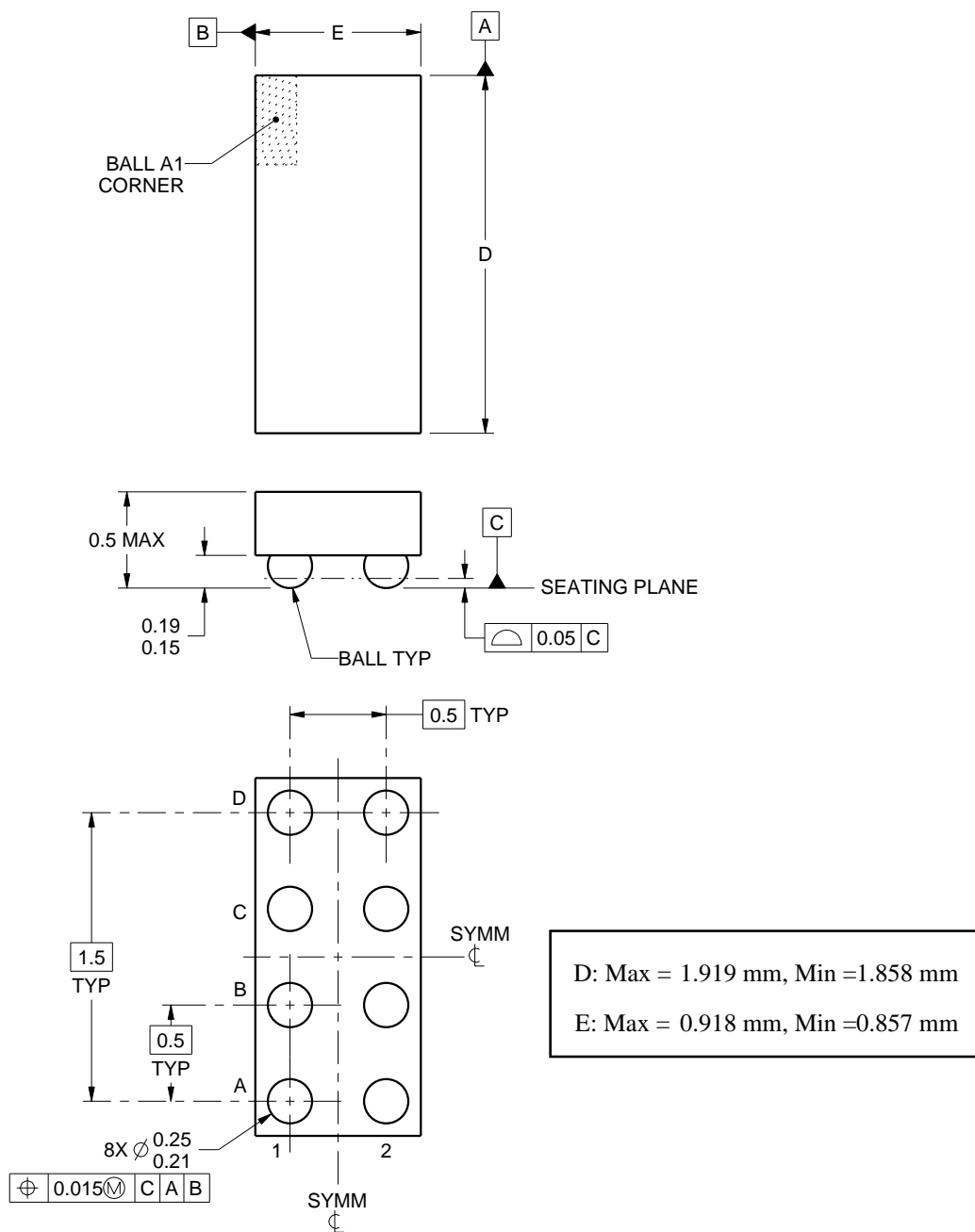
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

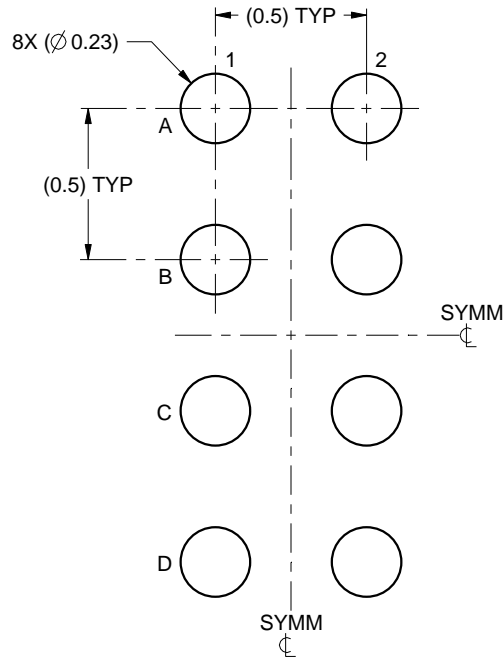
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

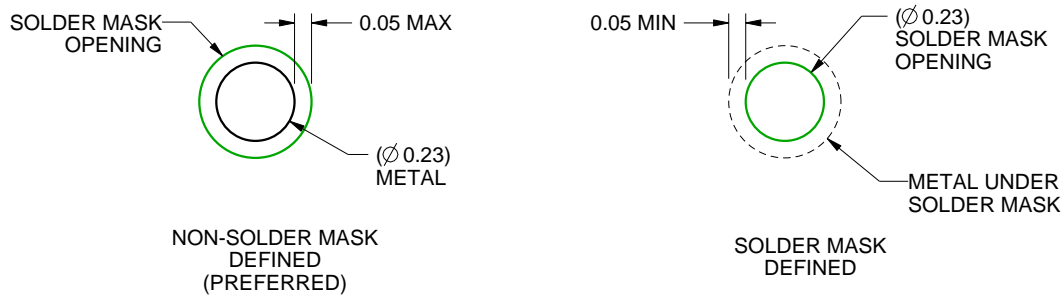
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

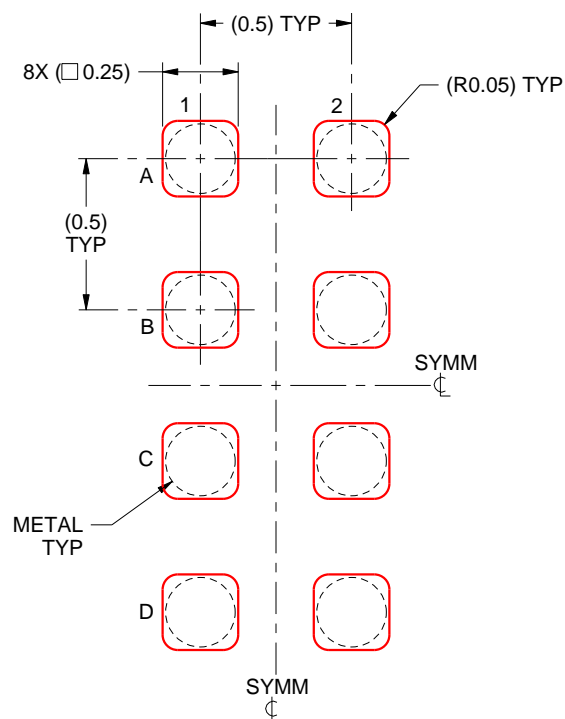
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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